EECS 112L Lab2 Report

Yifan Xu

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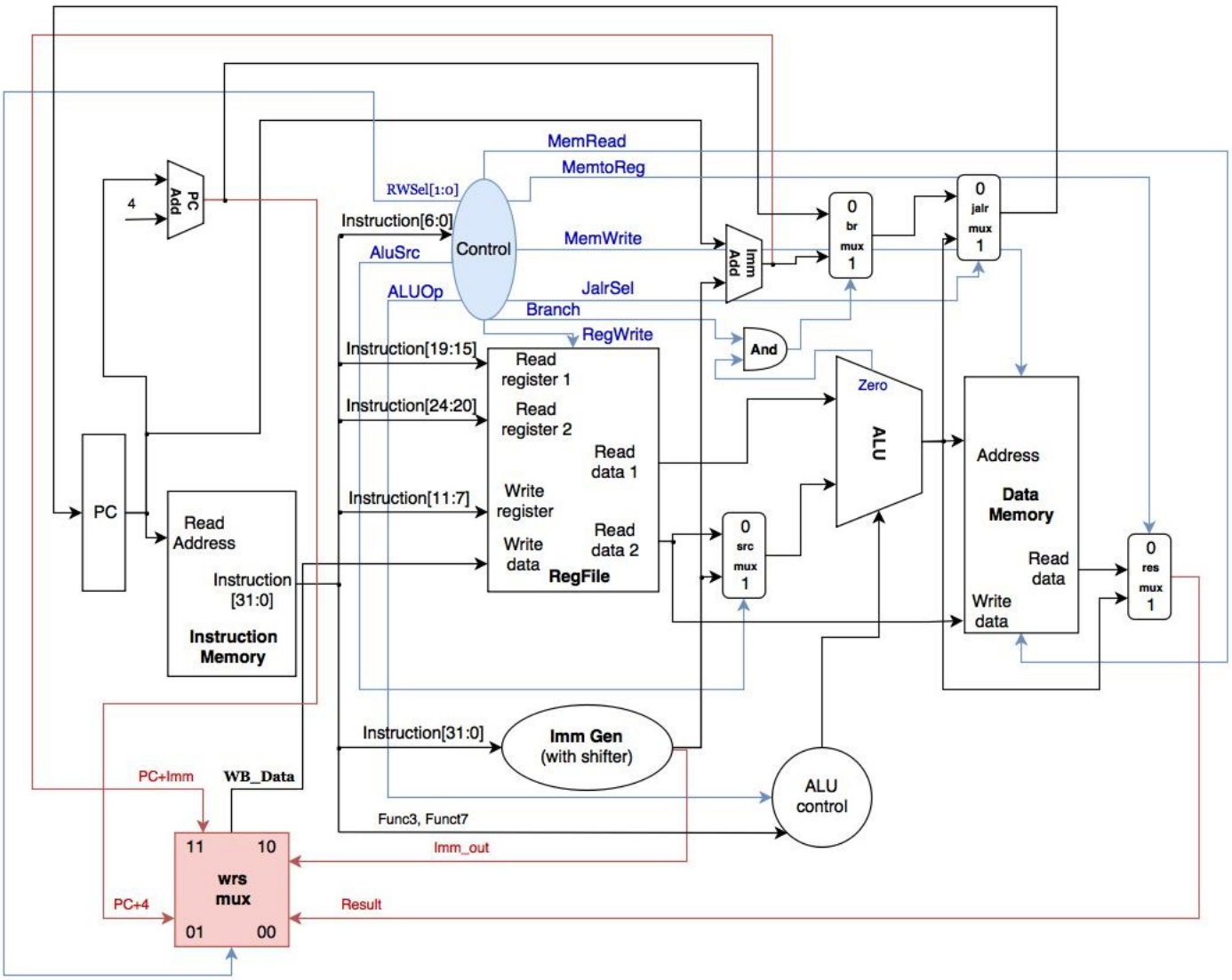
1 Block Analysis and Diagram

1.1 Block Diagram



1.2 Imm Gen

Imm_Gen.sv is now a combination of Shifter and Imm Generator. The output is 32 bits. For different type of instruction, it will generate a after-shift final value for directly operation and computation.

1.3 Controller

Three new output signals are generated as select controllers:

Branch 1 bit signal, connected to an AND gate with Zero Signal from ALU, result is the select of Branch Mux(brsmux, 2to1)
0: branch is not taken
1: branch is taken

JalrSel 1 bit signal, generated as select of Jalr Mux(jalrmux, 2to1)
0: jalr is not taken
1: jalr is taken

RWSel 2 bits signal, generated as select of Write Register Mux(wrmux,4to1)
00: Write Back Data
01: PC+4 (JAL/JALR)
10: Imm-gen (LUI)
11: Pc+Imm-gen (AUIPC)

1.4 ALU

The ALU block support 14 operations:

Opcode	Operation
0000	AND
0001	OR
0010	ADD
0011	XOR
0100	<<
0101	>>
0110	SUB
0111	>>>
1000	=
1001	≠
1010	Return True
1011	
1100	<
1101	>
1110	unsigned <
1111	unsigned >

Note, contrary to some other processors, equal and not equal here are doing comparison directly instead of calling subtract. As a result, the signal AluResult of all conditional operations is 32'b00000001 if condition is true, or 32'b00000000 if condition is false.

New output signal Zero is generated as select control for B-type and Jal/Jalr instructions. Zero signal is assigned as the lowest bit of AluResult. Therefore, whenever a B-type condition is true or Jal/Jalr is taken, Zero will be 1.

1.5 Branch Mux and Jalr Mux

Brach Mux is a 2 to 1 mux that in charge of selecting the next PC value. Two inputs are PC+4 from PC Adder and PC+Imm from Imm Adder. If Branch is taken, mux select will be 1, PC+Imm will be the output. If Branch is not taken, PC+4 will be the output.

Jalr Mux is a 2 to 1 mux works specifically when Jalr is taken. Under this circumstance, the next PC value should be R[rs1]+Imm, which is calculated and output by ALU in advance.

1.6 Data Memory

The new Data Memory can handle Store and Load Instruction of different size. A new input Funct3 is input into Data Memory to help decide how many bits that Store or Load should operate on.

For Load, there are LB, which load the most significant 8 bits of a memory block into a register. While LH load the last 16 bits and LW load all 32 bits. Since register is 32 bits, there will be a sign extension made on the final value depending on the least significant bit of the right side.

There are also LBU and LHU, which will treat data as unsigned value. This means the data memory will only generate 0 to fill those empty digits on the right side.

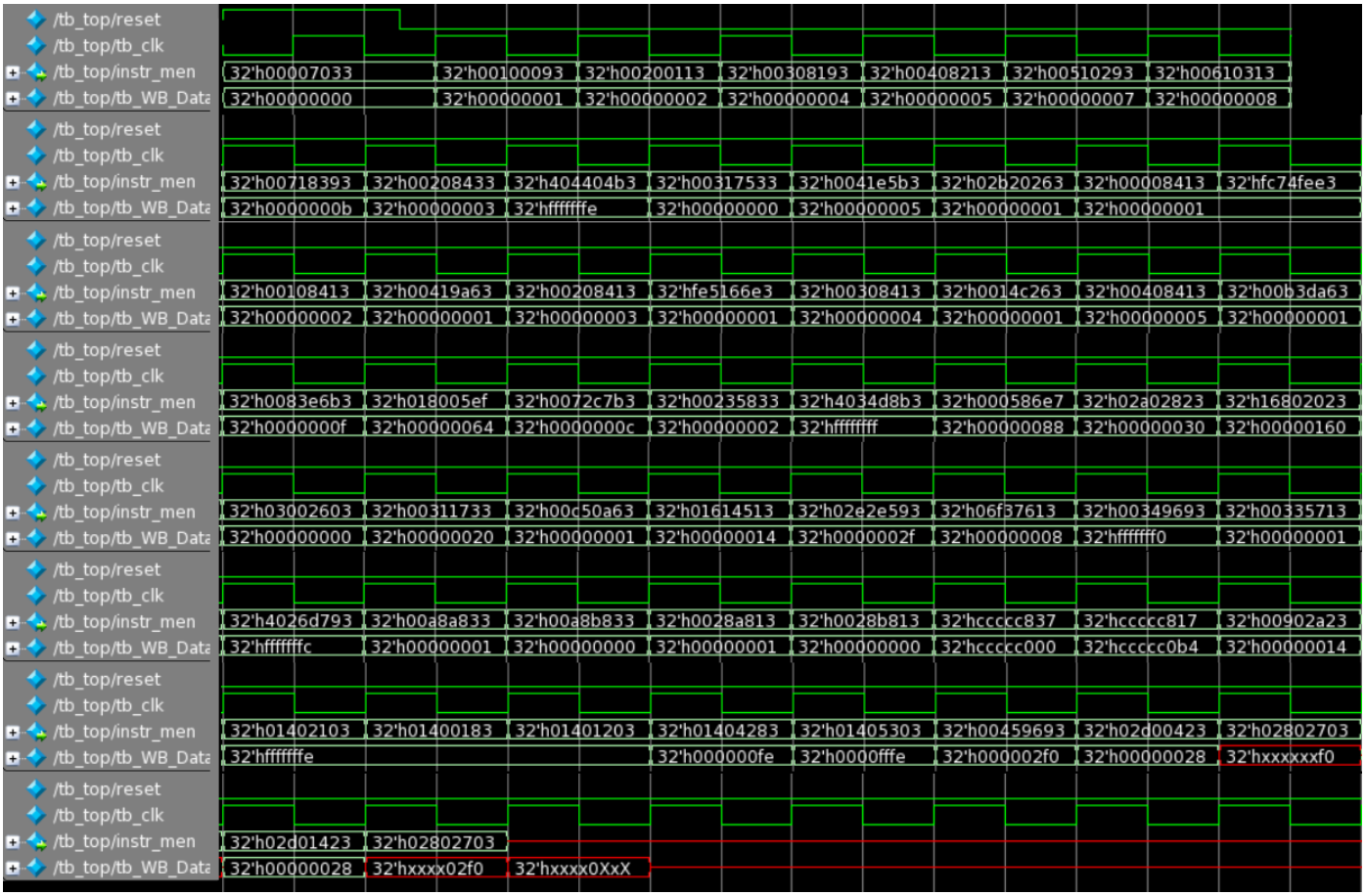
For Store, there are SB, which store the most significant 8 bits from current register into the target memory block. While SH store the last 16 bits and SW store all 32 bits. **Note, Store operation will only modify specific bits while left others untouched. There is no bits filling operation or sign extension.** For example, SB will only changed [7:0] bits of the target memory block. If memory is never initialized, [32:8] bits will all be x(unknown status)

1.7 Write Register Mux

A new Write Register Mux(wrmux) will in charge of generating the Write-Back Data to a specific Register, one of the input signal of RegFile. In the block diagram before, this part is marked in red.

Normally, the write-back-data from Result Mux(resmux) will always be selected. However, when JAL/JALR is taken, signal PC+4 will be selected and stored into corresponding register. When LUI is taken, Imm-Gen will be selected while PC+Imm will be stored only when AUIPC is taken.

2 Waveform



3 Synthesis Report

3.1 Critical Path

Critical Path Length 5.31

Critical Path Slack -3.34

Levels of Logic: 37.00
Critical Path Length: 5.31
Critical Path Slack: -3.34
Critical Path Clk Period: 4.00
Total Negative Slack: -53820.01

No. of Violating Paths: 17417.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00

3.2 Area

Combinational Area: 93501.357157
Noncombinational Area: 115258.882369
Buf/Inv Area: 6168.074989
Total Buffer Area: 3058.11
Total Inverter Area: 3109.96
Macro/Black Box Area: 0.000000
Net Area: 155176.720782

Cell Area: 208760.239526
Design Area: 363936.960308

3.3 Power

Cell ——— **Internal Power** —— **Leakage Power**
Totals (55111 cells) ——— 27.879mW ——— 173.917mW

Hierarchy	Switch Power	Int Power	Leak Power	Total Power	%
riscv	137.750	2.79e+04	1.74e+11	2.02e+05	100.0
dp (Datapath)	136.488	2.79e+04	1.74e+11	2.02e+05	100.0
data_mem (datamemory)	68.062	2.61e+04	1.60e+11	1.86e+05	92.0
rf (RegFile)	30.839	1.65e+03	1.10e+10	1.27e+04	6.3
instr_mem (instructionmemory)	5.631	7.042	2.59e+08	272.088	0.1
_seo_mux_C8 (_seo_mux_C8)	5.471	6.987	2.55e+08	267.232	0.1