Hardware addresses and connector details

The memory mapping is as follows:

Devices	Address range	Type of memory
27256 at U21	0000 – 7FFF	Program memory (Read only)
628128 at U22	8000 – FFFF	User Program memory (uppar bank)
628128 at U22	0000 – 7FFF	User Data memory (lower bank)
628128 at U22	8000 – DFFF	User Data memory (lower bank)

The addresses of 8255 are as follows:

8255A at U11	Address	Usage	
			The signals are available on connector J3 (J7 for kit no 41 to 50 with USB port.
PORT A	E800H	Available to user	
PORT B	E801H	Available to user	
PORT C	E802H	Available to user	
COMMAND PORT	E803H	Available to user	

* Sometime the assembler will not accept the port addresses as e.g. E800H, in that case write the port addresses as " 0E800H".

** The connector numbers are J7, J8, J10 in place of J3, J4, J6 respectively for the kits with USB port (Kit No. 41 to 50).

J6 DATA & CONTROL LINES

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	BCLK	2	P1.5
3	P1.6	4	P1.4
5	P1.7	6	P1.3
7	INT1*	8	P1.2
9	IOP	10	-
11	PSEN*	12	RST
13	BWR*	14	P1.1
15	BRD*	16	P1.0
17	GND	18	GND
19	BD1	20	BD0
21	BD3	22	BD2
23	BD5	24	BD4
25	BD7	26	BD6

Note: '-' indicates No Connection

J3 (8255 –1 at U11) PORTS CONNECTOR

PIN NO	SIGNAL
1	P1C4
2	P1C5
3	P1C2
4	P1C3
5	P1C0
6	P1C1
7	P1B6
8	P1B7
9	P1B4
10	P1B5
11	P1B2
12	P1B3
13	P1B0

PIN NO	SIGNAL
14	P1B1
15	P1A6
16	P1A7
17	P1A4
18	P1A5
19	P1A2
20	P1A3
21	P1A0
22	P1A1
23	P1C6
24	P1C7
25	VCC
26	GND

J4 ADDRESS LINES

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	TIN	2	TOUT
3	-	4	-
5	INT1	6	-
7	-	8	ALE
9	BA15	10	BA14
11	BA13	12	BA12
13	BA11	14	BA10
15	BA9	16	BA8
17	VCC	18	VCC
19	BA7	20	BA6
21	BA5	22	BA4
23	BA3	24	BA2
25	BA1	26	BA0

VECTOR ADDRESS TABLE FOR INTERRUPTS

Function	Interrupt source	Vector address	Trainer Address
External Interrupt 0	IE0	0003H	25FEH
Timer0 Interrupt	TF0	000BH	FFF0H
External Interrupt 1	IE1	0013H	FFF3H
Timer1 Interrupt	TF1	001BH	FFF6H
Serial Interrupt	RI & TI	0023H	FFF9H