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CSCU9V4 Systems - Tutorial 4

1. CPUs contain a number of registers. Some are visible to the programmer, and some are not. Consider the following registers:

   MAR, MDR, General register 6, PC, and Instruction Register.

   - Which can the programmer "see" and which not?
   - Why do you think it is organised in this way?

   All instructions are first fetched from the main memory and then executed.
   - Describe how the PC, MAR, MDR, Instruction Register, General Registers, and ALU input and output registers are used in the transfer and then execution of the instruction:

   MUL R4, R5, R6

   (which multiplies the contents of general registers R4 and R5, and leaves the result in general register R6.)

2. A processor has a 36 bit wide MAR, and a 32 bit wide MDR. Cells are 1 byte.
   - How much memory can it address?

   The processor can execute 1,000,000,000 instructions per second, and each instruction is a 32-bit word.
   - If there was no cache, how much data would need to be transferred from the memory to the CPU per second just to keep the processor supplied with instructions?
   - If there was a cache on the CPU, and the hit rate was 97%, how much data would need to be transferred from the memory to the CPU per second to keep the processor supplied with instructions?

3. A synchronous bus runs at 133Mhz. Transfers are 32 bits wide.
   - If one transfer runs each cycle, what is the maximum data transfer rate of this bus?

   The bus can also be used in burst mode. In this mode, the address is provided, then up to 32 transfers occur. The first transfer is takes a whole cycle, but transfers after this run at two per cycle. (The last half-cycle is used to prepare for the next transfer).
   - What is the maximum overall data rate for burst transfers?