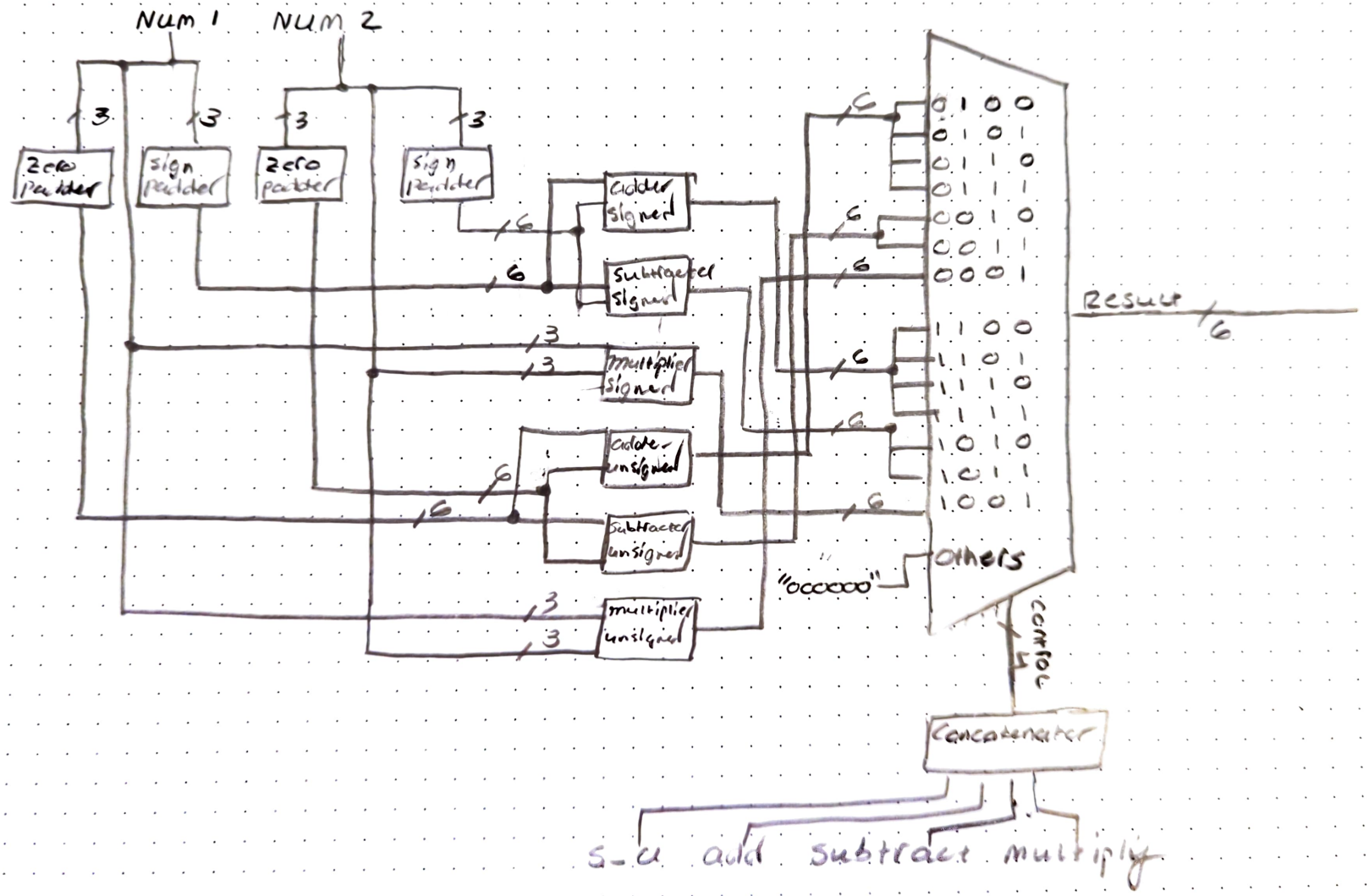
3 Bit ALU


Num 1
Num 2
3
3
3
3
zero padder
sign padder
zero padder
sign padder
6
6
adder signed
subtracter signed
3
3
multiplier signed
adder unsigned
6
6
subtracter unsigned
3
3
multiplier unsigned
6
6
6
6
6
"000000"
others
Result
6
control
4
Concatenator
S-U
add
subtract
multiply

```vhdl
-- VHDL 8 bit processor project
-- Three Bit ALU
-- James Hicks Oct 8 2023

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity three_bit_ALU is
    port (
            num1, num2      : in std_logic_vector (2 downto 0);
            s_u             : in std_logic;
            add             : in std_logic;
            subtract        : in std_logic;
            multiply        : in std_logic;
            result          : out std_logic_vector (5 downto 0)
        );
end three_bit_ALU;

architecture my_arch of three_bit_ALU is

    signal control : std_logic_vector (3 downto 0);

begin
    control <= s_u & add & subtract & multiply;
    with control select result <=
        std_logic_vector(unsigned("000" & num1) + unsigned(num2)) when "0100",
        std_logic_vector(unsigned("000" & num1) + unsigned(num2)) when "0101",
        std_logic_vector(unsigned("000" & num1) + unsigned(num2)) when "0110",
        std_logic_vector(unsigned("000" & num1) + unsigned(num2)) when "0111",
        std_logic_vector(unsigned("000" & num1) - unsigned(num2)) when "0010",
        std_logic_vector(unsigned("000" & num1) - unsigned(num2)) when "0011",
        std_logic_vector(unsigned(num1) * unsigned(num2)) when "0001",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) + signed(num2)) when
        "1100",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) + signed(num2)) when
        "1101",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) + signed(num2)) when
        "1110",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) + signed(num2)) when
        "1111",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) - signed(num2)) when
        "1010",
        std_logic_vector(signed(num1(2) & num1(2) & num1(2) & num1) - signed(num2)) when
        "1011",
        std_logic_vector(signed(num1) * signed(num2)) when "1001",
        "000000" when others;
end my_arch;
```

```vhdl
-- VHDL 8 bit processor project
-- Three Bit ALU Test Bench
-- James Hicks Oct 9 2023

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity three_bit_ALU_tb is
end three_bit_ALU_tb;

architecture tb_arch of three_bit_ALU_tb is

    signal num1, num2 : std_logic_vector(2 downto 0);
    signal control    : std_logic_vector(3 downto 0);
    signal result     : std_logic_vector(5 downto 0);

begin

    DUT : entity work.three_bit_ALU(my_arch)
        port map (
                    num1 => num1,
                    num2 => num2,
                    s_u => control(3),
                    add => control(2),
                    subtract => control(1),
                    multiply => control(0),
                    result => result
                );

    process begin
        for I in 0 to 15 loop
            num1 <= "101"; -- <- modify this for testing
            num2 <= "110"; -- <- modify this for testing
            control <= std_logic_vector(to_unsigned(I,4));
            wait for 1 ns;
        end loop;

        assert false report "end of test";
        wait;

    end process;

end tb_arch;
```

Documents\NES Clone Project\NES_Clone\VHDL Files\src\ALU\sim-1-1.vcd

View Help

From: 0 sec To: 8 ns | Marker: 11040 ps | Cursor: 0 sec

gnals

ime

7 and 7 unsigned

ontrol <= s_u & add & subtract & multiply

result is unsigned decimal

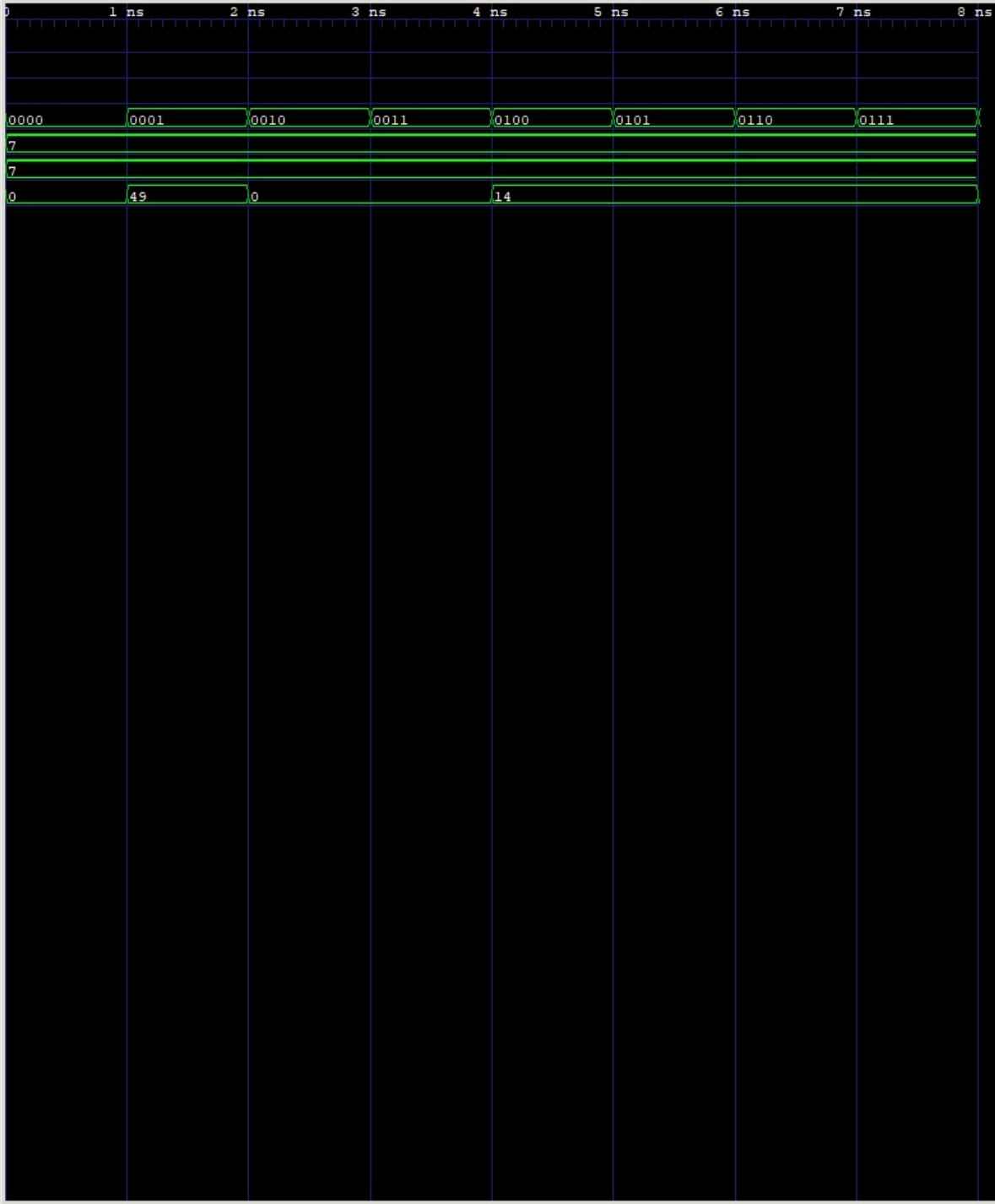
control[3:0] =1011

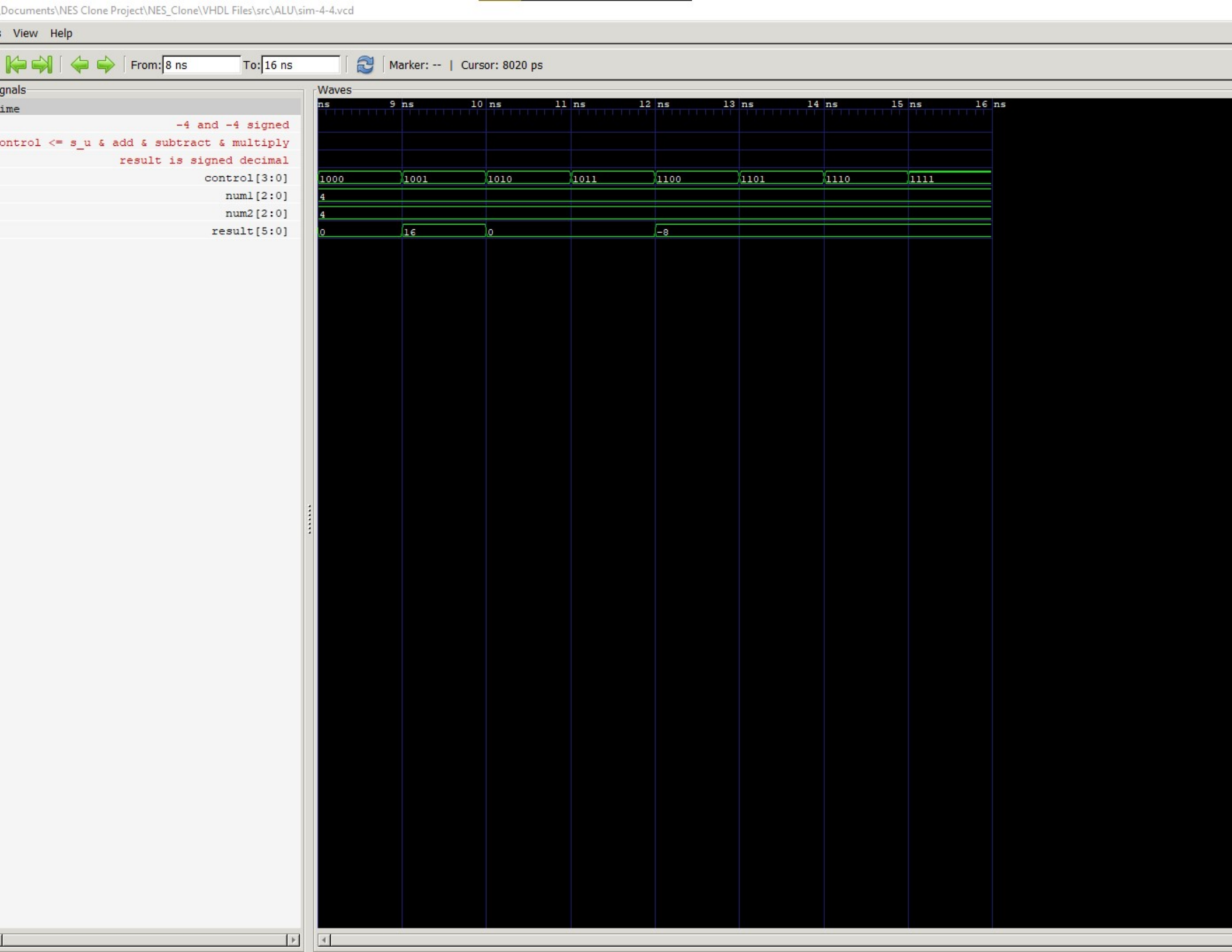
num1[2:0] =7

num2[2:0] =7

result[5:0] =0

Waves




Documents\NES Clone Project\NES_Clone\VHDL Files\src\ALU\sim-4-4.vcd
View
Help
From: 8 ns
To: 16 ns
Marker: --
Cursor: 8020 ps
gnals
ime
-4 and -4 signed
ontrol <= s_u & add & subtract & multiply
result is signed decimal
control[3:0]
num1[2:0]
num2[2:0]
result[5:0]
Waves
ns
9 ns
10 ns
11 ns
12 ns
13 ns
14 ns
15 ns
16 ns
1000
1001
1010
1011
1100
1101
1110
1111
4
4
0
16
0
-8

Documents\NES Clone Project\NES_Clone\VHDL Files\src\ALU\sim-4-4.vcd

View Help

From: 0 sec To: 8 ns Marker: -- | Cursor: 10 ps

gnals

ime

4 and 4 unsigned

ontrol <= s_u & add & subtract & multiply

result is signed decimal

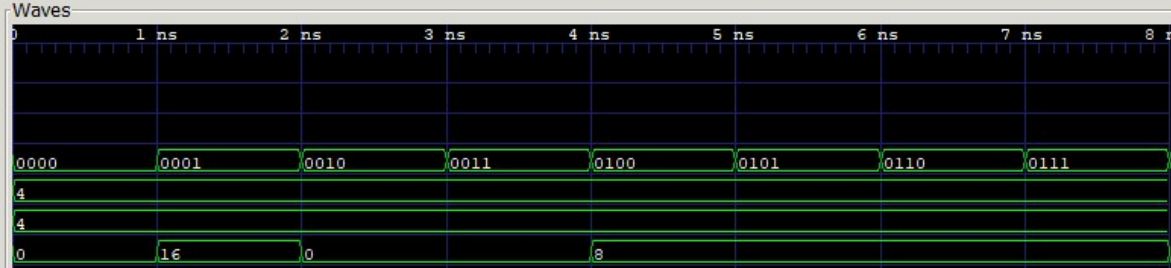
control[3:0]

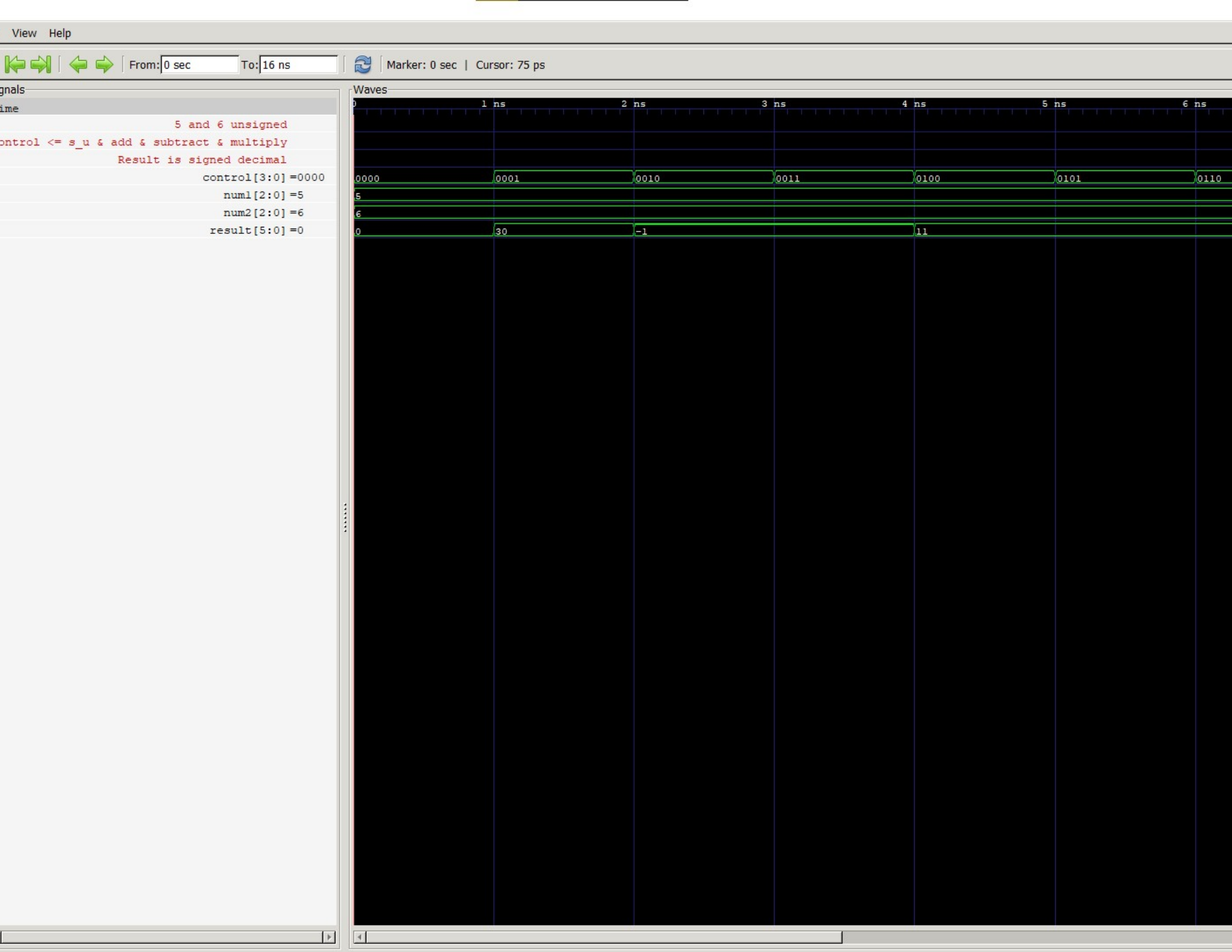
num1[2:0]

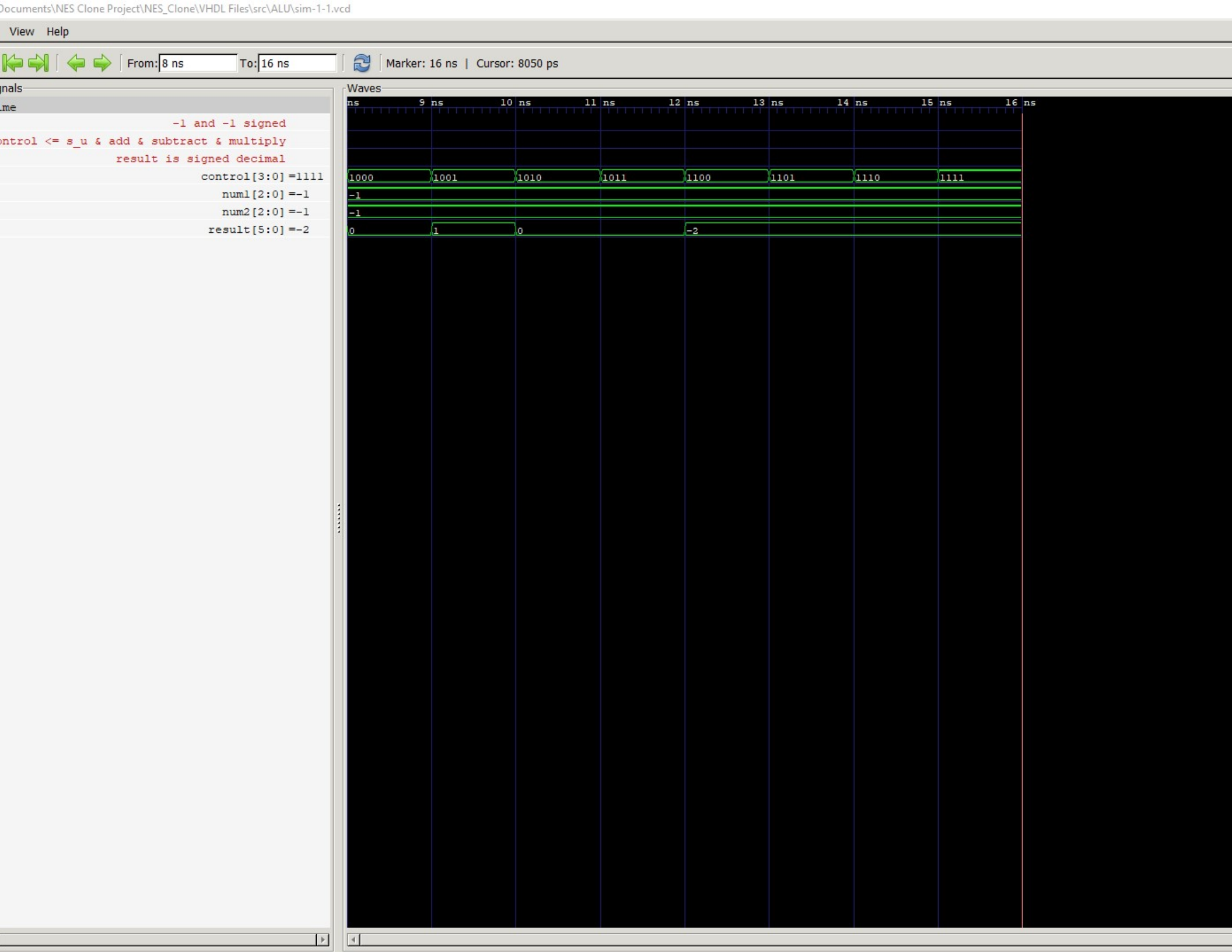
num2[2:0]

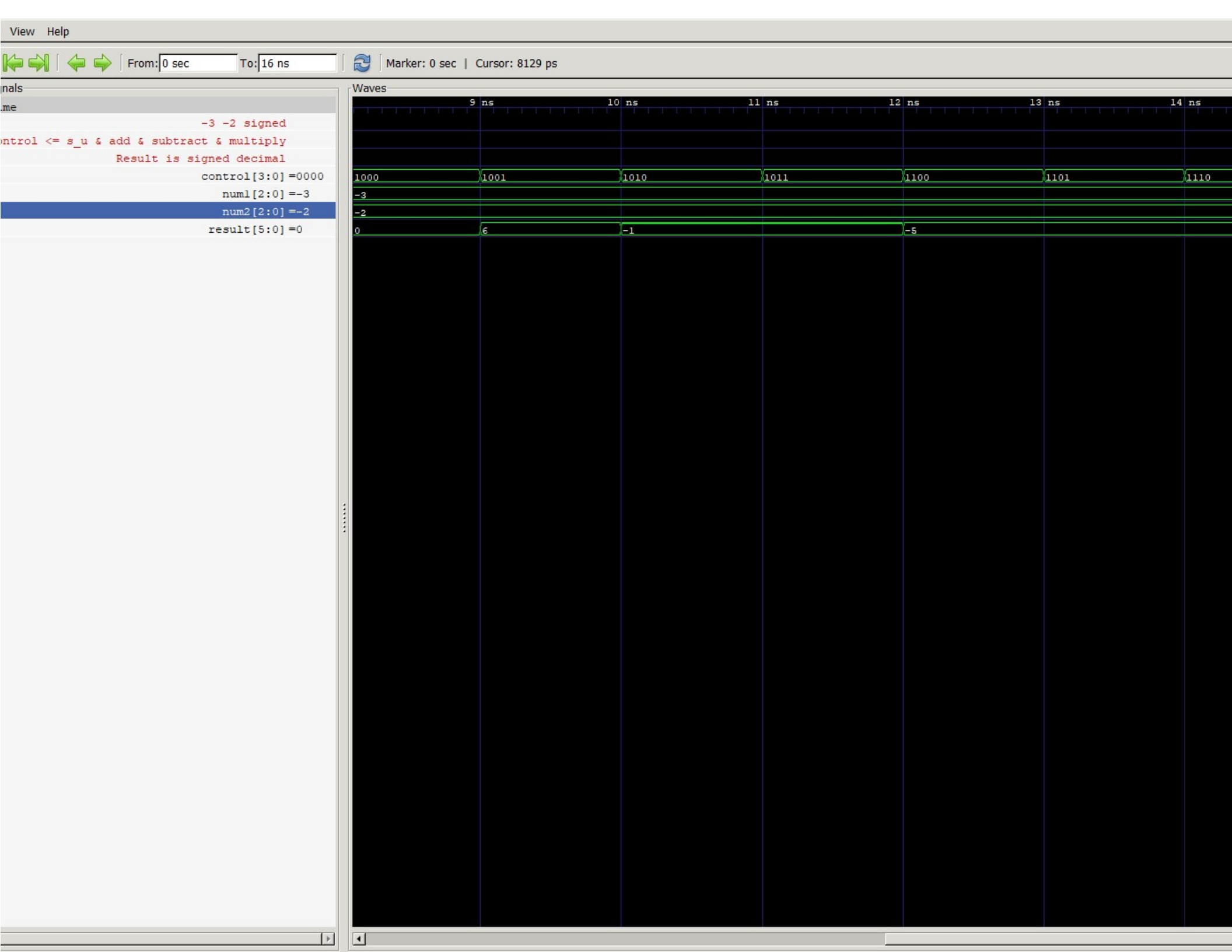
result[5:0]

Waves




View
Help
From: 0 sec
To: 16 ns
Marker: 0 sec | Cursor: 75 ps
gnals
ime
5 and 6 unsigned
ontrol <= s_u & add & subtract & multiply
Result is signed decimal
control[3:0] =0000
num1[2:0] =5
num2[2:0] =6
result[5:0] =0
Waves
1 ns
2 ns
3 ns
4 ns
5 ns
6 ns
0000
0001
0010
0011
0100
0101
0110
5
6
0
30
-1
11


Documents\NES Clone Project\NES_Clone\VHDL Files\src\ALU\sim-1-1.vcd
View
Help
From: 8 ns
To: 16 ns
Marker: 16 ns | Cursor: 8050 ps
gnals
me
-1 and -1 signed
ontrol <= s_u & add & subtract & multiply
result is signed decimal
control[3:0] =1111
num1[2:0] =-1
num2[2:0] =-1
result[5:0] =-2
Waves
ns
9 ns
10 ns
11 ns
12 ns
13 ns
14 ns
15 ns
16 ns
1000
1001
1010
1011
1100
1101
1110
1111
-1
-1
0
1
0
-2


View
Help
From: 0 sec
To: 16 ns
Marker: 0 sec | Cursor: 8129 ps
nals
me
-3 -2 signed
ntrol <= s_u & add & subtract & multiply
Result is signed decimal
control[3:0] =0000
num1[2:0] =-3
num2[2:0] =-2
result[5:0] =0
Waves
9 ns
10 ns
11 ns
12 ns
13 ns
14 ns
1000
1001
1010
1011
1100
1101
1110
-3
-2
0
6
-1
-5

```
## This file is a general .xdc for the Nexys A7-100T
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
#set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];


##Switches
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { num2[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { num2[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { num2[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { num1[0] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { num1[1] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { num1[2] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
#set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { SW[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
#set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { SW[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
#set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO L24N T3 34 Sch=sw[8]
#set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
#set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
#set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO L23P T3 A03 D19 14 Sch=sw[11]
set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { s_u }]; #IO_L24P_T3_35 Sch=sw[12]
set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { multiply }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { subtract }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { add }]; #IO_L21P_T3_DQS_14 Sch=sw[15]

## LEDs
set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { result[0] }]; #IO_L18P_T2_A24_15 Sch=led[0]
set_property -dict { PACKAGE_PIN K15   IOSTANDARD LVCMOS33 } [get_ports { result[1] }]; #IO_L24P_T3_RS1_15 Sch=led[1]
set_property -dict { PACKAGE_PIN J13   IOSTANDARD LVCMOS33 } [get_ports { result[2] }]; #IO_L17N_T2_A25_15 Sch=led[2]
set_property -dict { PACKAGE_PIN N14   IOSTANDARD LVCMOS33 } [get_ports { result[3] }]; #IO_L8P_T1_D11_14 Sch=led[3]
set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports { result[4] }]; #IO_L7P_T1_D09_14 Sch=led[4]
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports { result[5] }]; #IO_L18N_T2_A11_D27_14 Sch=led[5]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports { LED[6] }]; #IO_L17P_T2_A14_D30_14 Sch=led[6]
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports { LED[7] }]; #IO_L18P_T2_A12_D28_14 Sch=led[7]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports { LED[8] }]; #IO_L16N_T2_A15_D31_14 Sch=led[8]
#set_property -dict { PACKAGE_PIN T15   IOSTANDARD LVCMOS33 } [get_ports { LED[9] }]; #IO_L14N_T2_SRCC_14 Sch=led[9]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports { LED[10] }]; #IO_L22P_T3_A05_D21_14 Sch=led[10]
#set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCMOS33 } [get_ports { LED[11] }]; #IO_L15N_T2_DQS_DOUT_CSO_B_14 Sch=led[11]
```

```
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports { LED[12] }]; #IO_L16P_T2_CSI_B_14 Sch=led[12]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports { LED[13] }]; #IO_L22N_T3_A04_D20_14 Sch=led[13]
#set_property -dict { PACKAGE_PIN V12   IOSTANDARD LVCMOS33 } [get_ports { LED[14] }]; #IO_L20N_T3_A07_D23_14 Sch=led[14]
#set_property -dict { PACKAGE_PIN V11   IOSTANDARD LVCMOS33 } [get_ports { LED[15] }]; #IO_L21N_T3_DQS_A06_D22_14 Sch=led[15]

## RGB LEDs
#set_property -dict { PACKAGE_PIN R12   IOSTANDARD LVCMOS33 } [get_ports { LED16_B }]; #IO_L5P_T0_D06_14 Sch=led16_b
#set_property -dict { PACKAGE_PIN M16   IOSTANDARD LVCMOS33 } [get_ports { LED16_G }]; #IO_L10P_T1_D14_14 Sch=led16_g
#set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { LED16_R }]; #IO_L11P_T1_SRCC_14 Sch=led16_r
#set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { LED17_B }]; #IO_L15N_T2_DQS_ADV_B_15 Sch=led17_b
#set_property -dict { PACKAGE_PIN R11   IOSTANDARD LVCMOS33 } [get_ports { LED17_G }]; #IO_0_14 Sch=led17_g
#set_property -dict { PACKAGE_PIN N16   IOSTANDARD LVCMOS33 } [get_ports { LED17_R }]; #IO_L11N_T1_SRCC_14 Sch=led17_r

##7 segment display
#set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { CA }]; #IO_L24N_T3_A00_D16_14 Sch=ca
#set_property -dict { PACKAGE_PIN R10   IOSTANDARD LVCMOS33 } [get_ports { CB }]; #IO_25_14 Sch=cb
#set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports { CC }]; #IO_25_15 Sch=cc
#set_property -dict { PACKAGE_PIN K13   IOSTANDARD LVCMOS33 } [get_ports { CD }]; #IO_L17P_T2_A26_15 Sch=cd
#set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { CE }]; #IO_L13P_T2_MRCC_14 Sch=ce
#set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports { CF }]; #IO_L19P_T3_A10_D26_14 Sch=cf
#set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports { CG }]; #IO_L4P_T0_D04_14 Sch=cg
#set_property -dict { PACKAGE_PIN H15   IOSTANDARD LVCMOS33 } [get_ports { DP }]; #IO_L19N_T3_A21_VREF_15 Sch=dp
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports { AN[0] }]; #IO_L23P_T3_FOE_B_15 Sch=an[0]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports { AN[1] }]; #IO_L23N_T3_FWE_B_15 Sch=an[1]
#set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { AN[2] }]; #IO_L24P_T3_A01_D17_14 Sch=an[2]
#set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports { AN[3] }]; #IO_L19P_T3_A22_15 Sch=an[3]
#set_property -dict { PACKAGE_PIN P14   IOSTANDARD LVCMOS33 } [get_ports { AN[4] }]; #IO_L8N_T1_D12_14 Sch=an[4]
#set_property -dict { PACKAGE_PIN T14   IOSTANDARD LVCMOS33 } [get_ports { AN[5] }]; #IO_L14P_T2_SRCC_14 Sch=an[5]
#set_property -dict { PACKAGE_PIN K2    IOSTANDARD LVCMOS33 } [get_ports { AN[6] }]; #IO_L23P_T3_35 Sch=an[6]
#set_property -dict { PACKAGE_PIN U13   IOSTANDARD LVCMOS33 } [get_ports { AN[7] }]; #IO_L23N_T3_A02_D18_14 Sch=an[7]

##Buttons
#set_property -dict { PACKAGE_PIN C12   IOSTANDARD LVCMOS33 } [get_ports { CPU_RESETN }]; #IO_L3P_T0_DQS_AD1P_15 Sch=cpu_resetn
#set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports { BTNC }]; #IO_L9P_T1_DQS_14 Sch=btnc
#set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports { BTNU }]; #IO_L4N_T0_D05_14 Sch=btnu
#set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports { BTNL }]; #IO_L12P_T1_MRCC_14 Sch=btnl
#set_property -dict { PACKAGE_PIN M17   IOSTANDARD LVCMOS33 } [get_ports { BTNR }]; #IO_L10N_T1_D15_14 Sch=btnr
#set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports { BTND }]; #IO_L9N_T1_DQS_D13_14 Sch=btnd


```

```
82  ##Pmod Headers
83  ##Pmod Header JA
84  #set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports { JA[1] }];
    #IO_L20N_T3_A19_15 Sch=ja[1]
85  #set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { JA[2] }];
    #IO_L21N_T3_DQS_A18_15 Sch=ja[2]
86  #set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports { JA[3] }];
    #IO_L21P_T3_DQS_15 Sch=ja[3]
87  #set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports { JA[4] }];
    #IO_L18N_T2_A23_15 Sch=ja[4]
88  #set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports { JA[7] }];
    #IO_L16N_T2_A27_15 Sch=ja[7]
89  #set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports { JA[8] }];
    #IO_L16P_T2_A28_15 Sch=ja[8]
90  #set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports { JA[9] }];
    #IO_L22N_T3_A16_15 Sch=ja[9]
91  #set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports { JA[10] }];
    #IO_L22P_T3_A17_15 Sch=ja[10]
92
93  ##Pmod Header JB
94  #set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { JB[1] }];
    #IO_L1P_T0_AD0P_15 Sch=jb[1]
95  #set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { JB[2] }];
    #IO_L14N_T2_SRCC_15 Sch=jb[2]
96  #set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { JB[3] }];
    #IO_L13N_T2_MRCC_15 Sch=jb[3]
97  #set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports { JB[4] }];
    #IO_L15P_T2_DQS_15 Sch=jb[4]
98  #set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports { JB[7] }];
    #IO_L11N_T1_SRCC_15 Sch=jb[7]
99  #set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [get_ports { JB[8] }];
    #IO_L5P_T0_AD9P_15 Sch=jb[8]
100 #set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [get_ports { JB[9] }];
    #IO_0_15 Sch=jb[9]
101 #set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { JB[10] }];
    #IO_L13P_T2_MRCC_15 Sch=jb[10]
102
103 ##Pmod Header JC
104 #set_property -dict { PACKAGE_PIN K1    IOSTANDARD LVCMOS33 } [get_ports { JC[1] }];
    #IO_L23N_T3_35 Sch=jc[1]
105 #set_property -dict { PACKAGE_PIN F6    IOSTANDARD LVCMOS33 } [get_ports { JC[2] }];
    #IO_L19N_T3_VREF_35 Sch=jc[2]
106 #set_property -dict { PACKAGE_PIN J2    IOSTANDARD LVCMOS33 } [get_ports { JC[3] }];
    #IO_L22N_T3_35 Sch=jc[3]
107 #set_property -dict { PACKAGE_PIN G6    IOSTANDARD LVCMOS33 } [get_ports { JC[4] }];
    #IO_L19P_T3_35 Sch=jc[4]
108 #set_property -dict { PACKAGE_PIN E7    IOSTANDARD LVCMOS33 } [get_ports { JC[7] }];
    #IO_L6P_T0_35 Sch=jc[7]
109 #set_property -dict { PACKAGE_PIN J3    IOSTANDARD LVCMOS33 } [get_ports { JC[8] }];
    #IO_L22P_T3_35 Sch=jc[8]
110 #set_property -dict { PACKAGE_PIN J4    IOSTANDARD LVCMOS33 } [get_ports { JC[9] }];
    #IO_L21P_T3_DQS_35 Sch=jc[9]
111 #set_property -dict { PACKAGE_PIN E6    IOSTANDARD LVCMOS33 } [get_ports { JC[10] }];
    #IO_L5P_T0_AD13P_35 Sch=jc[10]
112
113 ##Pmod Header JD
114 #set_property -dict { PACKAGE_PIN H4    IOSTANDARD LVCMOS33 } [get_ports { JD[1] }];
    #IO_L21N_T3_DQS_35 Sch=jd[1]
115 #set_property -dict { PACKAGE_PIN H1    IOSTANDARD LVCMOS33 } [get_ports { JD[2] }];
    #IO_L17P_T2_35 Sch=jd[2]
116 #set_property -dict { PACKAGE_PIN G1    IOSTANDARD LVCMOS33 } [get_ports { JD[3] }];
    #IO_L17N_T2_35 Sch=jd[3]
117 #set_property -dict { PACKAGE_PIN G3    IOSTANDARD LVCMOS33 } [get_ports { JD[4] }];
    #IO_L20N_T3_35 Sch=jd[4]
118 #set_property -dict { PACKAGE_PIN H2    IOSTANDARD LVCMOS33 } [get_ports { JD[7] }];
    #IO_L15P_T2_DQS_35 Sch=jd[7]
119 #set_property -dict { PACKAGE_PIN G4    IOSTANDARD LVCMOS33 } [get_ports { JD[8] }];
    #IO_L20P_T3_35 Sch=jd[8]
120 #set_property -dict { PACKAGE_PIN G2    IOSTANDARD LVCMOS33 } [get_ports { JD[9] }];
    #IO_L15N_T2_DQS_35 Sch=jd[9]
121 #set_property -dict { PACKAGE_PIN F3    IOSTANDARD LVCMOS33 } [get_ports { JD[10] }];
    #IO_L13N_T2_MRCC_35 Sch=jd[10]
```

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122
123 ##Pmod Header JXADC
124 #set_property -dict { PACKAGE_PIN A14 IOSTANDARD LVCMOS33 } [get_ports { XA_N[1] }];
    #IO_L9N_T1_DQS_AD3N_15 Sch=xa_n[1]
125 #set_property -dict { PACKAGE_PIN A13 IOSTANDARD LVCMOS33 } [get_ports { XA_P[1] }];
    #IO_L9P_T1_DQS_AD3P_15 Sch=xa_p[1]
126 #set_property -dict { PACKAGE_PIN A16 IOSTANDARD LVCMOS33 } [get ports { XA N[2] }];
    #IO_L8N_T1_AD10N_15 Sch=xa_n[2]
127 #set_property -dict { PACKAGE_PIN A15 IOSTANDARD LVCMOS33 } [get_ports { XA_P[2] }];
    #IO_L8P_T1_AD10P_15 Sch=xa_p[2]
128 #set_property -dict { PACKAGE_PIN B17 IOSTANDARD LVCMOS33 } [get_ports { XA_N[3] }];
    #IO_L7N_T1_AD2N_15 Sch=xa_n[3]
129 #set_property -dict { PACKAGE_PIN B16 IOSTANDARD LVCMOS33 } [get ports { XA P[3] }];
    #IO_L7P_T1_AD2P_15 Sch=xa_p[3]
130 #set_property -dict { PACKAGE_PIN A18 IOSTANDARD LVCMOS33 } [get_ports { XA_N[4] }];
    #IO_L10N_T1_AD11N_15 Sch=xa_n[4]
131 #set_property -dict { PACKAGE_PIN B18 IOSTANDARD LVCMOS33 } [get_ports { XA_P[4] }];
    #IO_L10P_T1_AD11P_15 Sch=xa_p[4]
132
133 ##VGA Connector
134 #set_property -dict { PACKAGE_PIN A3 IOSTANDARD LVCMOS33 } [get_ports { VGA_R[0] }];
    #IO_L8N_T1_AD14N_35 Sch=vga_r[0]
135 #set_property -dict { PACKAGE_PIN B4 IOSTANDARD LVCMOS33 } [get_ports { VGA_R[1] }];
    #IO_L7N_T1_AD6N_35 Sch=vga_r[1]
136 #set_property -dict { PACKAGE_PIN C5 IOSTANDARD LVCMOS33 } [get_ports { VGA_R[2] }];
    #IO_L1N_T0_AD4N_35 Sch=vga_r[2]
137 #set_property -dict { PACKAGE_PIN A4 IOSTANDARD LVCMOS33 } [get_ports { VGA_R[3] }];
    #IO_L8P_T1_AD14P_35 Sch=vga_r[3]
138 #set_property -dict { PACKAGE_PIN C6 IOSTANDARD LVCMOS33 } [get_ports { VGA_G[0] }];
    #IO_L1P_T0_AD4P_35 Sch=vga_g[0]
139 #set_property -dict { PACKAGE_PIN A5 IOSTANDARD LVCMOS33 } [get_ports { VGA_G[1] }];
    #IO L3N T0 DQS AD5N 35 Sch=vga g[1]
140 #set_property -dict { PACKAGE_PIN B6 IOSTANDARD LVCMOS33 } [get_ports { VGA_G[2] }];
    #IO_L2N_T0_AD12N_35 Sch=vga_g[2]
141 #set_property -dict { PACKAGE_PIN A6 IOSTANDARD LVCMOS33 } [get_ports { VGA_G[3] }];
    #IO_L3P_T0_DQS_AD5P_35 Sch=vga_g[3]
142 #set_property -dict { PACKAGE_PIN B7 IOSTANDARD LVCMOS33 } [get_ports { VGA_B[0] }];
    #IO L2P T0 AD12P 35 Sch=vga b[0]
143 #set_property -dict { PACKAGE_PIN C7 IOSTANDARD LVCMOS33 } [get_ports { VGA_B[1] }];
    #IO_L4N_T0_35 Sch=vga_b[1]
144 #set_property -dict { PACKAGE_PIN D7 IOSTANDARD LVCMOS33 } [get_ports { VGA_B[2] }];
    #IO_L6N_T0_VREF_35 Sch=vga_b[2]
145 #set_property -dict { PACKAGE_PIN D8 IOSTANDARD LVCMOS33 } [get_ports { VGA_B[3] }];
    #IO_L4P_T0_35 Sch=vga_b[3]
146 #set_property -dict { PACKAGE_PIN B11 IOSTANDARD LVCMOS33 } [get_ports { VGA_HS }];
    #IO_L4P_T0_15 Sch=vga_hs
147 #set_property -dict { PACKAGE_PIN B12 IOSTANDARD LVCMOS33 } [get_ports { VGA_VS }];
    #IO_L3N_T0_DQS_AD1N_15 Sch=vga_vs
148
149 ##Micro SD Connector
150 #set_property -dict { PACKAGE_PIN E2 IOSTANDARD LVCMOS33 } [get_ports { SD_RESET }];
    #IO_L14P_T2_SRCC_35 Sch=sd_reset
151 #set_property -dict { PACKAGE_PIN A1 IOSTANDARD LVCMOS33 } [get_ports { SD_CD }];
    #IO_L9N_T1_DQS_AD7N_35 Sch=sd_cd
152 #set_property -dict { PACKAGE_PIN B1 IOSTANDARD LVCMOS33 } [get_ports { SD_SCK }];
    #IO_L9P_T1_DQS_AD7P_35 Sch=sd_sck
153 #set_property -dict { PACKAGE_PIN C1 IOSTANDARD LVCMOS33 } [get ports { SD CMD }];
    #IO_L16N_T2_35 Sch=sd_cmd
154 #set_property -dict { PACKAGE_PIN C2 IOSTANDARD LVCMOS33 } [get_ports { SD_DAT[0] }];
    #IO_L16P_T2_35 Sch=sd_dat[0]
155 #set_property -dict { PACKAGE_PIN E1 IOSTANDARD LVCMOS33 } [get_ports { SD_DAT[1] }];
    #IO_L18N_T2_35 Sch=sd_dat[1]
156 #set_property -dict { PACKAGE_PIN F1 IOSTANDARD LVCMOS33 } [get ports { SD DAT[2] }];
    #IO_L18P_T2_35 Sch=sd_dat[2]
157 #set_property -dict { PACKAGE_PIN D2 IOSTANDARD LVCMOS33 } [get_ports { SD_DAT[3] }];
    #IO_L14N_T2_SRCC_35 Sch=sd_dat[3]
158
159 ##Accelerometer
160 #set_property -dict { PACKAGE_PIN E15 IOSTANDARD LVCMOS33 } [get_ports { ACL_MISO }];
    #IO_L11P_T1_SRCC_15 Sch=acl_miso
161 #set_property -dict { PACKAGE_PIN F14 IOSTANDARD LVCMOS33 } [get_ports { ACL_MOSI }];
    #IO_L5N_T0_AD9N_15 Sch=acl_mosi
```

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#set_property -dict { PACKAGE_PIN F15   IOSTANDARD LVCMOS33 } [get_ports { ACL_SCLK }]; #IO_L14P_T2_SRCC_15 Sch=acl_sclk
#set_property -dict { PACKAGE_PIN D15   IOSTANDARD LVCMOS33 } [get_ports { ACL_CSN }]; #IO_L12P_T1_MRCC_15 Sch=acl_csn
#set_property -dict { PACKAGE_PIN B13   IOSTANDARD LVCMOS33 } [get_ports { ACL_INT[1] }]; #IO_L2P_T0_AD8P_15 Sch=acl_int[1]
#set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports { ACL_INT[2] }]; #IO_L20P_T3_A20_15 Sch=acl_int[2]

##Temperature Sensor
#set_property -dict { PACKAGE_PIN C14   IOSTANDARD LVCMOS33 } [get_ports { TMP_SCL }]; #IO_L1N_T0_AD0N_15 Sch=tmp_scl
#set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports { TMP_SDA }]; #IO_L12N_T1_MRCC_15 Sch=tmp_sda
#set_property -dict { PACKAGE_PIN D13   IOSTANDARD LVCMOS33 } [get_ports { TMP_INT }]; #IO_L6N_T0_VREF_15 Sch=tmp_int
#set_property -dict { PACKAGE_PIN B14   IOSTANDARD LVCMOS33 } [get_ports { TMP_CT }]; #IO_L2N_T0_AD8N_15 Sch=tmp_ct

##Omnidirectional Microphone
#set_property -dict { PACKAGE_PIN J5    IOSTANDARD LVCMOS33 } [get_ports { M_CLK }]; #IO_25_35 Sch=m_clk
#set_property -dict { PACKAGE_PIN H5    IOSTANDARD LVCMOS33 } [get_ports { M_DATA }]; #IO_L24N_T3_35 Sch=m_data
#set_property -dict { PACKAGE_PIN F5    IOSTANDARD LVCMOS33 } [get_ports { M_LRSEL }]; #IO_0_35 Sch=m_lrsel

##PWM Audio Amplifier
#set_property -dict { PACKAGE_PIN A11   IOSTANDARD LVCMOS33 } [get_ports { AUD_PWM }]; #IO_L4N_T0_15 Sch=aud_pwm
#set_property -dict { PACKAGE_PIN D12   IOSTANDARD LVCMOS33 } [get_ports { AUD_SD }]; #IO L6P T0 15 Sch=aud sd

##USB-RS232 Interface
#set_property -dict { PACKAGE_PIN C4    IOSTANDARD LVCMOS33 } [get_ports { UART_TXD_IN }]; #IO_L7P_T1_AD6P_35 Sch=uart_txd_in
#set_property -dict { PACKAGE_PIN D4    IOSTANDARD LVCMOS33 } [get_ports { UART_RXD_OUT }]; #IO L11N T1 SRCC 35 Sch=uart rxd out
#set_property -dict { PACKAGE_PIN D3    IOSTANDARD LVCMOS33 } [get_ports { UART_CTS }]; #IO_L12N_T1_MRCC_35 Sch=uart_cts
#set_property -dict { PACKAGE_PIN E5    IOSTANDARD LVCMOS33 } [get_ports { UART_RTS }]; #IO_L5N_T0_AD13N_35 Sch=uart_rts

##USB HID (PS/2)
#set_property -dict { PACKAGE_PIN F4    IOSTANDARD LVCMOS33 } [get_ports { PS2_CLK }]; #IO_L13P_T2_MRCC_35 Sch=ps2_clk
#set_property -dict { PACKAGE_PIN B2    IOSTANDARD LVCMOS33 } [get_ports { PS2_DATA }]; #IO_L10N_T1_AD15N_35 Sch=ps2_data

##SMSC Ethernet PHY
#set_property -dict { PACKAGE_PIN C9    IOSTANDARD LVCMOS33 } [get_ports { ETH_MDC }]; #IO_L11P_T1_SRCC_16 Sch=eth_mdc
#set_property -dict { PACKAGE_PIN A9    IOSTANDARD LVCMOS33 } [get_ports { ETH_MDIO }]; #IO_L14N_T2_SRCC_16 Sch=eth_mdio
#set_property -dict { PACKAGE_PIN B3    IOSTANDARD LVCMOS33 } [get_ports { ETH_RSTN }]; #IO_L10P_T1_AD15P_35 Sch=eth_rstn
#set_property -dict { PACKAGE_PIN D9    IOSTANDARD LVCMOS33 } [get_ports { ETH_CRSDV }]; #IO_L6N_T0_VREF_16 Sch=eth_crsdv
#set_property -dict { PACKAGE_PIN C10   IOSTANDARD LVCMOS33 } [get_ports { ETH_RXERR }]; #IO_L13N_T2_MRCC_16 Sch=eth_rxerr
#set_property -dict { PACKAGE_PIN C11   IOSTANDARD LVCMOS33 } [get_ports { ETH_RXD[0] }]; #IO_L13P_T2_MRCC_16 Sch=eth_rxd[0]
#set_property -dict { PACKAGE_PIN D10   IOSTANDARD LVCMOS33 } [get_ports { ETH_RXD[1] }]; #IO_L19N_T3_VREF_16 Sch=eth_rxd[1]
#set_property -dict { PACKAGE_PIN B9    IOSTANDARD LVCMOS33 } [get_ports { ETH_TXEN }]; #IO_L11N_T1_SRCC_16 Sch=eth_txen
#set_property -dict { PACKAGE_PIN A10   IOSTANDARD LVCMOS33 } [get_ports { ETH_TXD[0] }]; #IO_L14P_T2_SRCC_16 Sch=eth_txd[0]
#set_property -dict { PACKAGE_PIN A8    IOSTANDARD LVCMOS33 } [get_ports { ETH_TXD[1] }]; #IO_L12N_T1_MRCC_16 Sch=eth_txd[1]
#set_property -dict { PACKAGE_PIN D5    IOSTANDARD LVCMOS33 } [get_ports { ETH_REFCLK }]; #IO_L11P_T1_SRCC_35 Sch=eth_refclk
```

```
#set_property -dict { PACKAGE_PIN B8    IOSTANDARD LVCMOS33 } [get_ports { ETH_INTN }]; #IO_L12P_T1_MRCC_16 Sch=eth_intn

##Quad SPI Flash
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports { QSPI_DQ[0] }]; #IO_L1P_T0_D00_MOSI_14 Sch=qspi_dq[0]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports { QSPI_DQ[1] }]; #IO_L1N_T0_D01_DIN_14 Sch=qspi_dq[1]
#set_property -dict { PACKAGE_PIN L14   IOSTANDARD LVCMOS33 } [get_ports { QSPI_DQ[2] }]; #IO_L2P_T0_D02_14 Sch=qspi_dq[2]
#set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { QSPI_DQ[3] }]; #IO_L2N_T0_D03_14 Sch=qspi_dq[3]
#set_property -dict { PACKAGE_PIN L13   IOSTANDARD LVCMOS33 } [get_ports { QSPI_CSN }]; #IO_L6P_T0_FCS_B_14 Sch=qspi_csn
```

Since inputs are `STD_LOGIC_VECTORs`, you will need to convert them appropriately.

A. Design

The absolute first thing you should do is generate

a. The block diagram of the entity (i.e., just I/O ports), and
b. A neat and carefully labeled schematic of your circuit.

B. VHDL code:

Generate your VHDL code following your schematic exactly.

C. Testing:

Make sure you test a few cases, including extremes. For extra credit: if $s\_\bar{u} = 1$, your simulation should be presented as *signed decimals*; if $s\_\bar{u} = 0$, the simulation should use *unsigned decimals*. It is fine if you present the two simulations in two separate plots (i.e., no need to attempt to do both simulations in a single run, although you can if you want to).

D. Implementation

Download your system to the board. Verify its operation. Have the instructor check your implementation.

James Hicks

Lab 3: Your Name

+Exc

Instructor signature

Deliverables:

1. **(4 pts)** Copies of your block diagram and the carefully drawn and labeled circuit schematic.
2. **(4 pts)** A color-coded, readable version of each the VHDL code for your component(s).
3. **(4 pts)** A color-coded, readable version of each the VHDL code of your testbench.
4. **(4 pts)** Legible copies of your simulations. Make sure that you provide appropriate comments wherever needed, e.g., if something is not what you expected, or if the system fails, etc.
5. **(1 pt)** A copy of your constraints file.
6. **(3 pts)** A copy of the instructor signature.

All the deliverables should be in PDF format.

How to turn this in?

You should turn this in via Canvas.