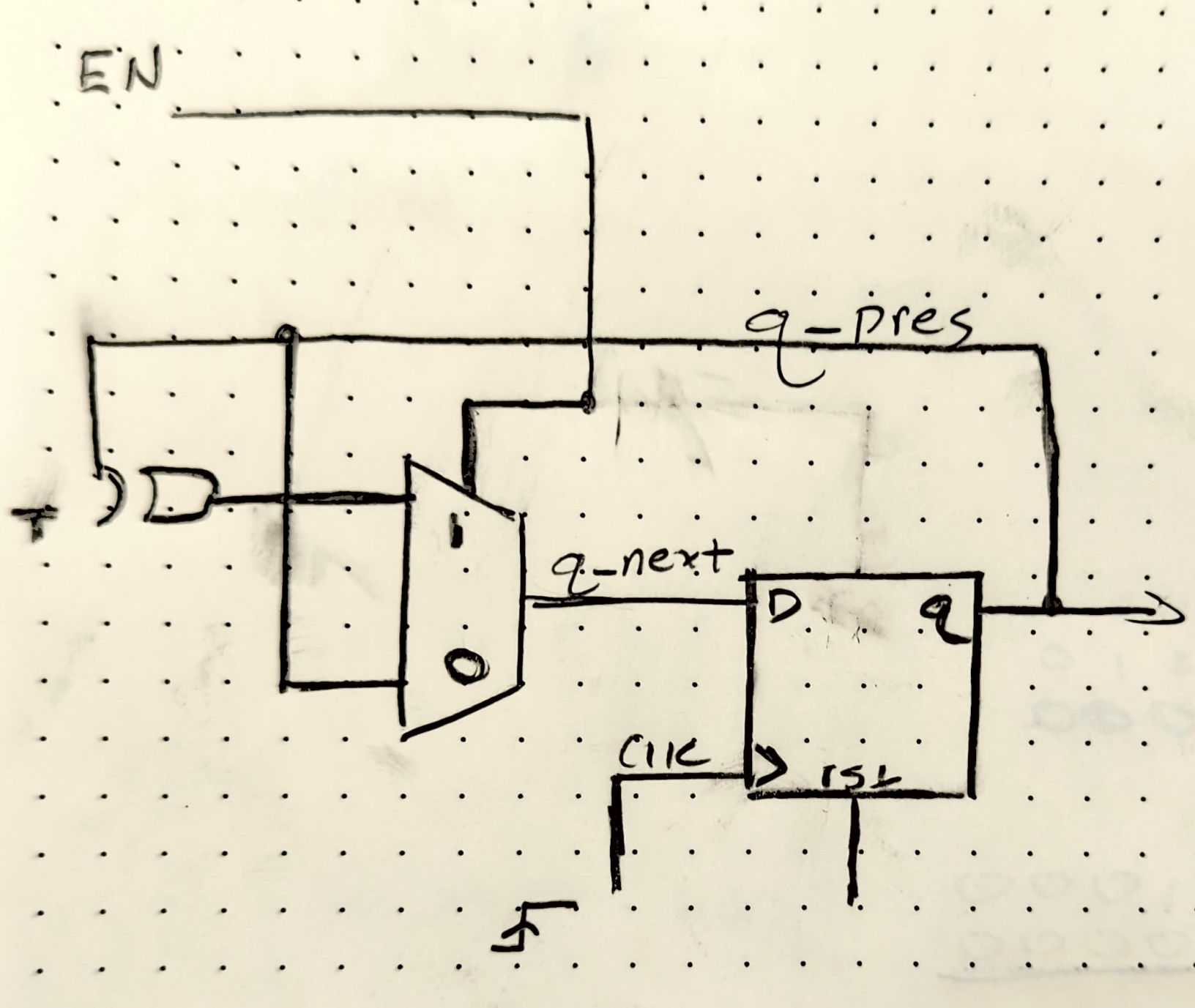
```vhdl
-- VHDL 8 bit processor Project
-- D Flip Flop Test Bench
-- James Hicks November 1 2023

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity d_ff_tb is
end d_ff_tb;

architecture tb of d_ff_tb is

    signal d, en, rst, clk, q : std_logic := '0';

    constant clk_period : time := 10 ns;

begin

    DUT: entity work.d_ff_en(two_seg_arch)
    port map( d   => d,
              en  => en,
              rst => rst,
              clk => clk,
              q   => q
            );

    -- clock process
    clk_process : process
    begin
        loop
            wait for clk_period / 2;
            clk <= not clk;
        end loop;
    end process;

    -- data  process
    data_process : process
    begin

        wait for 50 ns;
        d <= '1';
        wait for 30 ns;
        d <= '0';
        wait for 40 ns;
        d <= '1';
        wait for 10 ns;
        d <= '0';
        for I in 1 to 18 loop
            wait for 10 ns;
            d <= not d;
        end loop;
        wait for 50 ns;
        d <= '1';
        wait for 50 ns;
        d <= '0';
        wait for 20 ns;
        d <= '1';
        wait;
    end process;

    -- enable process
    en_process : process
    begin
        wait for 50 ns;
        en <= '1';
        wait for 160 ns;
        en <= '0';
        wait for 100 ns;
```

```
70          en <= '1';
71          wait;
72      end process;
73
74      -- termination process
75      termination_process : process
76      begin
77          wait for 450 ns;
78          assert false report "end of test" severity failure;
79      end process;
80
81      -- rst process
82      rst_process : process
83      begin
84          rst <= '1';
85          wait for 5 ns;
86          rst <= '0';
87          wait;
88      end process;
89  end tb;
```


EN
q_pres
D
1
0
q_next
D
q
CLK
RST

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity t_ff_en is
    Port ( t   : in STD_LOGIC;
           en  : in STD_LOGIC;
           rst : in STD_LOGIC;
           clk : in STD_LOGIC;
           q   : out STD_LOGIC);
end t_ff_en;

-- two segment architecture
architecture two_seg_arch of t_ff_en is

signal q_pres, q_next : std_logic;

begin

    -- next state logic
    q_next <= (t xor q_pres) when en='1' else
    (q_pres and (not en));

    d_ff_process: process( clk, rst ) -- en is not in list
    begin
        if (rst = '1') then
            q_pres <= '0';
        elsif (clk'event and clk='1') then
            q_pres <= q_next;
        end if;
    end process;

    -- output logic
    q <= q_pres;

end two_seg_arch;
```

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library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity t_ff_tb is
end t_ff_tb;

architecture tb of t_ff_tb is

    signal t, en, rst, clk, q : std_logic := '0';

    constant clk_period : time := 10 ns;

begin

    DUT: entity work.t_ff_en(two_seg_arch)
    port map( t   => t,
              en  => en,
              rst => rst,
              clk => clk,
              q   => q
            );

    -- clock process
    clk_process : process
    begin
        loop
            wait for clk_period / 2;
            clk <= not clk;
        end loop;
    end process;

    -- data  process
    t_process : process
    begin
        wait for 20 ns;
        t <= '1';
        wait for 30 ns;
        t <= '0';
        wait for 40 ns;
        t <= '1';
        for I in 1 to 9 loop
            wait for 10 ns;
            t <= not t;
        end loop;
        wait for 20 ns;
        t <= '1';
        wait;
    end process;

    -- enable process
    en_process : process
    begin
        wait for 20 ns;
        en <= '1';
        wait for 210 ns;
        en <= '0';
        wait for 30 ns;
    end process;

    -- termination process
    termination_process : process
    begin
        wait for 260 ns;
        assert false report "end of test" severity failure;
```

```
70      end process;
71
72      -- rst process
73      rst_process : process
74      begin
75          rst <= '1';
76          wait for clk_period / 2;
77          rst <= '0';
78          wait;
79      end process;
80  end tb;
```

Re: Lab 6

Rodriguez-Marek, Esteban <erodriguezma@ewu.edu>
Tue 11/7/2023 1:51 PM
To:Hicks, James <jhicks19@ewu.edu>
Confirming.

From: Hicks, James <jhicks19@ewu.edu>
Sent: Tuesday, November 7, 2023 1:27 PM
To: Rodriguez-Marek, Esteban <erodriguezma@ewu.edu>
Subject: Lab 6

Hello Dr. Rodriguez-Marek,

I showed you my lab 6 in class today and you told me to send you this email for verification.

Best Regards,
James Hicks