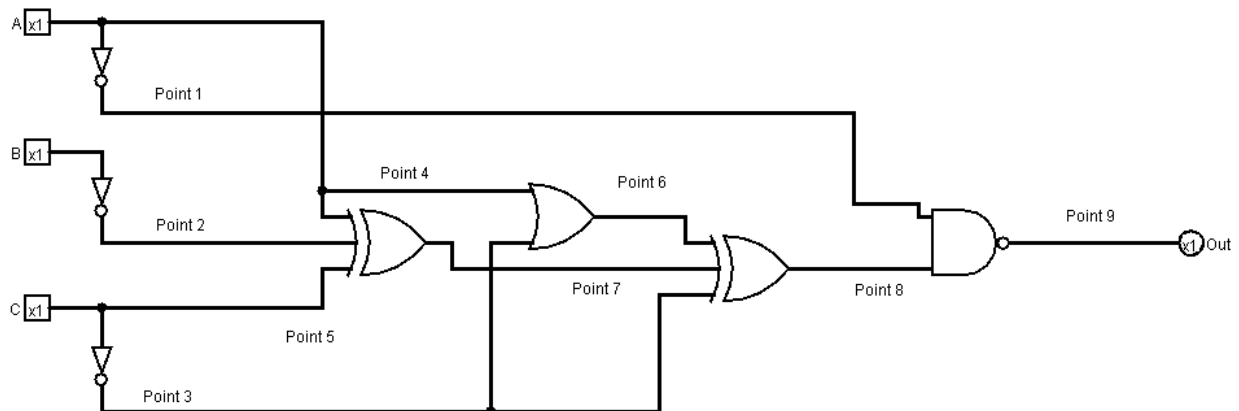


## Homework 2

### Written

1. (3 points) Given only an 8-1 multiplexer and constants 0 and 1 implement a circuit that behaves like the following function:  $m_2 + m_5 + m_6 + m_7$  There are 3 input variables for this problem  $x_2, x_1, x_0$ .
2. (3 points) Given only an 3-8 one hot decoder and an OR gate implement a circuit that behaves like the following function:  $m_0 + m_2 + m_6$  There are 3 input variables for this problem  $x_2, x_1, x_0$ .
3. (3 points) Use only 2 – 1 multiplexers to create an 8-1 multiplexer.
4. (4.5 points) Given the following circuit and the propagation delays in the following table, what are the propagation delays at each marked point? There are 9 separate points.

Component	Delay
Not	1 ns
OR	5 ns
XOR	3 ns
NAND	2 ns



5. (3 points) Given that each XOR gate has a delay of  $A$  ns, each AND gate has a delay of  $B$  ns, and each OR gate has a delay of  $C$  ns, what is the propagation delay of the worst case path in an  $N$  bit ripple carry adder?

## Logisim

For each of the following problems you are only allowed to use AND, OR, NOT, and XOR, unless otherwise specified. You may use all components under Wiring

1. (10 points) File name: shift3.circ. Create a circuit that is capable of performing logical left and right shifts on a 3 bit number. We will be shifting in 0's as the filler bits. See [here](#) for a description on logical shifting. You may use muxes on this problem. Hint: Use muxes on this problem.

Pin	Type	Description
Num	Input	The 3 bit number to be shifted
Shift_amount	Input	The 2 bit number specifying how much to shift num
Do_Right_Shift	Input	When 1 a right shift is to be preformed. When 0 a left shift is to be preformed
Shifted_Num	Output	The shifted number

2. (15 points) File name: 4bitAdder.circ. Create a 4 bit adder that uses carry look ahead.

Pin	Type	Description
A	Input	The first 4 bit number to be added
B	Input	The second 4 bit number to be added
Cin	Input	The incoming carry
Sum	Output	The result of adding A and B together
Cout	Output	1 if a carry occurred out of the 4 <sup>th</sup> bit when adding A and B together