Royal Digital I Calculator

Contents

Notes

- The symbol Ngp denotes a physical connector pin, where *c*=connector and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- The symbol ▲ without an additional label denotes VDD (–24V).
- Capacitance in microfarads unless otherwise indicated.
- These drawings based on unit with Serial No. 1G54100.
- See also the Royal Digital I Theory of Operation document. (madrona.ca/e/eec)

Log

- 2020 Mar: Initial drawing / bhilpert.
- 2020 Oct: State sequences replaced with simulator output / bh.
- 2021 Jan: Minor syntax corrections / bh.

Signal Names

Section	Signal	Description
Timing	ØC	Master clock, data capture phase.
	ØT	Master clock, toggle outputs phase.
	ØB1,2,4,8	Bit timing.
	ØD…	Digit timing (4 bits constitutes a digit).
	ØEON	Capture pulse at the end of number cycle.
Keyboard	KNUM	0::9 numeral key bit stream.
	KPN	Process a numeral key (state-synchronised latch).
	KPD	Process the decimal point key.
	KPO	Process an operation key.
	KC, KCE	Clear keys.
Control	STn	Primary states of the control state machine.
	OPAS	Add/Subtract operation to be performed.
	OPMD	Multiply/divide operation to be performed.
	OPAM	Add/Multiply.
	OPSD	Subract/Divide.
	OPM	Multiply operation.
	OPD	Divide operation.
	NEG	Negative number flag.
	DFLG	Temporary flag.
	ERR	Latched error or overflow state.
Registers	RX	X register bitstream.
	RY	Y register bitstream.
	N1,2,4,8	BCD numerals on their way to the display.
	R<0	Result Less Than Zero. Flag holding a carry/borrow indication from the arithmetic unit.
Counters	PLT	Primary Loop Tracker.
	DPC	Decimal Point Counter.
	DPC=N	DPC is Null – the shift register is empty.
	DPC<SP	DPC is less than the DP switch setting.
	DP	Signal to the display to turn on the decimal point at the appropriate time.

- A "~" in a signal name indicates the logical NOT operation.
- The character " • " in a signal name indicates the logical AND operation.
- The character "+" in a signal name indicates the logical OR operation.

Logic Presentation

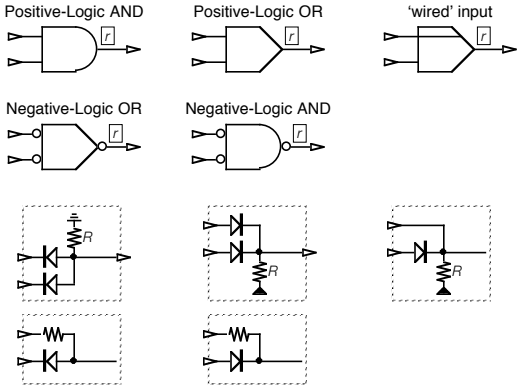
Gate symbols and signal names are presented in accordance with:
logic 1 = GND
logic 0 = V–24

The design uses primarily negative logic in the control portion and positive logic for data and registers.

Logic Implementation

The logic is implemented with a combination of early SSI and MSI MOS integrated circuits from the JMOS family, and discrete DTL. Most gates are constructed from discrete diodes and resistors. Inverters, active gates, flip-flops and more complex logic elements are contained in the integrated circuits. The active elements are open-drain outputs, closing to GND (logic 1), requiring external pull-down resistors to –24V (logic 0).

The internal construction of discrete gates is shown in the following diagrams. A wire–OR or wire–AND construction is indicated by the input line traversing the width of the gate. The design is heavily optimised for component reduction with many gates having one input formed from the pull-up/down load resistor, rather than a diode and fixed-supply resistor.



The diodes may be individual components or contained in 4-diode TSxxx modules. Gate inputs are identified either by a pin number in the case of a diode in a module, the ID of the discrete diode forming the input, or the R value in the case of a resistor.

For gates with fixed-supply load resistors (*R*), to reduce clutter, the resistors are indicated in the schematic by one of the following letters (*r*) in a box by the output.

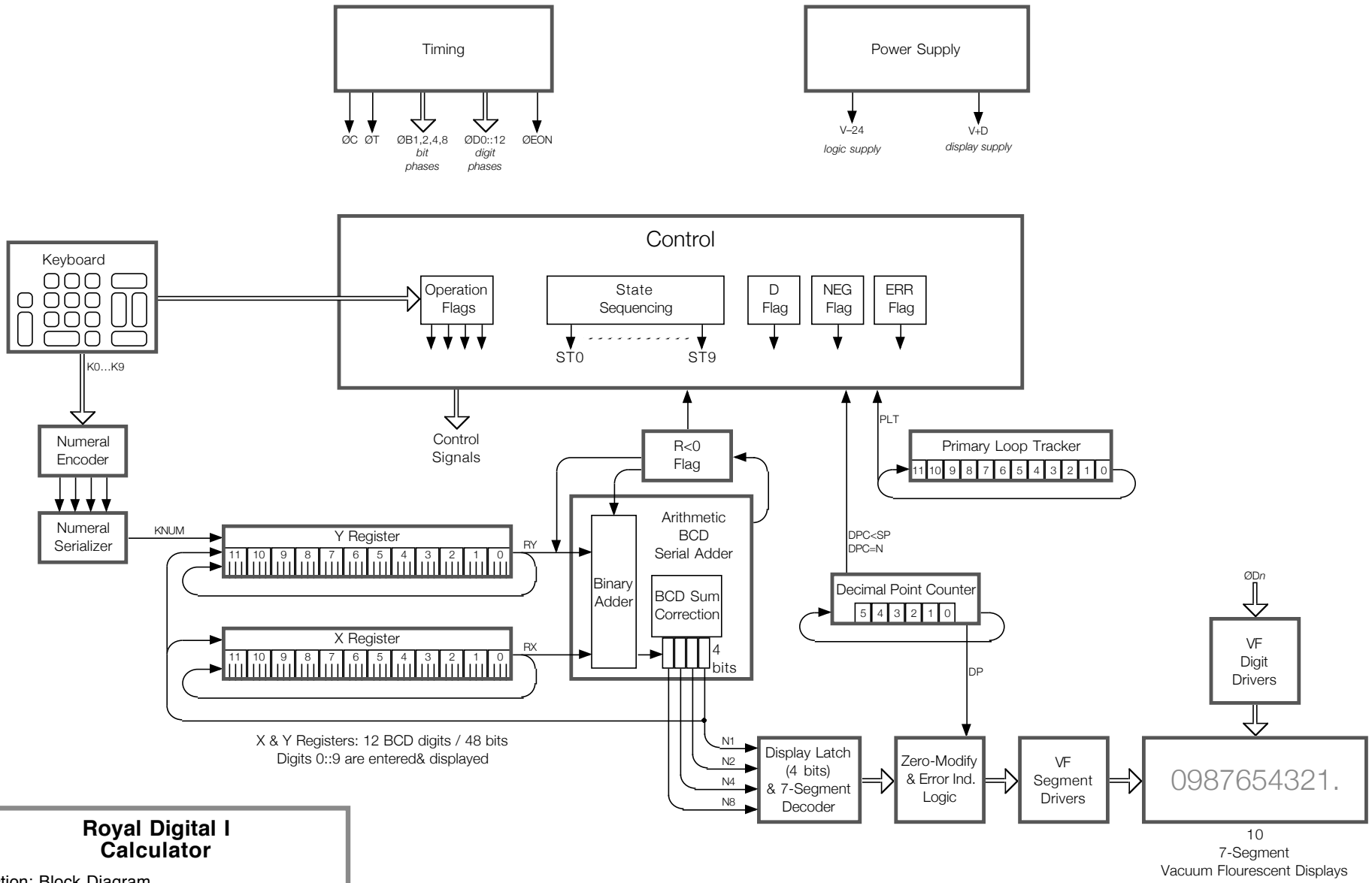
Symbol (*r*)	Resistance (*R*)	Symbol (*r*)	Resistance (*R*)
3	30K to VDD	a	100K to GND
5	50K to VDD	b	200K to GND
1	100K to VDD	c	10K to GND

Clocking Scheme

The flip-flops in the JMOS logic family are a form of Master/Slave D-type flip-flop with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while outputs are changed synchronously by a single clock signal.

ØC = Capture Input (master section clock)
ØT = Transition Input (slave section clock)

The state of the D input is captured when ØC is logic 0 (–24V). The Q output is set in accordance with the captured state when ØT goes to logic 0.



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Section: Block Diagram
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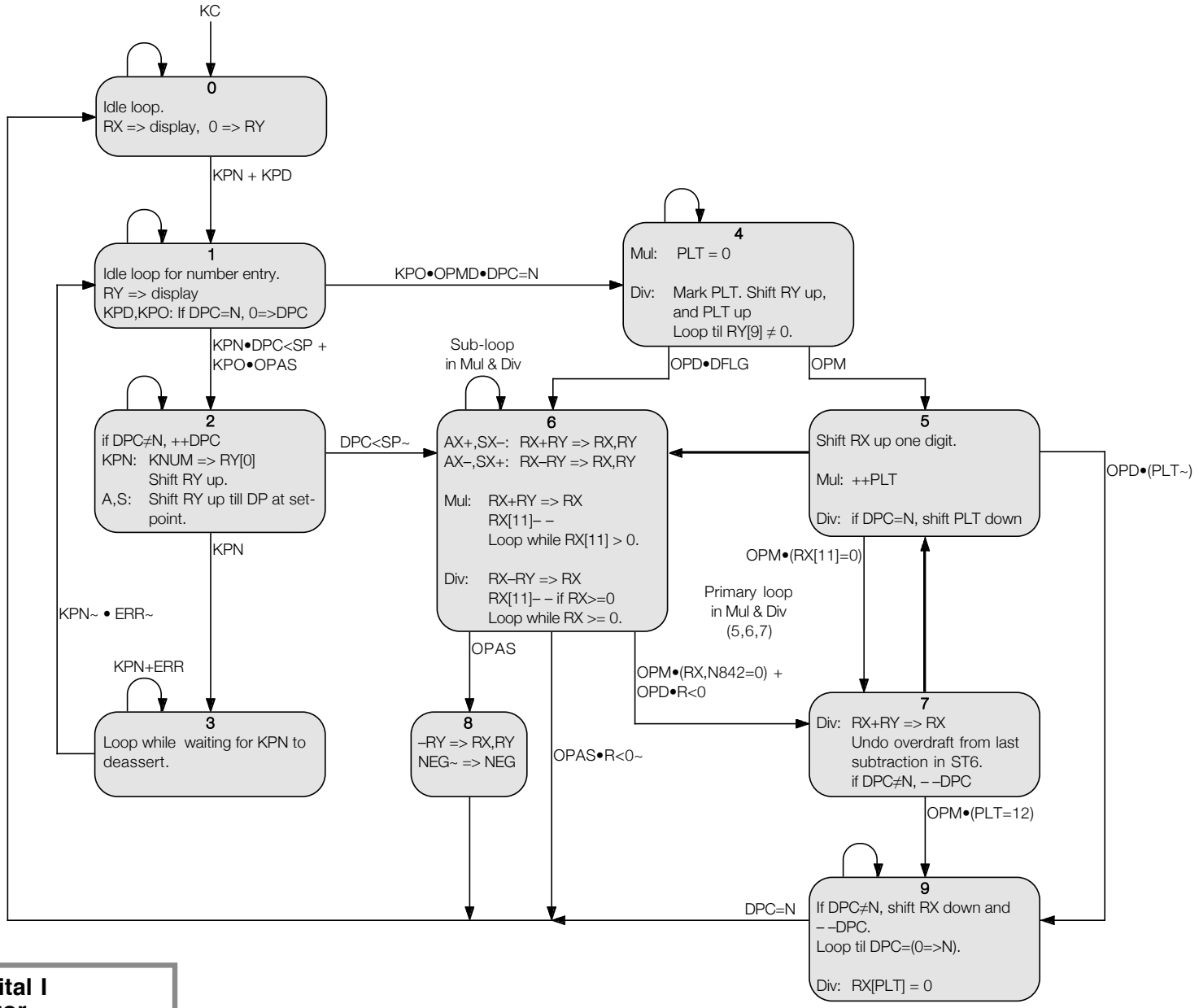

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Section: State Diagram
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Multiplication State-Sequence Example

Multiply 12*4.3 with DPSwitch=3 => 51.600

ERR	ST	OPss	PLT	DPC	NEG X	N	Y	N
			109876543210	543210	109876534210		109876543210	
KEYPRESS: C								
	0*	AS/AM	111111111111	.....	.....	0	.....	
KEYPRESS: 1								
	1	AS/AM	111111111111	.....	.....		.....	0
	2	AS/AM	11111111111.	.....	.....		1	0
	3	AS/AM	11111111111.	.....	.....		1	0
	3	AS/AM	11111111111.	.....	.....		1	0
	1*	AS/AM	11111111111.	.....	.....		1	0
KEYPRESS: 2								
	2	AS/AM	11111111111.	.....	.....		12	0
	3	AS/AM	11111111111.	.....	.....		12	0
	3	AS/AM	11111111111.	.....	.....		12	0
	1*	AS/AM	11111111111.	.....	.....		12	0
KEYPRESS: *								
	1	AS/AM	11111111111.	1	.....		12	0
	2	AS/AM	11111111111.	....1.	.....		...12.	0
	2	AS/AM	11111111111.	...1..	.....		..12..	0
	2	AS/AM	11111111111.	..1...	.....		.12...	0
	2	AS/AM	11111111111.	..1...	.....		.12...	0
	6	AS/AM	11111111111.	..1...	.....12...	0	.12...	0
	0*	MD/AM	11111111111.	.....	.....12...	0	.....	
KEYPRESS: 4								
	1	MD/AM	111111111111	.....	.....12...		.....	0
	2	MD/AM	11111111111.	.....	.....12...		4	0
	3	MD/AM	11111111111.	.....	.....12...		4	0
	3	MD/AM	11111111111.	.....	.....12...		4	0
	1*	MD/AM	11111111111.	.....	.....12...		4	0
KEYPRESS: .								
	1*	MD/AM	11111111111.	1	.....12...		4	0
KEYPRESS: 3								
	1	MD/AM	11111111111.	1	.....12...		4	0
	2	MD/AM	11111111111.	....1.	.....12...		43	0
	3	MD/AM	11111111111.	....1.	.....12...		43	0
	3	MD/AM	11111111111.	....1.	.....12...		43	0
	1*	MD/AM	11111111111.	....1.	.....12...		43	0

continue -->

ERR	ST	OPss	PLT	DPC	NEG X	N	Y	N
			109876543210	543210	109876534210		109876543210	
KEYPRESS: +								
	1	MD/AM	11111111111.	....1.	.....12...		43	0
	4	MD/AM	11111111111.	....1.	.....12...		43	0
	5	MD/AM	1111111111.1	....1.	.....12....	0	43	
	7	MD/AM	1111111111.1	....1.	.....12....	0	43	
	5	MD/AM	111111111.11	....1.	....12.....	0	43	
	7	MD/AM	111111111.11	....1.	....12.....	0	43	
	5	MD/AM	11111111.111	....1.	...12......	0	43	
	7	MD/AM	11111111.111	....1.	...12......	0	43	
	5	MD/AM	1111111.1111	....1.	..12.......	0	43	
	7	MD/AM	1111111.1111	....1.	..12.......	0	43	
	5	MD/AM	111111.11111	....1.	.12........	0	43	
	7	MD/AM	111111.11111	....1.	.12........	0	43	
	5	MD/AM	11111.111111	....1.	12.........	0	43	
	7	MD/AM	11111.111111	....1.	12.........	0	43	
	5	MD/AM	1111.1111111	....1.	2..........	1	43	
	6	MD/AM	111.11111111	....1.	2........43	0	43	
	7	MD/AM	111.11111111	....1.	2........43	0	43	
	5	MD/AM	11.111111111	....1.	.....43.	2	43	
	6	MD/AM	11.111111111	....1.	473	1	43	
	6	MD/AM	11.111111111	....1.	516	0	43	
	7	MD/AM	11.111111111	....1.	516	0	43	
	5	MD/AM	1.1111111111	....1.	....516.	0	43	
	7	MD/AM	1.1111111111	....1.	....516.	0	43	
	5	MD/AM	.11111111111	....1.	....516..	0	43	
	7	MD/AM	.11111111111	....1.	....516..	0	43	
	5	MD/AM	11111111111.	....1.	...516...	0	43	
	7	MD/AM	11111111111.	....1.	...516...	0	43	
	9	MD/AM	11111111111.	....1.	....516..		43	0
	9	MD/AM	11111111111.	.....	....516..		43	0
	0*	AS/AM	11111111111.	.....	....516..	0	.....	

- The state sequence examples were first derived from imagining the logic operation, then from a logic simulation, not from observation of the electronics.
- ST column: '*' indicates the state loops indefinitely until a key press/release.
- PLT, DPC columns: '.'=0
- Register columns: digit state at the end of the number cycle.
- N columns: the 4-bits of the N register where it is included in the bitstream of the associated X or Y register.

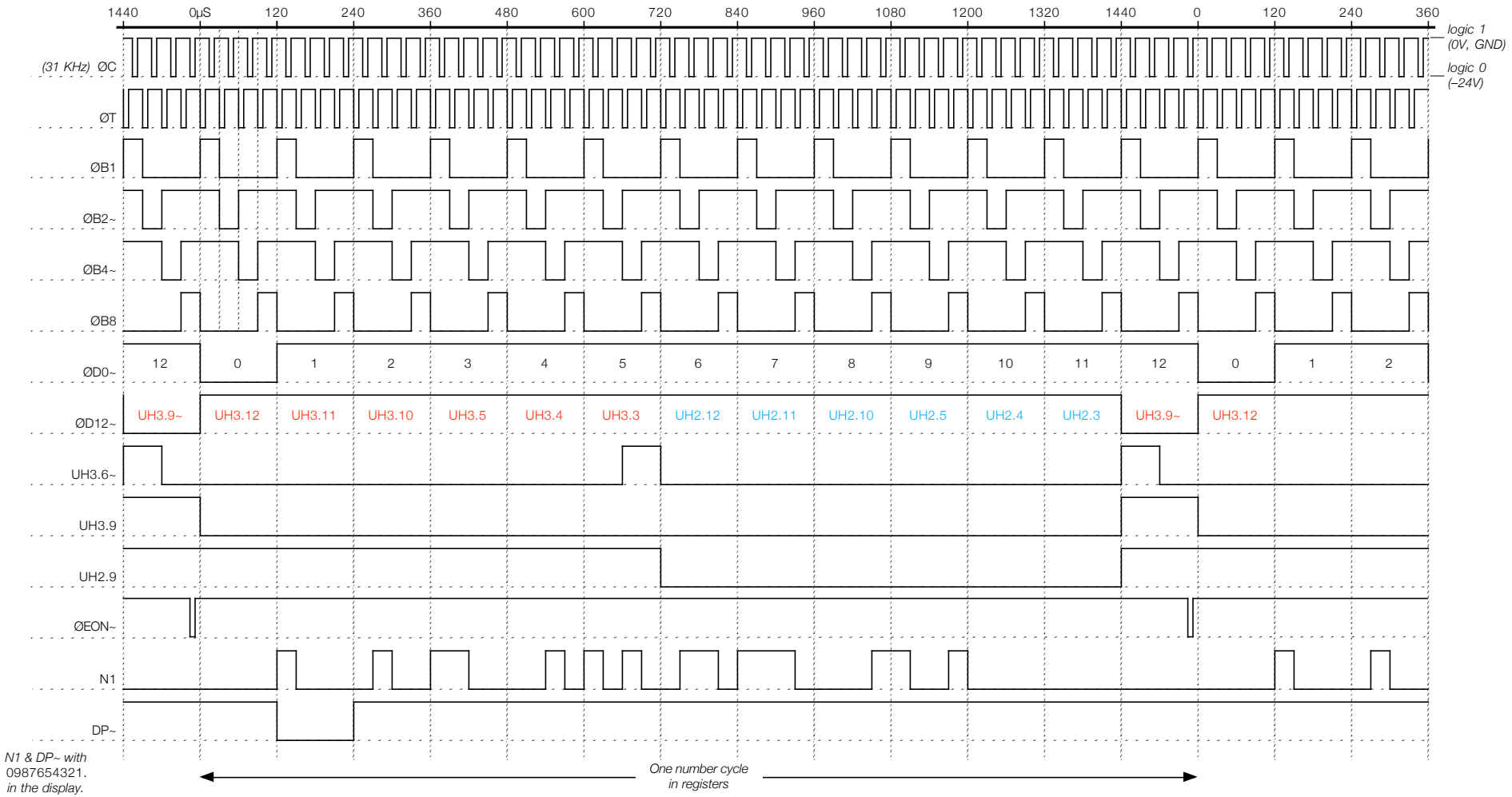
Division State-Sequence Example

Divide 12÷5 with DPSwitch=4 => 2.4000

ERR	ST	OPss	PLT	DPC	NEG	X	N	Y	N
			109876543210	543210		109876534210		109876543210	
KEYPRESS: C									
	0*	AS/AM	111111111111	.....		.....	0	.....	
KEYPRESS: 1									
	1	AS/AM	111111111111	.....		.....		.....	0
	2	AS/AM	11111111111.	.....		.....		1	0
	3	AS/AM	11111111111.	.....		.....		1	0
	3	AS/AM	11111111111.	.....		.....		1	0
	1*	AS/AM	11111111111.	.....		.....		1	0
KEYPRESS: 2									
	2	AS/AM	11111111111.	.....		.....		12	0
	3	AS/AM	11111111111.	.....		.....		12	0
	3	AS/AM	11111111111.	.....		.....		12	0
	1*	AS/AM	11111111111.	.....		.....		12	0
KEYPRESS: /									
	1	AS/AM	11111111111.	1		.....		12	0
	2	AS/AM	11111111111.	....1.		.....		.....12.	0
	2	AS/AM	11111111111.	...1..		.....		.....12..	0
	2	AS/AM	11111111111.	..1...		.....		.....12...	0
	2	AS/AM	11111111111.	.1....		.....		.....12....	0
	2	AS/AM	11111111111.	.1....		.....		.....12....	0
	6	AS/AM	11111111111.	.1....		.....12....	0	.....12....	0
	0*	MD/SD	11111111111.	.....		.....12....	0	.....	
KEYPRESS: 5									
	1	MD/SD	111111111111	.....		.....12....		.....	0
	2	MD/SD	11111111111.	.....		.....12....		5	0
	3	MD/SD	11111111111.	.....		.....12....		5	0
	3	MD/SD	11111111111.	.....		.....12....		5	0
	1*	MD/SD	11111111111.	.....		.....12....		5	0

continue -->

ERR	ST	OPss	PLT	DPC	NEG	X	N	Y	N
			109876543210	543210		109876534210		109876543210	
KEYPRESS: +									
	1	MD/SD	11111111111.	1		.....12....		5	0
	4	MD/SD	.11111111111	1		.....12....		.....5.	0
	4	MD/SD	..1111111111	1		.....12....		.....5..	0
	4	MD/SD	...111111111	1		.....12....		.....5...	0
	4	MD/SD	11111111	1		.....12....		.....5....	0
	4	MD/SD	1111111	1		.....12....		.....5.....	0
	4	MD/SD	111111	1		.....12....		.....5.....	0
	4	MD/SD	11111	1		.....12....		.....5.....	0
	4	MD/SD	1111	1		.....12....		.....5.....	0
	4	MD/SD	111	1		.....12....		.....5.....	0
	4	MD/SD	11	1		.....12....		.....5.....	0
	6	MD/SD	.........1.	1		95....12....	0	.....5.....	
	7	MD/SD	.........1.	.....		.....12....	0	.....5.....	
	5	MD/SD	........1..	.....		....12.....	0	.....5.....	
	6	MD/SD	........1..	.....		95...12.....	0	.....5.....	
	7	MD/SD	........1..	.....		.....12.....	0	.....5.....	
	5	MD/SD	.......1...	.....		....12......	0	.....5.....	
	6	MD/SD	.......1...	.....		95..12......	0	.....5.....	
	7	MD/SD	.......1...	.....		....12......	0	.....5.....	
	5	MD/SD	......1....	.....		...12.......	0	.....5.....	
	6	MD/SD	......1....	.....		95.12.......	0	.....5.....	
	7	MD/SD	......1....	.....		...12.......	0	.....5.....	
	5	MD/SD	.....1.....	.....		..12........	0	.....5.....	
	6	MD/SD	.....1.....	.....		9512........	0	.....5.....	
	7	MD/SD	.....1.....	.....		..12........	0	.....5.....	
	5	MD/SD	....1......	.....		.12.........	0	.....5.....	
	6	MD/SD	....1......	.....		962.........	0	.....5.....	
	7	MD/SD	....1......	.....		.12.........	0	.....5.....	
	5	MD/SD	...1.......	.....		12..........	0	.....5.....	
	6	MD/SD	...1.......	.....		.7..........	1	.....5.....	
	6	MD/SD	...1.......	.....		.2..........	2	.....5.....	
	6	MD/SD	...1.......	.....		97..........	2	.....5.....	
	7	MD/SD	...1.......	.....		.2..........	2	.....5.....	
	5	MD/SD	..1........	.....		2..........2	0	.....5.....	
	6	MD/SD	..1........	.....		15.........2	1	.....5.....	
	6	MD/SD	..1........	.....		1..........2	2	.....5.....	
	6	MD/SD	..1........	.....		.5.........2	3	.....5.....	
	6	MD/SD	..1........	.....		2	4	.....5.....	
	6	MD/SD	..1........	.....		95.........2	4	.....5.....	
	7	MD/SD	..1........	.....		2	4	.....5.....	
	5	MD/SD	.1.........	.....		24	0	.....5.....	
	6	MD/SD	.1.........	.....		95........24	0	.....5.....	
	7	MD/SD	.1.........	.....		24	0	.....5.....	
	5	MD/SD	.1.........	.....		.........24.	0	.....5.....	
	6	MD/SD	.1.........	.....		95.......24.	0	.....5.....	
	7	MD/SD	.1.........	.....		.........24.	0	.....5.....	
	5	MD/SD	1..........	.....		........24..	0	.....5.....	
	6	MD/SD	1..........	.....		95......24..	0	.....5.....	
	7	MD/SD	1..........	.....		........24..	0	.....5.....	
	5	MD/SD	1	.....		.......24...	0	.....5.....	
	9	MD/SD	1	.....		.......24...		.....5.....	0
	0*	AS/AM	111111111111	.....		.......24...	0	.....	



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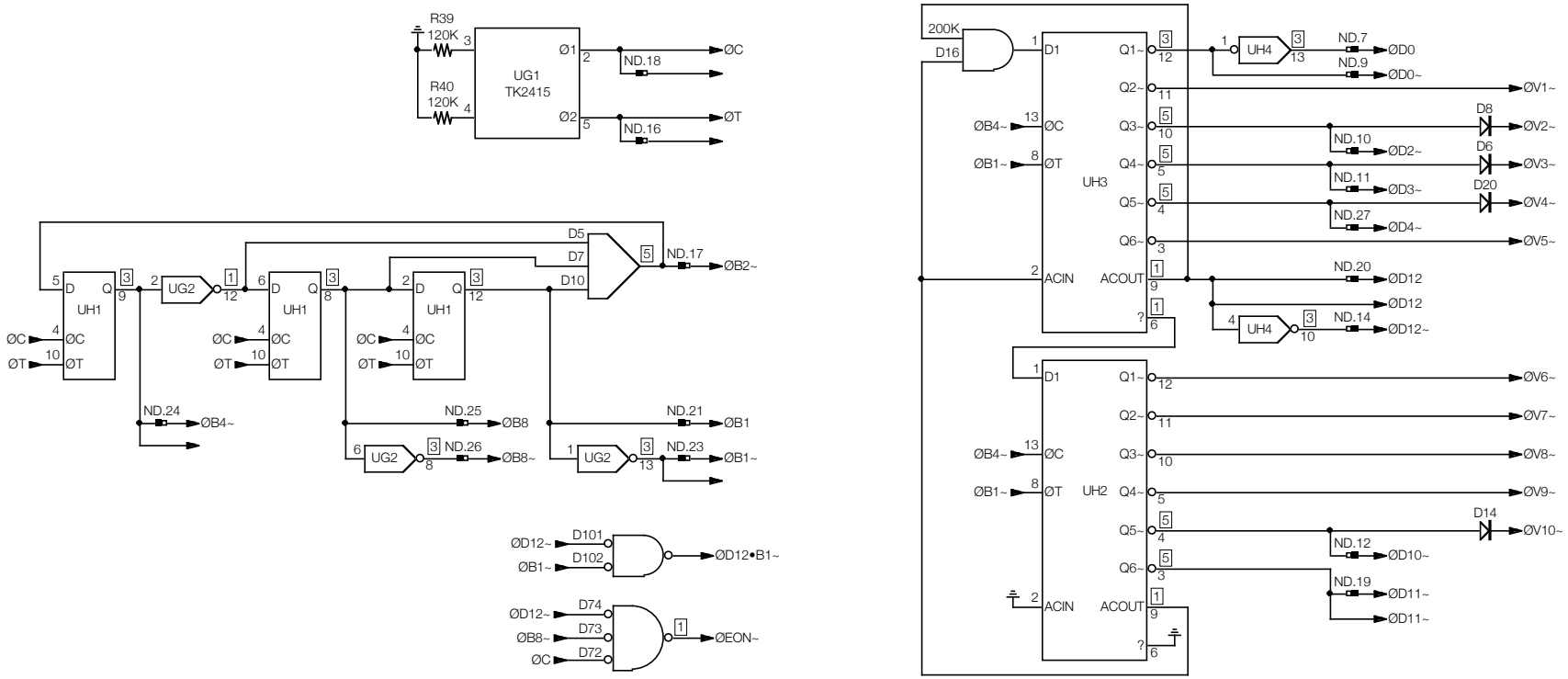

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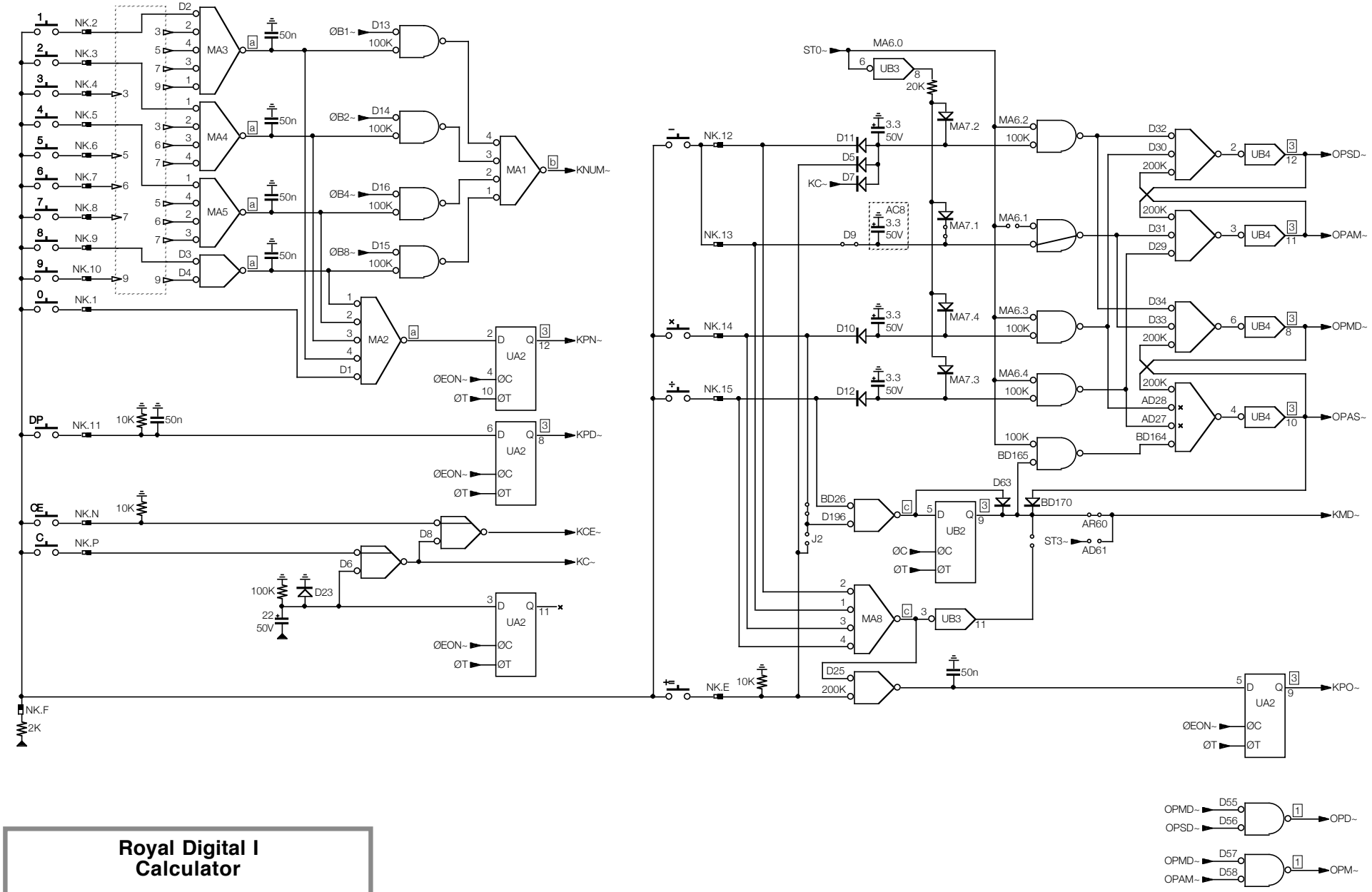

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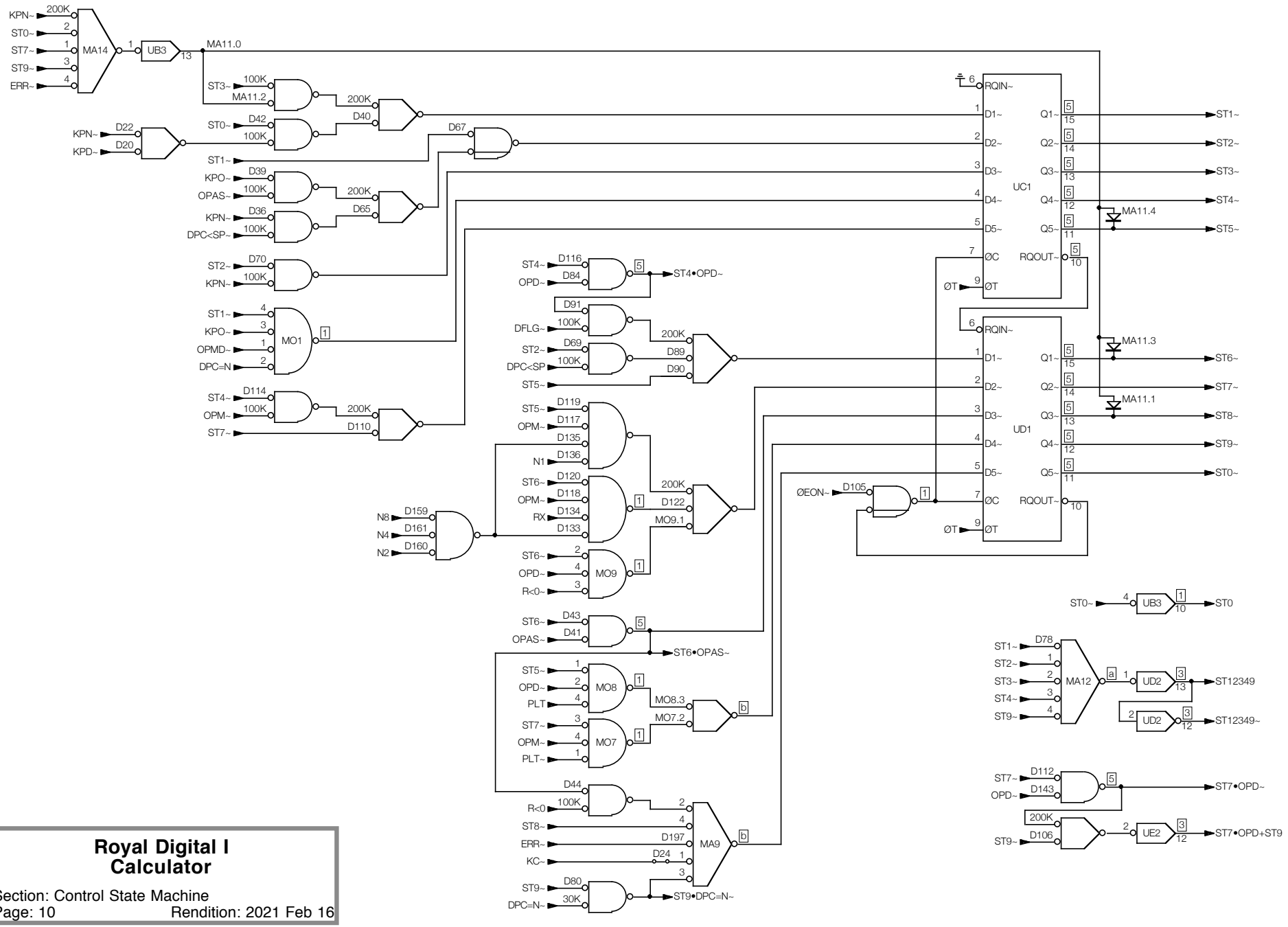

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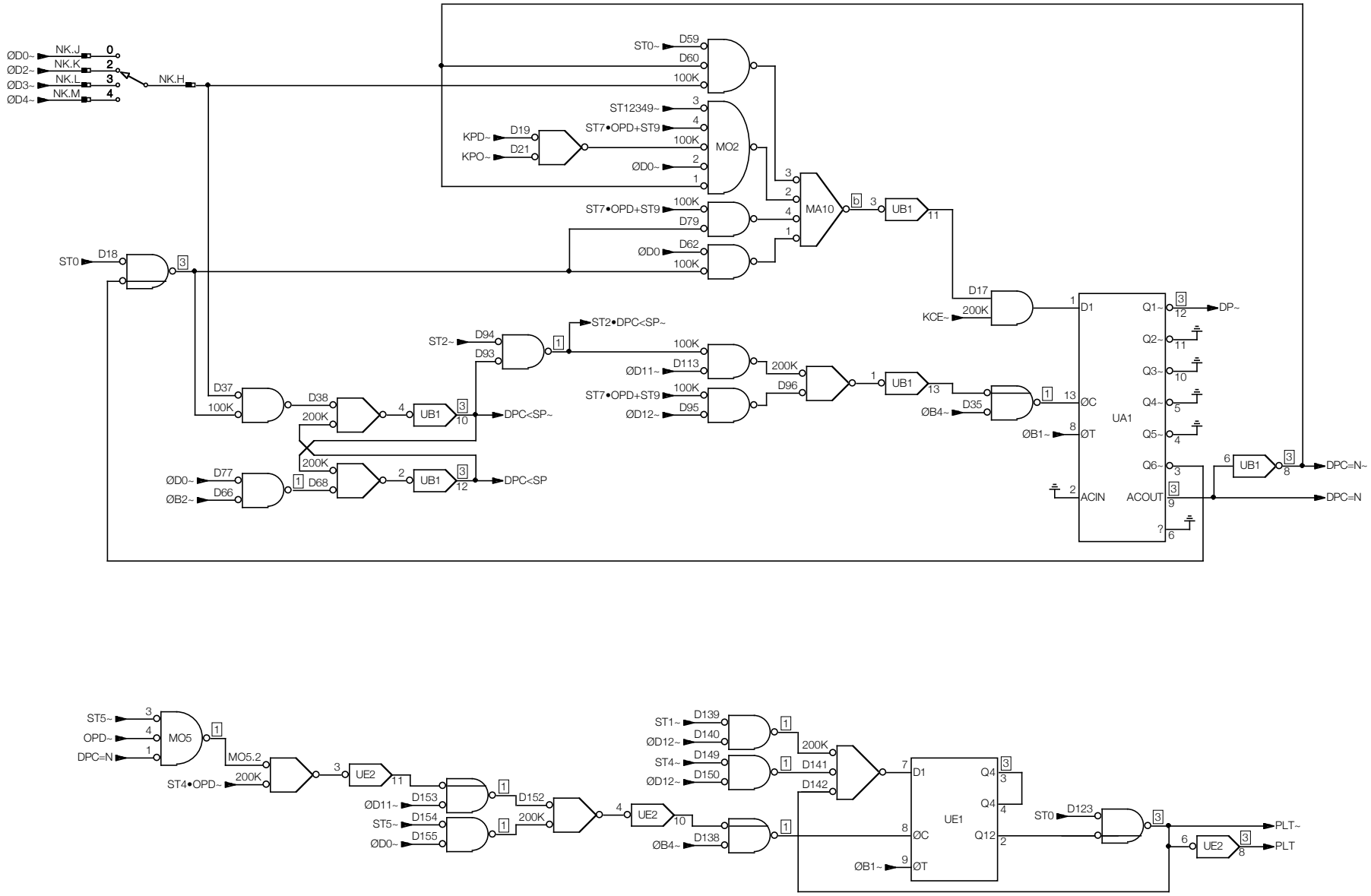

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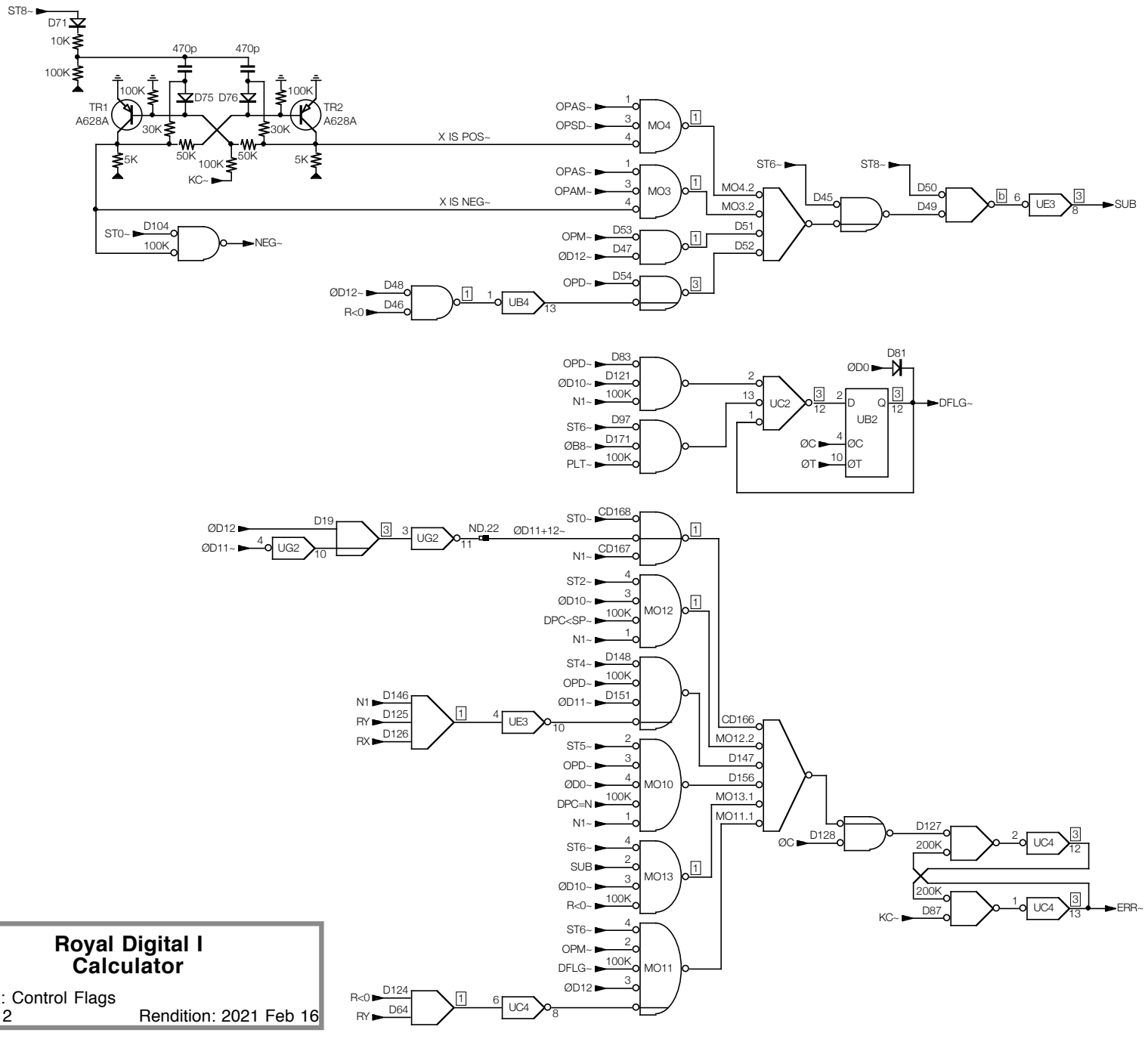

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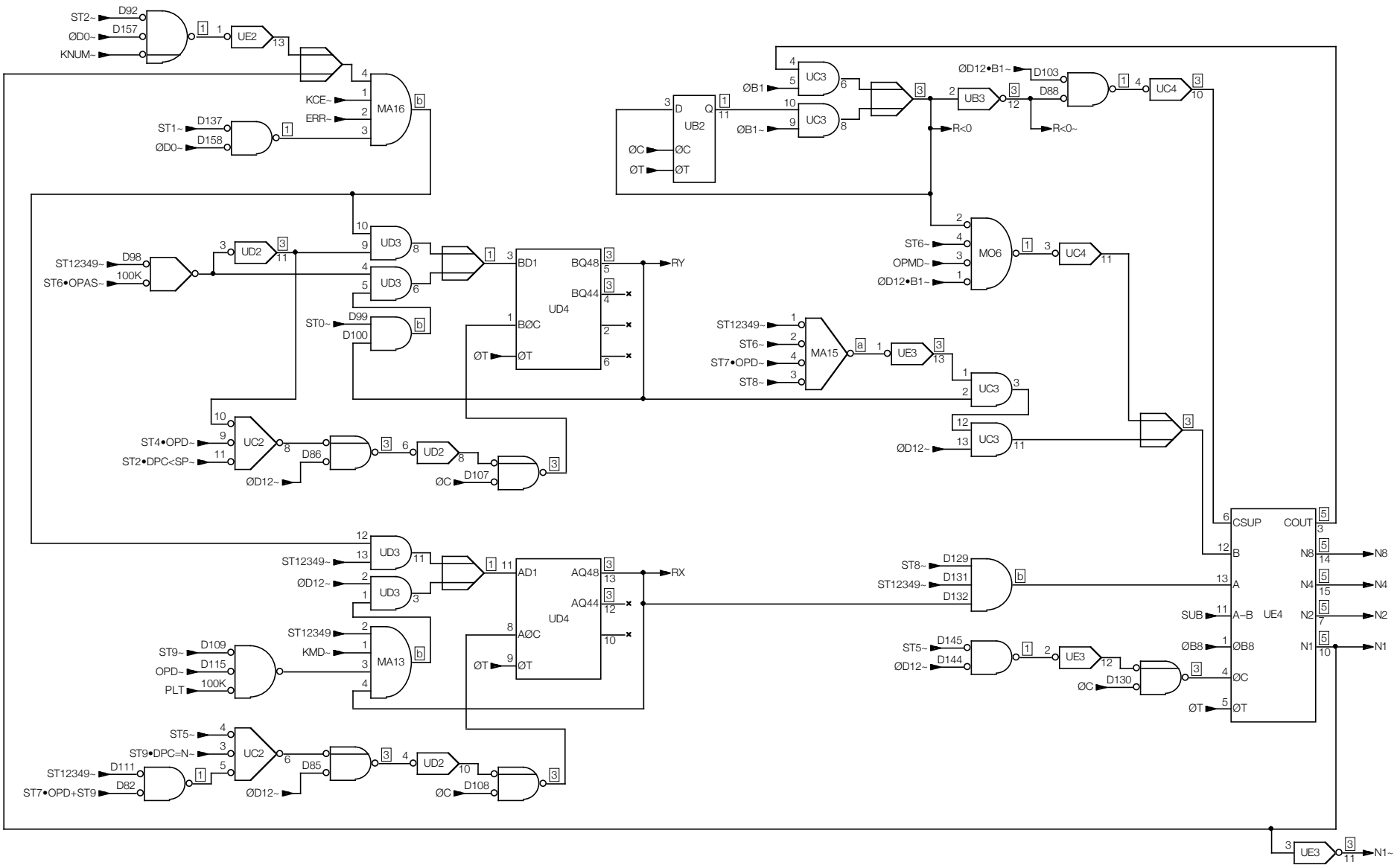

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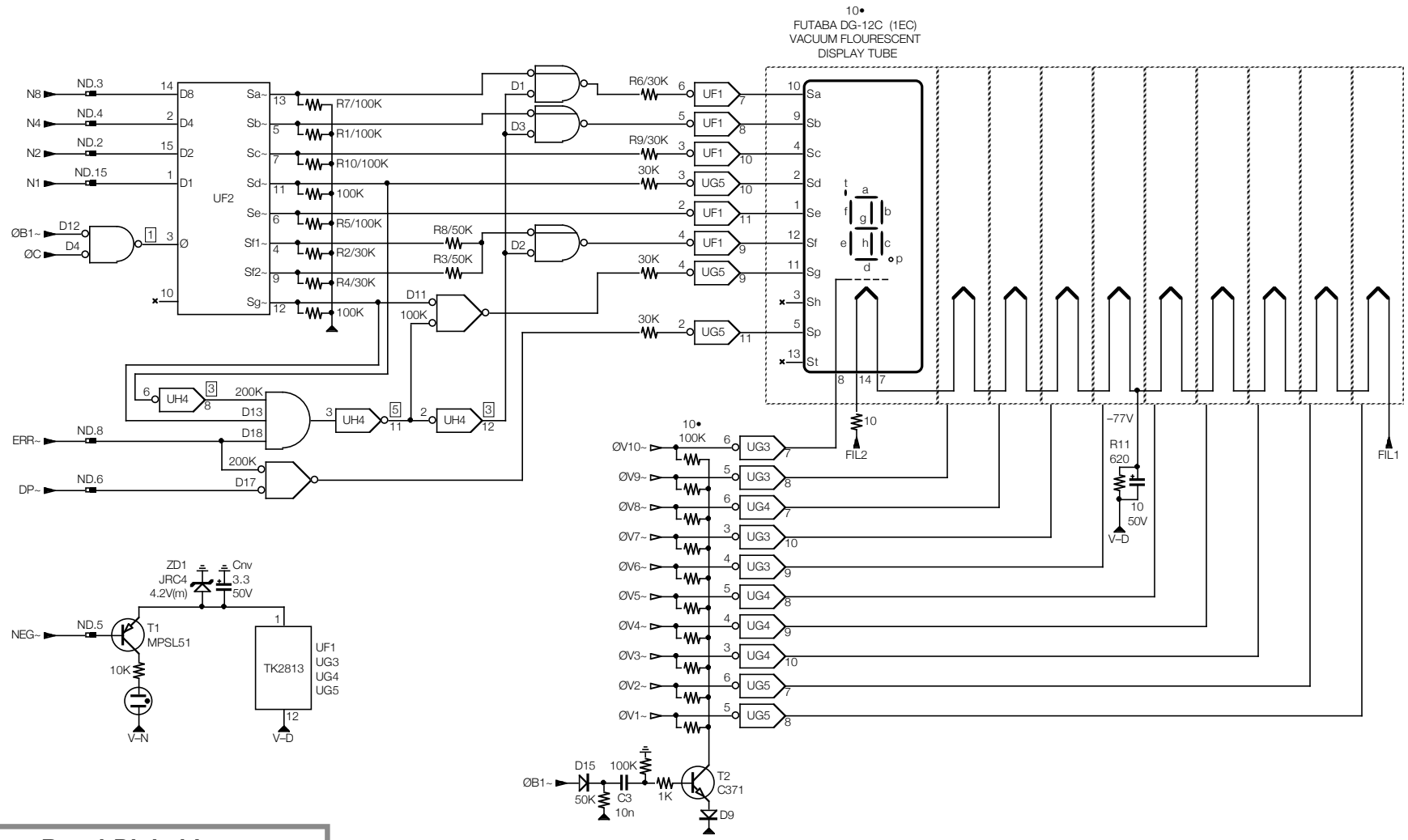

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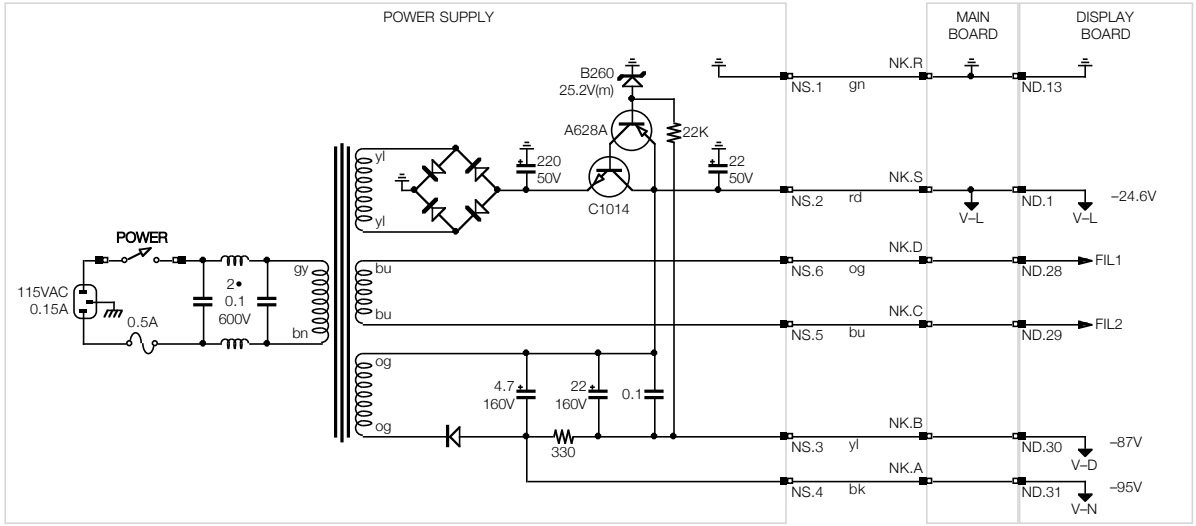

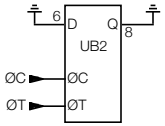

µPD10C	µPD11A	µPD13C	µPD101C	µPD102C	µPD107C	M5811	M5812	M58214	M58221	TK2415	TS509	TS511	TS048	TS078
7	10	7	7	7	7	8	7	8	8	7,8				
14	5		14	14	14	16	14	16	16	1,6				
UB2	UE1	UE2	UD3	UC2	UD4	UD1	UA1	UF2	UE4	UG1	MA1	MA2	MO1	MO5
UA2		UE3	UC3			UC1					MA3	MA4	MO2	MO7
		UD2					UH2				MA5	MA6	MO3	MO8
UH1		UC4					UH3				MA8	MA7	MO4	
		UB1									MA10	MA9	MO6	? MO12
		UB3									MA11	MA13	MO9	
		UB4									MA12	MA15	MO10	
											MA14	MA16	MO11	
		UH4											MO13	
		UG2												

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Section: Power Supply
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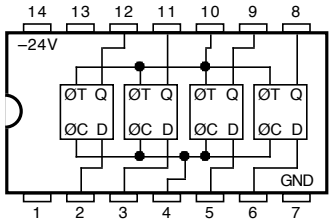
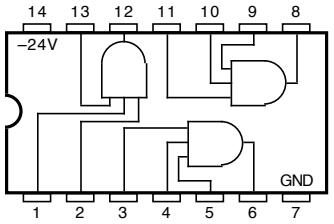
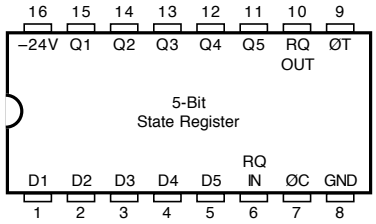
NEC
μPD10C



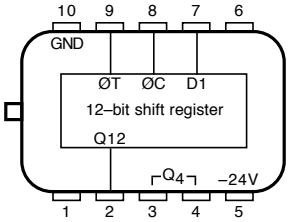
NEC
μPD102C



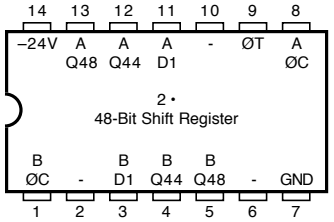
Mitsubishi
M5811



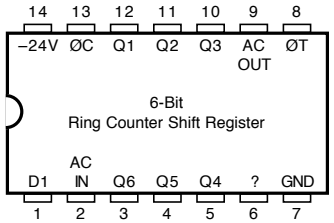
NEC
μPD11A



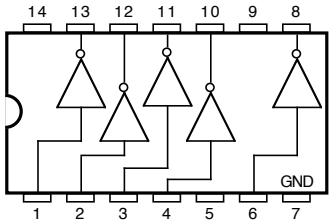
NEC
μPD107C



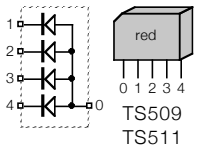
Mitsubishi
M5812



NEC
μPD13C

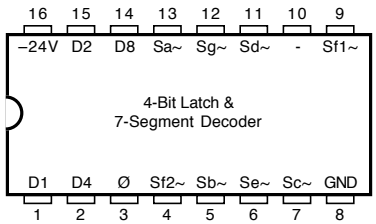


MA*n*

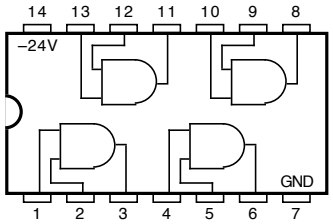


TS509
TS511

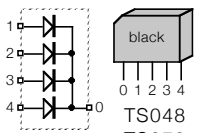
Mitsubishi
M58214



NEC
μPD101C

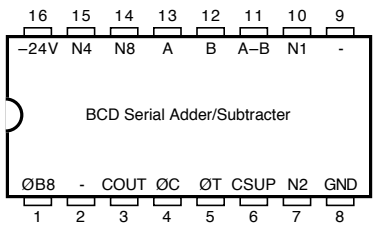


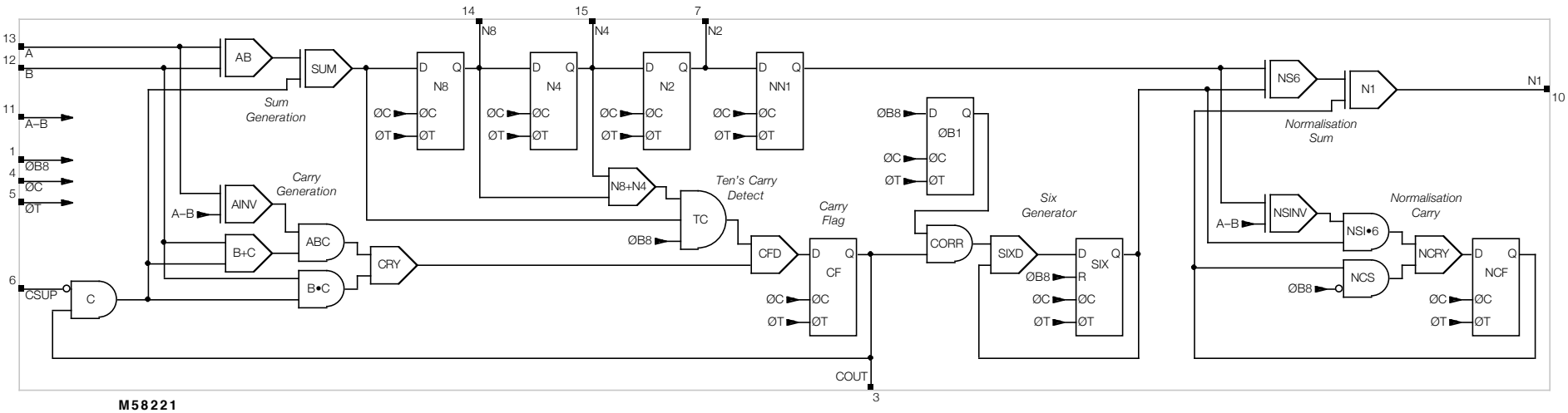
MO*n*



TS048
TS078

Mitsubishi
M58221





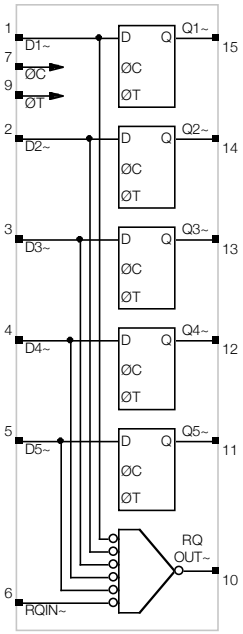
M58221
Serial BCD Arithmetic Unit

Performs BCD addition and subtraction on a serial bit-stream.

M5811
5-Bit State Register

States are active-low.

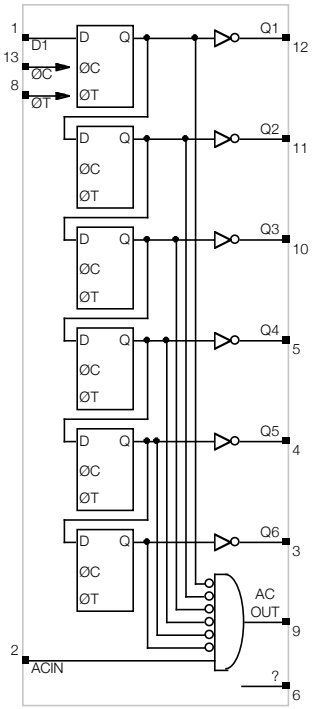
RQ: State request. With external clock-inhibition circuitry controlled by RQOUT, if no D inputs are requesting a state, the current state will loop. The loop exits when a D input goes low.



M5812
6-Bit Ring Counter Shift Register

AC: All Clear. Used to form a ring counter with one or more of these ICs.

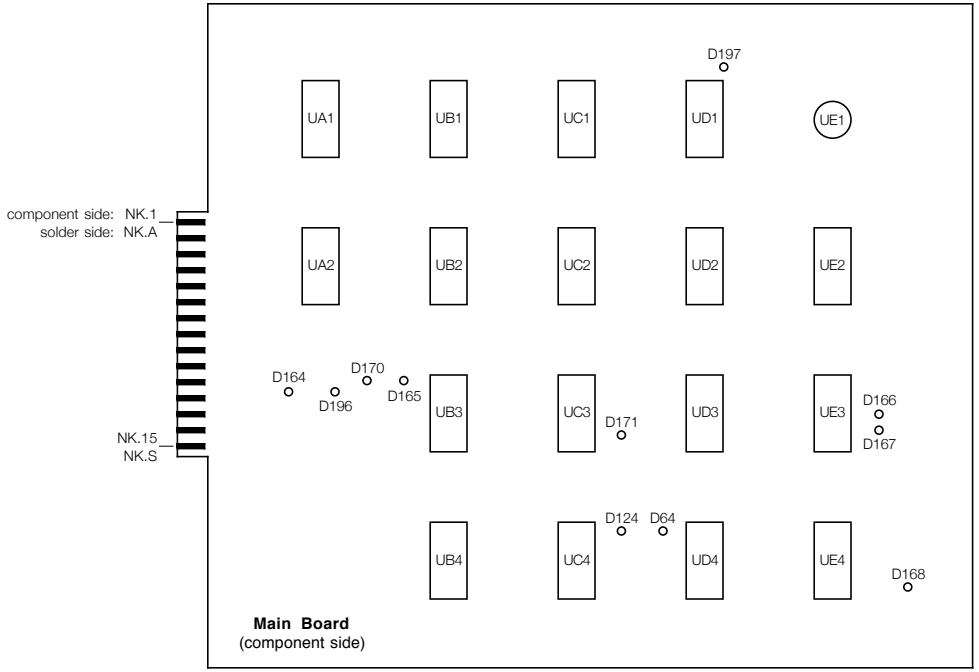
Behavior of pin 6 output not accounted for: transitions occur at inter-phase resolution.



• These diagrams present a functional-equivalent internal structure for the ICs, as inferred from reasoning and observation of behavior.

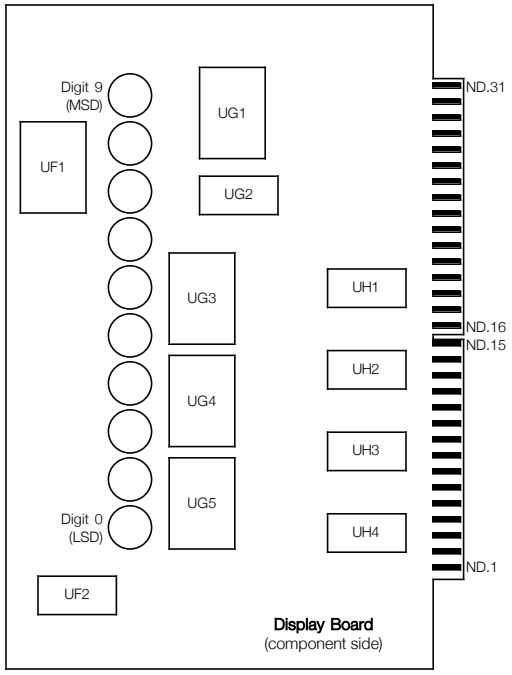
NK

K0	1	A	V–N
K1	2	B	V–D
K2	3	C	FIL2
K3	4	D	FIL1
K4	5	E	K+
K5	6	F	KCOM
K6	7	H	DPCOM
K7	8	J	DP0
K8	9	K	DP2
K9	10	L	DP3
KP	11	M	DP4
K–	12	N	KCE~
K–	13	P	KC~
K*	14	R	GND
K÷	15	S	V–L



ND

31	V–N
30	V–D
29	FIL2
28	FIL1
27	ØD4~
26	ØB8~
25	ØB8
24	ØB4~
23	ØB1~
22	ØD11+12~
21	ØB1
20	ØD12
19	ØD11~
18	ØC
17	ØB2~
16	ØT



15	N1
14	ØD12~
13	GND
12	ØD10~
11	ØD3~
10	ØD2~
9	ØD0~
8	ERR~
7	ØD0
6	DP~
5	NEG~
4	N4
3	N8
2	N2
1	V–L

Diodes on the main board are enumerated D1::D161, with the following exceptions and additions:

D9:	jumper
D24:	jumper
AD27:	not installed
AD28:	not installed
AD61:	not installed

BD164
BD165
CD166
CD167
CD168
BD170

D171
D196
D197

Diode and module IDs are sequenced top-down in columns, then left to right, for the board orientation shown, with the exceptions noted in the board diagram.