

The PDP8 with SystemVerilog

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Outline

- Starting Point
 - C Model
 - VHDL Model
- Design
 - Modules
 - Packages
 - Interface
- Verification
 - Simulation
 - Veloce Standalone
 - Veloce TBX
- Results
 - Trace Files
 - Register Report
 - Valid Memory

Starting Point

Two sources for starting point for this project:

- PDP8 model programed in C
 - Used as functional golden model
 - Ready to output test files
- PDP8 model written in VHDL
 - Used as inspiration for design
 - Some functional differences between VHDL and C model
 - SystemVerilog model designed to match C model

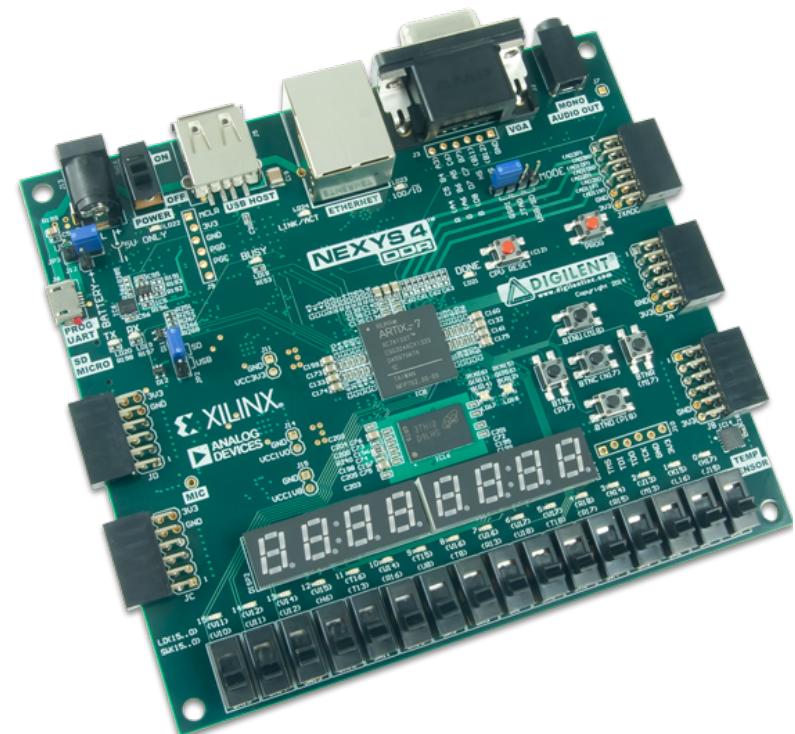
Starting Point

The PDP8/e



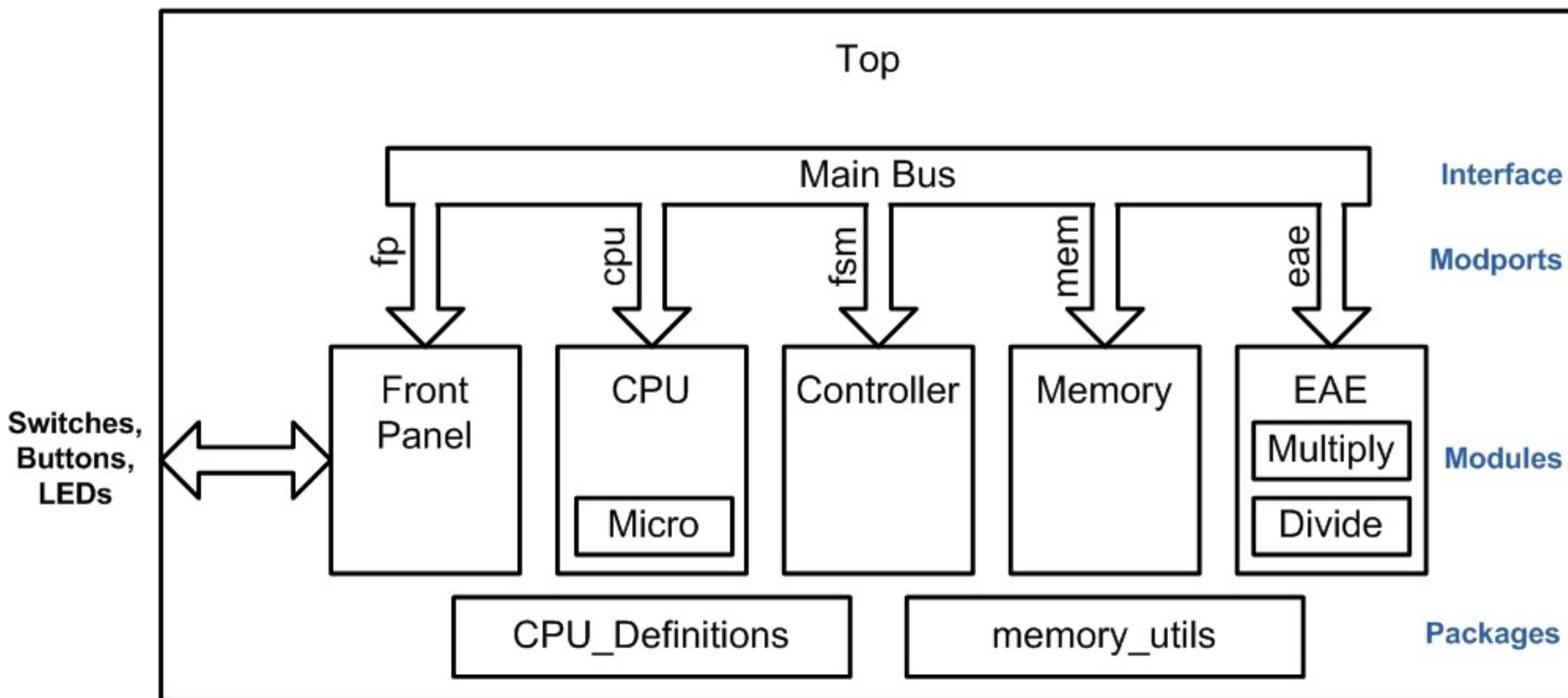
SystemVerilog model is designed to be used with this same board

Development board used for VHDL model



Design

Block Diagram



SystemVerilog Constructs

- Enumerated type definitions (logic type)
- Structs
- New procedural blocks
- Interface with modports
- Packages
- Void Functions
- Unique case

Questa Simulation

- Use file I/O and the front panel controls to load in compiled .as files
- Write .txt files from testbench and from C model
 - Op code and current state of all registers at the completion of each instruction
 - Branch trace file
 - Memory trace file
 - Valid Memory
- Script utilized to automate the process
 - Compiles .as program, SystemVerilog model
 - Loads and runs assembly program on both models
 - Compares output files for differences

Verification

Example File Output

memory_trace.txt

```
IF 0200
IF 0201
DR 0250
DW 0250
```

valid_memory.txt

Address	Contents
0200	7301
0201	7510
0202	3250
0203	7301

branch_trace.txt

```
Current PC: 0201, Target: 0203, Type: Conditional, Result: Taken
Current PC: 0204, Target: 0206, Type: Conditional, Result: Taken
Current PC: 0207, Target: 0211, Type: Conditional, Result: Taken
Current PC: 0212, Target: 0214, Type: Conditional, Result: Not Taken
```

opcode_output.txt

```
Opcode: 007, AC: 7777, Link: 0, MB: 0000, PC: 0212, CPMA: 0000
Opcode: 007, AC: 7777, Link: 0, MB: 0000, PC: 0213, CPMA: 0000
Opcode: 003, AC: 0000, Link: 0, MB: 7777, PC: 0214, CPMA: 0253
Opcode: 007, AC: 0000, Link: 0, MB: 7777, PC: 0215, CPMA: 0253
```

Veloce Emulator

- Started with synthesizable testbench and standalone mode
 - Simulated with Puresim
 - Synthesized design, and did basic tests with *writememh* and *readmemh*
- Switched to TBX mode
 - Synthesizable HDL transactor module running on emulator with design
 - Transactor makes DPI-C calls to HVL module running on Veloce workstation
 - Transactor calls C functions to perform file I/O as with the Questa simulation

Veloce Emulator

- Completed core of design, with ports and logic available to add peripherals in the future
- Achieved perfect match for all .txt file outputs between SystemVerilog model and C model in Questa simulation
- Achieved perfect match for all .txt file outputs in Puresim simulation
- Achieved match for all .txt file outputs in Veloce emulator, with exception of valid memory file
- Unclear why print valid memory operation causes Veloce workstation to run out of memory