**ECE571 – Project Proposal**

Sean Koppenhafer and Jonathan Waldrip

This proposal is for the final project for ECE571. The proposed project is to create a PDP8 simulator and testbench in SystemVerilog. Both members of the team have done work with a PDP8 design in the past, but not in SystemVerilog. We currently have a working version written in C, and synthesizable VHDL. It is our intention to use the core of the VHDL model to recreate a working SystemVerilog design that incorporates the CPU and memory portions of the PDP8. We would like to write a testbench that can load compiled assembly programs into the memory of the VHDL and SystemVerilog versions and run them simultaneously to compare performance. We are proposing to verify and compare the two models in the following areas:

* Valid memory at the end of a test
* Memory trace files
* Register state after every instruction and/or at the end of the test
* Branch trace files
* Total clock cycles
* Clock cycles per instruction

At the time of this proposal, we are still researching the best methods of utilizing the Veloce emulator for verification. We are tentatively planning to use TBX mode because Sean has some experience with it from ECE410 with Tom Schubert. In this case, a C program would be written that would allow us to interface with the HDL through DPI calls. We would like to explore the option of using the existing C code version of the PDP8 written by Sean to perform further verification using this method.

The following list is how the work is to be distributed among the team members:

* Sean: Creating the memory module for the SystemVerilog design. Possibly writing opcode implementation functions as well. Sean will focus more on verification and assembly programming.
* Jonathan: Writing the CPU logic (decode, effective address calculations, execution,etc). Will focus more on the design.
* Both: Implementing the testbench and Veloce emulator to verify the PDP8.