**ECE571 – Project Proposal**

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Our project will focus on creating a PDP8 simulator in SystemVerilog. Sean has a C version of the PDP8 simulator from ECE586 and Jon has a VHDL version from a past class at OIT. We plan to use the VHDL and C version of the simulator as “good models” to compare our SystemVerilog model against. Items that will be compared in the testbench may include:

* Valid memory at the end of a test
* Memory trace files
* Register state after every instruction or at the end of the test
* Branch trace files
* Total clock cycles ran
* Number of clock cycles ran by each instruction

For our verification method on the emulator, we are tentatively planning to use TBX mode because Sean has some experience with it from ECE410 with Tom Schubert. In this case, a C program would be written that would allow us to interface with the HDL through DPI calls.

Distributed workloads will look like this:

* Sean: Creating the memory module for the HDL. Possibly writing opcode implementation functions as well. Will focus more on the testbench.
* Jon: Writing the cpu logic (decode, effective address calculations, execution,etc). Will focus more on the design.
* Both: Writing the testbench to verify that PDP8 simulator works.