

# 1. Description

## 1.1. Project

Project Name	heat_plate_stm32
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	01/24/2024

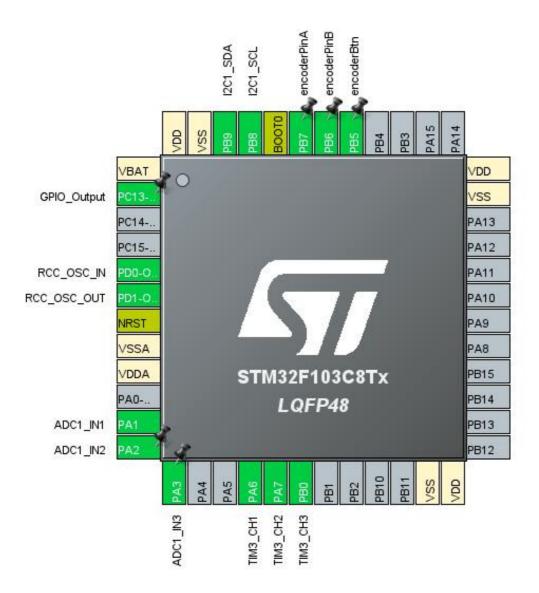
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

## 1.3. Core(s) information

Core(s)	Arm Cortex-M3

# 2. Pinout Configuration

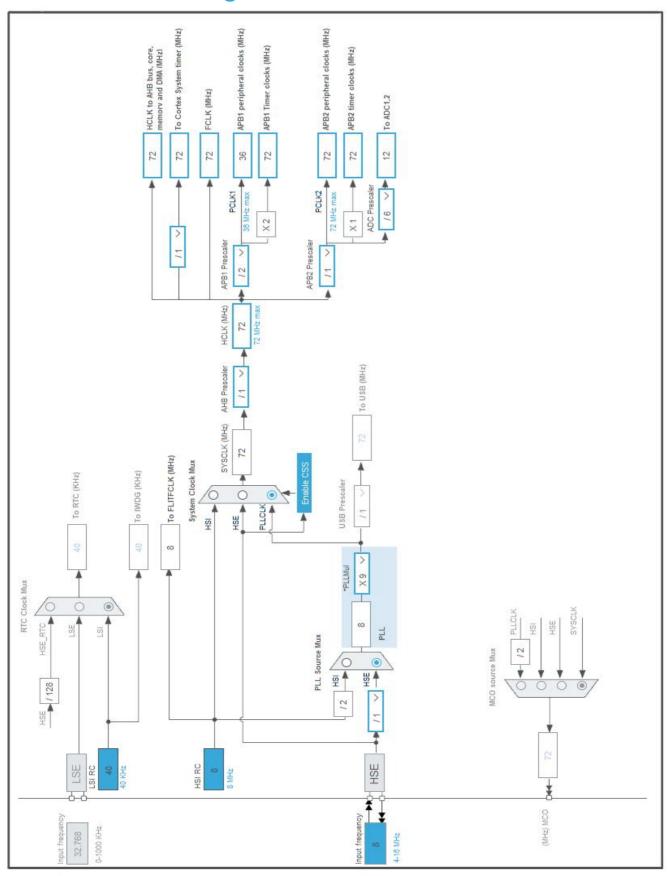


# 3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
11	PA1	I/O	ADC1_IN1	
12	PA2	I/O	ADC1_IN2	
13	PA3	I/O	ADC1_IN3	
16	PA6	I/O	TIM3_CH1	
17	PA7	I/O	TIM3_CH2	
18	PB0	I/O	TIM3_CH3	
23	VSS	Power		
24	VDD	Power		
35	VSS	Power		
36	VDD	Power		
41	PB5 *	I/O	GPIO_Input	encoderBtn
42	PB6 *	I/O	GPIO_Input	encoderPinB
43	PB7 *	I/O	GPIO_Input	encoderPinA
44	воото	Boot		
45	PB8	I/O	I2C1_SCL	
46	PB9	I/O	I2C1_SDA	
47	VSS	Power		
48	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

Name	Value	
Project Name	heat_plate_stm32	
Project Folder	C:\Users\sky.chu\STM32CubeIDE\workspace_1.12.1\heat_plate_stm32	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.5	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_I2C1_Init	I2C1
5	MX_TIM2_Init	TIM2
6	MX_TIM3_Init	TIM3

# 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
мси	STM32F103C8Tx
Datasheet	DS5319_Rev17

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

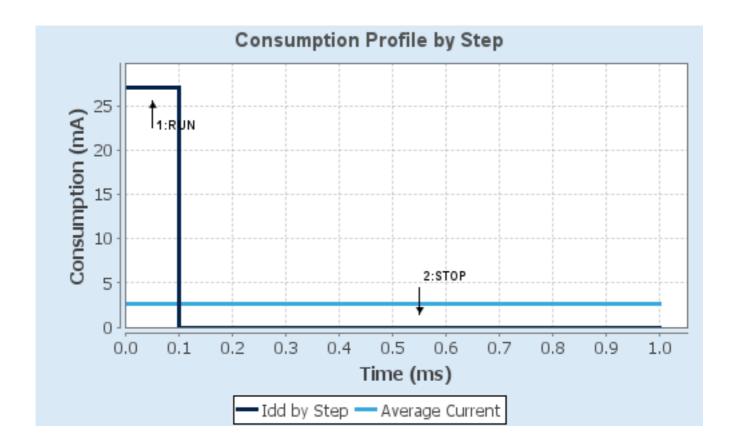
## 1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

### 1.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

### 1.6. Chart



# 2. Peripherals and Middlewares Configuration

2.1. ADC1 mode: IN1 mode: IN2 mode: IN3

2.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Enabled \*

Discontinuous Conversion Mode

Disabled

ADC Regular ConversionMode:

Enable Regular Conversions Enable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 1
Sampling Time 1.5 Cycles

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

2.2. I2C1 I2C: I2C

#### 2.2.1. Parameter Settings:

**Master Features:** 

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

**Slave Features:** 

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

#### 2.3. RCC

#### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 2.3.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

#### 2.4. SYS

**Debug: No Debug** 

Timebase Source: SysTick

#### 2.5. TIM2

**Clock Source: Internal Clock** 

#### 2.5.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

24-1 \*

Up

No Division

Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### 2.6. TIM3

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3

#### 2.6.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### **PWM Generation Channel 2:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

#### **PWM Generation Channel 3:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### \* User modified value

# 3. System Configuration

## 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	n/a	n/a	
	PA2	ADC1_IN2	Analog mode	n/a	n/a	
	PA3	ADC1_IN3	Analog mode	n/a	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	n/a	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	n/a	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	n/a	Low	
GPIO	PC13- TAMPER- RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	encoderBtn
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	encoderPinB
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	encoderPinA

## 3.2. DMA configuration

nothing configured in DMA service

## 3.3. NVIC configuration

## 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 and ADC2 global interrupts	unused			
TIM2 global interrupt	unused			
TIM3 global interrupt	unused			
I2C1 event interrupt	unused			
I2C1 error interrupt	unused			

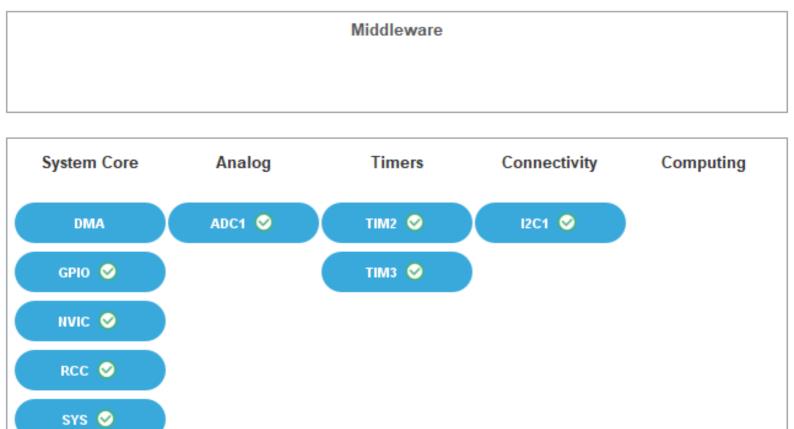
### 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

#### \* User modified value

# 4. System Views

- 4.1. Category view
- 4.1.1. Current



### 5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32f1\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1\_svd.zip

Description

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