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Assignment/Lab Title:	3-Stage Amplifier using NPN BJT

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Student Name	Student ID	Signature*

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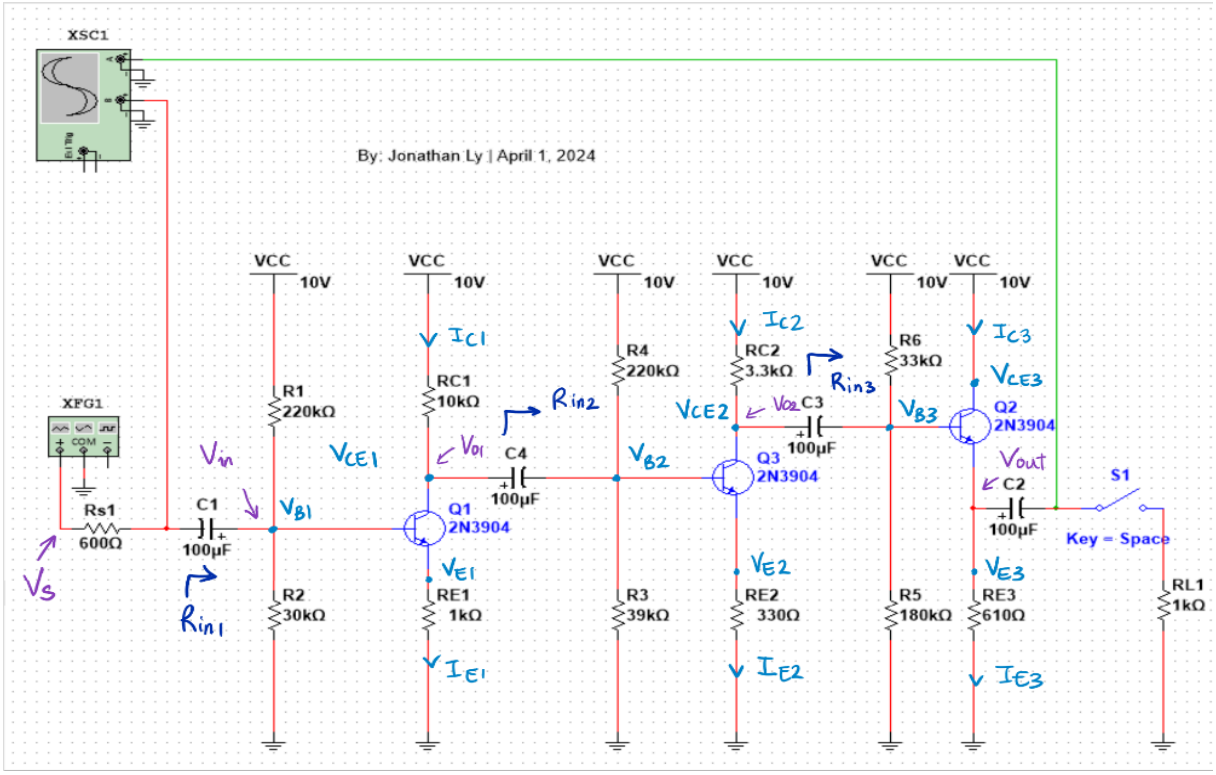
Figure 1.0: Multisim of 3-Stage Amplifier Circuit



Description

A 3-stage non-inverting Amplifier using E24 resistors and three 2N3904 BJT. This is non-inverting because both CE stages will give a 360 phase shift which is back to what the input phase was.

1. Introduction

The goal of this design project is to design an amplifier circuit made out of 2N3904 NPN Bipolar Junction Transistors using the required specifications from Table 1.1. The Appendix at the end of this report, contains: (1) formulas used for manual calculations, (2) manual calculation analysis and (3) a google link containing all necessary files. I will also simulate the design using Multisim to verify the design analysis.

Table 1.0: Design Specifications

Specifications

- Power supply: $+\mathbf{10V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than* 10 *mA*;**
- No-load voltage gain (at 1 kHz): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10\%})$;
- Maximum no-load output voltage swing (at 1 kHz): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at 1 kHz and with $R_L = 1\ k\Omega$): ***no smaller than* 90% *of the no-load voltage gain;***
- Maximum loaded output voltage swing (at 1 kHz and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at 1 kHz): ***no smaller than* 20 *kΩ***;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (−3dB response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than* 220 *kΩ from the E24 series***;
- Capacitors permitted: **0.1 *μF*, 1.0 *μF*, 2.2 *μF*, 4.7 *μF*, 10 *μF*, 47 *μF*, 100 *μF*, 220 *μF*;**
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

2. Designing & Analysis

The design of choice is a 3-Stage amplifier that consists of : (1) first stage as a Common Emitter, (2) second stage as another Common Emitter and (3) third stage as a Common Collector or also known as an Emitter Follower.

The reason for the first and second stage as both Common Emitter is because that a Common Emitter amplifier offers a high input impedance and low output impedance. One of the requirements outlined in Table 1.1 states that the input impedance must be at least 20 kΩ. The idea is to design the first stage with a gain $A_{V1} \approx 5$ and the second stage with a gain $A_{V2} \approx 10$. The formulas for a Common Emitter and Common Collector gain can be found in appendix of Table 6.0 and will be used for all calculations found in the appendix.

To initially design stage 1, the goal is to achieve a gain A_{V1} of approximately 5. Table 6.1 shows the calculations and analysis for stage 1. I first arbitrarily chose a quiescent current I_{C1} of 0.45 mA which meets the requirements of under 10 mA. Knowing that the gain A_{V1} equations involve the R_{C1}, R_{E1}, R_{in2} & g_{m1}. I must choose resistors wisely to achieve a gain of approximately 5 and keeping in mind the input resistance in stage 2 R_{in2} is parallel with $R_{C1,}$ which will greatly impact the gain of stage 1. So I decided to choose an equivalent resistance R_{eq} of approximately 5 kΩ. I

used the I_{C1}, R_{eq1} and g_{m1} to solve for R_{E1}. Once I got $R_{E1} \approx 1\ k\Omega$, I used the quiescent current formula to solve for $R_{C1} \approx 10\ k\Omega$. To Bias the V_B, I did KVL at the base of stage 1 and KCL at the base. I decided to choose R_1 as 220 kΩ since we want a large resistance for R_{in1}. We can calculate for V_E from first finding I_{E1} and knowing what R_{E1} is. After knowing all the unknown, I can calculate R_2 using the KCL at V_B. I will get $R_2 \approx 30\ k\Omega$. After that, I then calculate for R_{in1} to check if I met the input resistance requirement. The calculated R_{in} was approximately $R_{in1} \approx 23.2\ k\Omega$ which met the specification.

To design the stage 2, the formula and process is very similar to stage 1. Process work can be found under Table 6.2 in appendix. This time I chose $I_{C2} \approx 1.5$ mA which meets the conditions of under 10 mA and I was reaching for $A_{v2} \approx 10$. I acknowledge that R_{in3} will impact my gain, so I chose a the $R_{eq2} \approx 2.5\ k\Omega$. I chose $R_4 \approx 220\ k\Omega$ because I want R_{in2} to have a high input impedance. I proceeded to calculate for $R_3 \approx 39\ k\Omega$. Checking R_{in2} is approximately $R_{in} \approx 20.3\ k\Omega$ which meets the specification.

To design the stage 3, I tried and tested for the best R_{E3} resistance to get a gain of $A_{V3} \approx 1$. I found using a R_{E3} of 610 Ω to get $A_{V3} \approx 0.9957$. Since I chose R_{E3} as 610, the $I_{C3} \approx 9.8$ mA which is still under the requirement of 10 mA. I then repeated the same steps to find the biasing resistors. The $R_{in3} \approx 21.42\ k\Omega$ after calculations which is within specifications. Calculations for stage 3 can be found in Table 6.3 in appendix.

Table 2.0: Capacitance Calculations

Suppose I choose: C = 100 µF

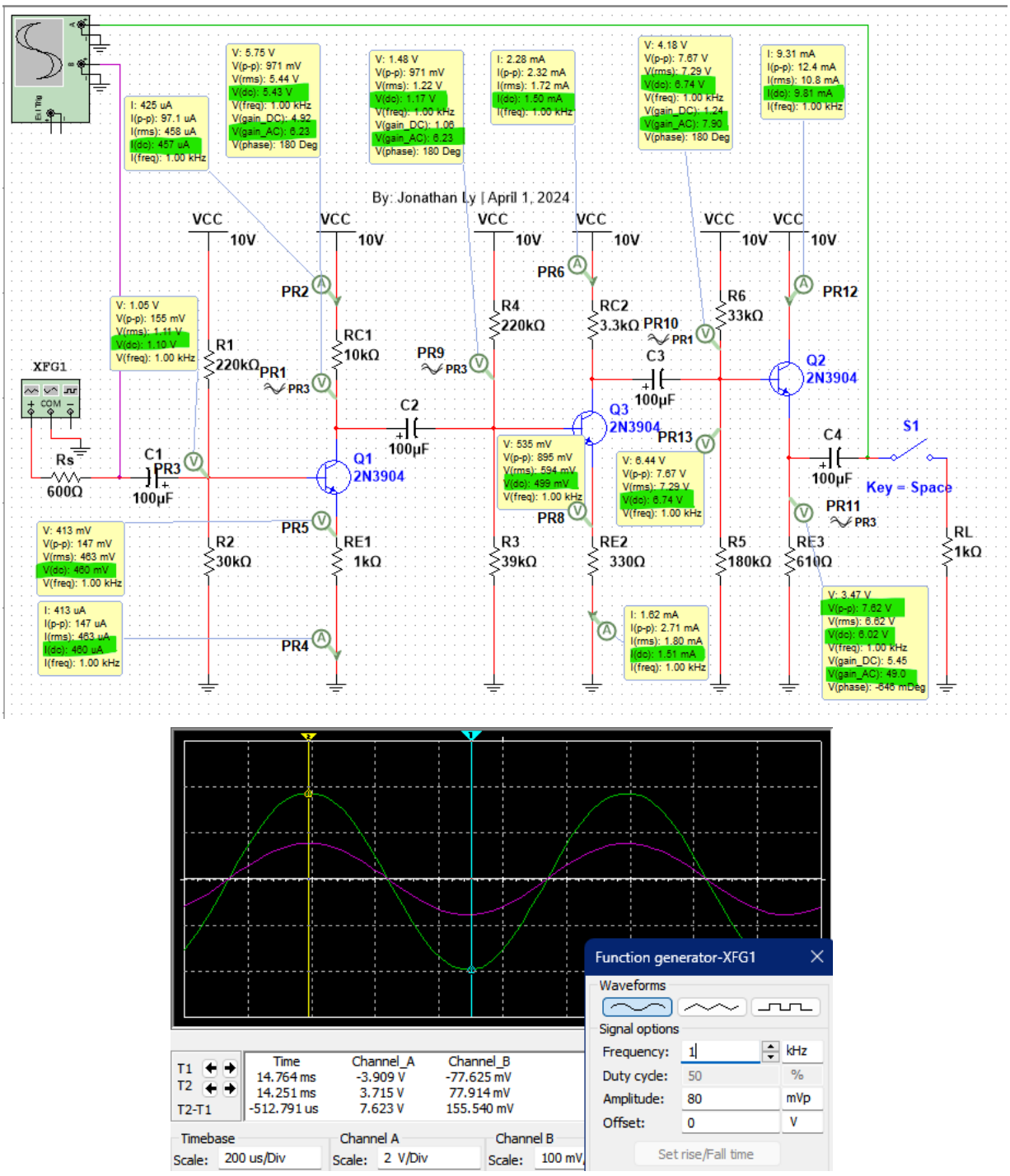
f_{min} = 20 hz	f_{max} = 50 khz
$R_{min} = \frac{1}{2\pi \bullet f_{in} \bullet C}$ $R_{min} = \frac{1}{2\pi \bullet (20) \bullet (100 \times 10^{-6})}$ $R_{min} \simeq 79.58\ \Omega$	$R_{max} = \frac{1}{2\pi \bullet f_{in} \bullet C}$ $R_{max} = \frac{1}{2\pi \bullet (50 \times 10^{3}) \bullet (100 \times 10^{-6})}$ $R_{max} \simeq 0.0318\ \Omega$

Description

When selecting a good isolating capacitor for between stages, input source and for load, I want the lowest possible input impedance that the circuit will present under AC conditions to have the lowest impact on the result of my circuit. When applying a minimum frequency of 20 hz, the resistance that the capacitor will present is around 80 Ω and with maximum frequency of 50 khz, the maximum resistance is around 0.03 Ω. These resistance values are very small so choosing the capacitor with capacitance of 100 µF will be desired for this circuit operating at that frequency.

3. Simulation on Multisim

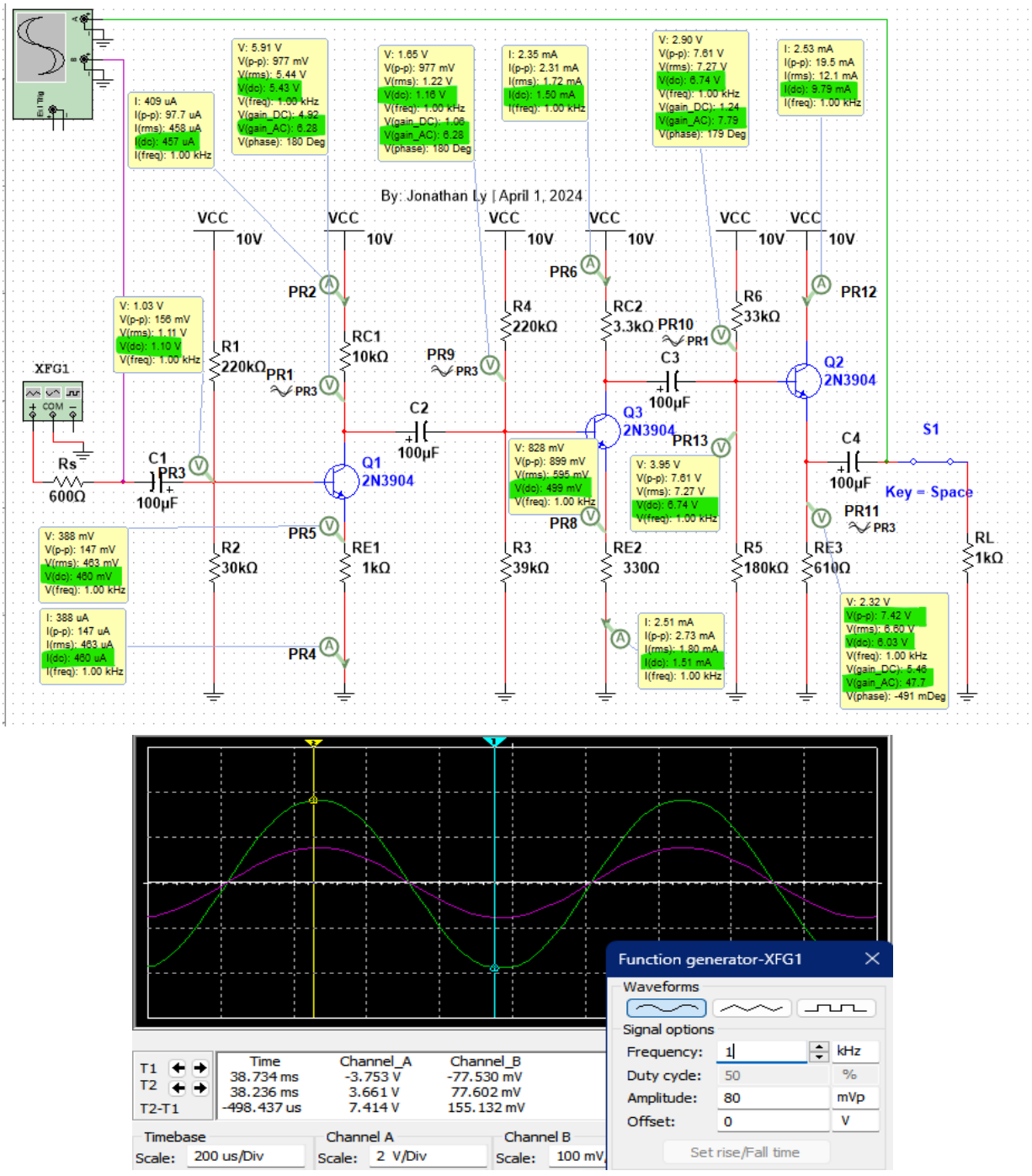
Figure 3.0: Multisim Simulation without load, $R_L = \infty$



Description

The circuit under test is without load, When inputting 80mV vp, I get 7.623 V vpp which is roughly 8 vpp. The gain is also roughly 49 which meets the specification within 10% of 50.

Figure 3.1: Multisim Simulation with load, R_L = 1 kΩ



Description

The circuit under test is with load. When inputting 80mV vp, I get 7.414 V vpp which is roughly over the 4 vpp requirement. The gain is also roughly 47.8 (within 90% of without load) which meets the specification.

4. Experimental Results

Table 4.0: Summary of Theoretical (Calculated) and Simulated Results		
Values (w/o load)	Theoretical	Simulated
A_{V1}	6.334	6.28
A_{V2}	8.233	7.90
A_{VT}	50.61	49.00
I_{C1}	0.45 mA	0.457 mA
I_{C2}	1.50 mA	1.50 mA
I_{C3}	9.80 mA	9.79 mA
V_{E1}	0.453 V	0.460 V
V_{E2}	0.4983 V	0.499 V
V_{E3}	6.6178 V	6.02 V
V_{B1}	1.153 V	1.10 V
V_{B2}	1.1983 V	1.16 V
V_{B3}	6.7178 V	6.75 V
Description		
When comparing Theoretical and Simulated respective values when no load is attached, the values look quite similar. Possible discrepancies might be due to rounding errors during calculation.		

5. Conclusions and Remarks

In summary, designing the 3-stage amplifier using Common Emitter in both stage 1 and stage 2 and also a Common Collector for stage 3 demonstrated that the design met with design specifications outlined in Table 1.0. The goal of reaching approximately gain $A_{VT} \approx 50$ without load and 90 % ($A_{VT} \approx 45$) of without load gain for with load were met. Also 8vpp without load is met when 80 mV Vp was input. Similarly the above 4vpp with load is met. For all R_{in} of each stage met the requirement of over 20 kΩ. In conclusion, the 3-stage amplifier design was successful according to the theoretical calculations and simulated results.

6. Appendix

Table 6.0: Derived Formulas used in Calculations

Formula	Common Emitter (Inverting of Output)	Common Collector (Emitter Follower)
$A_V = \frac{V_{OUT}}{V_{IN}}$	$\frac{g_m \bullet R_c // R_{in}}{1 + g_m R_E} = \frac{R_c // R_{in}}{\frac{1}{g_m} + R_E}$	$\frac{(\beta + 1) \bullet R_E}{(\beta + 1) \bullet R_E + r_{BE}} \approx 1$
R_{eq}	$R_{eq} = R_C // R_{in}$	
R_{in}	$R_{series} + R_{bias} // [r_{BE} + (\beta + 1)(R_E)]$	
KCL at V_B	$\frac{V_B - V_{cc}}{R_1} + \frac{V_B - 0}{R_2} + I_B = 0$	
V_E	$V_E = I_E \bullet R_E$	
KVL at base	$V_B = V_{BE,ON} + V_E$	
I_C	$I_c = \beta \bullet I_B$	
I_B	$I_E = I_c \bullet (1 + \beta)$	
r_{BE}	$r_{BE} = \frac{\beta}{g_m}$	
g_m	$g_m = \frac{I_C}{V_t}$	
Quiescent I_C	$I_{CQ} = \frac{V_{CEQ}}{R_C + R_E}; V_{CEQ} = \frac{V_{CC}}{2}$	
Capacitance	$f_{in} = \frac{1}{2\pi \bullet R_{in} \bullet C}$	

Definitions

A_V: Gain of amplifier.
R_{in}: Input Resistance of the amplifier.
R_c: Resistor at Collector.
R_E: Resistor at Emitter.
R_{eq}: Equivalent Resistance of R_c & R_{in} parallel.
R_{series}: Resistors that are in series in the base.
R_{bias}: Resistors that are for biasing the base (usually 2 resistors parallel).

R_1 // R_2: Means R_1 parallel to R_2 resistors.
r_{BE}: Internal resistance in BJT between base and emitter.
g_m: Transconductance of BJT.
I_B: Base current.
I_E: Emitter current.
I_C: Collector current.
V_E: Emitter voltage of Resistor R_E.
$V_{BE,ON}$: Approximately 0.7 V.
V_t = Approximately 26 mV.
V_{CEQ}: Quiescent voltage across V_C and V_E.
V_{cc}: supply voltage of 10V.

Table 6.1: Stage 1 Calculations (CE Amplifier)

Stage 1 Theoretical :

Goal $A_{V1} \approx 5$

let: $R_{eq1} = R_{C1} // R_{in2} \approx 5\ K\Omega$

Choose $I_{C1} \approx 0.45\ mA \leq 10^{mA}$ (condition met)

$V_{CE1} = \frac{1}{2} V_{cc} = 5^V$

$$I_{C1} = \frac{V_{CE1}}{R_{C1} + R_{E1}} \quad (1) \qquad g_{m1} = \frac{I_{C1}}{V_t} \quad (2)$$

$$\frac{1}{g_{m1}} \approx 57.7\ \Omega$$

$$I_{C1} \cdot R_{C1} + R_{E1} \cdot I_{C1} = V_{CE1}$$

$$R_{C1} = \frac{V_{CE1} - R_{E1} \cdot I_{C1}}{I_{C1}} = \frac{5^V - (1^{K\Omega})(0.45^{mA})}{(0.45^{mA})}$$

$R_{C1} = 10,111\ \Omega \approx 10K\Omega$

Since $R_{eq} = R_{C1} // R_{in2}$

if $R_{eq1} \approx 5^{K\Omega}$, then $R_{C1} = 10^{K\Omega}$

$R_{in2} \geq 10^{K\Omega}$

↳ input Resistance of stage 2.

$$A_{V1} = \frac{R_{C1} // R_{in2}}{\frac{1}{g_{m1}} + R_{E1}} = \frac{R_{eq1}}{\frac{1}{g_{m1}} + R_{E1}} \quad (3)$$

$A_{V1} \cdot \frac{V_t}{I_{C1}} + A_{V1} \cdot R_{E1} = R_{eq1}$ ← (2)

$$R_{E1} = \frac{R_{eq1} - A_{V1}\left(\frac{V_t}{I_{C1}}\right)}{A_{V1}}$$

$$R_{E1} = \frac{5^{K\Omega} - 5\left(\frac{26^{mV}}{0.45^{mA}}\right)}{5}$$

$R_{E1} = 942.22\ \Omega \approx 1K\Omega$

$I_{E1} = I_{C1}\left(1 + \frac{1}{\beta}\right)$

$I_{E1} = 0.45\,mA\left(1 + \frac{1}{150}\right)$

$I_{E1} = 0.453\,mA$

$V_{E1} = R_{E1} \cdot I_{E1}$

$= (1\,K\Omega)(0.453\,mA)$

$V_{E1} = 0.453\,V$

KVL @ base of stage 1

$V_B = V_{BE,ON} + V_E$

$V_B = 1.153\,V$

Biasing at V_{B1}:

$I_{B1} = \frac{I_{C3}}{\beta}$

$$\frac{V_{B1} - V_{CC}}{R_1} + \frac{V_b}{R_2} + I_{B1} = 0$$

$$r_{be} = \frac{\beta}{g_m} = \frac{\beta}{\left(\frac{I_{C1}}{V_t}\right)}$$

$r_{be} = 8,666.67\,\Omega$

$$R_2 = \frac{V_{B1}}{\left(\frac{V_{CC} - V_{B1}}{R_1} - I_{B1}\right)}$$

Suppose we choose $R_1 = 220\,K\Omega$

$$R_2 = \frac{1.153}{\left(\frac{10 - 1.153}{220\,K\Omega}\right) - \left(\frac{0.45\,mA}{150}\right)}$$

$R_2 = 30,983.26 \approx 30\,K\Omega$

$R_{in1} = R_S + R_1 \,//\, R_2 \,//\, [r_{be} + (\beta+1) \cdot R_{E1}]$

$= 600\,\Omega + 220\,K\Omega \,//\, 30\,K\Omega \,//\, [8,666.67\,\Omega + (151)(1\,K)]$

$R_{in1} = 23,254.24\,\Omega \geq 20\,K\Omega$ (Condition met)

Summary of Theoretical Stage 1:

$A_V = 5$ Assuming $R_{in2} \approx 10\,K\Omega$

$R_{C1} = 10\,K\Omega$

$R_{E1} = 1\,K\Omega$

$R_1 = 30\,K\Omega$

$R_2 = 220\,K\Omega$

$I_{C1} \approx 0.45\,mA$

$I_{E1} \approx 0.453\,mA$

$V_{E1} \approx 0.453\,mV$

$V_{B1} \approx 1.153\,V$

Table 6.2: Stage 2 Calculations (CE Amplifier)

Stage 2 theoretical :

Goal $A_{V1} \approx 10$

let: $R_{eq2} = R_{C2} \parallel R_{in3} \approx 2.5\ K\Omega$

Choose $I_{C2} \approx 1.5\ mA \leq 10\ mA$ (condition met)

$V_{CE1} = \frac{1}{2} V_{CC} = 5^V$

$I_{C2} = \frac{V_{CE2}}{R_{C2} + R_{E2}}$ ① $g_{m2} = \frac{I_{C2}}{V_t}$ ②

$I_{C2} R_{C2} + R_{E2} \cdot I_{C2} = V_{CE2}$

$R_{C2} = \frac{V_{CE2} - R_{E2} \cdot I_{C2}}{I_{C2}}$

$= \frac{5^V - (312)(1.5\ mA)}{(1.5\ mA)}$

$R_{C2} = 3{,}020\ \Omega \approx 3.3\ K\Omega$

$\frac{1}{g_{m2}} = \frac{26\ mV}{1.5\ mA}$

$\frac{1}{g_{m2}} \approx 17.3\ \Omega$

$I_{E1} = I_{C2}\left(1 + \frac{1}{\beta}\right)$

$I_{E2} = 1.5\ mA\left(1 + \frac{1}{150}\right)$

$I_{E2} = 1.51\ mA$

$V_{E2} = R_{E1} \cdot I_{E1}$

$= (330)(1.51\ mA)$

$V_{E2} = 0.4983^V$

$\frac{V_{B2} - V_{CC}}{R_4} + \frac{V_b}{R_3} + I_{B2} = 0$ ← $I_{B2} = \frac{I_{C2}}{\beta}$

$R_3 = \frac{V_{B2}}{\left(\frac{V_{CC} - V_{B2}}{R_4} - I_{B2}\right)}$

Suppose we choose $R_4 = 220\ K\Omega$

$R_3 = \frac{1.1983}{\left(\frac{10 - 1.1983}{220\ K\Omega}\right) - \left(\frac{1.5\ mA}{150}\right)}$

$R_3 = 39{,}933\ K\Omega \approx 39\ K\Omega$

$R_{in1} = R_3 \parallel R_4 \parallel [r_{be2} + (\beta + 1) \cdot R_{E1}]$

$= 39^{K\Omega} \parallel 220^{K\Omega} \parallel [2600 + \underbrace{151 \cdot (330)}_{52{,}430}]$

$R_{in2} = 20{,}300.64\ \Omega \geq 20\ K\Omega$ (conditions met)

Actual $R_{in3} = 2{,}859.60\ \Omega$

Suppose $R_{eq2} = 3.3^{K\Omega}$

$R_{eq2} = R_{C2} \parallel R_{in3}$

Then, $R_{C2} = 3.3^{K\Omega}$ & $R_{in} \geq 20^{K\Omega}$

$A_{V2} = \frac{R_{C2} \parallel R_{in3}}{\frac{1}{g_{m2}} + R_{E2}} = \frac{R_{eq2}}{\frac{1}{g_{m2}} + R_{E2}}$ ③

$A_{V2} \cdot \frac{V_t}{I_{C2}} + A_{V2} R_{E2} = R_{eq2}$ ← ②

$R_{E2} = \frac{R_{eq2} - A_{V2}\left(\frac{V_t}{I_{C2}}\right)}{A_{V2}}$

$R_{E2} = \frac{3.3^{K\Omega} - 10\left(\frac{26\ mV}{1.5\ mA}\right)}{10}$

$R_{E2} = 312.67^{\Omega} \approx 330\ \Omega$

KVL @ base of stage 1

$V_{B2} = V_{BE,ON} + V_{E2}$

$= 0.7 + 0.4983$

$V_{B2} = 1.1983\ V$

$r_{be2} = \frac{\beta}{\left(\frac{I_{C2}}{V_t}\right)}$

$= \frac{150}{\left(\frac{1.5\ mA}{26\ mV}\right)}$

$r_{be2} = 2600\ \Omega$

Table 6.3: Stage 3 Calculations (CC/ Emitter Follower)

Stage 3: Common Collector (Emitter follower):

$$A_{V3} = \frac{(\beta+1)R_{E3}}{(\beta+1)R_{E3} + r_{be} \parallel R_5 \parallel R_6} \approx 1$$

ignore R_5 & R_6 iff, $R_5 \parallel R_6 \gg r_{be}$

$$r_{be3} = \frac{\beta}{\left(\frac{I_{C3}}{V_t}\right)} = \frac{\beta \cdot V_t}{I_{C3}} = 150\left(\frac{26\,mV}{9.8\,mA}\right) = 397.9\,\Omega$$

Suppose $R_{E3} = 610$

$I_{C3} = 9.8\,mA \leq 10\,mA$

$$I_{E3} = I_{C3}\left(1 + \frac{1}{\beta}\right) = (9.8\,mA)\left(1 + \frac{1}{150}\right)$$

$I_{E3} = 9.866\,mA$

$$A_{V3} = \frac{(151)(610)}{(151)(610) + \left(\frac{(150)(26)}{9.8}\right)}$$

$A_{V3} = 0.9957 \approx 1$ (good)

$$V_{E3} = I_{E3} \cdot R_{E3} = (9.866\,mA)(610)$$

$V_{E3} = 6.017\,V$

$$V_{B3} = V_{BE,ON} + V_{E3} = 0.7 + 6.0178$$

$V_{B3} = 6.7178\,V$

$$r_{be3} = \frac{\beta}{\frac{I_{C3}}{V_t}}$$

$$R_{in3} = R_5 \parallel R_6 \parallel \left[r_{be3} + (1+\beta)R_{E3}\right]$$

$$= 180\,k\Omega \parallel 33\,k\Omega \parallel \left[397.9\,\Omega + (151)(610)\right]$$

$R_{in3} = 21,427.74\,\Omega \geq 20\,k\Omega$ (conditions met)

$$I_{B3} = \frac{I_{C3}}{\beta}$$

$$\frac{V_{B3} - V_{CC}}{R_6} + \frac{V_b}{R_5} + I_{B3} = 0$$

$$R_5 = \frac{V_{B3}}{\left(\frac{V_{CC} - V_{B3}}{R_6} - I_{B3}\right)}$$

Suppose we choose $R_6 = 33\,k\Omega$.

$$R_5 = \frac{6.7178}{\left(\frac{10 - 6.7178}{33\,k\Omega}\right) - \left(\frac{9.8\,mA}{150}\right)}$$

$R_5 = 196,845\,\Omega \approx 180\,k\Omega$

Table 6.4: Calculating Theoretical Total Gain (A_{VT})

Calculating theoretical gain of Input Stage + CE (Stage 1) + CE (stage 2) + CC (stage 3):

Input stage :

$$A_{VS} = \frac{V_{in}}{V_S} = \frac{R_{in1}}{R_{in} + R_S} = \frac{23,254.24}{23,254.24 + 600} \approx 0.9748$$

CE stage 1:

$$A_{V1} = \frac{V_{O1}}{V_{in}} = \frac{R_{C1} \,//\, R_{in2}}{\frac{1}{g_{m1}} + R_{E1}} = \frac{10\text{k}\Omega \,//\, 20,300.64\Omega}{57.\overline{7}\Omega + 1\text{k}\Omega} \approx 6.334$$

CE stage 2:

$$A_{V2} = \frac{V_{O2}}{V_{O1}} = \frac{R_{C2} \,//\, R_{in3}}{\frac{1}{g_{m2}} + R_{E2}} = \frac{3.3\text{k}\Omega \,//\, 21,427.74\Omega}{17.\overline{3}\Omega + 330\Omega} \approx 8.233$$

CE stage 3 :

$$A_{V3} = \frac{V_{out}}{V_{O2}} = \frac{(1+\beta) R_{E3}}{(1+\beta) R_{E3} + r_{be}} = \frac{(151)(610)}{(151)(610) + 397.9\Omega} \approx 0.9957$$

Approximate Theoretical Total Gain :

$$A_{VT} = \frac{V_{out}}{V_S} = \frac{V_{in}}{V_S} \times \frac{V_{O1}}{V_{in}} \times \frac{V_{O2}}{V_{O1}} \times \frac{V_{out}}{V_{O2}}$$

$$= 0.9748 \times 6.334 \times 8.233 \times 0.9957$$

$$A_{VT} \approx 50.61$$

∴ The total Gain (A_{VT}) of this 3-stage Amplifier Circuit is approximately 50.61

7. References

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