

TSPi Plan Summary: Form SUMP

| | | | |
|------------|-------------|------------|-------------------------------|
| Name | Lee Fui Yee | Date | 9 th December 2014 |
| Team | Five Stars | Instructor | Mdm Nurfaeza Jali |
| Part/Level | Iteration | Cycle | 1 |

| Product Size | Plan | Actual |
|---------------------------------|-------------|------------|
| Requirements pages (SRS) | 32 | 41 |
| Other text pages | | |
| High-level design pages (SDS) | 15 | 15 |
| Detailed design lines | | |
| Base LOC (B) (measured) | | |
| Deleted LOC (D) | | |
| | (Estimated) | (Counted) |
| Modified LOC (M) | | |
| | (Estimated) | (Counted) |
| Added LOC (A) | 3000 | 4064 |
| | (N-M) | (T-B+D-R) |
| Reused LOC (R) | | |
| | (Estimated) | (Counted) |
| Total New and Changed LOC (N) | 3000 | 4064 |
| | (Estimated) | (A+M) |
| Total LOC (T) | 3000 | 4064 |
| | (N+B-M-D+R) | (Measured) |
| Total New Reuse LOC | | |
| Estimated Object LOC (E) | | |
| Upper Prediction Interval (70%) | | |
| Lower Prediction Interval (70%) | | |

| Time in Phase (hours) | Plan | Actual | Actual % |
|------------------------------|------|--------|----------|
| Management and miscellaneous | 4 | 4 | 1.31 |
| Launch | 5 | 5 | 1.64 |
| Strategy and planning | 21 | 19 | 6.23 |
| Requirements | 15 | 13 | 4.26 |
| System test plan | 18 | 16 | 5.25 |
| Requirements inspection | 5 | 5 | 1.64 |
| High-level design | 13 | 13 | 4.26 |
| Integration test plan | 3 | 3 | 0.98 |
| High-level design inspection | 5 | 5 | 1.64 |
| Implementation planning | 4 | 4 | 1.31 |
| Detailed design | 15 | 13 | 4.26 |
| Detailed design review | 10 | 9 | 2.95 |
| Test development | 8 | 6 | 1.97 |
| Detailed design inspection | 18 | 18 | 5.90 |
| Code | 128 | 120 | 39.34 |
| Code review | 5 | 5 | 1.64 |
| Compile | 2 | 2 | 0.66 |
| Code inspection | 7 | 7 | 2.30 |
| Unit test | 8 | 7 | 2.30 |
| Build and integration | 2 | 2 | 0.66 |
| System test | 18 | 16 | 5.25 |
| Documentation | 10 | 10 | 3.28 |
| Postmortem | 4 | 3 | 0.98 |
| Total | 328 | 305 | 100.00 |
| Total Time UPI (70%) | | | |
| Total Time LPI (70%) | | | |

(continued)

TSPi Plan Summary: Form SUMP (continued)

| Defects Injected | Plan | Actual | Actual % |
|------------------------------|-------------|---------------|-----------------|
| Strategy and planning | - | - | - |
| Requirements | - | - | - |
| System test plan | - | - | - |
| Requirements inspection | - | - | - |
| High-level design | - | - | - |
| Integration test plan | - | - | - |
| High-level design inspection | - | - | - |
| Detailed design | - | - | - |
| Detailed design review | - | - | - |
| Test development | - | - | - |
| Detailed design inspection | - | - | - |
| Code | - | - | - |
| Code review | - | - | - |
| Compile | - | - | - |
| Code inspection | - | - | - |
| Unit test | - | - | - |
| Build and integration | - | - | - |
| System test | - | - | - |
| Total Development | - | - | - |
| Defects Removed | Plan | Actual | Actual % |
| Strategy and planning | - | - | - |
| Requirements | - | - | - |
| System test plan | - | - | - |
| Requirements inspection | - | - | - |
| High-level design | - | - | - |
| Integration test plan | - | - | - |
| High-level design inspection | - | - | - |
| Detailed design | - | - | - |
| Detailed design review | - | - | - |
| Test development | - | - | - |
| Detailed design inspection | - | - | - |
| Code | - | - | - |
| Code review | - | - | - |
| Compile | - | - | - |
| Code inspection | - | - | - |
| Unit test | - | - | - |
| Build and integration | - | - | - |
| System test | - | - | - |
| Total Development | - | - | - |