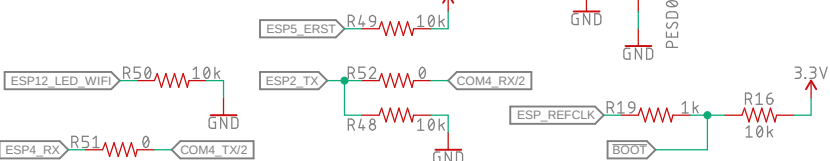
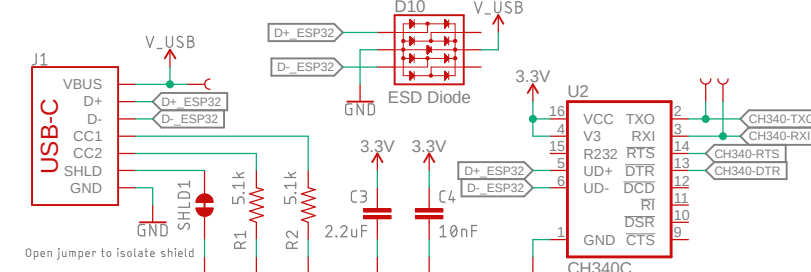


ESP32 WROVER

Use boot control pins with caution: 0, 2, 5, 12, 15
 I08: Avoid device connections.
 I02: Avoid external pullups - will cause bootload fail.
 I05: Has builtin pullup at POR.
 I012: Avoid external pullups - will cause bootload fail.
 I015: Has builtin pullup at POR. Also pulled up by R_SDA.
 ADC2 is unavailable when WIFI is enabled.

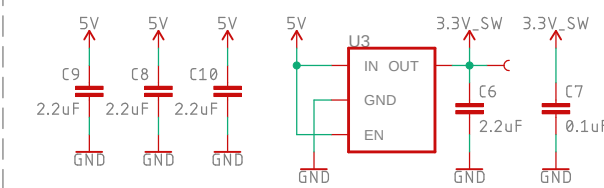


ESP32 USB-C

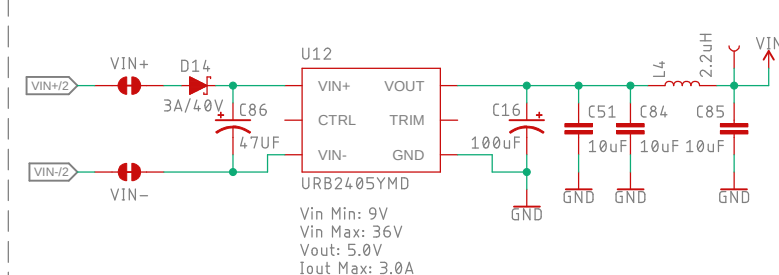


Secondary Power

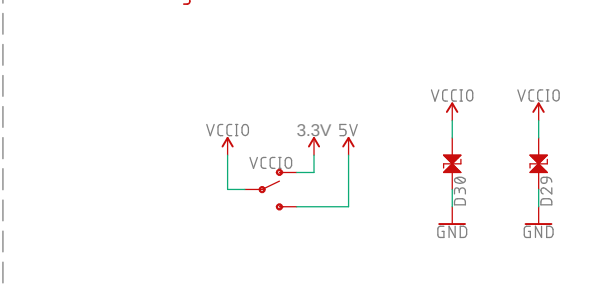
AP7361C-33
 Vin Max: 6.0V
 Iout Max: 1A (Limit 1.5A Typ)
 Vdo: 360mV @ 1A
 Output Discharge: 100Ω Typ



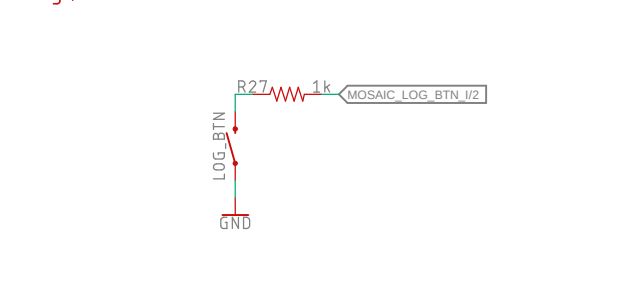
Power In



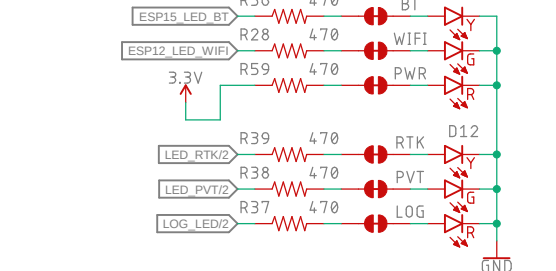
I/O Level Shifting



Log / Unmount SD Button

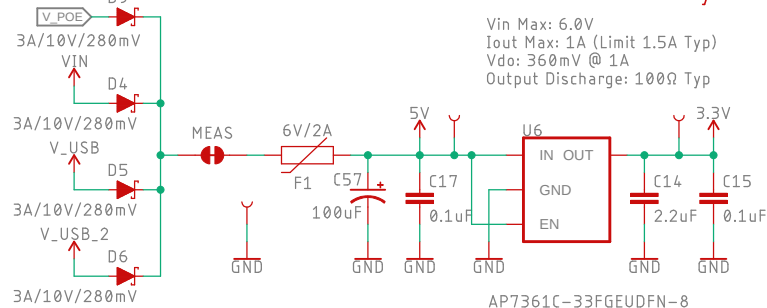


LEDs

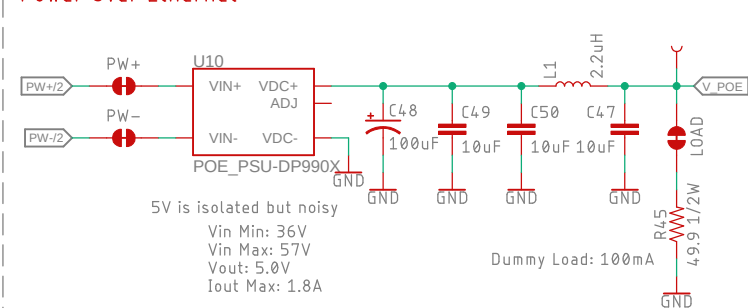


Primary Power

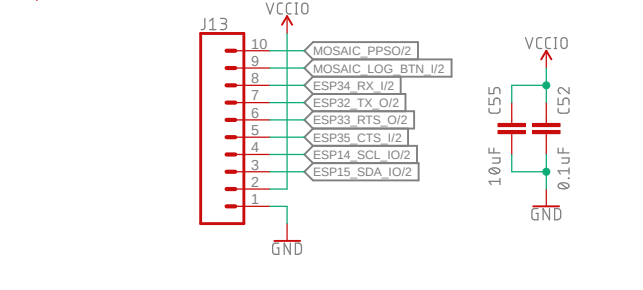
Vin Max: 6.0V
 Iout Max: 1A (Limit 1.5A Typ)
 Vdo: 360mV @ 1A
 Output Discharge: 100Ω Typ



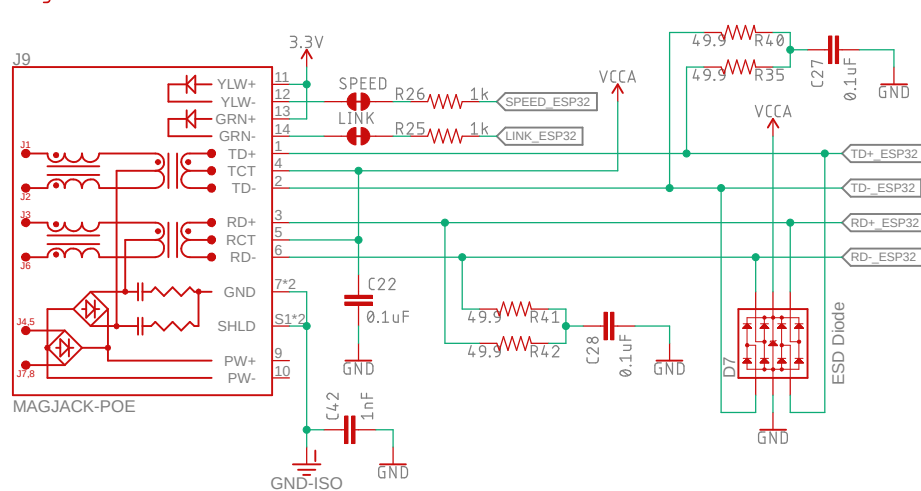
Power Over Ethernet



I/O Connector



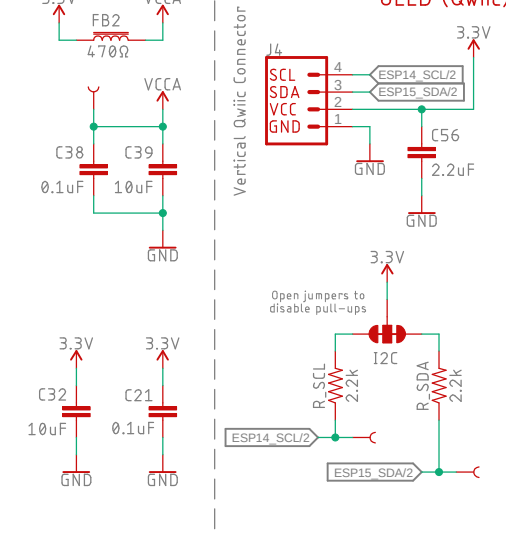
Mag Jack - ESP32



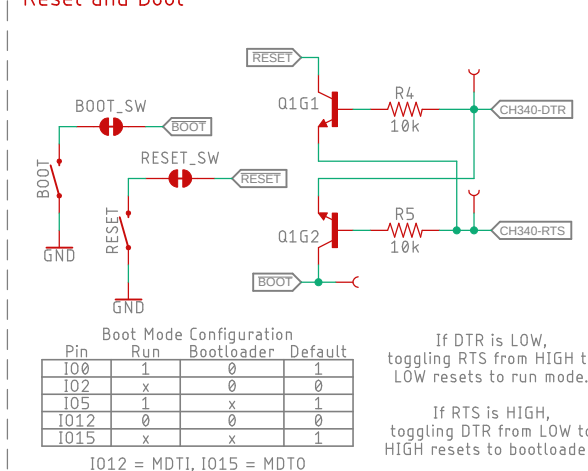
Ethernet PHY - ESP32

ESP32 GPIO0 - Ethernet PHY RMII Reference Clock (50MHz):
 Take care of the signal integrity of REF_CLK in the hardware design.
 Keep the trace as short as possible.
 Keep it away from RF devices and inductor elements.

OLED (Qwiic)



Reset and Boot



Pin	Run	Bootloader	Default
I00	1	0	1
I02	x	0	0
I05	1	x	1
I012	0	0	0
I015	x	x	1

If DTR is LOW,
 toggling RTS from HIGH to
 LOW resets to run mode.
 If RTS is HIGH,
 toggling DTR from LOW to
 HIGH resets to bootloader.

USB Track Impedance: Differential Pair
<https://saturnpcb.com/saturn-pcb-toolkit/>
 Prepreg thickness: 0.2mm (7.87 mil). Er = 4.6
 10.5 mil track with 9.5 mil gap (20 mil center to center) = 90 Ohms

RF Track Impedance: Coplanar Waveguide with Ground Calculations
 Ground is on layer 2. Prepreg thickness: 0.2mm. Er = 4.6
 12.5 mil track with 5 mil gap = 50 Ohms
<https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm>

ESP32 GPIO0 - Ethernet PHY RMII Reference Clock (50MHz):
 Take care of the signal integrity of REF_CLK in the hardware design.
 Keep the trace as short as possible.
 Keep it away from RF devices and inductor elements.



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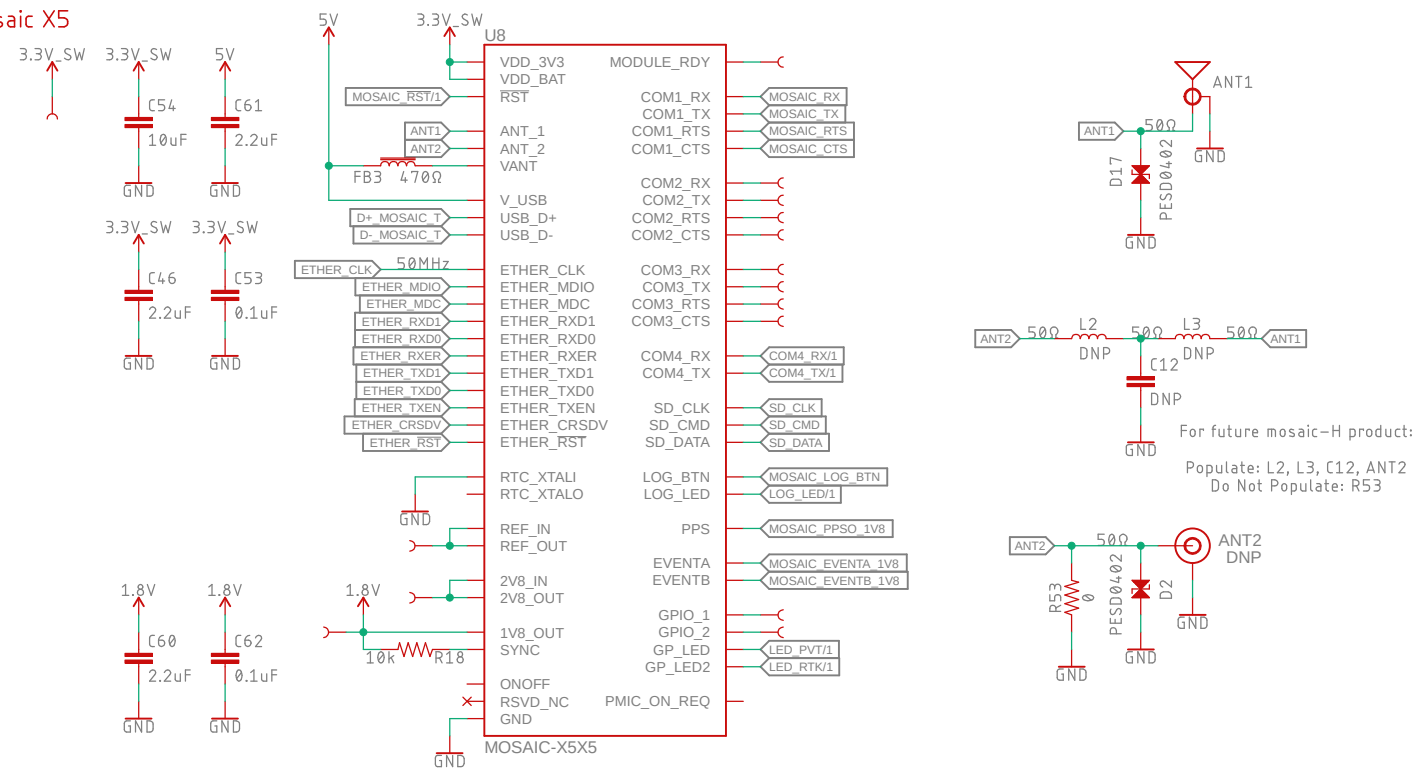
Design by: Paul Clark

REV:
 v10

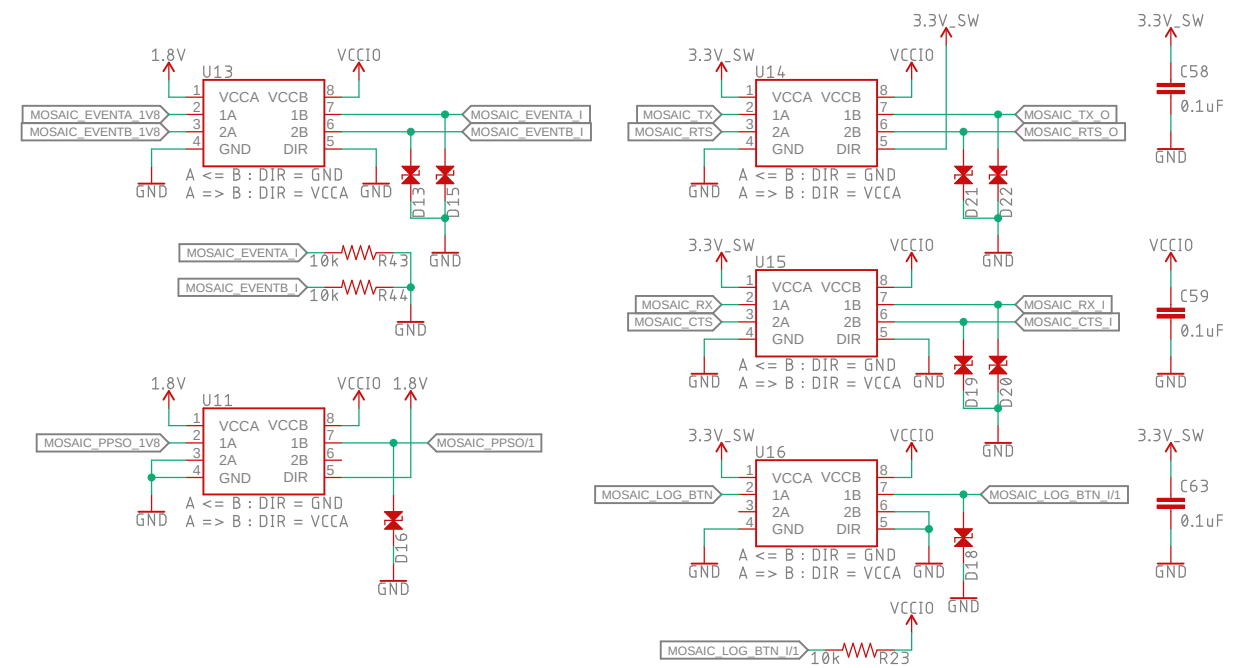
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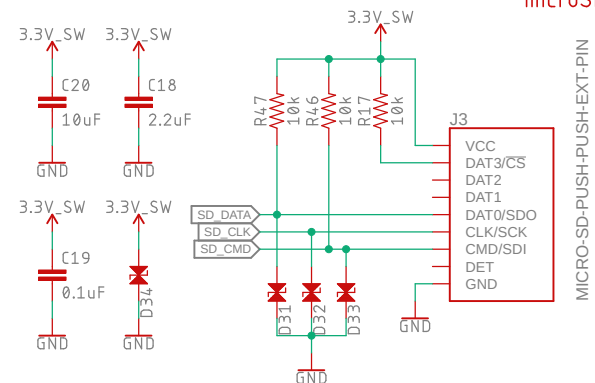
Mosaic X5



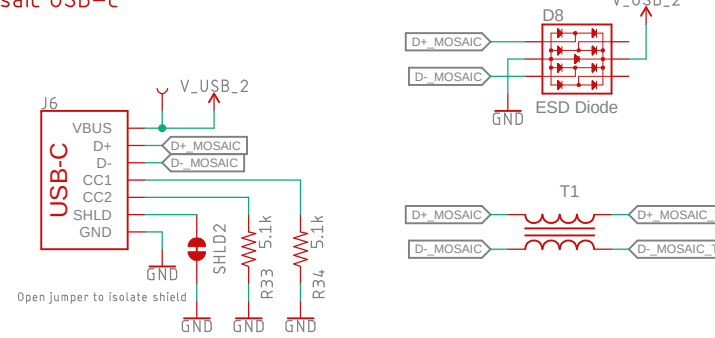
Mosaic IO Level Shifting



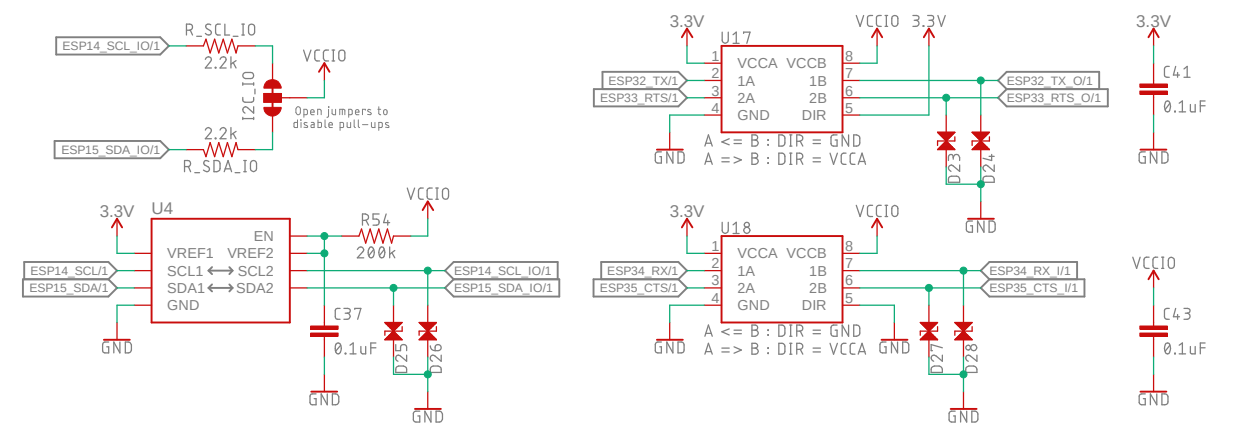
microSD



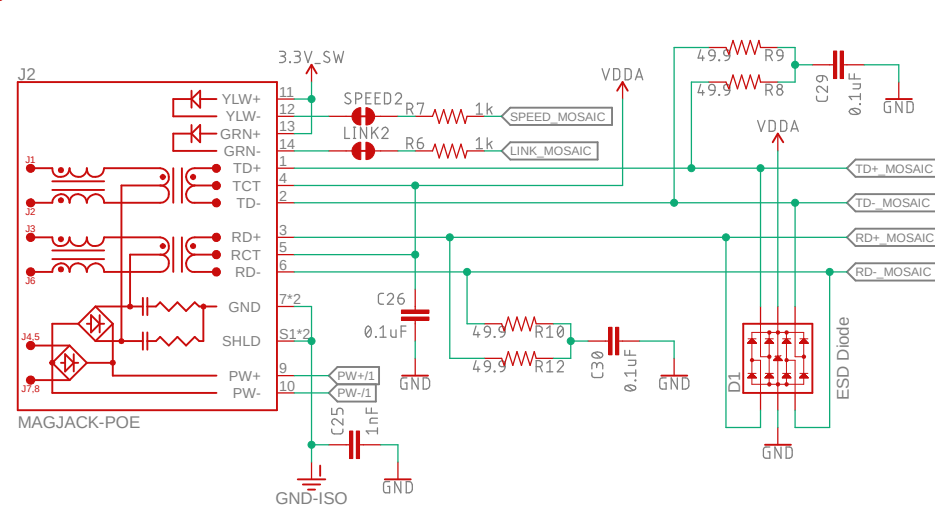
Mosaic USB-C



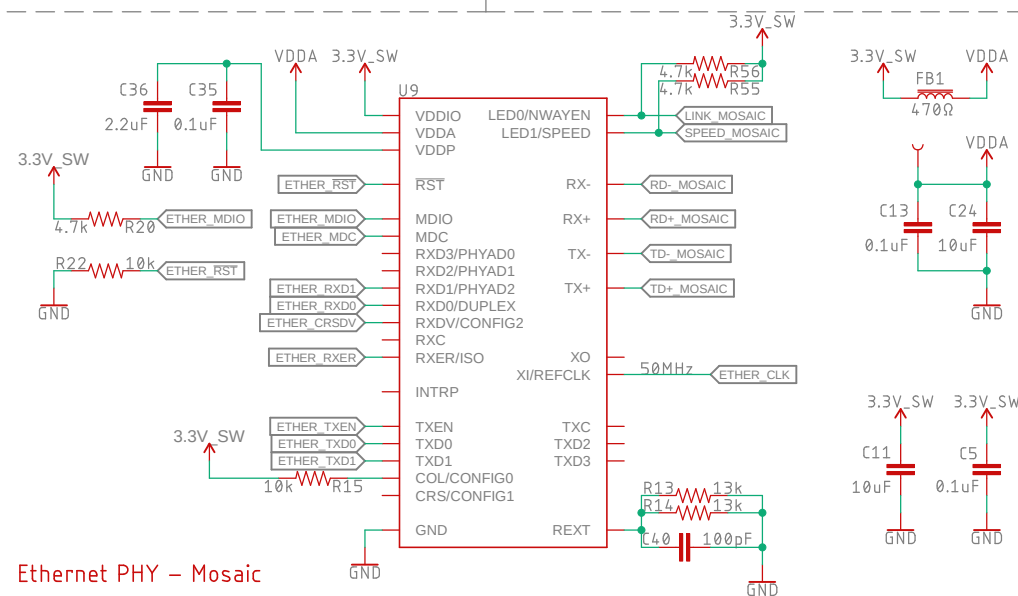
ESP32 IO Level Shifting



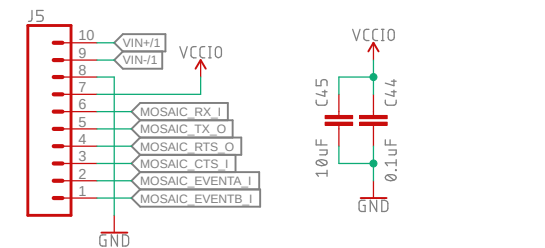
Mag Jack – Mosaic



Ethernet PHY – Mosaic



I/O Connector



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TITLE: RTK_mosaic-X5

Design by: Paul Clark

REV: v10

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Sheet: 2/2