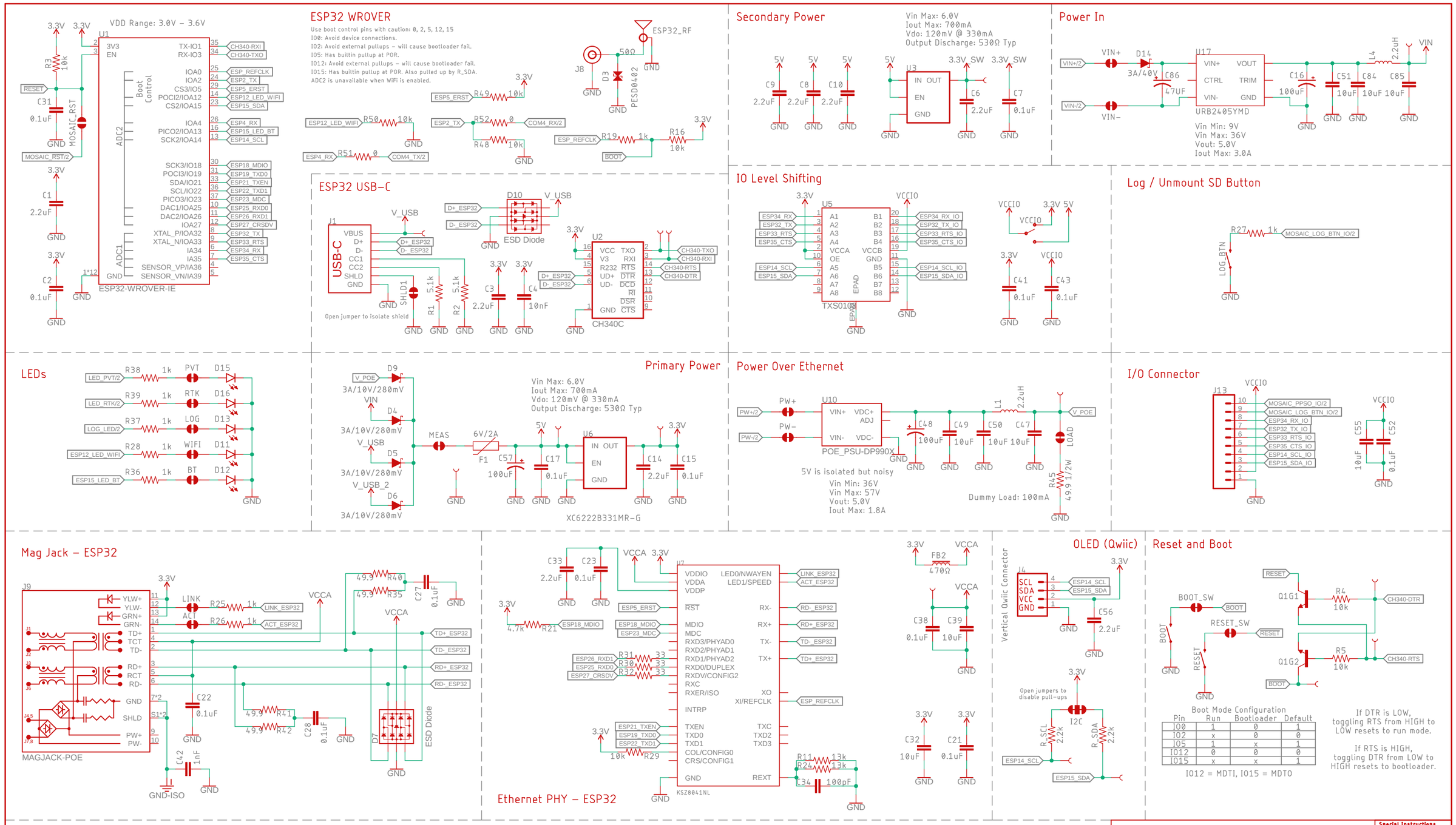
ESP32 WROVER
Use boot control pins with caution: 0, 2, 5, 12, 15
IO0: Avoid device connections.
IO2: Avoid external pullups – will cause bootloader fail.
IO5: Has builtin pullup at POR.
IO12: Avoid external pullups – will cause bootloader fail.
IO15: Has builtin pullup at POR. Also pulled up by R_SDA.
ADC2 is unavailable when WiFi is enabled.
VDD Range: 3.0V – 3.6V
ESP32-WROVER-IE
Secondary Power
Vin Max: 6.0V
Iout Max: 700mA
Vdo: 120mV @ 330mA
Output Discharge: 530Ω Typ
Power In
URB2405YMD
Vin Min: 9V
Vin Max: 36V
Vout: 5.0V
Iout Max: 3.0A
ESP32 USB-C
ESD Diode
CH340C
IO Level Shifting
TXS0108E
Log / Unmount SD Button
LEDs
Primary Power
Vin Max: 6.0V
Iout Max: 700mA
Vdo: 120mV @ 330mA
Output Discharge: 530Ω Typ
XC6222B331MR-G
Power Over Ethernet
POE_PSU-DP990X
5V is isolated but noisy
Vin Min: 36V
Vin Max: 57V
Vout: 5.0V
Iout Max: 1.8A
Dummy Load: 100mA
I/O Connector
Mag Jack – ESP32
MAGJACK-POE
Ethernet PHY – ESP32
KSZ8041NL
OLED (Qwiic)
Vertical Qwiic Connector
Reset and Boot
Boot Mode Configuration
Pin Run Bootloader Default
IO0 1 0 1
IO2 x 0 0
IO5 1 x 1
IO12 0 0 0
IO15 x x 1
IO12 = MDTI, IO15 = MDTO
If DTR is LOW, toggling RTS from HIGH to LOW resets to run mode.
If RTS is HIGH, toggling DTR from LOW to HIGH resets to bootloader.
Open jumpers to disable pull-ups
Open jumper to isolate shield
USB Track Impedance: Differential Pair
https://saturnpcb.com/saturn-pcb-toolkit/
Prepreg thickness: 0.2mm (7.87 mil). Er = 4.6
10.5 mil track with 9.5 mil gap (20 mil center to center) = 90 Ohms
RF Track Impedance: Coplanar Waveguide with Ground Calculations
Ground is on layer 2. Prepreg thickness: 0.2mm. Er = 4.6
12.5 mil track with 5 mil gap = 50 Ohms
https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm
open hardware
sparkfun
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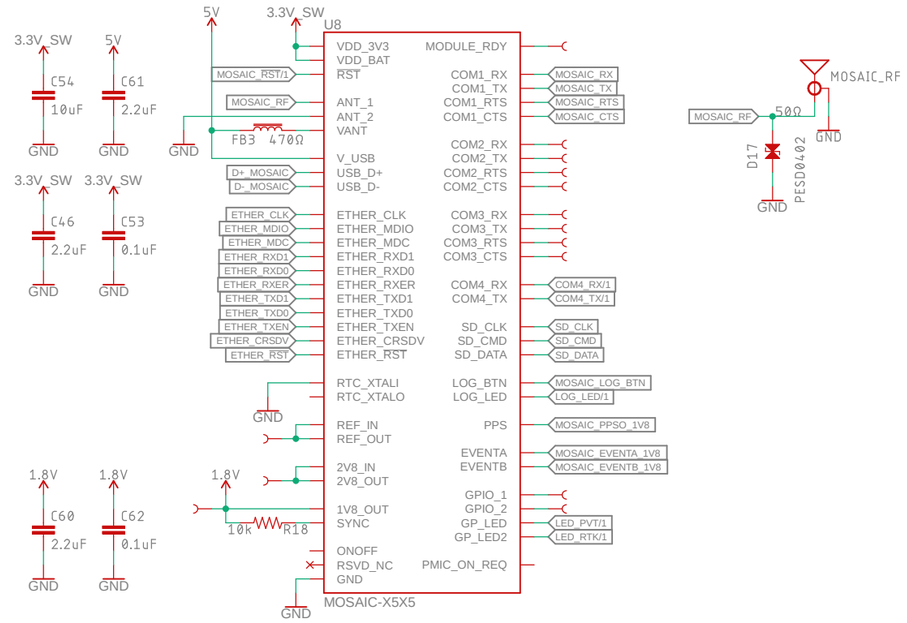
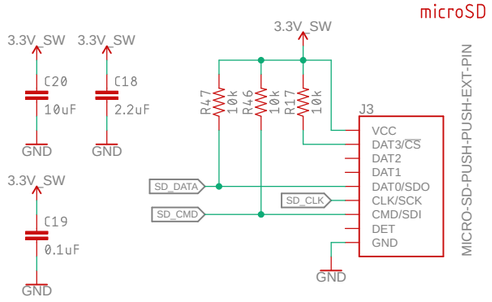
https://creativecommons.org/licenses/by-sa/4.0/
Special Instructions
No clean process
TITLE: RTK_Mosaic_X5
Design by: Paul Clark
REV: v01
Date: 19/07/2023 16:53
Sheet: 1/2

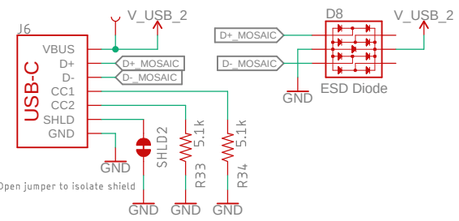
Mosaic X5



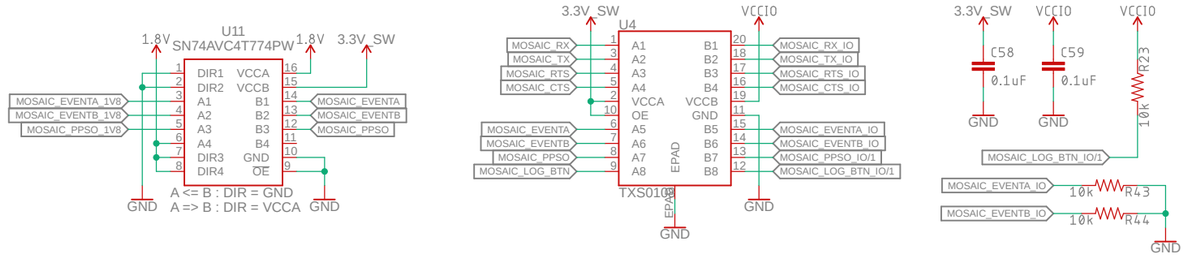
microSD



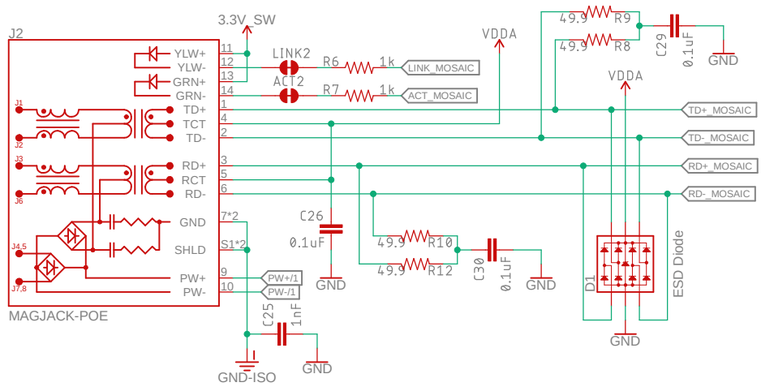
Mosaic USB-C



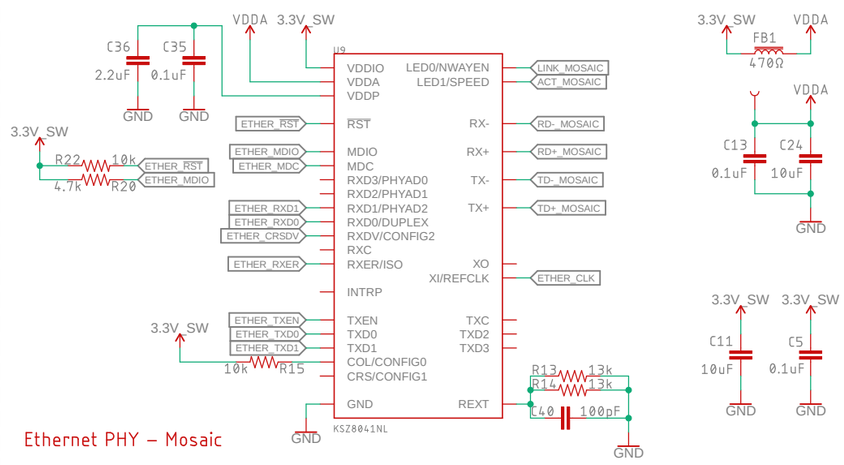
IO Level Shifting



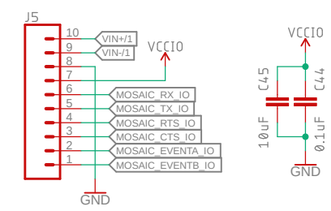
Mag Jack – Mosaic



Ethernet PHY – Mosaic



I/O Connector



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TITLE: RTK_Mosaic_X5

Design by: Paul Clark

REV: V01

Date: 19/07/2023 16:53

Sheet: 2/2