

I n d e x

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EXPERIMENT NO. 1

AIM :- Measurement of the following using Cathode Ray Oscilloscope (CRO) :-

- (a) DC voltage
- (b) Peak and RMS value of AC voltage
- (c) Time period and frequency of Periodic Signals.

INSTRUMENTS :-

- (1) CRO
- (2) Function generator
- (3) Power Supply

THEORY :-

A cathode Ray Oscilloscope (CRO) is a device used to visualize and analyze electrical signals by converting them into graphical waveforms. It operates using a cathode ray tube (CRT), which produces a focused beam of electrons directed into a phosphorescent screen. The beam's vertical movement is controlled by the input electrical signal, representing the signal's voltage, while its horizontal movement is managed by a timebase generator, which creates a uniform sweep across the screen to represent time. This allows the CRO to display the waveform of the signal, providing insights into its amplitude, frequency, and phase. Key components of a CRO include the CRT, vertical and horizontal deflection systems, amplifiers and a power supply. Users can adjust controls like time and voltage

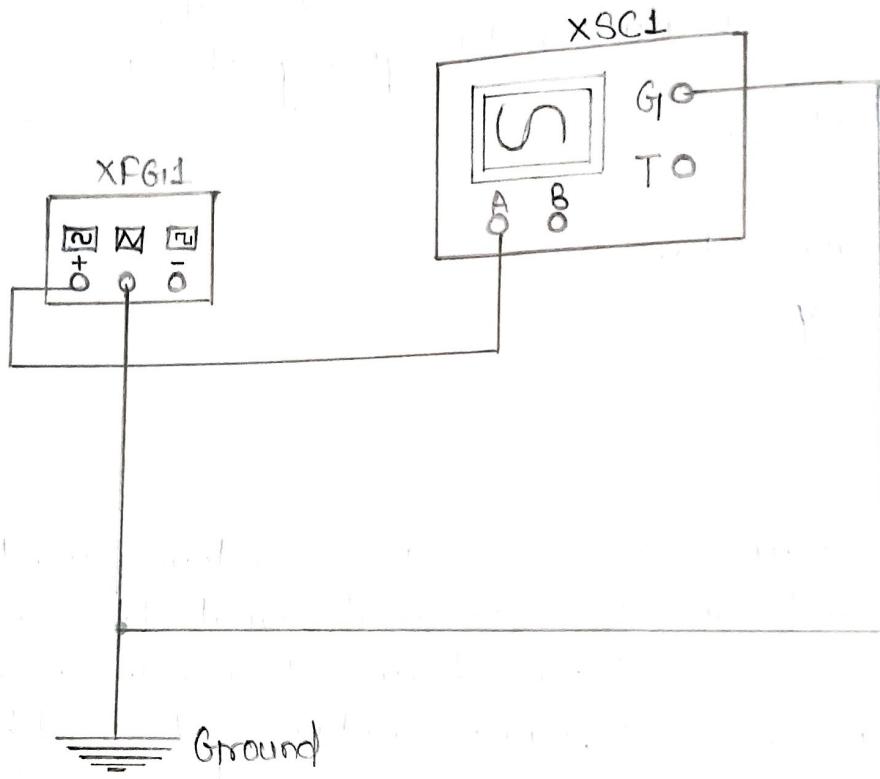


FIG: CIRCUIT FOR STUDY OF CRO

scales to analyze the signal more effectively. CROs are widely used in electronics and engineering to test circuits, measure signal characteristics, and troubleshoot faults. Despite their versatility, CROs are increasingly replaced by modern digital storage Oscilloscopes (DSOs), which offer enhanced features like digital signal processing, waveform storage, and probability. However, the CRO remains a foundational tool for understanding the behavior of electrical systems.

PROCEDURE :-

for DC voltage measurement :-

- (1) Connect the CRO probes to the output of function generator.
- (2) Keep frequency of the function generator at zero and amplitude to any value.
- (3) Get the DC voltage by CRO.

for AC voltage measurement :-

- (1) Connect the CRO probes to the output of function generator.
- (2) Observe the peak values (V_p) of the wave currently selected.
- (3) Observation should be calculated the RMS value of the ac signal by the given formula $V_{rms} = (V_p / \sqrt{2})$.
- (4) Observe the Time-period (T) of the wave selected.
- (5) Calculate the frequency by $f = 1/T$.
- (6) Change the both voltage and time period scale and repeat the step 2 to step 5 for three different readings.
- (7) Take another waveform (sinel/square/triangular) and repeat step 2 to step 6.

OBSERVATIONS:-

for DC voltage :

(1) From function generator Input frequency = 50 Hz

(2) From CRO :

Scales on volts/div. (volts) = 1

No. of divisions for voltage = 1

DC voltage (v) = 2

For Sine wave measurements :

(1) From function generator :

Input voltage : 2 volts, Input frequency : 50 Hz

(2) From CRO :

	Scale on No. volts/div	Scale on Time/div	No. of div. for Peak voltage	No. of div. for Time period	V _p (v _p)	V _{rms} ($\frac{V_p}{\sqrt{2}}$)	T (ms)	f (Hz)
1.	2	5	2/2 = 1	4	1	$\frac{1}{\sqrt{2}}$	20	50
2.	2	5	2/2 = 1	2	1	$\frac{1}{\sqrt{2}}$	10	100
3.	2	5	2/2 = 1	1.3	1	$\frac{1}{\sqrt{2}}$	6.5	153

For Square wave measurements:

(1) From function generator:

Input voltage: 2 volts, Input frequency: 50 Hz

(2) From CRO:

Sn.	Scale No. of volts/div (v)	Scale on Time/div (ms)	No. of div. for Peak voltage (Vp)	No. of div. for Time period (T)	V_{rms} $(V_{rms} = \frac{V_p}{\sqrt{2}})$	T (ms)	Frequency (Hz)
1.	2	5	$2/2 = 1$	4	1	1	50
2.	2	5	$2 \cdot 2/2 = 1 \cdot 1$	2	1.1	1.1	100
3.	2	5	$2 \cdot 4/2 = 2 \cdot 2$	1.82	1.2	1.2	151

For Triangular Wave Measurements:

(1) From function generator:

Input voltage: 2 volts, Input frequency: 50 Hz

(2) From CRO:

Sn.	Scale No. of volts/div (v)	Scale on Time/div (ms)	No. of div. for Peak voltage (Vp)	No. of div. for Time period (T)	V_{rms} $(V_{rms} = \frac{V_p}{\sqrt{3}})$	T (ms)	Frequency (Hz)	
1.	2	5	$2 \cdot 2/2 = 1 \cdot 1$	4	1.1	$1 \cdot 1/\sqrt{3}$	20	50
2.	2	5	$2 \cdot 2/2 = 1 \cdot 1$	2	1.1	$1 \cdot 1/\sqrt{3}$	10	100
3.	2	5	$2 \cdot 2/2 = 1 \cdot 1$	1.32	1.1	$1 \cdot 1/\sqrt{3}$	6.6	151

RESULT :-

This experiment involves measuring DC voltage, peak and RMS values of AC voltage, and time period and frequency of periodic signals (sine, square and triangular waves) using a cathode Ray Oscilloscope (CRO), function generator, and power supply. The expected results include accurate reading of set voltages, verification of ohm's law, and confirmation of waveform characteristics. Measurements reveal that increasing voltage causes electrons to flow faster, increasing current flow. The CRO displays a flat horizontal line for DC voltage and waveform patterns for AC signals. Time period and frequency measurements verify the relationship $T = \frac{1}{f}$. Observations confirm theoretical concepts, such as $V_p = f \times V_{rms}$ for sine waves and duty cycle for square waves.

EXPERIMENT NO. 2

AIM :- Measurement of unknown frequency using Lissajous pattern.

APPARATUS REQUIRED :- (a) Hardware

(1) CRO

(2) Function Generator

(3) Power Supply

(b) Software

(1) Multisim

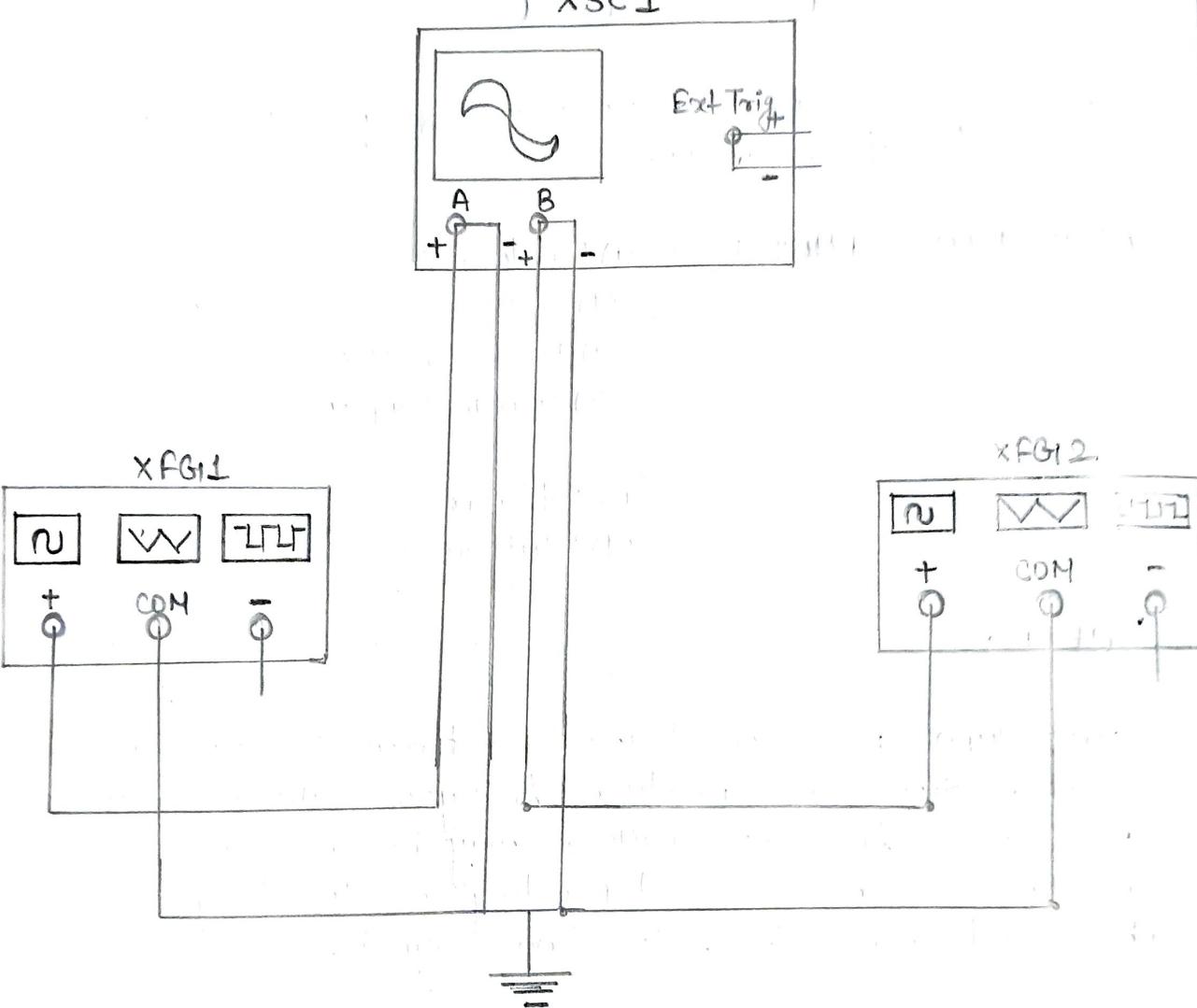
THEORY

Two super-position of the two harmonic functions such as sine wave produce Lissajous Pattern on the CRO screen. Lissajous pattern may be a straight line, an ellipse or a circle depending on the frequency, phase and amplitude of the two signals.

A straight line results when the two waves are in phase or exactly 180° out of phase with each other.

A circle is displayed when the phase difference is 90° and the signals are equal in amplitude.

If f_v corresponds the frequency of vertical deflection voltage and f_h corresponding to the horizontal deflection voltage then,



Circuit diagram for the measurement of unknown frequencies using Lissajous pattern

(1)

(2)

(3)

(4)

(5)

(6)

$$\frac{f_y}{f_x} = \frac{\text{No. of horizontal tangencies (HT)}}{\text{No. of vertical tangencies (VT)}}$$

Where,

Horizontal Tangency (HT): It is the no. of times a fictitious straight line taken at any one horizontal side of the Lissajous Pattern (Up/Down) serves as a tangent to the Lissajous pattern.

Vertical Tangency (VT): It is the no. of times a fictitious straight line taken at any one vertical side of the Lissajous Pattern (Up/Down) serves as a tangent to the Lissajous pattern.

Hence, f_y can be found if f_x is known.

PROCEDURE (HARDWARE) :-

- (1) An oscillator of unknown frequency is connected to the vertical plate of the CRO, and standard oscillator of known frequency is connected to the horizontal plate.
- (2) Adjust the voltage of the two oscillators to give a pattern of suitable size.
- (3) Vary slightly the frequency of the test oscillator until a simple Lissajous pattern is obtained. Read known frequency f_x .
- (4) Find HT + VT from Lissajous Pattern.
- (5) Calculate f_y by the given formula.
- (6) Repeat the steps 3 and step 4 and take three different readings.

PROCEDURE (SOFTWARE) :-

- (1) Double click on the multisim software.
- (2) Select and drag the instruments and components for the required arrangement and make the necessary connections.
- (3) Run the program.
- (4) Adjust the scales on the CRO front panel and take the readings.
- (5) Any change of the signal parameters can be done by stop the run button and double click on the function generator and on the component properties.

OBSERVATION (HARDWARE) :-

Sr. No.	f_x (Hz)	Horizontal Tangency (HT)	Vertical Tangency (VT)	$f_y = \frac{HT}{VT} f_x$ (Hz)
(1)	200	1	2	$\frac{1}{2} \times 200 = 100 \text{ Hz}$
(2)	250	2	5	$\frac{2}{5} \times 250 = 100 \text{ Hz}$
(3)	200	3	4	$\frac{3}{4} \times 200 = 150 \text{ Hz}$

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OBSER

Sr.

No.

1.

2.

3.

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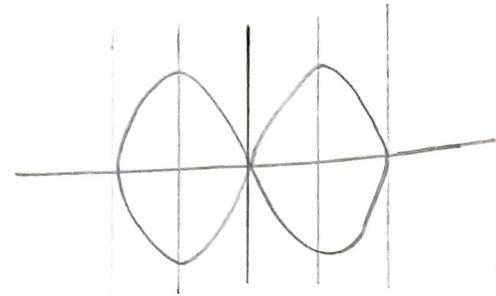
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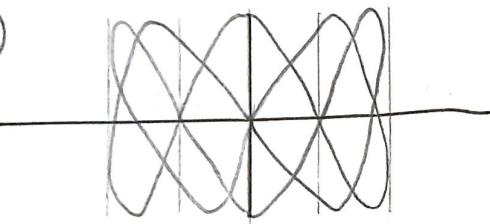
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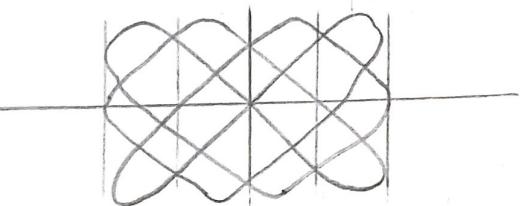


Figure ① ② ③ are Lissajous pattern

OBSERVATION (SOFTWARE) :-

Sr. No.	f_x (Hz)	Horizontal Tangency (HT)	Vertical Tangency (VT)	$f_y = \frac{HT}{VT} f_x$ (Hz)
1.	100	6	4	$\frac{6}{4} \times 100 = 150$
2.	100	4	2	$\frac{4}{2} \times 100 = 200$
3.	100	3	1	$\frac{3}{1} \times 100 = 300$

RESULT :-

The experiment to measure an unknown frequency using Lissajous patterns involves comparing the unknown frequency with a known reference frequency by displaying both signals on an oscilloscope. By analyzing the closed-loop pattern and counting the lobes in the horizontal and vertical directions, the frequency ratio can be determined. Using this ratio, and the reference frequency, the unknown frequency is calculated accurately.

EXPERIMENT NO. 3

AIM :- Realisation of Basic logic gates (AND, OR, NOT) using NAND Gate (IC7400).

INSTRUMENTS REQUIRED :- (1) Bread Board/Trainer kit
(2) D.C. Power Supply

CIRCUIT COMPONENTS :- (1) IC7400
(2) Connecting Wires

THEORY :-

The NAND Gate is said to be a universal gate because any all other gates as well as any digital system can be implemented with it. Combinational circuits and sequential circuits as well can be constructed with this gate because the flip-flop circuit can form two NAND gates connected back to back.

The NAND (Not-AND) gate has an output that is normally at logic level '1' and only goes "LOW" to logic level "0" when all of its inputs are at logic level '1'. The logic NAND Gate is the reverse or "complementary" form of the AND Gate. The logic or Boolean expression for a given logic gate NAND is that for logical addition, which is the opposite to the AND Gate, and which it performs on the complements of the inputs. The Boolean expression for a logic NAND Gate is denoted by a single dot or full

stop symbol (.) , with a line or overline(—) over the expression to signify the not or logical negation of the NAND gate giving us the Boolean expression of $A \cdot B = Q$.

Then we can define the operation of a two-input digital logic NAND gate as bring.

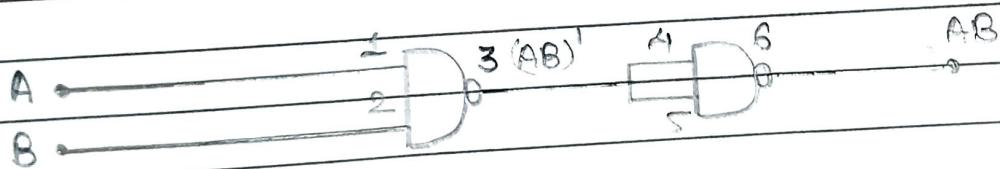
"If either A or B are NOT true, then Q is true".

Logic NAND gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape is that of a standard AND Gate, with a circle, sometimes called an "inversion" bubble at its output to represent the NOT gate symbol with the logical operation of the NAND gates given.

The implementation of the AND, OR, and NOT operations with NAND gates is shown. The NOT operation is obtained from a one-input NAND Gate. The AND operation requires two NAND Gates. The first produces the inverted AND and the second acts as an inverter to produce the normal output. The OR operation is achieved through a NAND gate with additional inverters in each input.

PROCEDURE :-

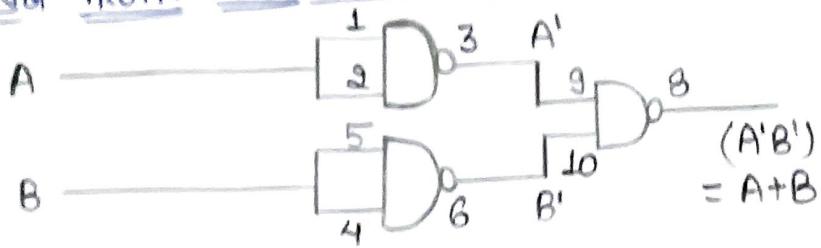
- (1) Connect the circuit as shown in the circuit diagram.
- (2) Before switching on power supply, make sure that the connection are correct.
- (3) Apply the input logic state code mentioned in observation Table in terms of +5 volts for state -1 and 0 volts for stable-0.
- (4) Observe the output states.
- (5) Verify the result of the truthness.
- (6) Repeat steps 3 to 5 for all possible combination.

OBSERVATIONS:-(1) VERIFYING TRUTH TABLE OF AND GATE

INPUT	OUTPUT	
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

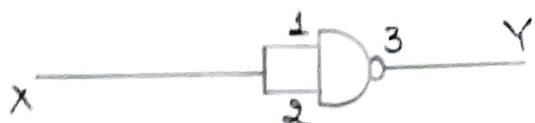
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2. VERIFYING TRUTH TABLE OF OR GATE



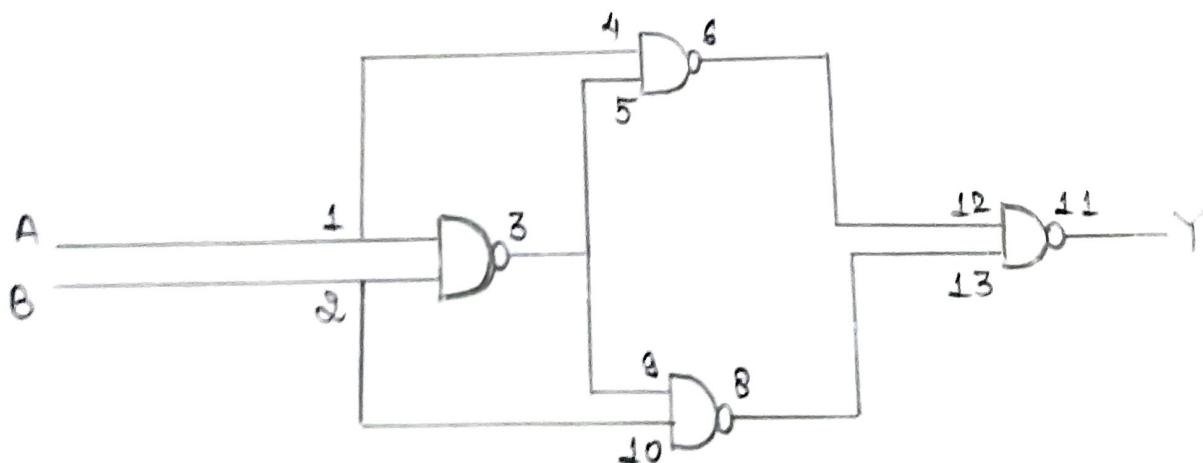
INPUT	OUTPUT	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. VERIFYING TRUTH TABLE OF NOT GATE



INPUT	OUTPUT
X	Y
0	1
1	0

4. VERIFYING TRUTH TABLE OF XOR GATE



INPUT	OUTPUT	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

RESULT:-

(1) AND → It gives output as 1 when both the inputs are 1 else gives 0 as result.

(2) OR → It gives output as 1 when either or both inputs are 1 else gives 0.

(3) NOT → It gives 0 as output when input is 1 and gives 1 as output when input is 0.

(4) XOR → It gives 1 as output when both the inputs are dissimilar else gives 0 if both the inputs are similar.



EXPERIMENT NO. 4

AIM :- Implementation of the Boolean Expression

$F = (A \cdot B \cdot C + D \cdot F)$ using AND Gates (IC 7408) and OR Gate (IC 7432).

INSTRUMENTS REQUIRED :- (1) Bread Board / Trainer kit
 (2) D.C. Power Supply

CIRCUIT COMPONENTS :- (1) IC 7408

(2) IC 7432

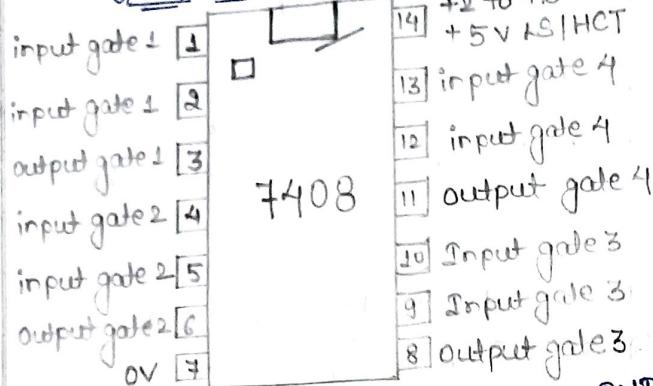
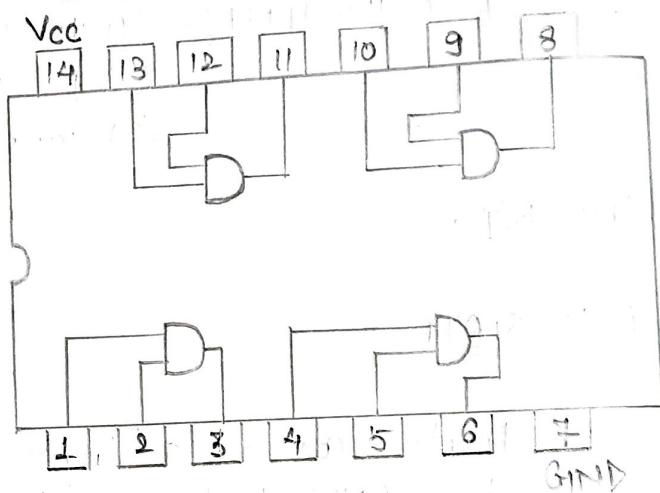
(3) Connecting wires

THEORY :-

AND GATE

The output state of a "Logic AND Gate" only returns "Low" again when ANY of its inputs are at a logic level "0". In other words for a large AND gate, any low input will give a low output.

The logic or Boolean expression given for a digital logic AND gate is that for a logical Multiplication which is denoted by a single dot or full stop symbol (.) giving us the Boolean Expression of $A \cdot B = Q$.

PIN DIAGRAM OF IC 7408QUAD 2 INPUTS AND GATEThen
ANDINTERNAL GATE CONNECTION OF IC 7408The 2-input Logic AND Gate

Symbol	Truth Table
A •	B A Q
B •	0 0 0
	0 1 0
	1 0 0
	1 1 1
2-input AND Gate	
Boolean Expression $Q = A \cdot B$	Read as A and B gives Q

Logic
prod
sym
of +OR
Th
ag
wiT
C
b
A

Then we can define the operation of a 2-input logic AND gate as being:

"If both A and B are true, then Q is true."

Logic AND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the AND gate.

OR Gate

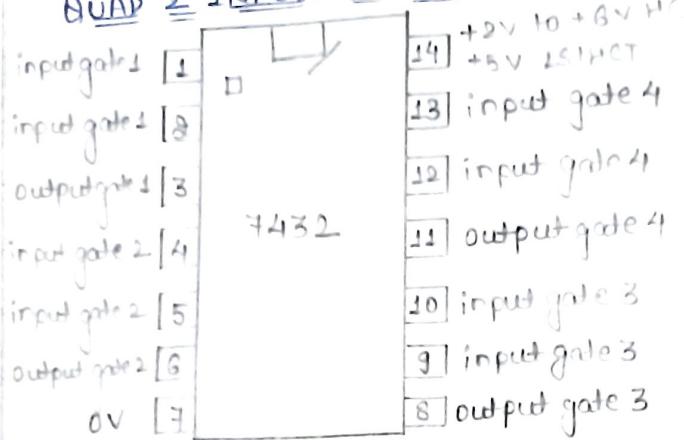
The output, Q of a "Logic OR Gate" only returns "Low" again when all of its inputs are at a logic level "0". In other words for a logic OR gate, any "HIGH" input will give a "HIGH", logic level "1" output.

The logic or Boolean expression given for a digital logic OR gate is that for logical Addition which is denoted by a plus sign, (+) given us the Boolean expression of $A + B = Q$.

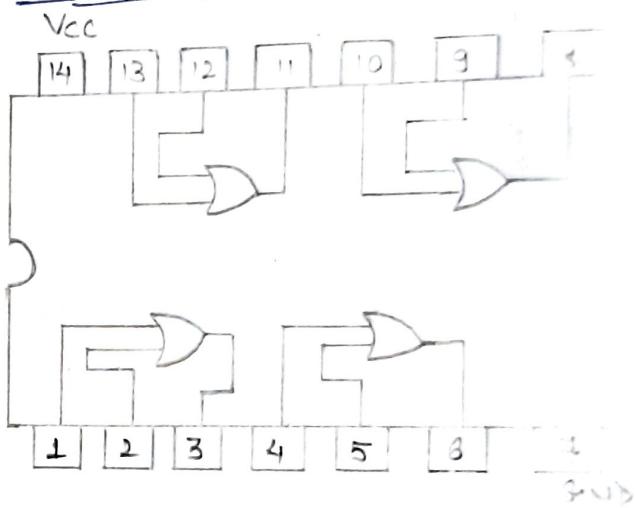
Thus a logic OR gate can be correctly described as an "Inclusive OR Gate" because the output is true when both of its inputs are true (HIGH).

PIN DIAGRAM OF IC 7432

QUAD 2 INPUTS OR GATE



INTERNAL GATE CONNECTION OF IC 7432



The 2-input Logic OR Gate

Symbol	Truth Table
	$B \quad A \quad Q$
	0 0 0
	0 1 1
	1 0 1
	1 1 1
2-input OR Gate	
Boolean Expression $Q = A + B$	Read as A or B gives Q

Then we can define the operation of a 2-input logic OR gate as being:

"If either A or B is true, then Q is true."

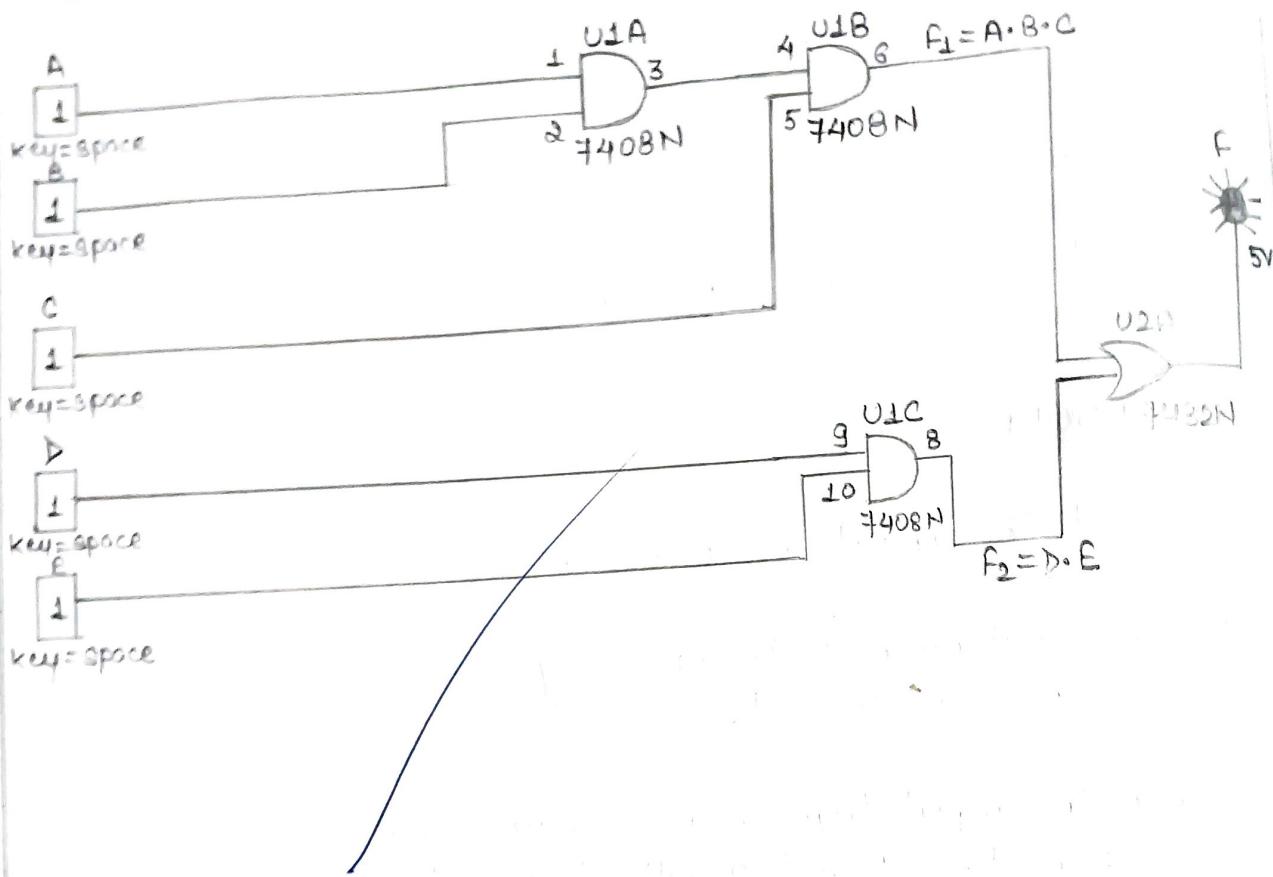
Logic OR Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the OR Gate.

PROCEDURE:-

- (1) Connect the circuit as shown in the circuit diagram.
- (2) Before switching ON Power Supply, make sure that the connections are correct.
- (3) Apply the input logic as per Truth Table in terms of +5 volts for state-1 and 0 volts for state-0.
- (4) Observe the output states.
- (5) Verify the result of truthness.
- (6) Repeat steps from 3 to 5 for all possible combinations.

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FUNC

EXPERIMENTAL SETUP

(1)

(2)

OBSERVATIONS:-FUNCTION TABLE

INPUTS					INTERMEDIATE FUNCTIONS		FINAL OUTPUT	
A	B	C	D	E	$f_1 = A \cdot B \cdot C$	$f_2 = D \cdot E$	$F = A \cdot B \cdot C + D \cdot E$	
1	1	1	0	0	1	0	1	
1	0	1	1	1	0	1	1	
0	0	1	1	1	0	1	1	
1	0	0	1	0	0	0	0	
0	0	0	1	1	0	1	1	
0	0	0	1	0	0	0	0	
0	1	1	1	1	0	1	1	
0	0	0	0	1	0	0	0	
1	1	0	1	0	0	0	0	
1	1	1	1	1	1	1	1	

RESULT:-

- (1) The experiment validates the concept of Boolean algebra by practically realizing the logic of Boolean expressions using logic gates (AND and OR).
- (2) The use of AND and OR gates in combination allows us to construct any Boolean expression. AND gates produce the intersection of conditions, while OR gates capture the union.

EXPERIMENT NO. 5

AIM :- To determine the forward and reverse bias characteristics of PN Junction diode.

INSTRUMENTS REQUIRED :- (1) Power Supply }
(2) Ammeter }
(3) Voltmeter }
(4) Multisim → Software → Hardware

CIRCUIT COMPONENTS :- (1) Diode
(2) Resistance
(3) Connecting wires and breadboard.

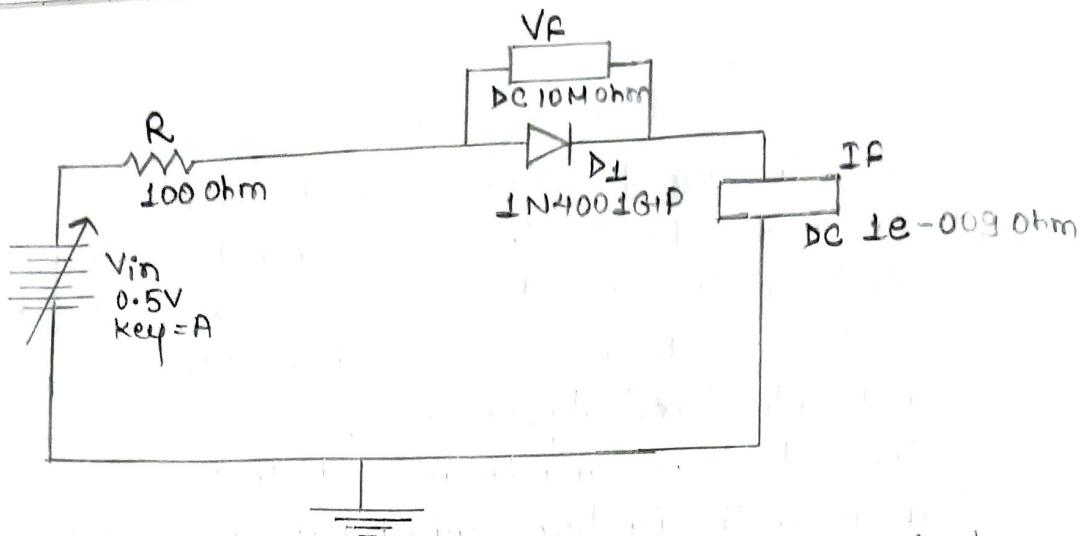
THEORY :-

In a piece of semiconductor material, if one half is doped by P-type impurity and the other half is doped by N-type impurity, a PN Junction is formed. The plane dividing the two halves or zones is called PN Junction. The N-type material has high concentration of free electrons while P-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over the P-side and hold the holes on the N-side. This process is called diffusion. As the free electrons move across the junction from N-type to P-type, the donor ions become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons

that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on the P-side of the junction. This net negative charge on the P-side prevents further diffusion of electron in to the P-side. Similarly, the net positive charge on the N-side repels the holes crossing from P-side to N-side. Thus, a barrier is set up near the junction which prevents further movement of charge carriers. As the consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between P and N region, which is called the potential barrier, junction barrier, diffusion potential, or contact potential, V_0 . The magnitude of the contact potential V_0 varies with doping levels and temperature. V_0 is 0.3V for germanium and 0.72V for silicon.

FORWARD BIAS

When positive terminal of the battery is connected to the P-type and negative terminal to the N-type of the PN diode, the bias is known as forward bias. Under the forward bias condition, the applied positive potential repels the holes in P-type region so that the holes move towards the junction and the applied negative potential repels the electron in the N-type region and the electron move towards the junction. Eventually, when the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear. A feature

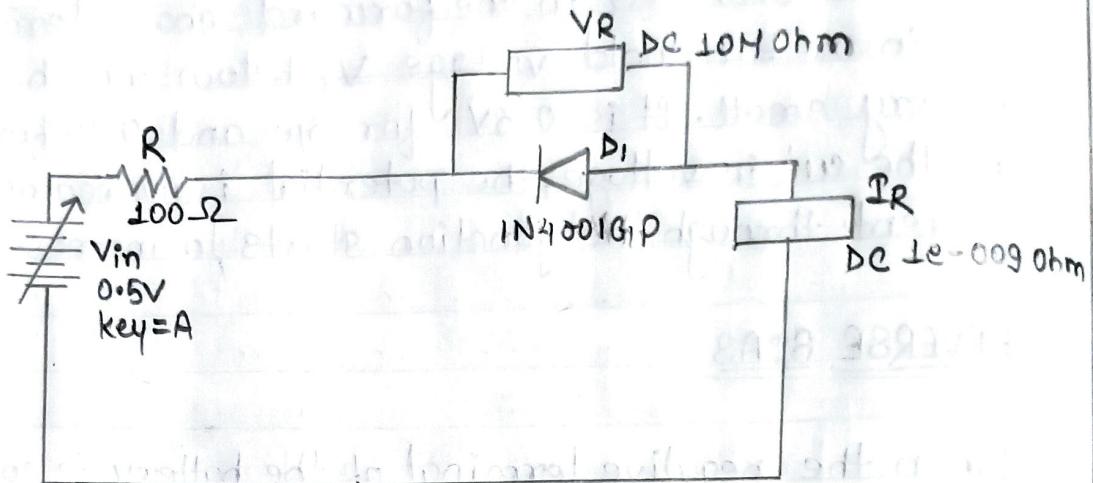


Circuit Diagram for forward Bias PN Diode

worth to be noted in the forward characteristics is the cut in or threshold voltage V_T , below which the current is very small. It is 0.3V for Ge and 0.7V for Si respectively. At the cut in voltage, the potential is overcome and the current through the junction starts to increase rapidly.

REVERSE BIAS

When the negative terminal of the battery is connected to the P-type and positive terminal of the battery is connected to the N-type of the PN junction, the bias applied is known as reverse bias. Under applied reverse bias, holes which form the majority carriers on the P-side moves towards the negative terminal of the battery and electron which form the majority carrier of the N-side are attracted towards the positive terminal of the battery. Hence, the width of the depletion region which is depleted of the mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both the directions. Therefore, theoretically no current should flow in the external circuit. But in practice, a very small current of the order of a few microamperes flows under reverse bias. Electron forming covalent bonds of the semiconductor atoms in the P and N-type regions may absorb sufficient energy from heat and light to cause



Circuit Diagram for Reverse Bias PN Diode

breaking of some covalent bonds. Hence, electron-hole pairs are continually produced in both the regions. Under the reverse bias condition, the thermally generated holes in the P-region are attracted towards the negative terminal of the battery and the electrons in the N-region are attracted towards the positive terminal of the battery. Consequently, the minority carriers, electrons on the P-region and holes in the N-region, wander over to the junction and flow towards their majority carrier side giving rise to a small reverse current. This current is known as reverse saturation current, I_0 . The magnitude of reverse current depends upon the junction temperature because the major source of minority carriers is thermally broken covalent bonds. For large applied reverse bias, the free electrons from the N-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electrons from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called as an avalanche of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as breakdown voltage, V_{BD} .

PN DIODE APPLICATIONS

An ideal PN diode is a two terminal polarity sensitive device that has zero resistance when it is forward biased and infinite resistance when it is reverse biased. Due to this characteristic the diode finds number of applications as given below.

- (1.) Rectifier
- (2.) Switch
- (3.) Clamper
- (4.) Clipper
- (5.) Demodulation detector circuits.

PROCEDURE

- (1) Connect the circuit as shown.
- (2) Bring the variable voltage of the DC source to zero. The current through milliammeter should also be zero.
- (3) Increase the variable voltage of the DC source slowly and in steps. Corresponding to each setting, note down the voltmeter and milliammeter readings.
- (4) Do not exceed the current beyond the current rating of the diode. This completes the observation of V-I characteristics of the forward biased diode.
- (5) Plot current (I_F) voltage (V_F) by choosing proper scales.
- (6) Make the connections as shown in.
- (7) Repeat the steps 2 and 3. This completes observation for V-I characteristics of reverse biased diode.
- (8) Plot current (I_R) and voltage (V_R) by choosing proper scales.

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OBSERVATIONSFORWARD BIAS (SOFTWARE)

Sr. No.	INPUT VOLTAGE (V)	V_f (V)	I_f (mA)
(1.)	0.5	0.341	0.159
(2.)	1	0.422	0.578
(3.)	1.5	0.459	1.041
(4.)	2	0.482	2.001
(5.)	2.5	0.499	2.487
(6.)	3	0.513	2.976
(7.)	3.5	0.524	3.406
(8.)	4	0.534	3.958
(9.)	4.5	0.542	4.451
(10.)	5	0.549	4.944
(11.)	5.5	0.556	5.438
(12.)	6	0.562	5.933
(13.)	6.5	0.567	6.428
(14.)	7	0.572	6.923
(15.)	7.5	0.577	7.419
(16.)	8	0.581	7.915
(17.)	8.5	0.585	8.411
(18.)	9	0.589	8.907
(19.)	9.5	0.593	9.404
(20.)	10	0.596	

OBS

RE

OBSERVATIONSREVERSE BIAS (SOFTWARE)

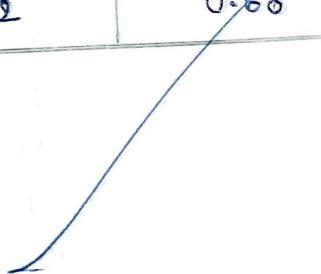
Sr. No.	INPUT VOLTAGE (v)	V_r (v)	I_r (mA)
1.	0.5	0.499	0.72
2.	1	0.999	0.77
3.	1.5	1.499	0.82
4.	2	1.999	0.87
5.	2.5	2.499	0.92
6.	3	2.999	0.97
7.	3.5	3.499	1.02
8.	4	3.999	1.07
9.	4.5	4.499	1.12
10.	5	4.999	1.17
11.	5.5	5.499	1.22
12.	6	5.999	1.27
13.	6.5	6.499	1.32
14.	7	6.999	1.37
15.	7.5	7.499	1.42
16.	8	7.999	1.47
17.	8.5	8.498	1.52
18.	9	8.998	1.57
19.	9.5	9.498	1.62
20.	10	9.998	1.64

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OBSERVATIONS

FORWARD BIAS (HARDWARE)

S. No.	INPUT VOLTAGE (V)	V_f (V)	I_f (mA)
1.	0.93	0.53	0.4
2.	1.68	0.57	1.1
3.	2.20	0.59	1.64
4.	3.03	0.61	2.46
5.	3.21	0.61	2.70
6.	4.14	0.63	3.62
7.	5.21	0.64	4.68
8.	6.22	0.65	5.70
9.	8.80	0.67	8.33
10.	9.92	0.68	9.46



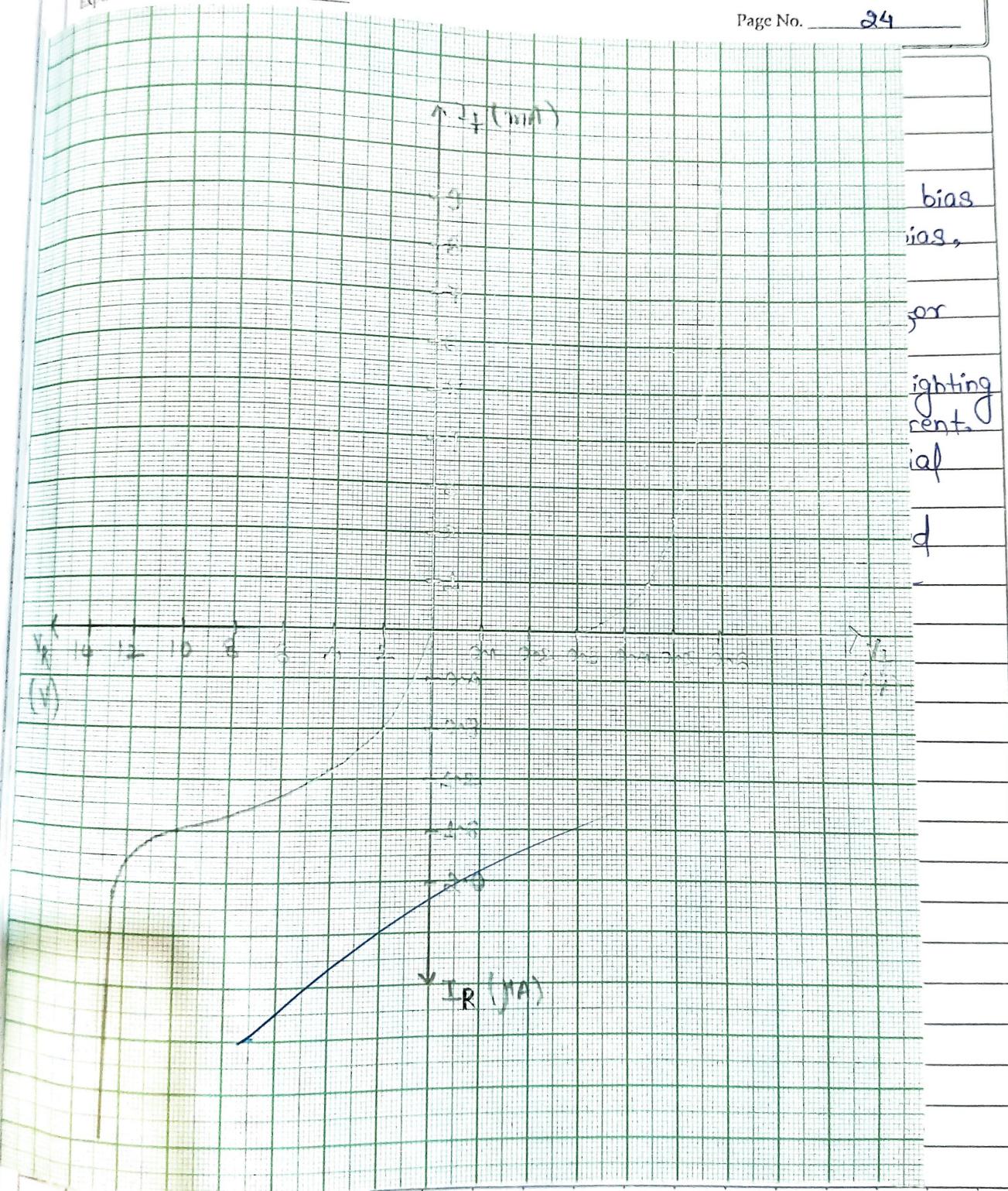
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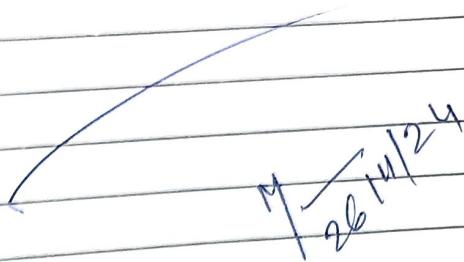


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RESULT

The experiment to determine the forward and reverse bias characteristics of a PN junction diode. Under forward bias, the diode allowed significant current flow once the applied voltage exceeded the threshold (typically $\sim 0.7\text{V}$, for silicon diodes), confirming its low resistance state.

In reverse bias, negligible current was observed, highlighting its high resistance state, except for a small leakage current. The $V-I$ characteristics were plotted, showing an exponential rise in current for forward bias and nearly constant current for reverse bias until breakdown. This verified the diode's unidirectional conduction and suitability for rectifying circuits.



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EXPERIMENT NO. 6

AIM :- Measurement of rectification efficiency and ripple factor of Half wave rectifier circuit with and without C-filter.

APPARATUS REQUIRED :-

(1.) Power Supply

(2.) CRO

(3.) Multimeter

(4.) Half Wave Rectifier Circuit

(5.) Circuit Board

CIRCUIT COMPONENTS :-

(1.) Capacitor $C = 500\mu F$

(2.) Resistor $R_L = 1K\Omega$

THEORY :-

Because of their ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert ac voltage into dc voltage. Rectifiers are found in all dc power supplies that operate from an ac voltage source. A power supply is an essential part of each electronic system from the simplest to the most complex.

The half-wave rectifier converts Ac to pulsating DC using a diode, allowing current flow only during the positive half-cycle.

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HALF-WAVE RECTIFIER :-

During positive half-cycle of the input voltage, the diode D_1 is in forward bias and conducts through the load resistor R_L . Hence, the current produces an output voltage across the load resistor R_L , which has the same shape as the +ve half cycle of the input voltage.

During the negative half cycle of the input voltage, the diode is reverse biased and there is no current through the circuit i.e., the voltage across R_L is zero. The net result is only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified output voltage is the value measured on dc-voltmeter.

RIPLE FACTOR

The output of a rectifier consists of a d.c. component and an a.c. component (also known as ripple). The a.c. component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output; the smaller this component, the more effective is the rectifier.

The ratio of r.m.s value of a.c. component to the d.c. component in the rectifier output is known as ripple factor.

Ripple factor (r) is defined as :

$$r = \frac{\text{rms value of the ac component}}{\text{d.c. value of the rectifier curve}} = \frac{I_{ac, \text{rms}}}{I_{dc}}$$

Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

RECTIFICATION EFFICIENCY

The ratio of d.c. power output to the applied input a.c. power is known as Rectification Efficiency.

Rectification Efficiency or Ratio of Rectification (η) is defined as :

$$\eta = \frac{\text{d.c. power delivered to load}}{\text{a.c. input power from the Transformer}} = \frac{P_{dc}}{P_{ac}}$$

PROCEDURE

- (1.) Connect a multimeter in series and a CRO in shunt across the load.
- (2.) Connect the circuit as a Half wave rectifier without filter (k_1 and k_2 are open) and with C-filter (k_1 is open and k_2 is short). Tabulate readings of $I_{ac, \text{rms}}$ and I_{dc} without filter and with C-filter.
- (3.) Calculate ripple factor (r), rectification efficiency (η) without filter and with C-filter.
- (4.) Observe waveforms on CRO.

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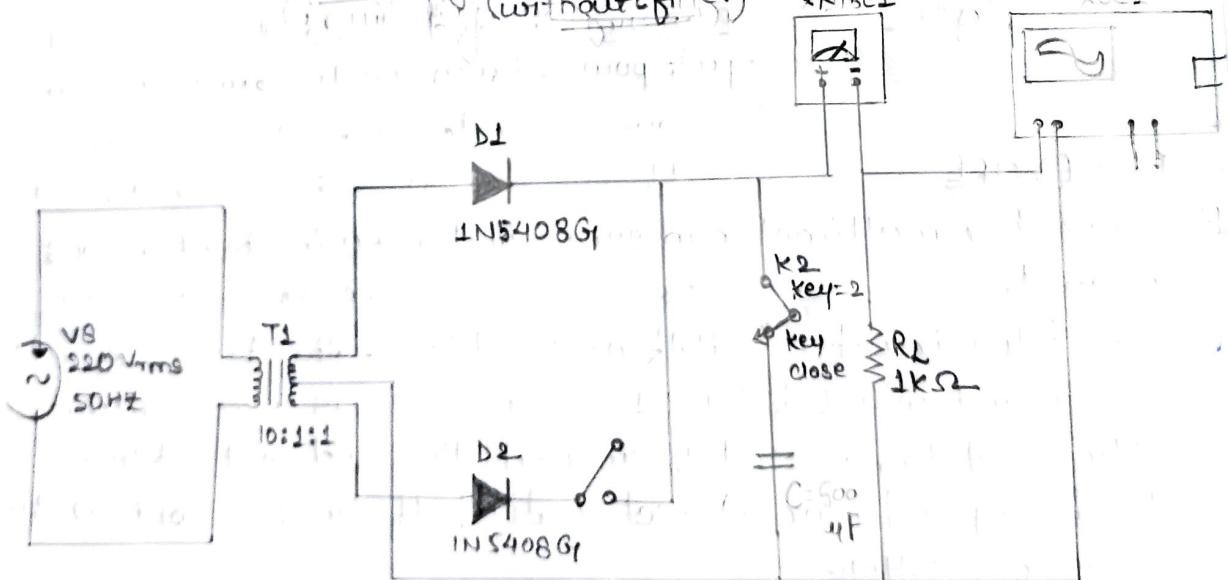
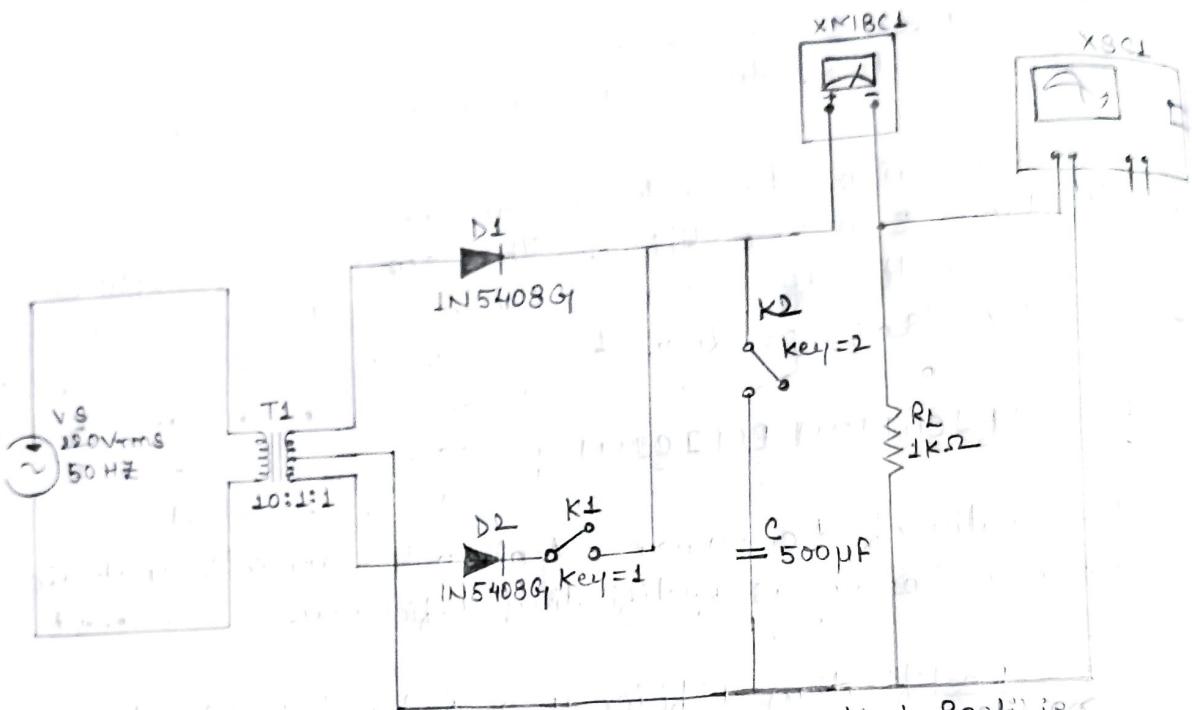
OBSERVATIONTYPES
RECTIFIERS

- i) HALF
RECTIFIERS
FILTER
- ii) HALF
RECTIFIERS
FILTER

Circuit

i) For

ii)



Circuit diagram of Half-wave diode Rectifier (with C filter)

OBSERVATIONS :-

TYPES OF RECTIFICATION	I_{AC}	I_{DC}	I_{rms}	Ripple factor (r)	Rectification efficiency (η)
i) HALF WAVE RECTIFIER (WITHOUT FILTER)	12.57	10.23	16.206	1.228	40%
ii) HALF WAVE RECTIFIER (WITH FILTER)	13.02	10.52	16.738	1.226	40%

CALCULATION :-

i) For $I_{AC} = 12.57$ and $I_{DC} = 10.23$ (WITHOUT FILTER)

$$I_{rms} = \sqrt{(I_{AC,rms}^2 + I_{DC}^2)} = \sqrt{(12.57)^2 + (10.23)^2} = 16.206$$

$$\text{Ripple factor (r)} = \frac{I_{AC,rms}}{I_{DC}} = \frac{12.57}{10.23} = 1.228$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \left(\frac{I_{DC}}{I_{rms}} \right)^2 = \left(\frac{10.23}{16.206} \right)^2 \approx 0.40 \approx 40\%.$$

ii) For $I_{AC} = 13.02$, and $I_{DC} = 10.52$ (WITH FILTER)

$$I_{rms} = \sqrt{(I_{AC,rms}^2 + I_{DC}^2)} = \sqrt{(13.02)^2 + (10.52)^2} = 16.738$$

$$\text{Ripple factor (r)} = \frac{I_{AC,rms}}{I_{DC}} = \frac{13.02}{10.52} = 1.226$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \left(\frac{I_{DC}}{I_{rms}} \right)^2 = \left(\frac{10.52}{16.738} \right)^2 \approx 0.40 \approx 40\%.$$

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EXPERIMENT NO. 7

AIM :- Measurement of rectification efficiency and ripple factor of full-wave rectifier circuit with and without C-filter.

APPARATUS REQUIRED :-

- (1) Power Supply
- (2) CRO
- (3) Multimeter
- (4) Full wave Rectifier Circuit
- (5) Circuit Board

CIRCUIT COMPONENTS :-

- (1) Capacitor $C = 500 \mu F$

(2) Resistor $R_L = 1 k\Omega$

THEORY :-

Because of their ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert ac voltage into dc voltage. Rectifiers are found in all dc power supplies that operate from an ac voltage source. A power supply is an essential part of each electrode system from the simplest to the most complex.

The full-wave rectifier converts AC to DC using diodes, producing a continuous output voltage by rectifying both half cycles of AC.

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FULL WAVE RECTIFIER :-

The circuit of a center-tapped full wave rectifier uses two diodes D_1 & D_2 . During the positive half cycle of secondary voltage (input voltage), the diode D_1 is forward biased and D_2 is reverse biased. The diode D_1 conducts and current flows through load resistor R_L . During negative half cycle, diode D_2 becomes forward biased, and D_1 reverse biased. Now, D_2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L , during both the half cycles and will get unidirectional current flow.

RIPPLE FACTOR

The output of a rectifier consists of a d.c. component and an a.c. component (also known as ripple). The a.c. component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output, the smaller this component, the more effective is the rectifier.

The ratio of rms value of a.c. component to the d.c. component in the rectifier output is known as ripple factor.

$$\eta = \frac{\text{rms value of ac component}}{\text{d.c. value of rectifier wave}} = \frac{I_{ac,\text{rms}}}{I_{dc}}$$

Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

RECTIFICATION EFFICIENCY

The ratio of d.c. power output to the applied input a.c. power is known as Rectification Efficiency.

$$\eta = \frac{\text{d.c. power delivered to load}}{\text{a.c. input power from the transformer}} = \frac{P_{dc}}{P_{ac}}$$

PROCEDURE

- (1) Connect a multimeter in series and a CRO in shunt across the load.
- (2) Connect the circuit as a full-wave Rectifier without filter (K_1 is short and K_2 is open) and with C-filter (K_1 and K_2 are short). Tabulate readings of I_{ac} and I_{dc} without filter and with C-filter.
- (3) Calculate ripple factor (η), rectification efficiency (η) without filter and with C-filter. Compare these measured values with their respective theoretical values.
- (4) Observe waveforms on CRO.

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OBSERVATION

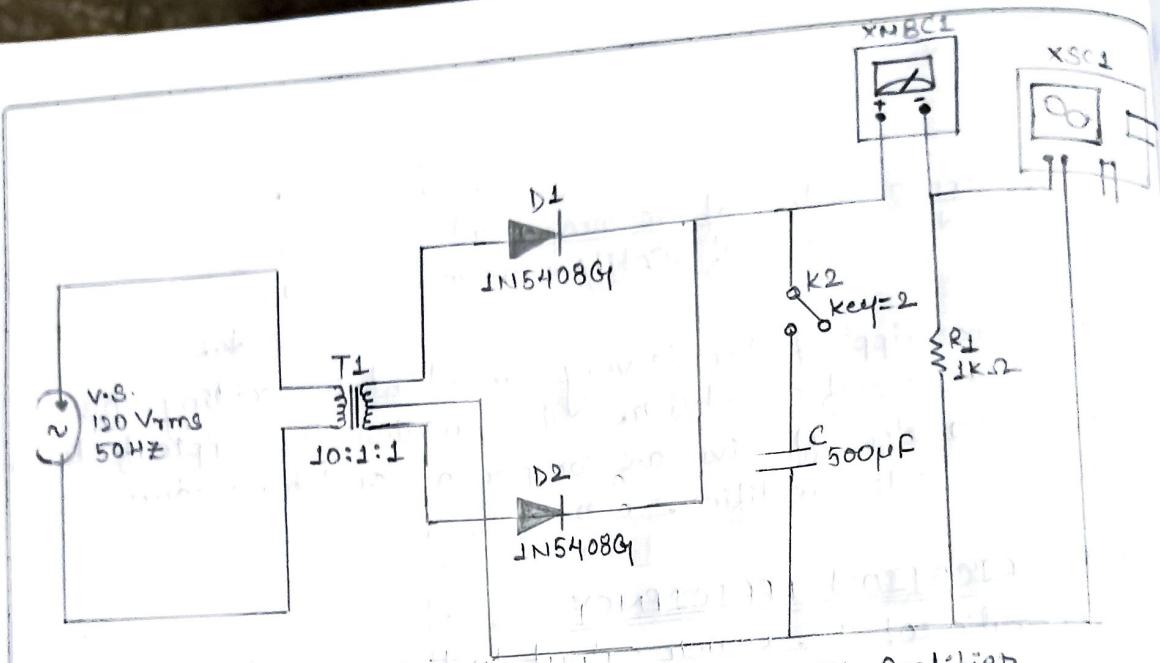
TYPE OF

- FULL-WAVE DIODE RECTIFIER FILTER
- FULL-WAVE DIODE FILTER

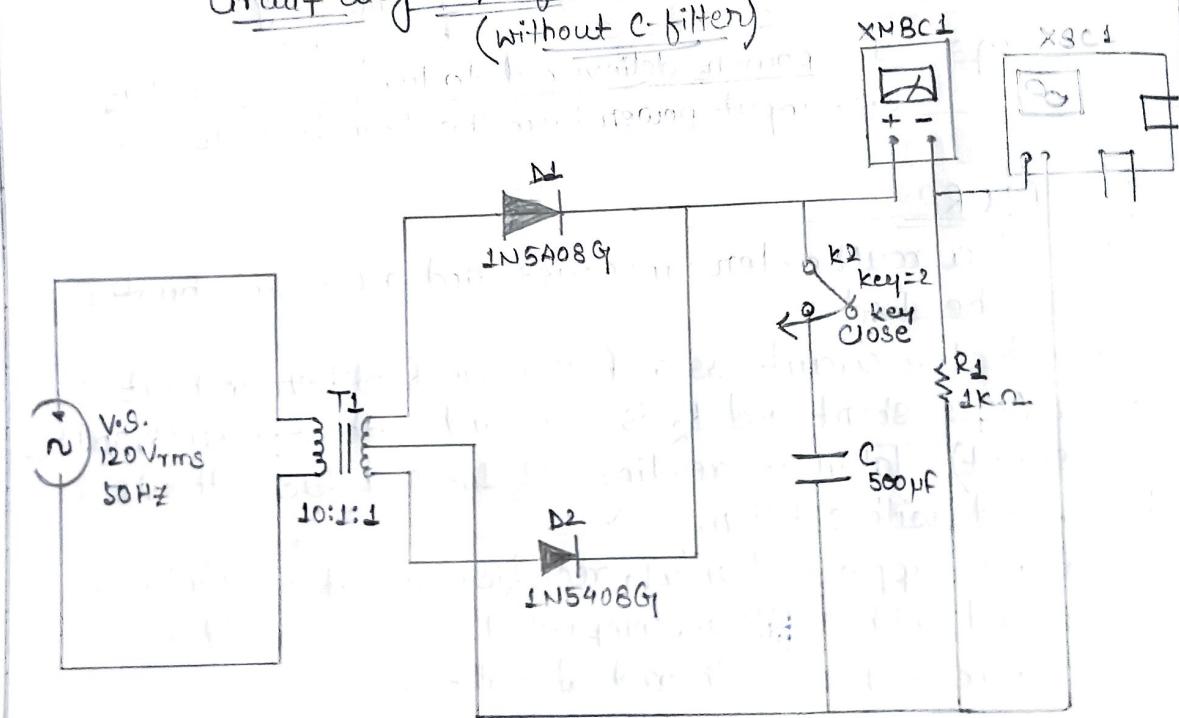
CALC.

(i) For

(ii) For



Circuit diagram of full-wave diode Rectifier
(without C-filter)



Circuit diagram of full-wave diode Rectifier
(with C-filter)

OBSERVATIONS :-

TYPES OF RECTIFICATION	I_{AC}	I_{DC}	I_{rms}	Ripple factor (r)	Rectification Efficiency (%)
i) FULL-WAVE RECTIFIER (WITHOUT FILTER)	5.06	10.32	11.493	0.490	80%
ii) FULL-WAVE RECTIFIER (WITH FILTER)	5.08	10.41	11.583	0.487	80%

CALCULATIONS :-(i) For $I_{AC} = 5.06$ and $I_{DC} = 10.32$ (WITHOUT FILTER)

$$I_{rms} = \sqrt{I_{AC,rms}^2 + I_{DC}^2} = \sqrt{(5.06)^2 + (10.32)^2} = 11.493$$

$$\text{Ripple factor } (r) = \frac{I_{AC,rms}}{I_{DC}} = \frac{5.06}{10.32} = 0.490$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \left(\frac{I_{DC}}{I_{rms}} \right)^2 = \left(\frac{10.32}{11.493} \right)^2 \approx 0.80 = 80\%.$$

(ii) For $I_{AC} = 5.08$ and $I_{DC} = 10.41$ (WITH FILTER)

$$I_{rms} = \sqrt{I_{AC,rms}^2 + I_{DC}^2} = \sqrt{(5.08)^2 + (10.41)^2} = 11.583$$

$$\text{Ripple factor } (r) = \frac{I_{AC,rms}}{I_{DC}} = \frac{5.08}{10.41} = 0.487$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \left(\frac{I_{DC}}{I_{rms}} \right)^2 = \left(\frac{10.41}{11.583} \right)^2 \approx 0.80 = 80\%.$$

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RESULT:-

The experiment showed higher rectification efficiency and reduced ripple factor in a full-wave rectifier with a C-filter, compared to without, confirming improved DC output smoothness and overall performance.

EXPERIMENT NO. 8

AIM:- To determine the reverse bias characteristics of zener diode and application as a voltage regulator.

APPARATUS REQUIRED:- (1) Power Supply
(2) DC voltmeter
(3) DC Ammeter

CIRCUIT COMPONENTS:- (1) Resistor 470Ω, 1.5K, 2.2K, 3.3K,
5.6K, 12K
(2) Zener EC 3Z 12A 1Z12

THEORY:-

Zener Diode: A zener diode is a silicon pn-junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of zener diode is set by carefully controlling the doping level during manufacture. When a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically and this is the key to zener diode operation.

Zener Breakdown:- Zener diodes are designed to operate in reverse breakdown. Two types of reverse breakdown in a zener diode are avalanche and zener. The avalanche effect, occurs in both rectifiers and zener diodes at a sufficiently high reverse voltage. Zener breakdown

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occurs in both rectifiers and zener diodes at a low reverse voltages. A zener diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (V_Z), the field is intense enough to pull electrons from their valence bands and create current. Zener diodes with breakdown voltages of less than approximately 5V operate predominantly in zener breakdown. Those with breakdown voltages greater than approximately 5V operate predominantly in avalanche breakdown. Both types, however, are called zener diodes. Zeners are commercially available with breakdown voltages from less than 1V to more than 250V with specified tolerances from $\pm 1\%$ to $\pm 20\%$.

Zener Regulation: from the reverse portion of a zener diode's characteristics curve we notice that as the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current I_Z . At this point, the breakdown effect begins, the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the zener breakdown voltage (V_Z) remains essentially constant although it increases slightly as the zener current I_Z increases.

Zener regulation is the ability to keep the reverse voltage across its terminals essentially constant is the key feature of the zener diode. A zener diode operating in breakdown acts a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse current values. A minimum value of reverse current I_{ZK} , must be maintained in order to keep the diode in breakdown for voltage regulation. When the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also there is a maximum current I_{ZM} above which the diode may be damaged due to excessive power dissipation. So, basically the zener diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from I_{ZK} to I_{ZM} . A nominal zener voltage, V_Z is usually specified on a datasheet at a value of reverse current called the zener test current.

To prevent high current from flowing into the zener (for it may be damaged) a series resistor is included. After breakdown the voltage across the zener remains constant even if the input voltage across varies or the load current changes.

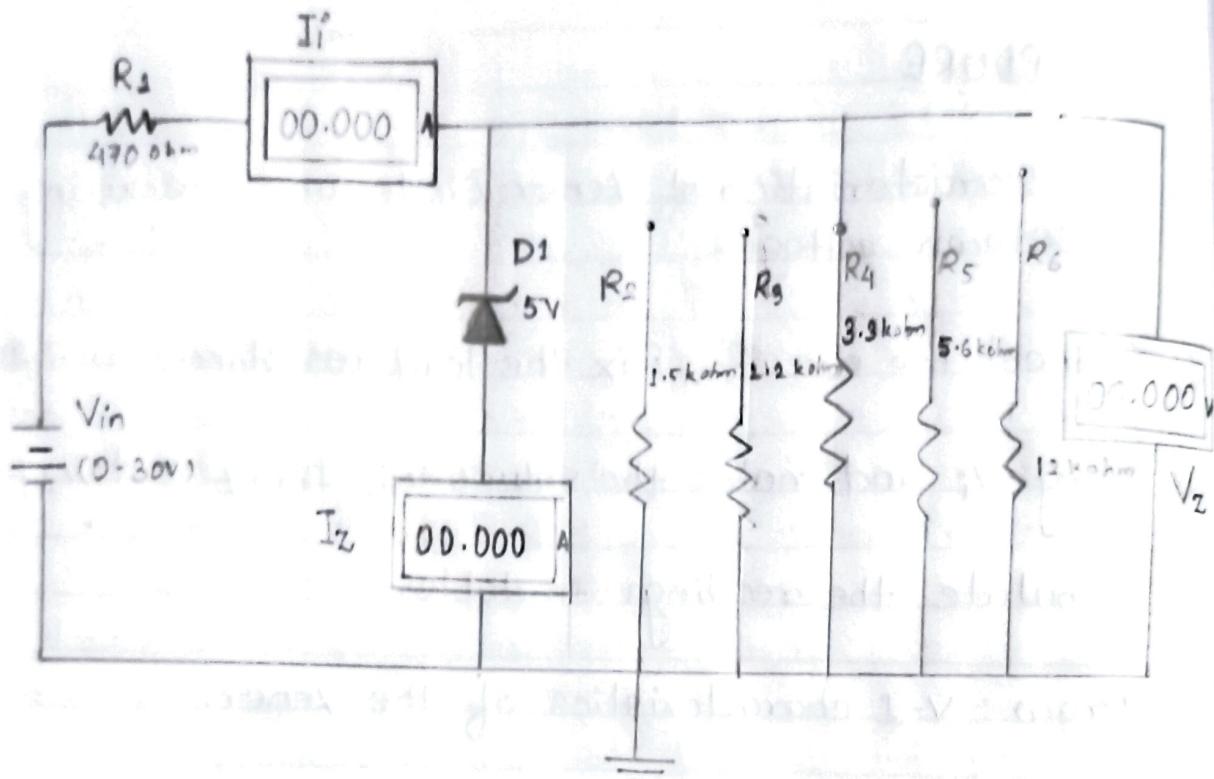
PROCEDURE

A: for Characteristic of Zener Diode and measuring the Breakdown voltage:

- (1.) Connect the circuit. Fix the load resistance to $2.2\text{k}\Omega$
- (2.) Vary V_i and notes the values of I_i, I_Z and V_Z/V_{DC} .
- (3.) Tabulate the readings in table.
- (4.) Draw $V-I$ characteristics of the zener.
- (5.) Find out the Breakdown voltage (V_Z) of the zener diode.

B: for study voltage regulation characteristics of zener diode:

- (1.) keep $V_{in} > V_Z$ (fixed)
- (2.) Vary load (By connecting different load resistances) and measure I_i, I_Z and V_Z/V_{DC}
- (3.) Tabulate the readings in table.
- (4.) Plot the variation in V_Z against R_L .



Circuit diagram to find Zener diode characteristics

OBSERVATIONS

A S.No.	VOLTS (V)	I_i (mA)	I_Z (mA)	V_Z (V)
1.	0.65	0.29	0	0.492
2.	0.942	0.42	0	0.709
3.	1.238	0.55	0	0.932
4.	1.519	0.67	0	1.140
5.	2.115	0.915	0	1.593
6.	2.704	1.08	0	2.037
7.	3.442	1.491	0	2.591
8.	4.42	1.91	0	3.343
9.	5.50	2.387	0	4.13
10.	6.66	3.02	0	5.01
11.	7.36	3.33	0	5.53
12.	8.68	3.98	0	6.49
13.	10.01	4.58	0	7.48
14.	11.83	5.47	0	8.85
15.	12.61	5.83	0	9.42
16.	13.24	6.10	0	9.88
17.	14.02	6.49	0	10.47
18.	14.41	6.53	0	10.77
19.	15.24	7.10	0	11.39
20.	16.09	7.51	0	12.02
21.	16.25	7.64	0.21	12.03

B.

$$V_{\text{input}} = 16.49 \text{ V}$$

S. No.	R_L (k Ω)	I_i (mA)	I_Z (mA)	V_Z (V)
1.	1.5	8.08	0	12.32
2.	2.2	7.99	3.24	12.06
3.	3.2	7.95	5.19	12.11
4.	5.6	7.85	6.01	12.13
5.	12	7.91	5.65	15.77

Expt

V_Z

RESULT