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RESEARCH ARTICLE

Lianzhen HUANG, Jiangang LI, Dongjun ZHANG

Frequency-controlable sine signal based on PWM and its implementation on FPGA

Abstract A sine generation method that the different frequent sine signals can be generated by the different Pulse-Width Modulation (PWM) signals generated by Field-Programmable Gate Array (FPGA) through low-pass filter of fixed parameters was proposed. The method just takes a few FPGA resources and was proved feasible by the theory. The experiment results and theory analysis tally.

Keywords Pulse-Width Modulation (PWM), Field-Programmable Gate Array (FPGA), frequency controllable

1 Introduction

Many methods to generate sine signal have been proposed so far. All of them have different characteristics. The common methods are introduced in the chapter of "Sine Signal Generation Techniques" of National Semiconductor Application Note [1]. The sine generated by Analog method can obtain good performance, but it is difficult to realize the controllability by pure analog circuit. Direct Digital Frequency Synthesis (DDS) is a kind of digital method to realize sine signal. Generally, a serial of phase shift control value are stored in RAM/ROM by DDS. According to the phase shift control value, the controller output a serial of corresponding digital signal. These signal that pass through some analog components can be changed to the expected analog sine. The main analog components are DA and analog filters [2] usually. However, one shortage of these methods is that it needs high frequency conversion of DA chip. The other shortage is that it does not benefit overall system cost. Some methods [3] eliminated the DA component, which are also base on DDS method. The controller output Pulse-Width Modulation (PWM) signal. When the PWM signal pass through the designed analog filters, the expected sine signal is obtained. Then the sine signal can be converted to many kind of signals by passing some simple module. And the amplitude is so.

In many sine signal applications, the system only need the frequency is controlled, and amplitude is constant. Such as the application of position demodulation of resolver. The system expects for 1 to 20 kHz sine signal as exciting signal for different applications. However the amplitude of those sine signal must be constant [4]. Aiming at this kind of applications, this thesis puts forward a method based on PWM, which can realize frequency controllable and amplitude constant. This method need not DA chip and amplitude-control module, which can reduce the cost. The Field-Programmable Gate Array (FPGA) controller can output multichannel timing strict PWM signal [5]. To duce the resource of FPGA, a method base on the symmetry of sine signal is used. This theory and experiment thesis prove the feasibility and correctness of this thesis.

2 PWM spectrum analysis

PWM is a coding method that coding the analog signal to digital signal. Any analog signals can be realize by PWM as long as enough bandwidth in theory. PWM need carrier signal to modulate the signal. Triangle signal is usually used as carrier signal. Figure 1 is the diagram that modulate sine signal by triangle signal. And the corresponding PWM signal is here. The modulation with triangle signal can suppress the odd harmonic components better, but triangle signal need to switch between add and subtract continuously which is more complex to realize and takes more resource.

Therefore, the sawtooth signal is proposed as carrier signal to modulation in this thesis. The add operation is

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Lianzhen HUANG, Jiangang LI (✉), Dongjun ZHANG
Shenzhen Graduate School, Harbin Institute of Technology, Shenzhen 518055, China
E-mail: Jiangang_lee@163.com

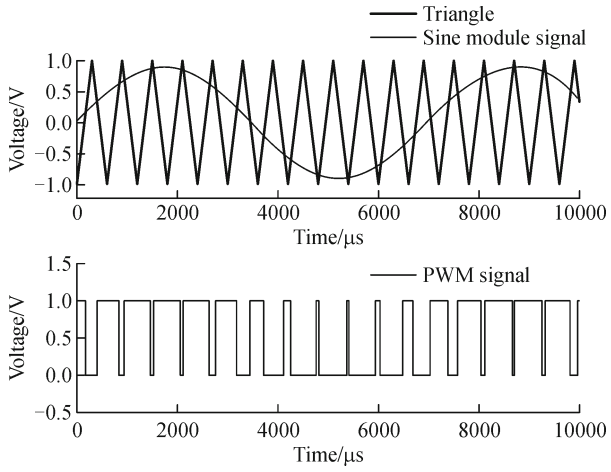

Fig. 1 Triangle signal carrier

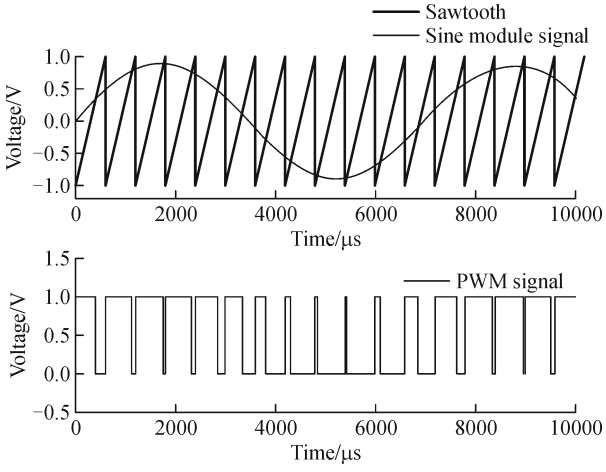

Fig. 2 Sawtooth signal carrier

required only, That is very easy to implement in FPGA. Figure 2 is the modulation with sawtooth signal as carrier signal.

After the modulation of sine signal, the corresponding PWM is obtained. Now we need to analyse the PWM. As the PWM signal is periodic signal, Fourier Series [6] method is used to analyse the PWM signal.

Supposed the PWM signal is $f(t)$, its period is T. Then let the controller clock cycle is T_{clk}, and sawtooth carrier signal period is T_{c}. Let

$$T_{\text{c}} = MT_{\text{clk}}, \tag{1}$$

$$T = NT_{\text{c}} = NMT_{\text{clk}}, \tag{2}$$

where, M and N are both positive integer.

Equation (1) means one sawtooth period takes M clock cycles. So the M determines the resolution of sawtooth signal. Equation (2) means the ratio of carrier signal frequency and sine signal frequency.

$$f(t) = \sum_{n=0}^{\infty}\sum_{i=0}^{N-1}\Bigg(H(nT + MT_{\text{clk}}i) - H\Bigg(MT_{\text{clk}}i + T_{\text{clk}}R\Bigg(\frac{M}{2}\Bigg(\sin\frac{2\pi i}{N} + 1\Bigg)\Bigg)\Bigg)\Bigg). \tag{3}$$

$H(t)$ is unit step function, as

$$H(t) = \begin{cases} 1, & t \geqslant 0, \\ 0, & t < 0, \end{cases} \tag{4}$$

and $R(x)$ is INTPART function of real X. Let

$$S_i = \frac{1}{2}\Bigg(\sin\frac{2\pi i}{N} + 1\Bigg), \tag{5}$$

$$\Delta_i = R(MS_i). \tag{6}$$

As $f(t)$ is periodic signal, so the first cycle signal just is analyzed here.

$$f(t) = \sum_{i=0}^{N-1}\Big(H(MT_{\text{clk}}i) - H(MT_{\text{clk}}i + T_{\text{clk}}\Delta_i)\Big). \tag{7}$$

By Fourier series,

$$f(t) = \sum_{-\infty}^{+\infty} C_n \mathrm{e}^{\mathrm{j}n\omega_0 t}, \tag{8}$$

where

$$C_n = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\mathrm{e}^{-\mathrm{j}n\omega_0 t}\mathrm{d}t. \tag{9}$$

Then, the discrete spectrum of $f(t)$ is obtained.

$$A(\omega) = 2\|C_n\|. \tag{10}$$

By Eqs. (3) and (9),

$$\begin{aligned} C_n &= \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\mathrm{e}^{-\mathrm{j}n\omega_0 t}\mathrm{d}t \\ &= \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}}\sum_{i=0}^{N-1}(H(MT_{\text{clk}}i) - H(MT_{\text{clk}}i + T_{\text{clk}}\Delta_i))\mathrm{e}^{-\mathrm{j}n\omega_0 t}\mathrm{d}t \\ &= \frac{1}{T}\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}\frac{-1}{\mathrm{j}n\omega_0}\Big(\mathrm{e}^{-\mathrm{j}n\omega_0(MT_{\text{clk}}i + T_{\text{clk}}\Delta_i)} - \mathrm{e}^{-\mathrm{j}n\omega_0(MT_{\text{clk}}i)}\Big), \end{aligned} \tag{11}$$

where

$$\omega_0 = \frac{2\pi}{T}, \tag{12}$$

$$T = NMT_{\text{clk}}. \tag{13}$$

By Euler's Formula

$$\mathrm{e}^{-\mathrm{j}a} = \cos a - \mathrm{j}\sin a. \tag{14}$$

Then

$$\begin{aligned} C_n &= \frac{1}{T}\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}\frac{1}{n\omega_0}\left(\left(\sin\frac{2\pi n(Mi+\Delta_i)}{NM} - \sin\frac{2\pi nMi}{NM}\right)\right. \\ &\quad \left. + \mathrm{j}\left(\cos\frac{2\pi n(Mi+\Delta_i)}{NM} - \cos\frac{2\pi nMi}{NM}\right)\right) \\ &= \frac{1}{2n\pi}\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}\left(\left(\sin\frac{2\pi n(Mi+\Delta_i)}{NM} - \sin\frac{2\pi nMi}{NM}\right)\right. \\ &\quad \left. + \mathrm{j}\left(\cos\frac{2\pi n(Mi+\Delta_i)}{NM} - \cos\frac{2\pi nMi}{NM}\right)\right). \end{aligned} \tag{15}$$

Let n take 0 to 1000. The function $A(n\omega_0)$ is the discrete spectrum of $f(t)$. And the fundamental frequency of PWM signal is the expected sine signal. To calculate each harmonic attenuation relativing fundamental signal by $p(n)$.

$$p(n) = 20\lg\frac{f(\omega_n)}{f(\omega_0)}. \tag{16}$$

Figure 3 is the graphs of each harmonic attenuation relativing fundamental signal when N and M take different value. From this figure, we can see that the main harmonic signal is centralized on frequency $kN\omega_0$. From Fig. 3(b), we find that when k is 1, the attenuation is only -7.081 dB. By Eq. (17), $kN\omega_0$ is the harmonics of sawtooth signal. Because the sine signal is modulated on the sawtooth, the amplitudes whose frequency are the same as sawtooth carrier signal's harmonics must be higher than others.

$$N\omega_0 = \frac{N}{T} = \frac{N}{NT_{\text{c}}} = \frac{1}{T_{\text{c}}} = \omega_{\text{c}}. \tag{17}$$

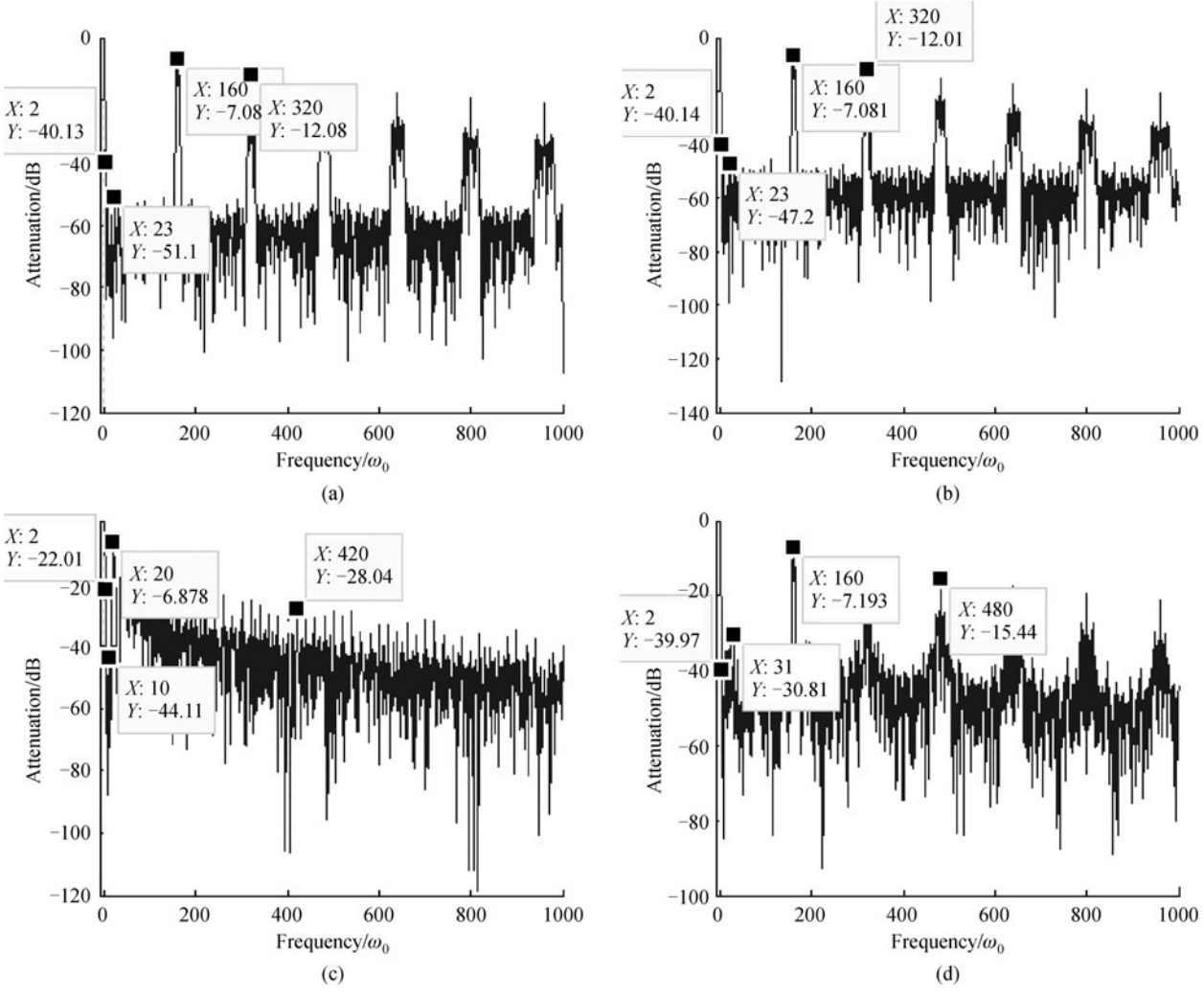

Fig. 3 Amplitude attenuation of every harmonic relative to base frequency when N and M take different values. (a) N and M for 160 and 100; (b) N and M for 160 and 50; (c) N and M for 20 and 100; (d) N and M for 160 and 10

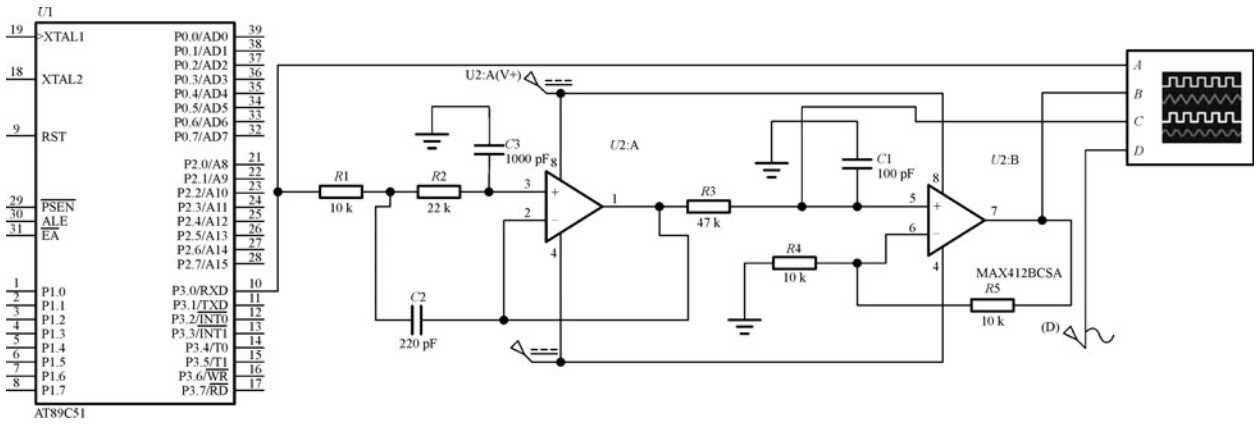

Fig. 4 PWM and three orders filter circuit

From Fig. 3, we find that there are three aspects that parameter N influences the amplitude frequency spectrum. First, N influences the attenuation of harmonics of $kN\omega_0$. The attenuation grows with N. However the relationship isn't very obvious. Second, N influences the attenuation of second harmonic. The attenuation grows with N too. In the same condition that the M is 100, when the N is 160, the attenuation of second harmonic is -40 dB. And the attenuation just is -22 dB when the N is 20. Third, when the N is bigger, the difference of PWM fundamental frequency and carrier fundamental frequency is larger. Then, the requirement of steep characteristics of analog filters to filter the carrier signal is less.

The parameter M determines the accuracy of carrier signal. By the observation and comparison of Fig. 3, we know that the main influence of M is to attenuate the amplitude of all frequency except $kN\omega_0$ of the amplitude frequency spectrum of PWM. The larger the difference between the harmonic's frequency and $kN\omega_0$, the larger the attenuation. According to this analysis, the frequency controllable sine signal can be generated in this way. First, select appropriate parameter M and N according to the quality requirement of sine signal. Then, designing appropriate filters to filter the harmonics of frequency $k\omega_c$. In fact, the parameters of analog filters are just determined by the sawtooth signal period T_c, and have nothing to do with the expected sine frequency. The Sine frequency is controlled by parameter N. The N must larger than a particular value. It is a least value N with which all the harmonics of PWM satisfy requirement after the parameter fixed analog filters when the sawtooth carrier period is T_c.

Figure 4 is simulation diagram. In this simulation, the analog filter is designed as three-order filter. There third-order filter is also used to reverse and amplify.

Figure 5 is the simulation result of Fig. 4. The N is 200, and the M is 100. The first line is a standard sine signal. The second line is PWM output. The third line is the PWM after two-order filter signal. The last line is the PWM after

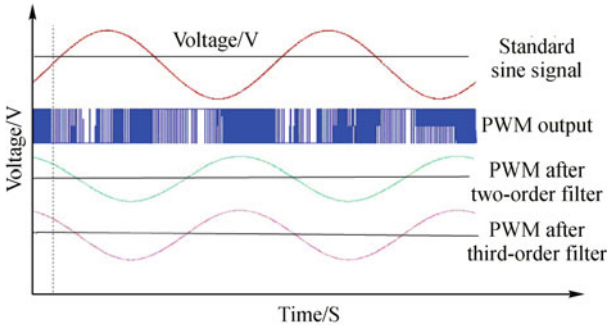

Fig. 5 Signals for PWM pass through three orders filter

third-order filter signal. The theory and simulation show that the after the PWM pass through two-order filter a reasonable sine signal is obtained.

3 Sine signal realization

3.1 PWM output with least FPGA resource

According to the PWM realization theory, a serial of sine signal value *reg_sine* with same phase difference of every two adjacent value. In one carrier period, the output of PWM is determined by the current count *reg_count* and the current sine value *reg_sine*. If *reg_count* < *reg_sine*, FPGA output low, else FPGA output high.

Usually, the program need to store a serial of *reg_sine*. In this thesis, we just store the difference of adjacent value to reduce the consumption of FPGA resource. The algorithm get next sine value by current value plus/minus the difference simply. On the other side, the algorithm make full use of sine function symmetry. From Fig. 6, we can see that the sine value increase from minimum to maximum, then decrease from maximum to minimum, and so repeat. So, the algorithm just need to store half of value.

The main resource of FPGA is register which is good at

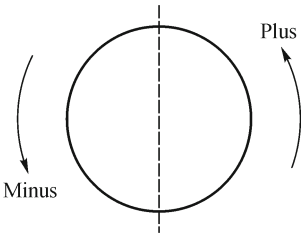

Fig. 6 Changing trend of sine function

shift operation. So a ring structure is used to store the data. After the read operation, the ring structure data shift every time. According to Fig.7, the expected PWM signal can be generated.

3.2 Analog filter circuit

According to the parameters, FPGA gets the PWM signal. Then the PWM signal change to differential signal. The output signal must pass through an effective analog filter circuit [7]. The filter can be the bandpass-flat bart woz low-pass filter, or chebyshev low-pass filter with bandpass ripple or other filter. What kind of filter to be used is depend on the application requirement. The purpose of filter is to filter the harmonics relating carrier signal. The experiment takes the three-order chebyshev low-pass filter in this thesis. The steep characteristics of chebyshev filters at cut-off frequency is better. The schematic like Fig. 4.

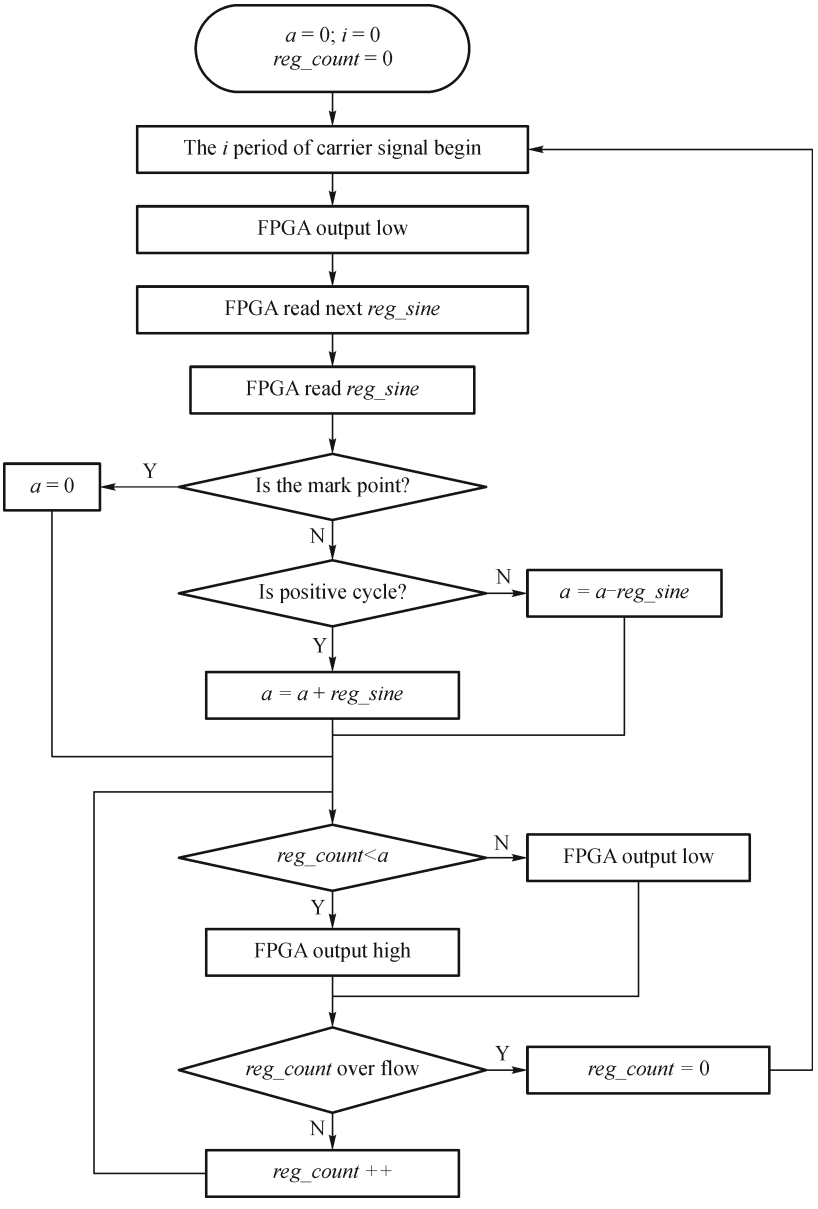

Fig. 7 Flow chart for FPGA output PWM

4 Experiment result and analysis

Controller FPGA output differential PWM signal according to the expected sine signal frequency. After the PWM signal pass through the filter, the correct sine signal is obtained. Figure 8 is the amplitude frequency spectrum of one way of differential PWM signal. Comparing with Figs. 3 and 8, we can find they are consistent with each other.

After the output PWM signal pass through the filter, we get the sine signal. By changing the parameter *N*, we get different frequency sine signal. Just as Fig. 9. In this experiment, this thesis generates a serial of sine with different frequency: 2, 4, 8 kHz, and so on.

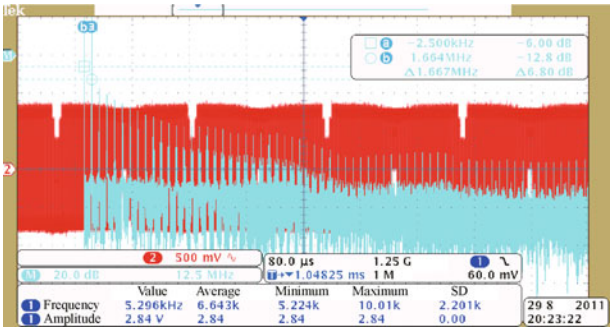

Fig. 8 FPGA output PWM and its spectrum

5 Conclusion

According to the FPGA characteristic, this thesis selects the sawtooth signal as carrier to generate the PWM signal. This thesis proves that the correct sine signal can be gotten with reasonable sawtooth signal frequency and resolution according to the system clock cycle and expected sine signal frequency. The PWM just need to pass through a simple low-pass filter. To reduce the logical resource, this thesis proposed a method that just store the limited increment value, which is full use of the symmetry of sine signal. At last, this thesis shows the feasibility and correctness of the algorithm by experiment.

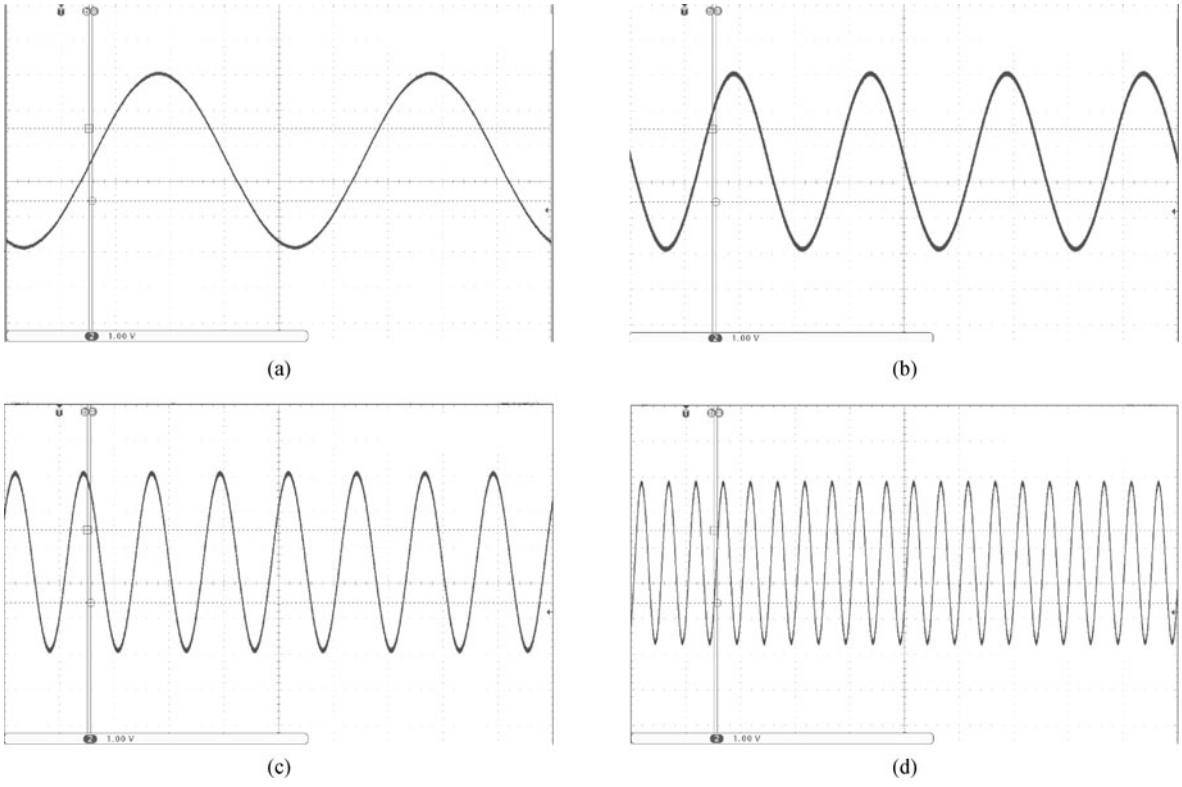

Fig. 9 Different frequency sine signals. (a) 2 kHz sine signal; (b) 4 kHz sine signal; (c) 8 kHz sine signal; (d) 20 kHz sine signal

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