PWM Signal Generator

by,

Bhushan Borse (BT18EEE064)

Suyash Dharaskar (BT18EEE065)

Arihant Gaur (BT18EEE066)

Department of Electrical and Electronics Engineering

Visvesvaraya National Institute of Technology Nagpur 440 010 (India)

Date of submission:15/5/2020

Aim: PWM Signal Generator

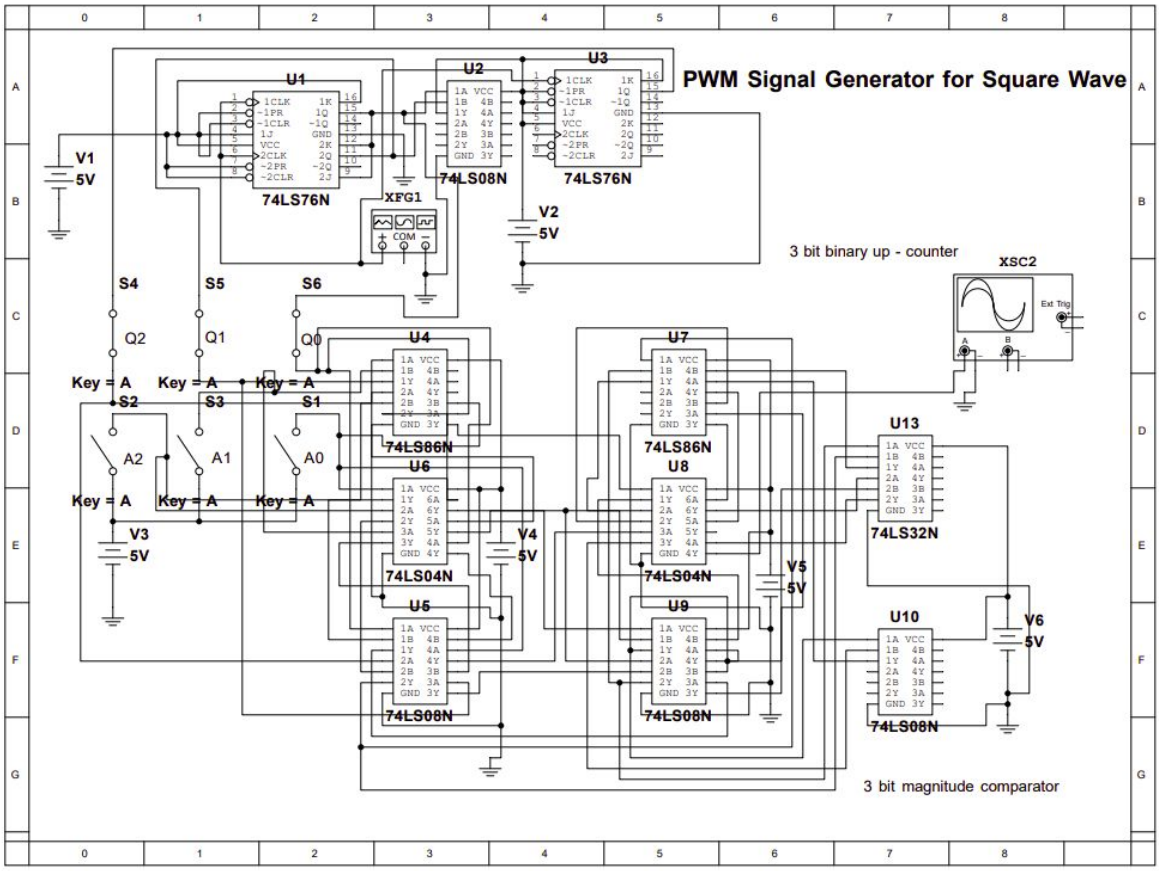
Design a circuit that can generate a PWM scheme for power electronic devices, which require a gate signal for switching and setting the switching frequency for converting one voltage form to another. The duty cycle variation has been quantized.

Components Used

1. Battery (5V) x 6
2. Ground Connections x 6
3. Switches x 6
4. 74LS76N (JK Flip Flop) x 2
5. 74LS08N (AND Gate) x 4
6. 74LS04N (NOT Gate) x 2
7. 74LS86N (XOR Gate) x 2
8. 74LS32N (OR Gate) x 1
9. Digital Oscilloscope (NI Multisim) x 1
10. Function Generator x 1

The simulations have been made on NI Multisim (Version 14), which is provided by National Instruments.

Circuit Diagram



Methodology

For the sake of comparison between the expected result and practical result, the PWM scheme was first made using the traditional method, involving the use of IC 555.

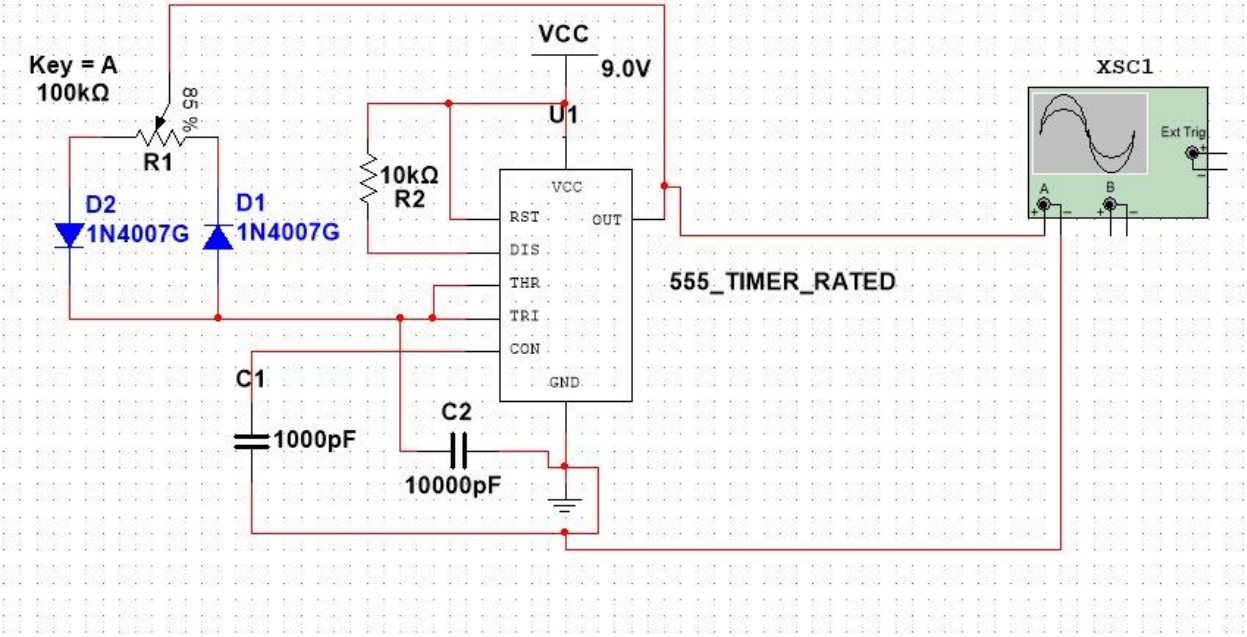


Fig. 1: PWM Signal Generator Using IC 555

As shown in Fig. 1, on varying the value of the potentiometer 'R1', we can alter the duty cycle of the obtained square wave. The timer, in this case, is in a standard astable multivibrator mode. The 'ON' time of the IC is decided by the time taken by the capacitor 'C1' to be charged to 2/3rd of Vcc and similarly, the 'OFF' time is decided by its discharging time below 1/3rd of Vcc. If the potentiometer jockey slides towards the left, that is towards the diode with the anode connected to it separates the 'ON' time, whereas, for the one with the cathode connected, the 'OFF' time is separated. Therefore, when the jockey slides to the left, it results in a decreased 'ON' time and increased 'OFF' time and vice versa. This phenomenon can be seen in Fig. 2, which is the **expected result.**

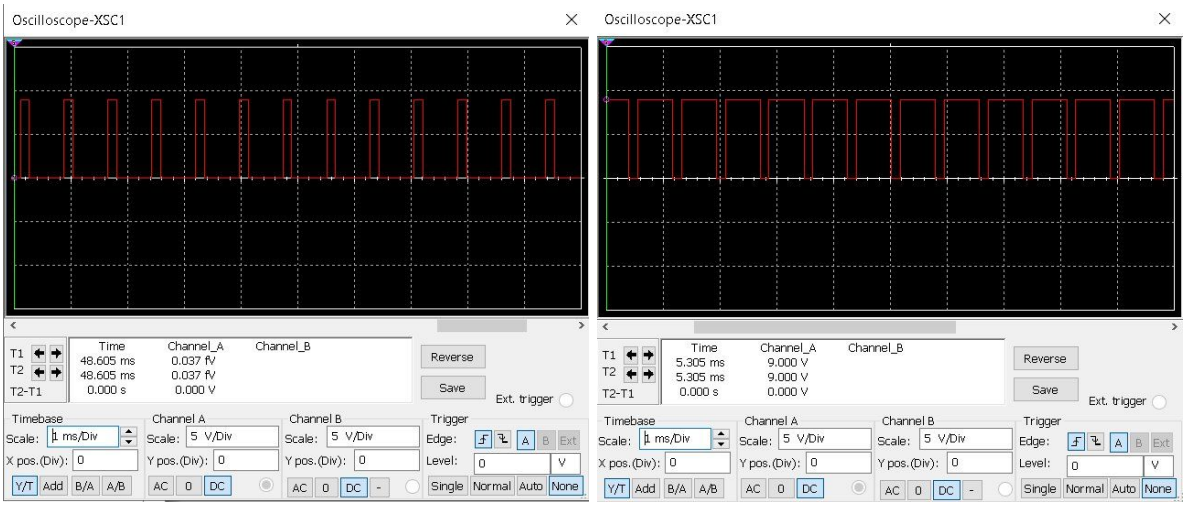


Fig.2: PWM Technique Applied to a Square Wave With Duty Cycles 20% and 80% Respectively

The frequency of the PWM signal can also be derived from F = 0.693 * R1 * C2, where the notations are taken from Fig. 1.

Taking a look at the proposed circuit it is evident that the PWM technique has been applied only with the help of digital electronic components. The circuit applies the PWM technique in a quantized sense, that is, the duty cycle can be varied in steps (8 steps in this case), rather than continuous variation by changing the value of the potentiometer. The circuit has been divided into two parts:

1. 3-bit binary up - counter.
2. 3-bit magnitude comparator.

3 - Bit Binary up - Counter

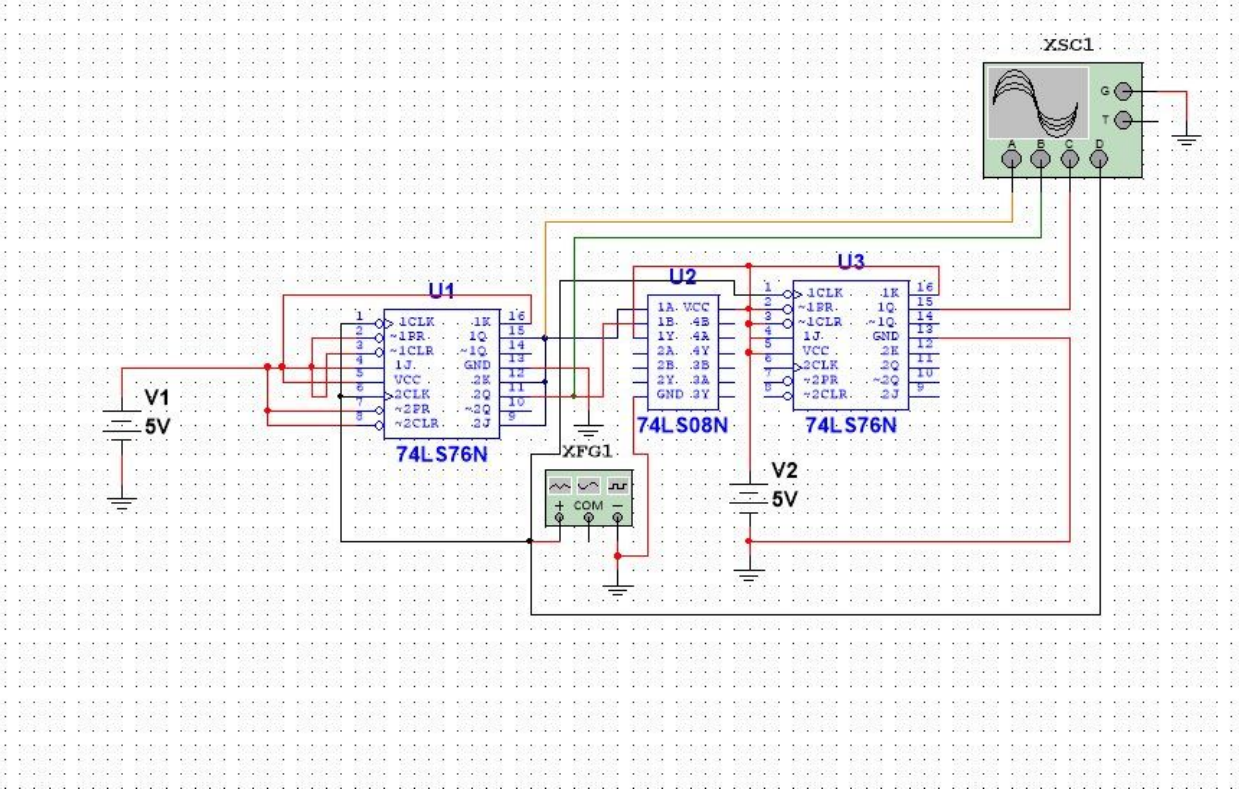


Fig. 3: 3 - Bit Binary up - Counter

A binary counter is essentially a circuit that counts in binary format from 0 to 2^N, where N is the number of bits involved. Here N = 3, so the circuit will count from 000 to 111. This can be achieved by exploiting a unique property of JK flip flop, that is, the toggle mode when both the inputs are high and the clock pulse is provided, which can be seen in the truth table as shown in Table 1.

Table 1: Truth Table of Jk Flip Flop

J	K	CLK	Q
0	0	↑	Q_0 (no change)
0	1	↑	0

1	0	↑	1
1	1	↑	Toggles

The excitation table for the setup is shown in Table 2, in accordance with the output we desire.J_0K_0, J_1K_1 and J_2K_2 are the inputs to the three flip flops that will yield the next state.

Table 2: Excitation Table for 3 - Bit Binary up - Counter

Present State	Next State	J_2K_2	J_1K_1	J_0K_0
111	110	x0	x0	x1
110	101	x0	x1	1x
101	100	x0	0x	x1
100	011	x1	1x	1x
011	010	0x	x0	x1
010	001	0x	x1	1x
001	000	0x	0x	x1
000	111	1x	1x	1x

Where ‘x’ is defined as the “don’t care” condition. This can be solved using K - maps as shown in Fig. 4.

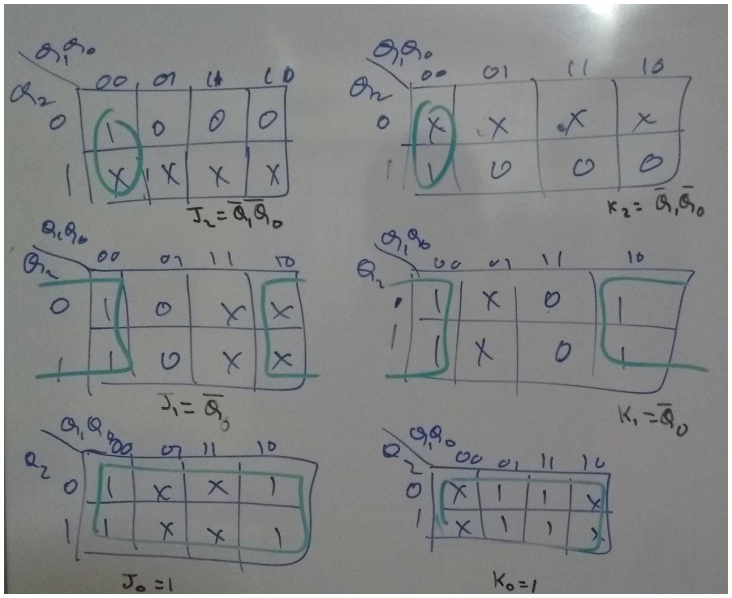


Fig. 4: Solving Table 1 Using Karnaugh Maps (k - Maps), Along With Obtaining the Logic Equations

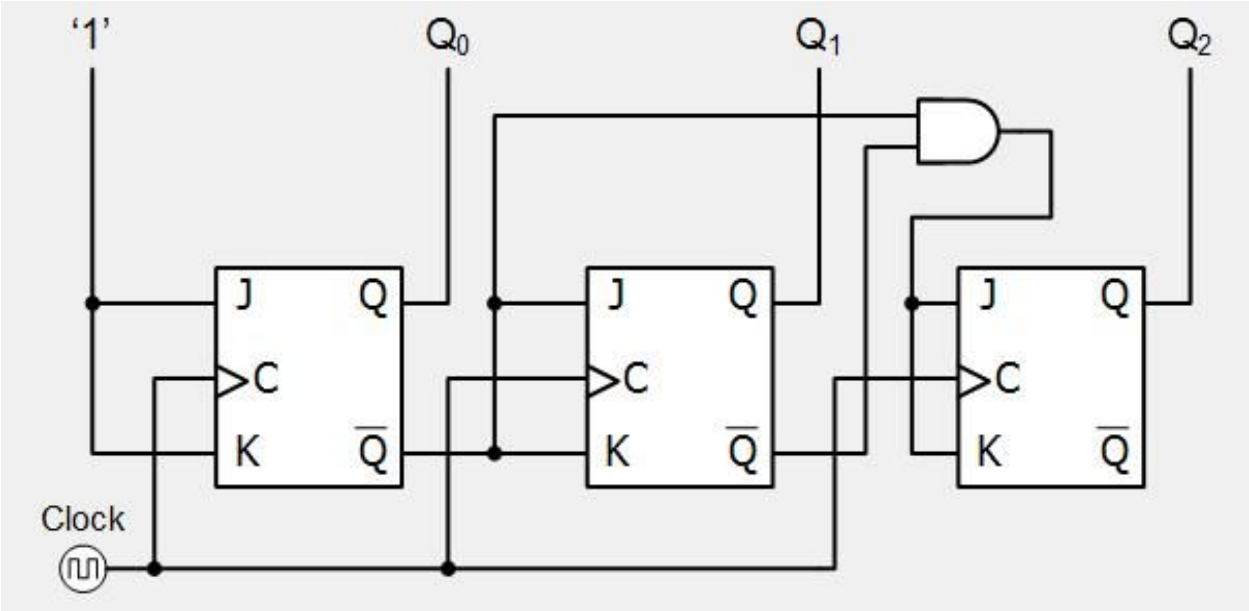


Fig. 5: Equivalent Circuit Obtained from the Equations

The circuit is obtained and has been simulated to get Fig. 3. The results are shown in Fig. 6, where probing is done for the left figure on the clock and the right figure on the outputs for each of the JK flip flops.

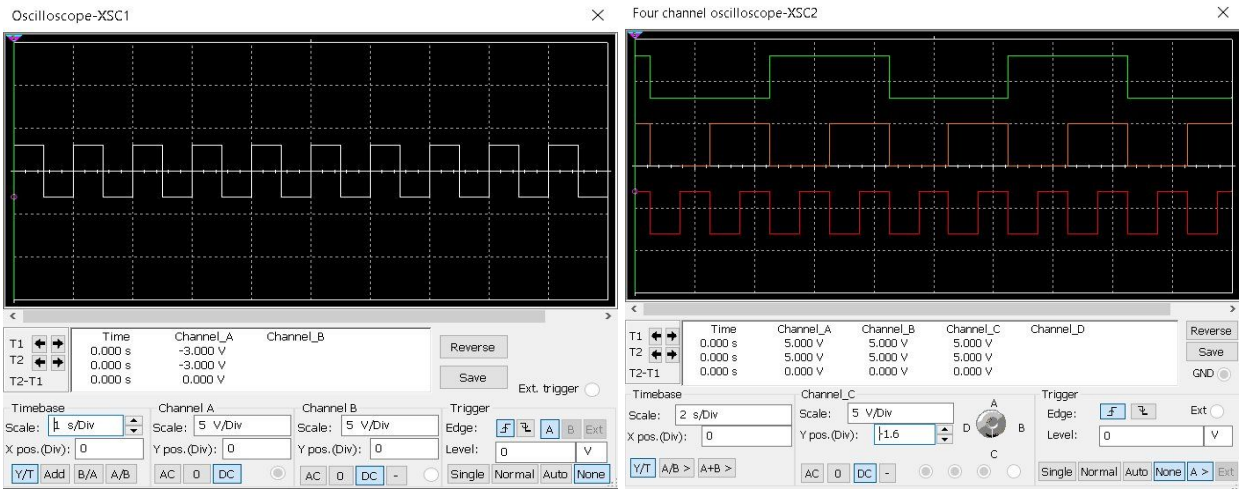


Fig. 6: Left: Clock Pulse Fed to Jk Flip Flop (frequency Is 1Hz in This Snapshot). Right: Green Colour Indicates MSB, Whereas Red Indicates LSB

3-bit Magnitude Comparator

For binary data comparison, we use combinational circuits that can compute the relative magnitude of two binary numbers. Implementing it in hardware requires working with binary numbers to understand the working. So, given two numbers 'A' and 'B', there are three obvious outcomes. The number 'A' can be greater than 'B', equal to 'B' or less than 'B'. Here, we are considering 3 - bit numbers. Making the truth table for 3-bit numbers can be quite cumbersome since there will be 64 different possibilities to take into consideration. Therefore the truth table of 2 - bit magnitude comparator is drawn for demonstration in Table 3.

Table 3: Truth Table for 2 - Bit Magnitude Comparator

A_1	A_0	B_1	B_0	A < B	A = B	A > B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Solving this using K - maps, we get Fig. 8. There are three maps drawn for each of the cases, with a total of 16 possibilities, therefore, it is easy to calculate. However, for 3 - bit, there are more combinations, so only the final circuit diagram obtained is shown in Fig. 9. The circuit diagram is then integrated with the original up - counter setup, to form the final circuit.

Procedure

The circuit starts with an up - counter circuit, as explained before (the datasheets for the ICs used in this circuit have also been provided in the enclosures). The output obtained from the up - counter circuit is denoted as ‘Q2’, ‘Q1’ and ‘Q0’, from MSB to LSB. Being a 3 bit counter, the numbers go from 000 to 111, with every step occurring as per the frequency of the clock cycle. To show that the circuit used can handle higher frequencies, the clock frequency was set to 1 MHz. A switch is present at each of the outputs for the counter. Now, the three user - controlled bits are initialized as ‘A2’, ‘A1’ and ‘A0’, ordered from MSB to LSB. Whenever the user enters one of the binary combinations, given that the output of the counter is dynamic, we shall get a dynamic output. Suppose the value of ‘A’ has been set to 011 that is, the binary equivalent of 3. Therefore, the magnitude of ‘A’ is greater than ‘Q’, till the

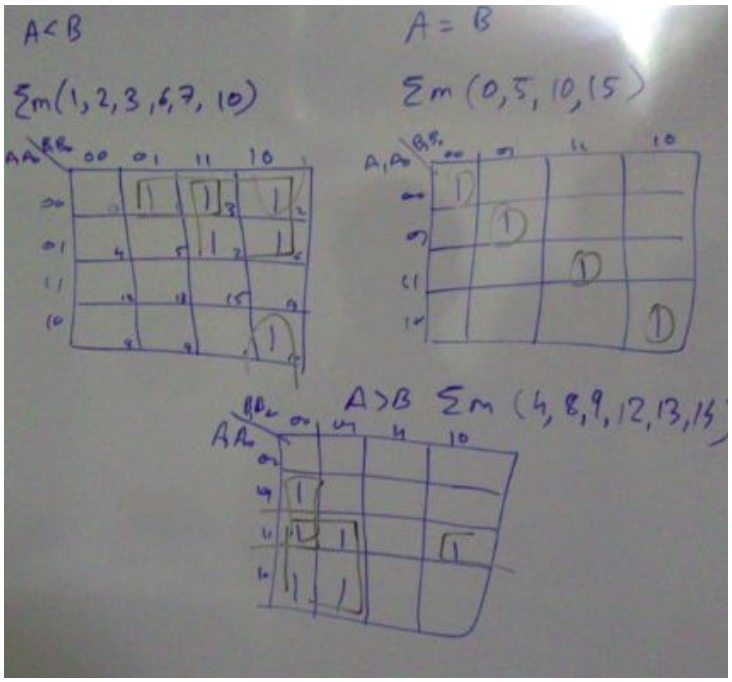


Fig. 7: K - Maps Obtained for 2 - Bit Magnitude Comparator

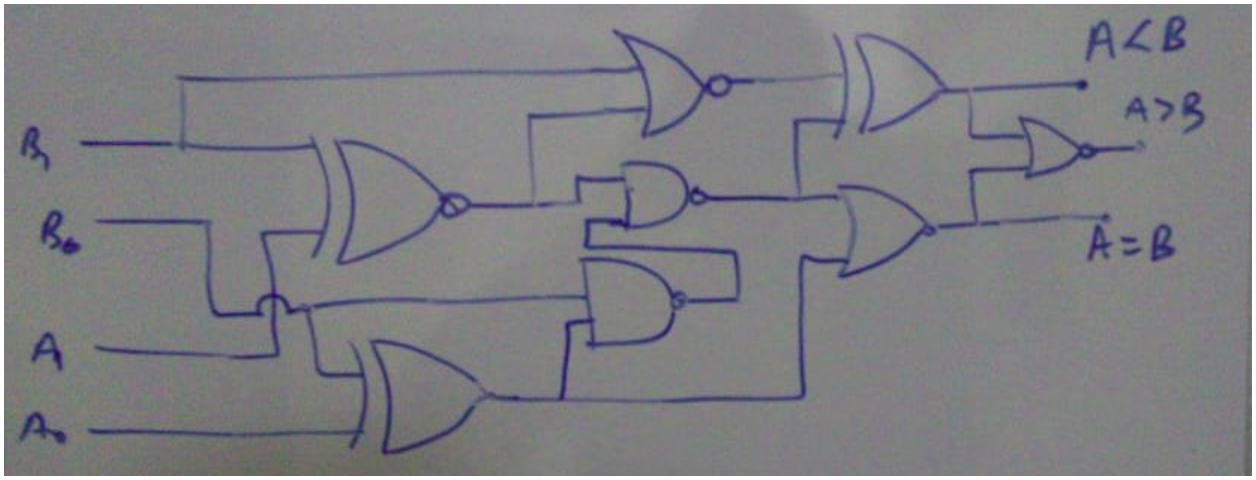


Fig. 8: 2 - Bit Magnitude Comparator

decimal equivalent at ‘Q’ hits 3, where they are equal, followed by ‘Q’ being greater than ‘A’. So, for the interval 0 to 3, the output has been set high, whereas it is low for the rest of the interval. Therefore, we get a square wave, where the pulse width is determined by the user, by entering the binary equivalent of any number between 0 and 7. So, having 000 at ‘A’ means minimum duty cycle and 111 means the highest duty cycle. The results have been shown in Fig. 10, 11 and 12, where the variation of the duty cycle with the binary equivalent number is seen.

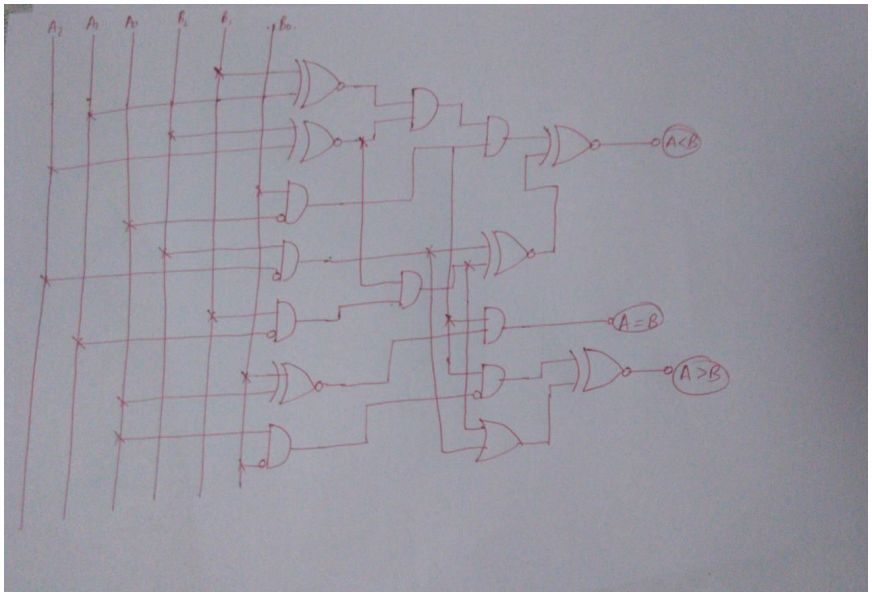


Fig. 9: 3 - Bit Magnitude Comparator

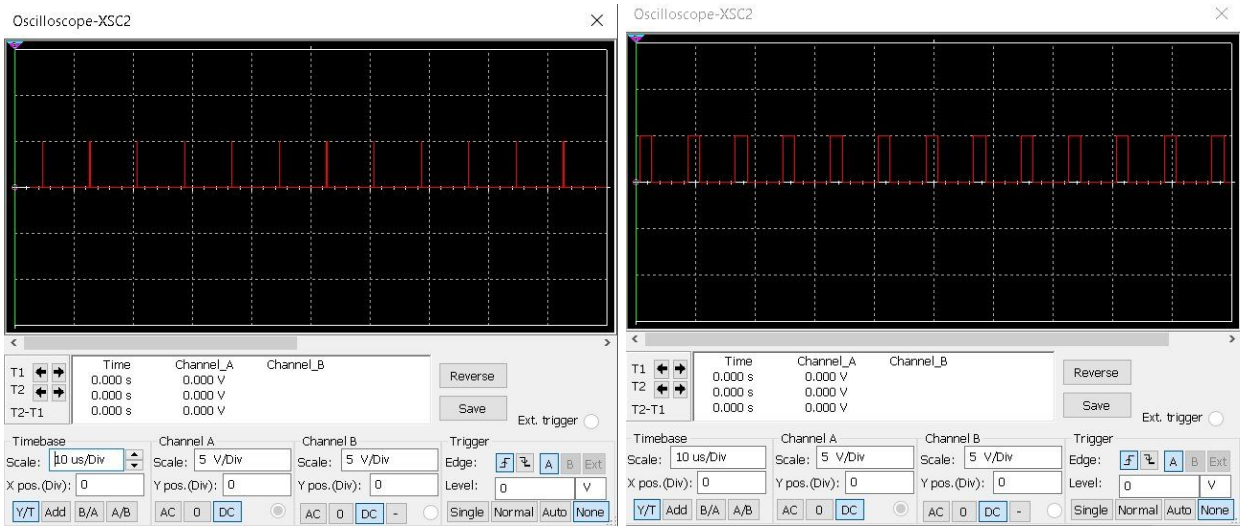


Fig. 10: Left: 000. Right: 010

One important thing to note is that since the devices that are used in the simulation are not ideal, therefore, due to thermal noise as well as other factors such as voltage fluctuations, there are some instances at 000, 011 and 101 where short and sharp voltage spikes are seen (width of 0.5 nanoseconds). One such distortion has been shown in Fig. 12 for the case of 101 binary.

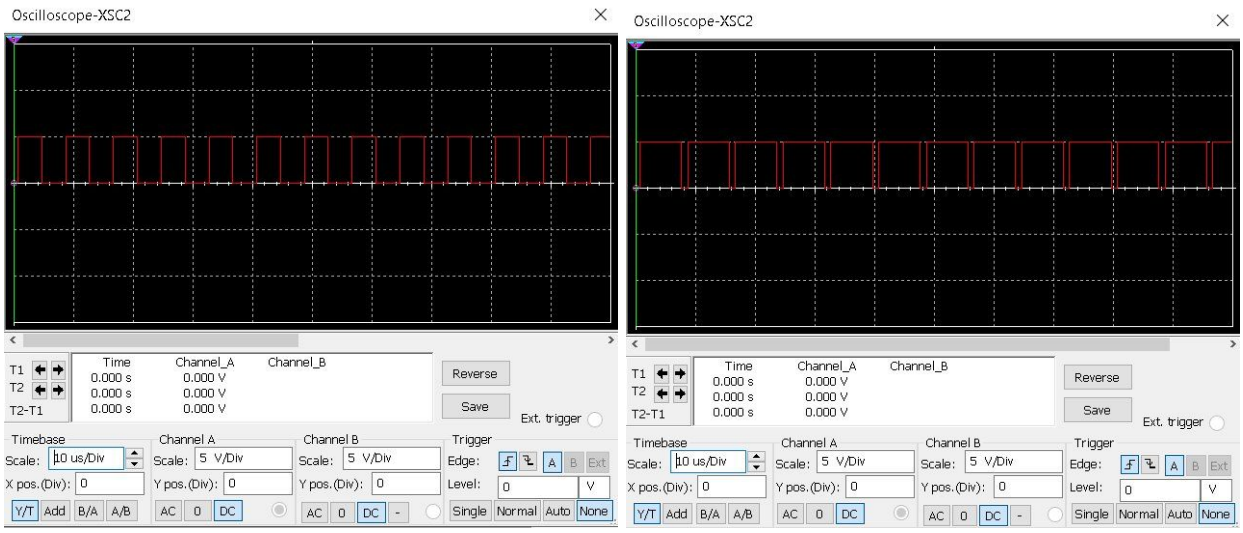


Fig. 11: Left: 100, Right: 111

Fig. 12: 101

Enclosures

The .zip file submitted consists of the following items.

1. Project Report (which is currently being read)
2. Simulation File (.ms14 format)
3. Demonstration video
4. 74LS76N datasheet (Motorola)
5. 74LS08N datasheet (Motorola)
6. 74LS04N datasheet (Motorola)
7. 74LS86N datasheet (Motorola)
8. 74LS32N datasheet (Motorola)
9. README file