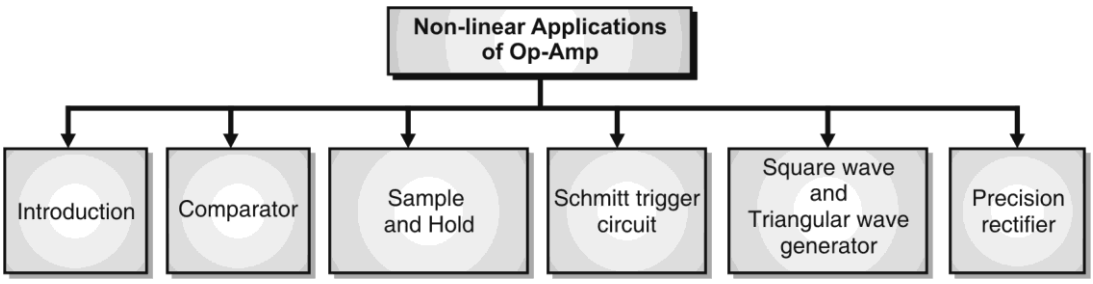
MODULE - **3**

Non-Linear Applications of Op-Amp

University Prescribed Syllabus

Comparators : Inverting comparator, non-inverting comparator, zero crossing detector, window detector, peak detector, sample and hold circuits. Schmitt Triggers : Inverting schmitt trigger, non-inverting schmitt trigger, Waveform Generators : Square wave generator and triangular wave generator, Precision Rectifiers : Half wave and full wave precision rectifiers.

This chapter can be divided into six sections as shown in the chart C3.1.1.



C3.1.1

INTRODUCTION

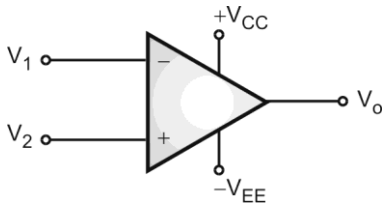
Explain the non-linear applications of op-amp.

- An operational amplifier when uses open-loop configuration or positive feedback, it operates in non-linear mode.
- In non-linear mode, op-amp switches between positive and negative saturation levels.
- The non-linear applications of op-amp are comparators, precision rectifiers, Schmitt trigger, peak detectors, sample and hold circuits, clippers and clampers circuits.

Explain the open-loop configuration of op-amp.

In open-loop configuration of op-amp :

- No feedback is used.
- Gain is very high. Ideally it is infinite.
- For very small input voltage, output voltage is switched to $\pm V_{sat}$.

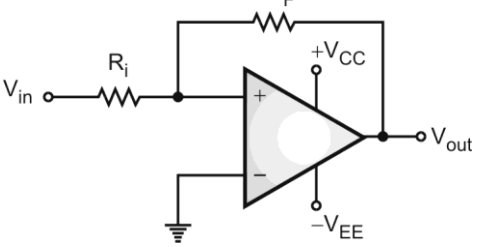


(1C1)**Fig. 3.1.1 : Open-loop configuration**

- The value of $\pm V_{sat}$ is 90% of d.c. supply voltage, i.e., $+V_{CC}$ and $-V_{EE}$ applied to 7 and 4 pins of op-amp IC741.

Explain the positive feedback in operational amplifier.

- When the feedback resistance 'R_F' is connected between output terminal and non-inverting terminal, then the circuit is said to be using positive feedback.
- Gain of positive feedback is large.
- It is used in oscillators.
- Schmitt trigger circuit also uses positive feedback.



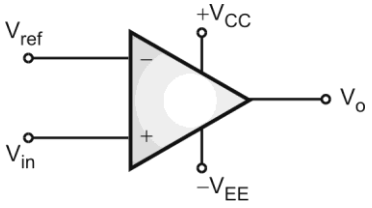
(1C2)**Fig. 3.1.2 : Positive feedback circuit**

COMPARATOR

With neat circuit explain the working of comparator circuit.

MU - Q. 1(a), Dec. 18, 5 Marks

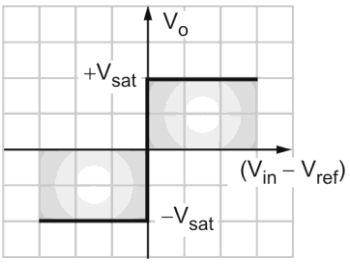
- Comparator compares the signal voltage on one input of an op-amp with a known voltage called reference voltage on the other input.
- It uses open loop op-amp with two inputs.
- It compares the two inputs and generates a single output.
- Gain of the open loop comparator is ideally infinite, but practically the output voltage is $\pm\ V_{sat}$.



(1C3) **Fig. 3.2.1 : Basic comparator**

- $\pm V_{sat}$ is 90% of d.c. supply voltage, i.e., $\pm V_{CC}$.
- Fig. 3.2.2 shows basic comparator circuit and its ideal transfer characteristics.
- Depending on input applied to inverting or non-inverting terminals of an op-amp, comparators are of two types :

  (i) Inverting comparator (ii) Non - inverting comparator



(1C4) **Fig. 3.2.2 : Ideal transfer characteristics of comparator**

Write short note on characteristics of comparator.

The important characteristics of a comparator are :

1. **Speed of operation :** The output of the comparator must switch rapidly between saturation levels and also respond instantly to any change in conditions at its input.

- Bandwidth of the comparator is large. Speed of operation depends on bandwidth. Higher the bandwidth, higher is the speed of the operation.

2. **Accuracy :** The accuracy of comparator depends on its voltage gain, CMRR (Common mode rejection ratio), input offsets and thermal drifts.

- High voltage gain requires very small input difference voltage (V_{id}) to cause comparators output voltage to switch between saturation levels, i.e., $\pm V_{sat}$ because $V_o = A_d \cdot V_{id}$.
- Also high CMRR helps to reject common mode input voltages such as noise at the input terminals.

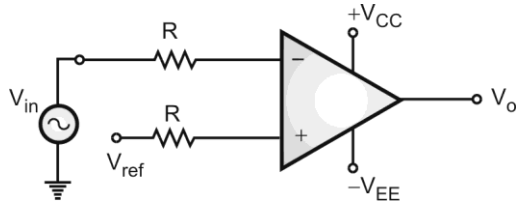
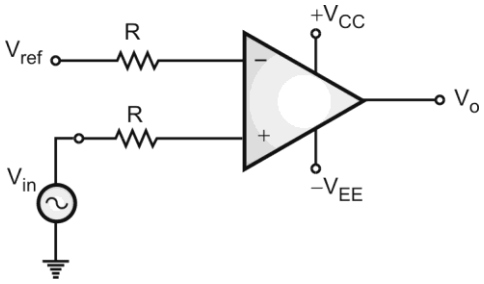
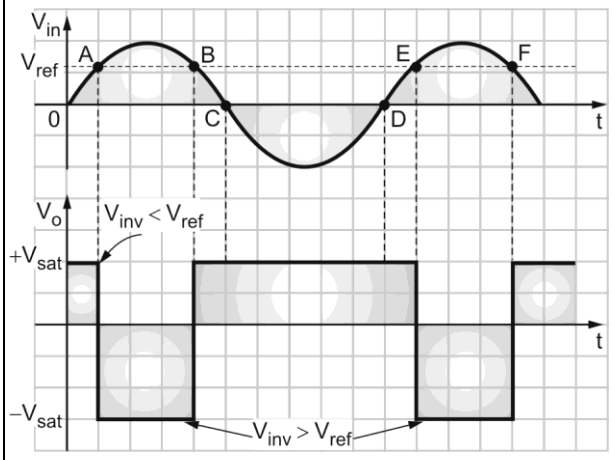
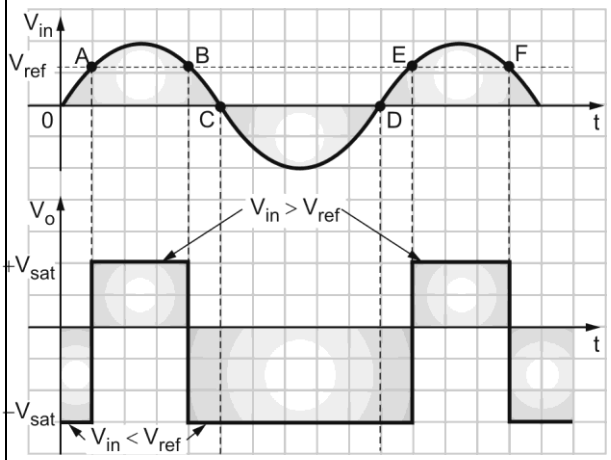
$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

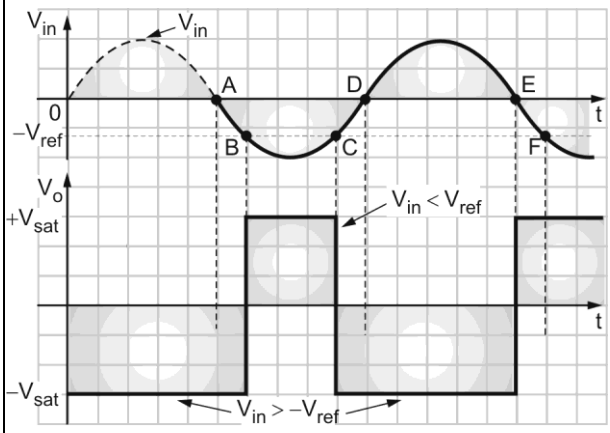
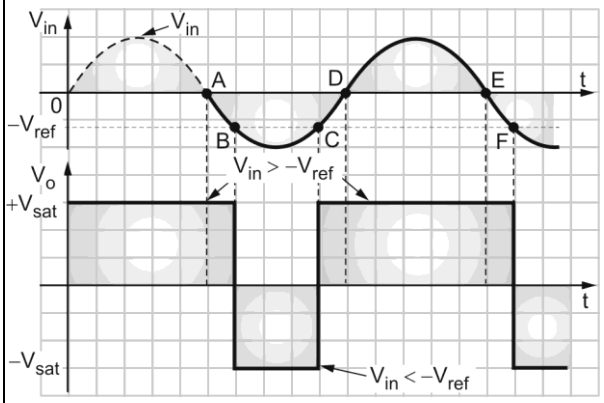
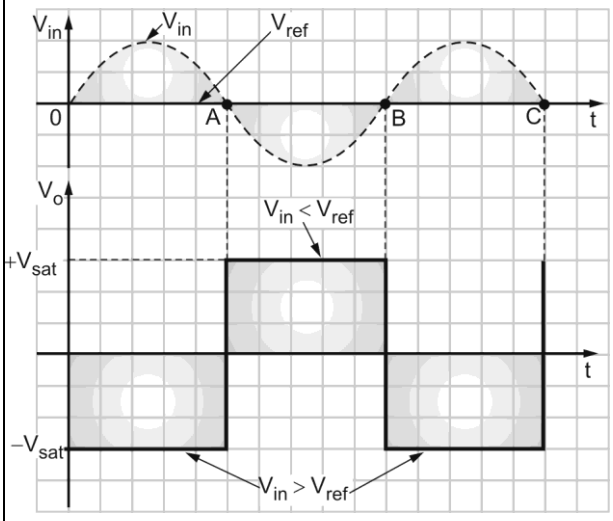
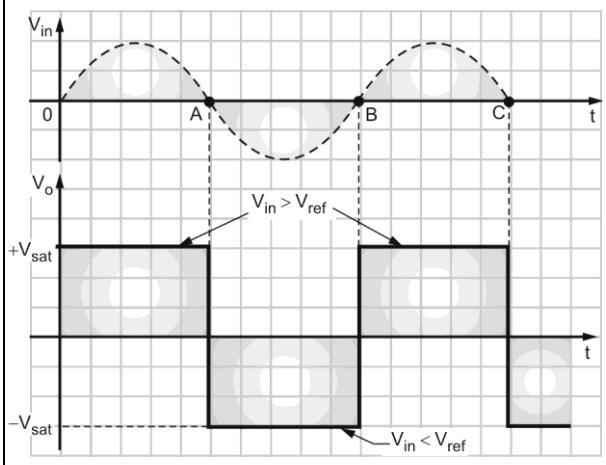
- Also input offset voltage and input offset current must be negligible.
- Changes in input offset voltage and input offset current due to temperature variations should be very small.

3. **Compatibility of the output :** The output of comparator must swing between two logic levels suitable for a logic family like TTL (Transistor Transistor Logic), i.e., $+ V_{sat}$ and $- V_{sat}$ .Comparison between Inverting and Non-Inverting Comparator

UQ. 3.2.3 Differentiate between inverting and non-inverting comparators.

MU - Q. 1(c), May 16, 4 Marks

Sr. No.	Inverting comparator	Non-inverting comparator
1.	Input signal is applied to inverting terminal of op-amp and fixed d.c reference voltage is applied to non-inverting terminal of op-amp.	Input signal is applied to non-inverting terminal of op-amp and fixed d.c. reference voltage is applied to inverting terminal of op-amp.
2.	 **Fig. 3.2.3 : Circuit diagram of inverting comparator**	 **Fig. 3.2.4 : Circuit diagram of non - inverting comparator**
3.	When V_{ref} is positive d.c voltage : As shown in Fig. 3.2.5 From 0 to A, $V_{in} < V_{ref}$, so output is + V_{sat}. From A to B, $V_{in} > V_{ref}$, so output is – V_{sat}. From BCDE, $V_{in} < V_{ref}$, so output is + V_{sat}.  **Fig. 3.2.5**	When V_{ref} is positive d.c voltage : As shown in Fig. 3.2.6, From 0 to A, $V_{in} < V_{ref}$, so output is – V_{sat}. From A to B, $V_{in} > V_{ref}$, so output V_o is + V_{sat}. From BCDE, $V_{in} < V_{ref}$, so output is – V_{sat}  **Fig. 3.2.6**
4.	When V_{ref} is negative :	When V_{ref} is negative :

Sr. No.	Inverting comparator	Non-inverting comparator
	 (1C9)**Fig. 3.2.7** From OAB, $V_{in} > -V_{ref}$, so output $V_o = -V_{sat}$ From BC, $V_{in} < -V_{ref}$, so output $V_o = +V_{sat}$ From CDE, again $V_{in} > -V_{ref}$, $\therefore \quad V_o = -V_{sat}$	 (1C10)**Fig. 3.2.8** From OAB, $V_{in} > -V_{ref}$, so output $V_o = +V_{sat}$ From BC, $V_{in} < -V_{ref}$, so output $V_o = -V_{sat}$ From CDE, again $V_{in} > -V_{ref}$, $\therefore \quad V_o = +V_{sat}$
5.	When V_{ref} is zero :  (1C11)**Fig. 3.2.9** From 0 to A, $V_{in} > V_{ref}$, so, $V_o = -V_{sat}$ From A to B, $V_{in} < V_{ref}$, i.e., negative So, $V_o = +V_{sat}$	When V_{ref} is zero :  (1C12)**Fig. 3.2.10** From 0 to A, $V_{in} > V_{ref}$, so, $V_o = +V_{sat}$ From A to B, $V_{in} < V_{ref}$, i.e., negative So, $V_o = -V_{sat}$

✳ **Note :** If greater signal is inverting, then $V_o = -V_{sat}$ and if greater signal is non - inverting then $V_o = +V_{sat}$.

UEx. 3.2.1 MU - Q. 1(e), Dec. 17, Q. 1(b), Dec. 19, 5 Marks

If the input to the ideal comparator shown in Fig. Ex. 3.2.1 is a sinusoidal signal of 8 volt peak to peak without any D.C. component, then check whether the duty cycle of the output of comparator is 33.33% or 25% or 20% prove it.

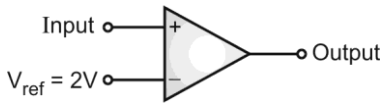


Fig. Ex. 3.2.1

☑ **Soln. :**

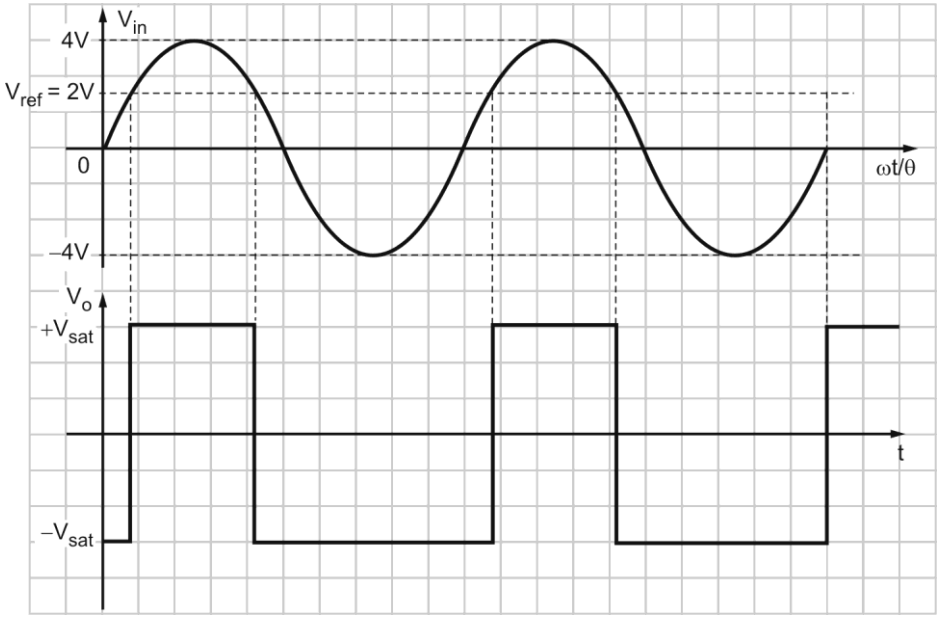


Fig. Ex. 3.2.1(a)

– From the output waveforms shown in Fig. 3.2.1(a), input signal crosses the reference point of 2V at two points in the positive half cycle of the input signal. Therefore at the two crossing points, we can have the equation,

$$4 \sin\theta = 2 \qquad \therefore \quad \sin\theta = \frac{2}{4}$$

$$\therefore \quad \theta = \sin^{-1}\left(\frac{2}{4}\right) \qquad \therefore \quad \theta = 30°$$

– Thus, at $\theta = 30°$, input signal crosses the reference point. Since there are two reference points in the positive half cycle of input signal and both are symmetric from both the ends. So we get two angles corresponding to two crossings as follows,

$$\theta_1 = 30° - 0 \quad \text{and} \quad \theta_2 = 180° - 30°$$

$\therefore \quad \theta_1 = 30° \qquad \therefore \quad \theta_2 = 150°$

Thus between $\theta_1 = 30°$ to $\theta_2 = 150°$

Output voltage is high (+ V_{sat}). The complete cycle of input signal corresponds to $\theta = 360°$.

– Thus the duty cycle of the output square wave can be represented as follows,

$$D = \frac{T_{ON}}{T} \qquad \therefore \quad D = \frac{(\theta_2 - \theta_1)}{\theta} = \frac{150° - 30°}{360°} = \frac{120°}{360°} = \frac{1}{3} = 33.33\%$$

Thus the duty cycle of the output square wave is 33.33%.

Applications of Comparator

Write some applications of comparator.

Some important applications of comparator are :

1. Zero-crossing detector
2. Peak detector
3. Window detector
4. Level detector
5. A/D converter
6. V-F converter
7. Switching regulator

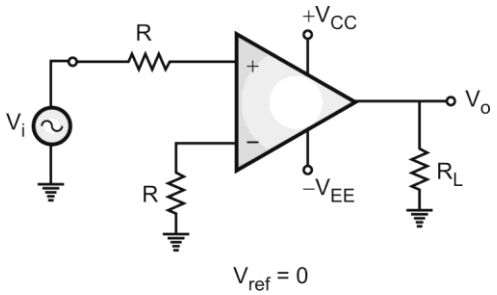
Zero Crossing Detector

Explain zero-crossing detector with neat diagram. **MU - Q. 4(c), May 15, 4 Marks**

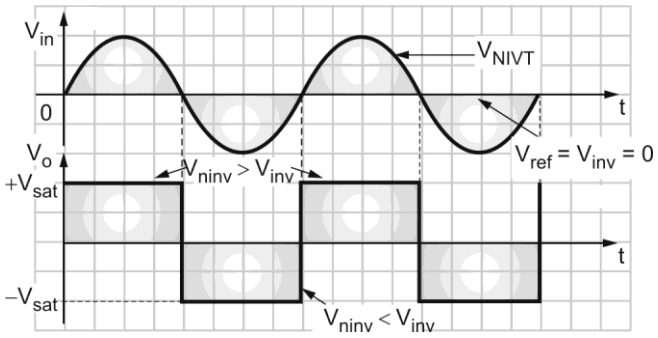
– It is the non-inverting comparator whose reference voltage is kept at ground potential.

– It is also known as sine wave to square wave converter.

– Fig. 3.2.11(a) shows the circuit diagram of zero-crossing detector and Fig. 3.2.11(b) shows the input and output waveforms.



(a) Circuit diagram of zero-crossing detector



(b) Input and output waveforms of zero-crossing detector

Fig. 3.2.11

– Input is applied to non-inverting terminal and the ground reference is applied to inverting terminal.

– When the input is turned 'ON', for positive half cycle of applied input signal, the non-inverting terminal input (positive signal) is greater than the inverting terminal input (zero level) of comparator.

– This will generate + V_{sat} output.

- This output will remain as it is for full positive half cycle because the above condition is satisfied for entire positive half cycle.
- Now, for negative half cycle, the inverting terminal input (zero level) is greater than the non-inverting terminal input (negative signal) of comparator.
- This will generate – V_{sat} output.

  Thus whenever the input crosses the reference axis (zero level), its output can be switched from + V_{sat} to – V_{sat} and vice-versa.
- Due to this behavior of the circuit, it is known as zero-crossing detector.

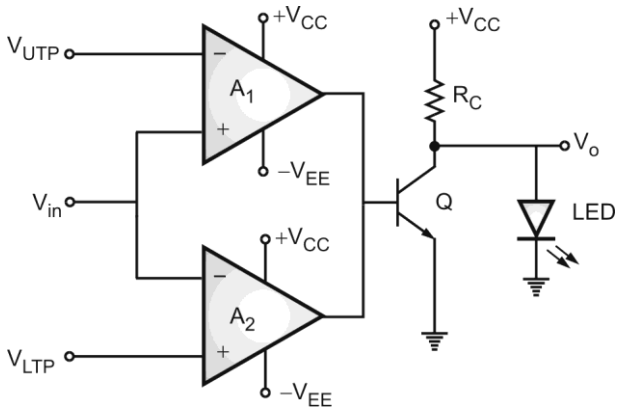
Window Detector

Write short note on : Window detector.

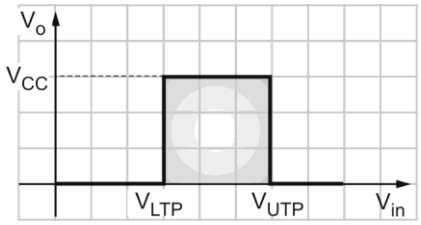
MU - Q. 6(5), Dec. 14, 5 Marks, Q. 6(a), Dec. 16, 4 Marks

Explain op-amp as window detector. **MU - Q. 1(e), May 19, 5 Marks**

- Window detector circuit is used to mark the instant at which an unknown input is between two threshold levels.
- Circuit diagram and output waveform is as shown in Fig. 3.2.12(a) and Fig. 3.2.12(b).



(1C15)**Fig. 3.2.12(a) : Circuit diagram of window detector**



(1C16)**Fig. 3.2.12(b) : Output waveform**

- Here two op-amps are used along with switching transistor.
- Op-amp A_1 is acting as non-inverting comparator whose non-inverting terminal is connected to input while the upper threshold level acting as reference voltage V_{UTP} is connected to inverting terminal.
- Similarly op-amp A_2 is acting as inverting comparator whose inverting terminal is connected to input while reference voltage V_{LTP} is connected to non-inverting terminal.
- LED indicator is turned 'ON' only when applied input is in between a window created by the threshold levels V_{UTP} and V_{LTP}.
- The working of the circuit is explained with the help of Table 3.2.1.

Table 3.2.1

Sr. No.	Input	Output of op-amp A_1	Output of op-amp A_2	Status of transistor 'Q'	Output voltage V_o	Status of LED
1.	$V_{in} < V_{LTP}$	0V	$+ V_{sat}$	ON	0V	OFF
2.	$V_{LTP} \leq V_{in} \leq V_{UTP}$	0V	0V	OFF	$\simeq + V_{CC}$	ON
3.	$V_{in} > V_{UTP}$	$+ V_{sat}$	0V	ON	0V	OFF

Peak Detector

Explain working of peak detector. **MU - Q. 1(e), Dec. 16, 4 Marks**

Short note on : Peak detector circuit. **MU - Q. 6(d), May 19, 5 Marks**

- The function of the peak detector is to capture the positive peak value of the input signal.
- Fig. 3.2.13 shows the circuit diagram of peak detector.

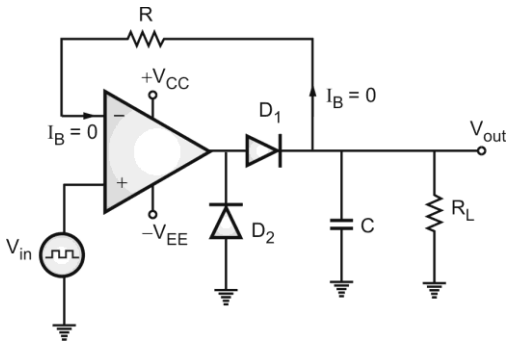


Fig. 3.2.13 : Circuit diagram of peak detector

During positive half cycle

- Output is initially zero; i.e., $V_{inv} = 0$ and when positive voltage is applied at non-inverting terminal of op-amp, then $V_{Ninv} > V_{inv}$.
- Output of op-amp at point A becomes $+ V_{sat}$.
- Diode 'D_1' is ON, i.e., forward biased and diode 'D_2' is OFF, i.e., reverse biased and capacitor 'C' charges to the positive peak value V_p of the input voltage V_{in} with upper plate positive.
- Thus during positive half cycle, op-amp acts as a voltage follower, as shown in Fig. 3.2.14.

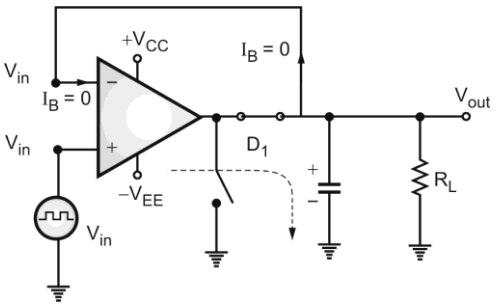


Fig. 3.2.14 : Equivalent circuit of peak detector during positive half cycle

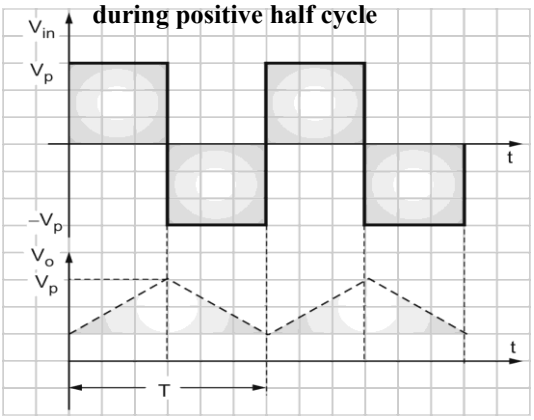
During negative half cycle

During negative half cycle, output is $V_{inv} > V_{ninv}$.

Hence diode 'D_1' is reverse biased and voltage across capacitor 'C' is retained. The only discharge path for 'C' is through 'R_L' since the bias current i_B is negligible.

- For proper operation of the circuit, the charging time constant (CR_f) and discharging time constant (CR_L) must satisfy the following conditions :

$$CR_f << \frac{T}{10} \text{ and } CR_L >> 10\ T$$



Where R_f is the forward resistance of the diode, R_L is the load resistance and T is the time period.

- The diode D_2 conducts during the negative half cycle of V_{in}, thus preventing the op-amp from going into saturation.

Fig. 3.2.15 : Input and output waveforms

SAMPLE-AND-HOLD

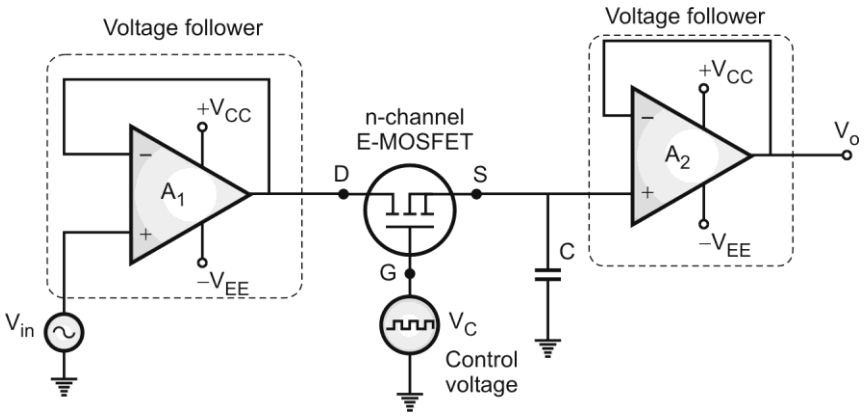
UQ. 3.3.1 Write short note on : Sample and hold circuit.

MU - Q. 6(4), Dec. 14, 5 Marks, Q. 6(B), Dec. 17, 10 Marks

The function of the sample-and-hold circuit is to sample an analog input signal and hold this value over a last sampled value until input is sampled again.

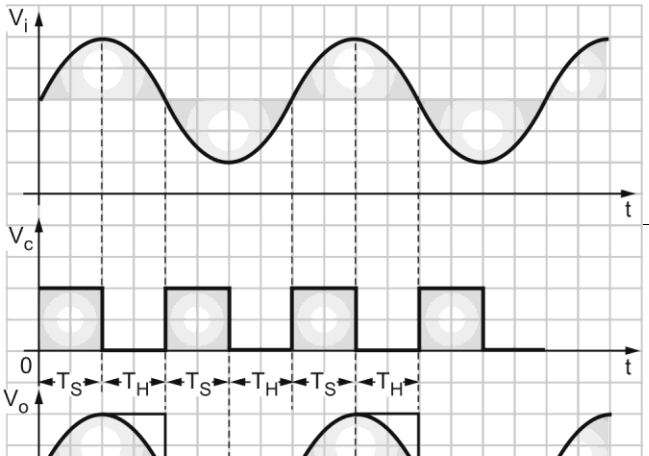
Circuit diagram of sample-and-hold is shown in Fig. 3.3.1.

- The n-channel E-MOSFET works as a switch and is controlled by the control voltage V_c.
- Capacitor 'C' stores the charge.
- The analog signal V_{in} to be sampled is applied to the drain of E-MSOFET and the control voltage V_c is applied to its gate.



(1C69)**Fig. 3.3.1 : Circuit diagram of sample-and-hold**

- When V_c is positive, the E-MOSFET turns 'ON' and the capacitor 'C' charges to the instantaneous value of V_{in}. Thus the input voltage V_{in} appears across the capacitor 'C' and then at the output through voltage follower A_2.
- During the time when control voltage V_c is zero, the E-MOSFET is OFF.
- The capacitor 'C' cannot discharge, due to the high input impedance of the voltage follower A_2. Capacitor 'C' holds the voltage across it.



- The time period T_S, the period during which voltage across the capacitor is equal to input voltage is called **'sample periods'**.
- The time period T_H of V_c during which the voltage across the capacitor is held constant is called **'hold period'**.
- The frequency of the control voltage should be kept higher than the input so as to retrieve the input from output waveform.
- The input and output waveforms for sample-and-hold circuit is shown in Fig. 3.3.2.

Fig. 3.3.2 : Input and output waveform

GQ. 3.3.2 State some applications of sample-and-hold circuit.

1. A/D converter
2. Digital interfacing
3. Pulse-amplitude detection
4. Switched capacitor filter
5. Analog de-multiplexers
6. Time interval measurements
7. Pulse-height to pulse-width conversion

What are the advantages of sample-and-hold circuit ?

- It reduces the cross-talk in the MUX.
- The primary use of the sample-and-hold circuit is to hold the sampled analog input voltage constant during the conversion time of A/D converter.
- In case of multichannel ADCs, synchronization can be achieved by sampling signals from all the channels at the same time.

SCHMITT TRIGGER CIRCUIT

Inverting Schmitt Trigger

Write short note on : Schmitt trigger. **MU - Q. 6(3), Dec. 14, 5 Marks**

With the help of a neat diagram, input and output waveforms and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expressions for the upper and lower threshold levels. Explain how these levels can be varied. **MU - Q. 3(a), May 17, 10 Marks, Q. 4(b), May 18, 10 Marks, Q. 2(a), May 19, 10 Marks**

UQ. 3.4.3 *Draw a neat circuit diagram and input-output waveforms of an inverting Schmitt trigger. Give the expressions for its threshold levels.* **MU - Q. 1(D), Dec. 17, 5 Marks**

- This circuit generates symmetric square wave output whenever any kind of signal is applied to its inverting terminal. Hence this circuit is also known as **Square wave converter.**
- Fig. 3.4.1 shows symmetric schmitt trigger circuit.
- In this circuit, input signal is applied to inverting terminal.
- Positive feedback is used, i.e., feedback network is applied between output terminal and non-inverting terminal of an OP-AMP.

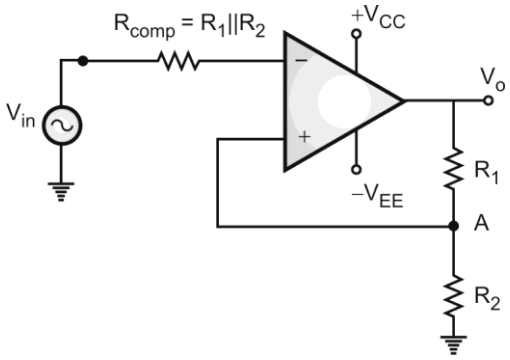


Fig. 3.4.1 : Circuit diagram of symmetric inverting schmitt trigger

- Due to positive feedback, voltage gain of this circuit is very large.
- Due to large voltage gain, input voltage V_{in} triggers the output voltage V_o to $+ V_{sat}$ or $- V_{sat}$ every time it exceeds certain voltage levels.
- These voltage levels are called 'upper threshold point voltage (V_{UTP})' and 'lower threshold point voltage (V_{LTP}).'
- Difference between these two threshold voltages is known as **hysteresis width**.
- These threshold voltages are obtained between resistances R_1 and R_2, i.e. point A.

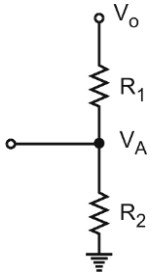


Fig. 3.4.2

- Due to positive feedback and high voltage gain, when output voltage $V_o = + V_{sat}$, the voltage at point 'A' is referred as V_{UTP} and it is given by,

$$V_A = V_o \left(\frac{R_2}{R_1 + R_2} \right) \text{ (Due to voltage divider network)}$$

where V_o is a total voltage, R_2 is the resistance connected to ground, V_A is the voltage across R_2

Since $V_o = + V_{sat}$; $\therefore \quad V_A = V_{UTP} = + V_{sat} \left(\frac{R_2}{R_1 + R_2} \right)$

Let $\beta = \frac{R_2}{R_1 + R_2}$; $\therefore \quad \mathbf{V_{UTP} = + V_{sat} \cdot \beta}$

Similarly when $V_o = - V_{sat}$, the voltage at point 'A' is referred as V_{LTP} and it is given by,

$$V_A = V_{LTP} = - V_{sat} \left(\frac{R_2}{R_1 + R_2} \right)$$

$$\therefore \mathbf{V_{LTP} = - V_{sat} \cdot \beta}$$

Hysteresis width V_H is given by,

$$V_H = V_{UTP} - V_{LTP} = +V_{sat} \cdot \beta - (-V_{sat} \cdot \beta)$$

$$\mathbf{V_H = 2\beta \cdot V_{sat}}$$

Fig. 3.4.3 shows the input and output waveforms for symmetric schmitt trigger.

✳ **Note :** Take alternate V_{UTP} and V_{LTP} points. V_o remains constant from one V_{UTP} to V_{LTP} pair.

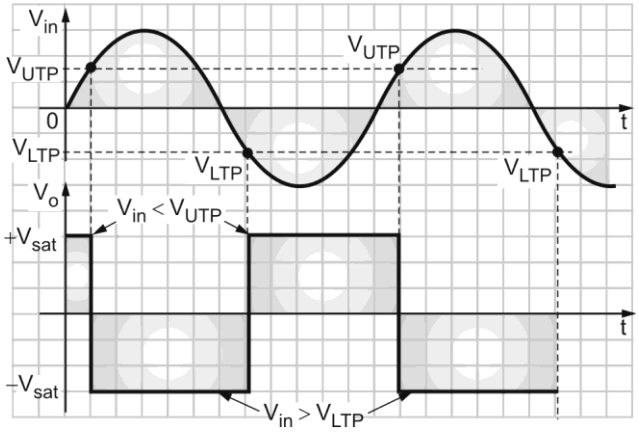


Fig. 3.4.3 : Input and Output waveforms for symmetric schmitt trigger

✳ **Note :** Here V_{in} is connected to inverting terminal and V_{ref}, i.e., V_{UTP}, or V_{LTP}, is connected to non-inverting terminal. So when $V_{inv} > V_{non\text{-}inv}$, then $V_o = -V_{sat}$ and when $V_{inv} < V_{non\text{-}inv}$, then $V_o = +V_{sat}$

– Hysteresis plot is plotted between output voltage V_o and input voltage V_{in}. V_o changes from $+V_{sat}$ to $-V_{sat}$ between V_{UTP} and V_{LTP}.

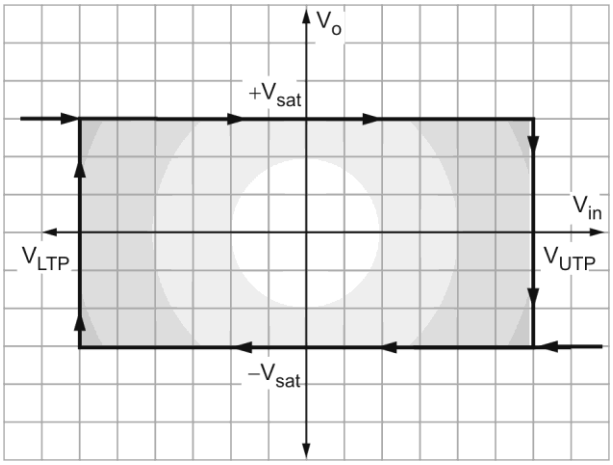


Fig. 3.4.4 : Hysteresis plot

Ex. 3.4.1

Design a symmetric schmitt trigger circuit if V_{UTP} = + 2V and V_{LTP} = – 2V. Draw output when + 10 V_{P-P} sine wave is applied.

☑ **Soln. :**

Given : $V_{UTP} = +2V, V_{LTP} = -2V$

Assume $\pm V_{CC} = \pm 12$ V

and $\pm V_{sat}$ = 90% of $V_{CC} = \frac{90}{100} \times 12 = 10.8$ V

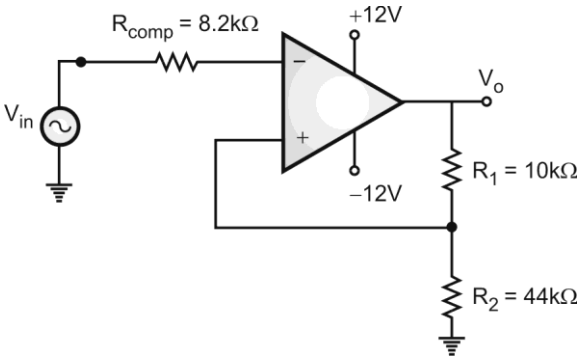
- **Step 1 :** We know,

$$V_{UTP} = +V_{sat} \times \beta \quad \ldots(1)$$

and $$\beta = \frac{R_2}{R_1 + R_2} \quad \ldots(2)$$

From Equation (1)

$$\beta = \frac{V_{UTP}}{+V_{sat}} = \frac{2}{10.8} \quad \therefore \beta = \mathbf{0.185}$$



(1C21)**Fig. Ex. 3.4.1 : Symmetric Schmitt trigger circuit with designed values**

- **Step 2**

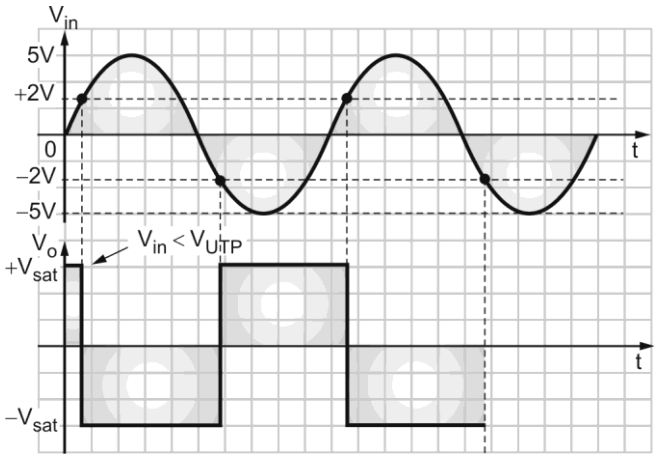
Let $R_2 = 10$ k $\qquad \beta = \frac{R_2}{R_1 + R_2}$

$$\therefore 0.185 = \frac{10}{R_1 + 10}$$

$$\therefore \mathbf{R_1 = 44\ k\Omega}$$

and $R_{comp} = R_1 \parallel R_2 = 44\text{ k} \parallel 10\text{ k}$

$$\mathbf{R_{comp} = 8.2\ k\ \Omega}$$



(1C22)**Fig. Ex. 3.4.1(a) : Input and output waveforms**

UEx. 3.4.2 **MU - Q. 3(a), Dec. 19, 10 Marks**

Design a Schmitt trigger circuit to convert 5V, 1kHz sinusoidal signal to square wave using 741IC, $V_{UT} = 0.8$ V, $V_{LT} = -0.8$ V and : $\pm V_{sat} \pm 11$ V. Draw its transfer characteristics, input and output waveforms.

☑ **Soln. :**

Given : $V_{UTP} = 0.8$ V, $V_{LTP} = -0.8$ V, $\pm V_{sat} = \pm 11$ V

- **Step 1 :** We know that

$$V_{UTP} = +V_{sat} \times \beta \quad \ldots(1) \quad \text{and} \quad \beta = \frac{R_2}{R_1 + R_2} \quad \ldots(2)$$

From Equation (1)

$$\beta = \frac{V_{UTP}}{+V_{sat}} = \frac{0.8}{11}$$

$$\therefore \beta = 0.072$$

- **Step 2 :** Let $R_2 = 10\ k\Omega$

$\therefore$ From Equation (2)

$$0.072 = \frac{10\ k}{R_1 + 10\ k}$$

$$\therefore 0.072\ R_1 + 0.072 \times 10\ k = 10\ k$$

$$\therefore R_1 = \frac{10\ k - 0.72\ k}{0.072}$$

$$\therefore R_1 = 128\ k\Omega$$

$$\text{And } R_{comp} = R_1 \,||\, R_2 = 10\ k \,||\, 128\ k$$

$$= \frac{10 \times 128}{10 + 128} = \frac{1280}{138}$$

$$\therefore R_{comp} = 9.27\ k\Omega$$

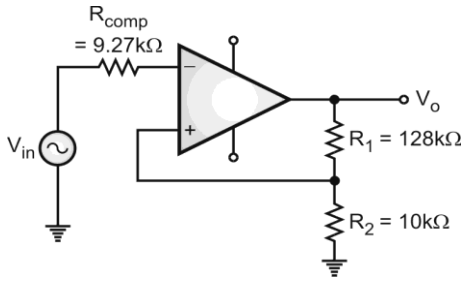


Fig. Ex. 3.4.2

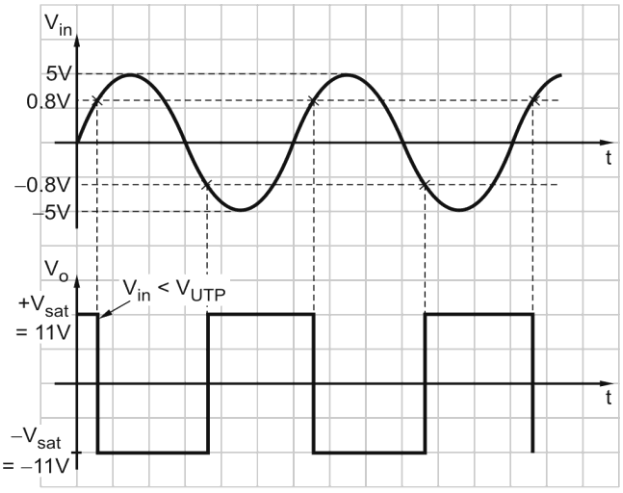


Fig. Ex. 3.4.2(a)

Explain with a neat circuit diagram, working of inverting asymmetric schmitt trigger with its input-output waveform and hysteresis plot.

- This circuit generates asymmetric square wave output whenever any kind of signal is applied to its inverting terminal. Hence this circuit is known as **Asymmetric schmitt trigger**. Fig. 3.4.5 shows asymmetric schmitt trigger circuit.
- In this circuit, input signal is applied to inverting terminal. Positive feedback, network is applied between output terminal and non-inverting terminal of an op-amp.
- Due to positive feedback, voltage gain is very large.
- Due to large voltage gain, input voltage V_{in} triggers the output voltage V_o to $+V_{sat}$ or $-V_{sat}$, every time it exceeds certain voltage levels.

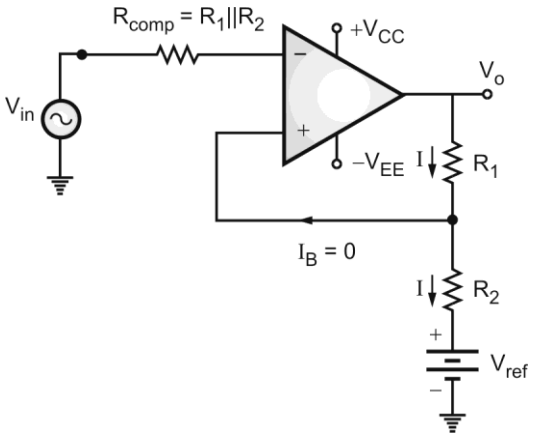


Fig. 3.4.5 : Circuit diagram of Asymmetric inverting schmitt trigger

- These voltage levels are called 'Upper Threshold Point Voltage (V_{UTP})' and 'Lower Threshold Point Voltage (V_{LTP}).'Difference between these two threshold voltages is known as **Hysteresis width**.
- In asymmetric schmitt trigger circuit d.c. voltage source is connected, i.e., V_{ref}, as shown in Fig. 3.4.5.
- These threshold voltages are obtained between resistances R_1 and R_2 at point A.
- Due to positive feedback and high voltage gain, when output voltage $V_o = +V_{sat}$, the voltage at point 'A' is referred as V_{UTP} and it is given by,

$$V_A = I \cdot R_2 + V_{ref} \qquad \text{but,} \quad I = \frac{V_o - V_{ref}}{R_1 + R_2} \quad \therefore \quad V_A = \left(\frac{V_o - V_{ref}}{R_1 + R_2} \right) \cdot R_2 + V_{ref}$$

$$V_A = V_{ref} + \left(\frac{R_2}{R_1 + R_2} \right) (V_o - V_{ref})$$

Let, $\beta = \dfrac{R_2}{R_1 + R_2}$

$\therefore \quad V_A = V_{ref} + \beta \cdot (V_o - V_{ref})$; At UTP, $V_A = V_{UTP}$ and $V_o = +V_{sat}$

$$\therefore \quad \mathbf{V_{UTP} = V_{ref} + \beta (V_{sat} - V_{ref})}$$

Similarly when $V_o = -V_{sat}$, the voltage at point 'A' is referred as V_{LTP} and it is given by,

$$\mathbf{V_A = V_{LTP} = V_{ref} + \beta (-V_{sat} - V_{ref})}$$

and $V_H = V_{UTP} - V_{LTP}$

$\therefore \quad V_H = [V_{ref} + \beta (V_{sat} - V_{ref})] - [V_{ref} + \beta (-V_{sat} - V_{ref})]$

$$V_H = V_{ref} + \beta V_{sat} - \beta V_{ref} - V_{ref} + \beta V_{sat} + \beta V_{ref}$$

$$\mathbf{V_H = 2 \beta V_{sat}}$$

Fig. 3.4.6 and Fig. 3.4.7 shows the input and output waveforms for two cases of asymmetric schmitt trigger.

Case 1 : Here $|V_{UTP}| \neq |V_{LTP}|$ and V_{UTP} is positive and V_{LTP} is negative

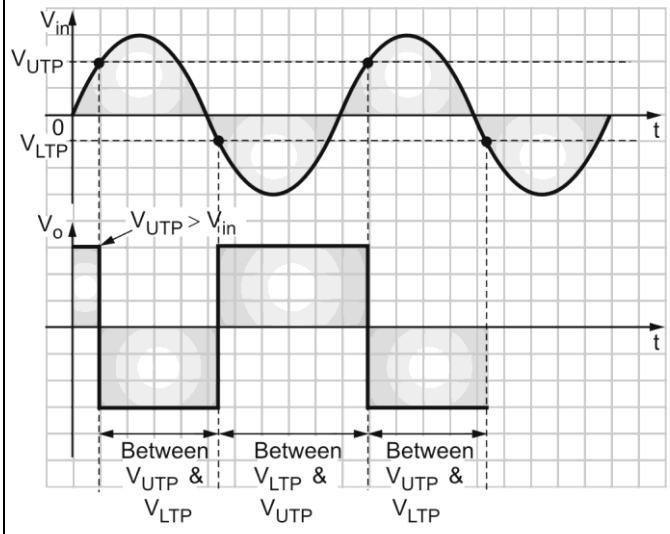


Fig. 3.4.6 : Input and output waveforms

Case 2 : Here $|V_{UTP}| \neq |V_{LTP}|$ and V_{UTP} and V_{LTP}, both are positive

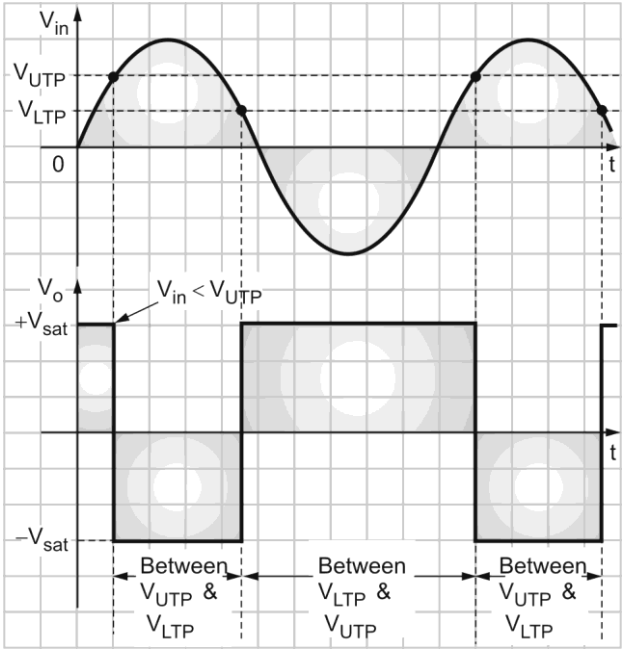


Fig. 3.4.7 : Input and output waveforms

Hysteresis loop for asymmetric schmitt trigger.

Case 1 : When V_{LTP} is negative and V_{UTP} is positive

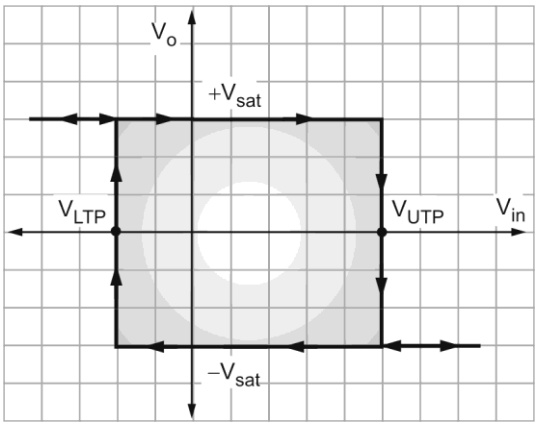


Fig. 3.4.8 : Hysteresis loop

Case 2 : When V_{LTP} and V_{UTP}, both are positive

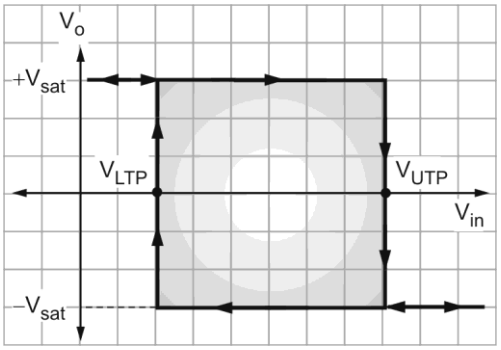


Fig. 3.4.9 : Hysteresis loop

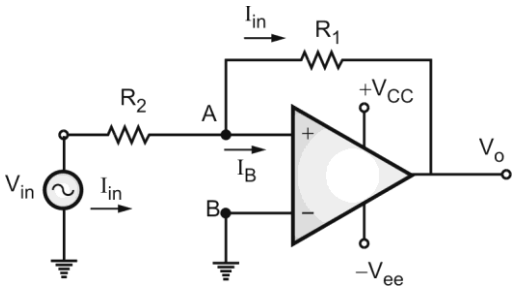
Non-Inverting Schmitt Trigger

UQ. 3.4.5 *With the help of a neat diagram and voltage transfer characteristics explain the working of a non-inverting Schmitt trigger. Derive the expression for the threshold levels and explain how they can be varied.*

MU - Q. 3(a), May 16, Q. 3(b), Dec. 16, Q. 4(a), Dec. 18, 10 Marks

Fig. 3.4.10 shows the non-inverting Schmitt trigger circuit.

- The input is applied to the non-inverting input terminal of the op-amp.



(2C6) **Fig. 3.4.10 : Non-inverting Schmitt trigger**

- In this circuit, positive feedback is used i.e. output is feedback to the non-inverting input terminal.
- Due to positive feedback, voltage gain is very large and output gets saturated.
- V_A is the voltage at point A.

$$V_A = I_{in} \cdot R_2 \qquad \ldots(3.4.1)$$

$A \rightarrow$ $I_B = 0$, I_{in} entirely passes through R_1.

$$\therefore I_{in} = \frac{V_o}{R_1} \qquad \ldots(3.4.2)$$

$\therefore$ Put Equation (3.4.2) in Equation (3.4.1)

$$V_A = \frac{V_o}{R_1} \cdot R_2$$

V_o is saturated to $+ V_{sat}$ and $- V_{sat}$, when $V_o = + V_{sat}$

$$V_{UTP} = \frac{R_2}{R_1} \quad (+ V_{sat})$$

$$\therefore \quad V_{UTP} = V_{sat} \left(\frac{R_2}{R_1}\right) \qquad \ldots(3.4.3)$$

where V_{UTP} is the upper threshold point voltage and when $V_o = - V_{sat}$ then

$$V_{LTP} = \frac{R_2}{R_1} \quad (- V_{sat})$$

$$\therefore \quad V_{LTP} = - V_{sat} \left(\frac{R_2}{R_1}\right) \qquad \ldots(3.4.4)$$

where V_{LTP} is the lower threshold point voltage.

Threshold levels can be varied by changing the values of resistors R_1 and R_2.

Hysteresis width is the difference between V_{UTP} and V_{LTP} and is denoted by H.

$$\therefore \quad H = V_{UTP} - V_{LTP} = 2\, V_{sat} \frac{R_2}{R_1}$$

– If the sinusoidal input is applied to the non-inverting Schmitt trigger circuit then the input and output waveforms can be shown as in Fig. 3.4.11.

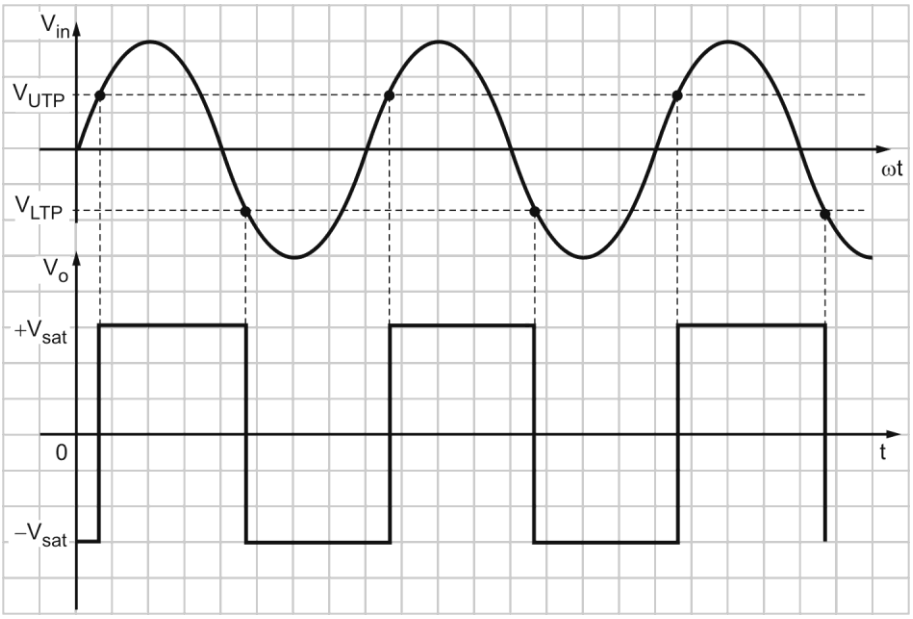
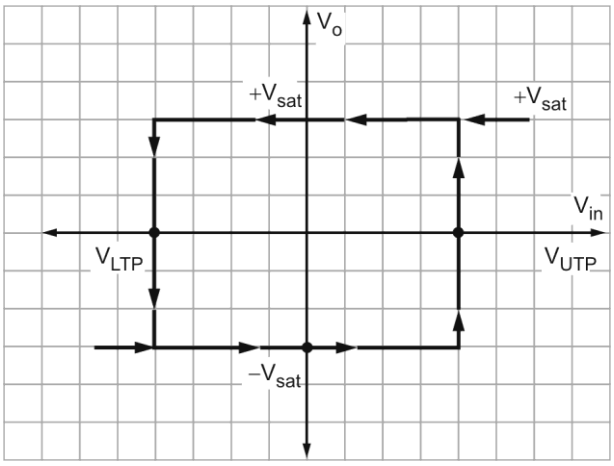


Fig. 3.4.11 : Input and output waveforms

– The transfer characteristic i.e. Hysteresis is shown in Fig. 3.4.12.

– When V_{in} is greater than V_{UTP} and V_{LTP} then V_o changes from $-V_{sat}$ to $+V_{sat}$.

– When V_{in} is less than V_{LTP} and V_{UTP} then V_o changes from $+V_{sat}$ to $-V_{sat}$.



(2C8)**Fig. 3.4.12 : Hysteresis (Transfer characteristics)**

- In this characteristics output continues in its + V_{sat} level unless and until the input becomes more negative than V_{LTP}.
- At lower threshold point, the output changes its state from positive saturation + V_{sat} to negative saturation – V_{sat}.
- It remains in negative saturation till V_{in} increases beyond its upper threshold level V_{UTP}.

Ex. 3.4.3

Design a schmitt trigger for V_{UTP} = 3V and V_{LTP} = – 2V with general purpose op-amp 741. Assume $V_{CC} = \pm$ 12 V. Draw detailed diagram with designed values.

☑ **Soln. :**

Given : $V_{UTP} = 3$ V and $V_{LTP} = -2$ V.

Since $V_{UTP} \neq V_{LTP}$, we will design asymmetric schmitt trigger circuit.

$V_{CC} = \pm 12$ V

$\therefore \quad V_{sat} = 90\%$ of V_{CC} ; $\qquad V_{sat} = \frac{90}{100} \times 12 = 10.8$ V

▸ **Step 1**

$V_H = V_{UTP} - V_{LTP} \qquad V_H = 3 - (-2) \qquad \mathbf{V_H = 5\ V}$

▸ **Step 2**

For asymmetric schmitt trigger circuit V_H is given by,

$V_H = 2\beta \cdot V_{sat} \qquad \therefore \quad \beta = \frac{V_H}{2 \cdot V_{sat}} = \frac{5}{2 \times 10.8} \qquad \therefore \quad \mathbf{\beta = 0.231}$

▸ **Step 3 : Calculate R_1 and R_2**

We know,

$$\beta = \frac{R_2}{R_1 + R_2}$$

Let $R_2 = 10\ k\Omega \qquad \therefore \quad 0.231 = \frac{10\ k}{R_1 + 10k}$

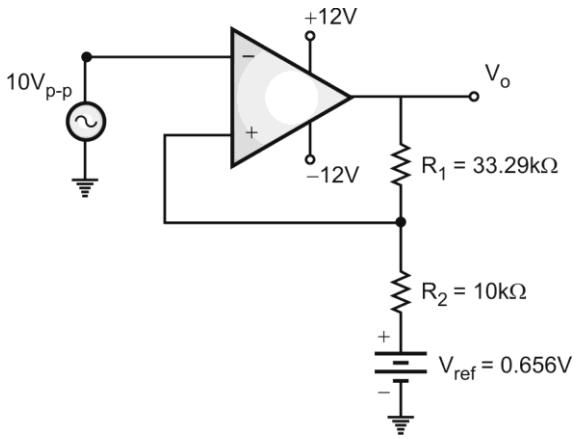
$\therefore \quad (R_1 + 10k)\ 0.231 = 10k$

$\therefore \quad 0.231\ R_1 + 10k \times 0.231 = 10k$

$0.231\ R_1 = 10k - 2.31\ k$

$0.231\ R_1 = 7.69\ k$

$\therefore \quad \mathbf{R_1 = 33.29\ k}$



(1C28) **Fig. Ex. 3.4.2 : Circuit diagram of asymmetric schmitt trigger with designed values**

- **Step 4 : Calculate V_{ref}**

$$V_{UTP} = V_{ref} + \beta (V_{sat} - V_{ref})$$

$$3 = V_{ref} + 0.231 (10.8 - V_{ref})$$

$$3 = V_{ref} + 0.231 \times 10.8 - 0.231 V_{ref}$$

$$0.769 V_{ref} = 0.505$$

$$\therefore \quad \mathbf{V_{ref} = 0.656\ V}$$

Comparison between Schmitt Trigger and Comparator

GQ. 3.4.6 Compare Schmitt trigger and comparator.

Sr. No.	Schmitt trigger	Comparator
1.	Positive feedback is used.	Feedback is not used.
2.	The op-amp is used in closed-loop mode.	Op-amp is used in open-loop mode.
3.	Input signal is compared with V_{UTP} or V_{LTP} obtained at other input terminal depending on output voltage, $+V_{sat}$ or $-V_{sat}$.	Input is compared with d.c. reference voltage applied to other input terminal.
4.	False triggering due to noise voltage is not possible because of feedback.	False triggering due to noise voltage is possible.
5.	Voltage gain is high, due to positive feedback.	Open loop voltage gain is very high, i.e., for 741 it is 2×10^5.
6.	Depending on input signal applied to inverting or non-inverting terminal, schmitt trigger can be used as inverting or non-inverting schmitt trigger.	Depending on input applied to inverting or non-inverting terminal, comparator can be used as inverting or non-inverting comparator.
7.	Applications of schmitt trigger are square wave converter, ON-OFF controllers.	Applications are zero-crossing detector, window detector.

WAVEFORM GENERATOR

3.5.1 Square Wave Generator

UQ. 3.5.1 *Draw the circuit diagram for a square waveform generator using op-amps. With the help of waveforms at suitable points in the circuit explain it's working. If the duty cycle is to be varied, what modification is required in the circuit. If the output of the square wave is to be clipped to ± V_X how is it obtained ?*

MU - Q. 3(b), Dec. 14, 10 Marks

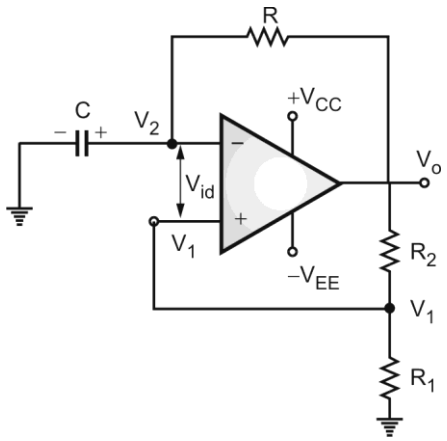
UQ. 3.5.2 *Draw the circuit diagram of a square waveform generator using op-amp. With the help of waveforms at suitable points in the circuit explain its working. Explain how duty cycle can be varied?*

MU - Q. 3(b), May 16, 10 Marks, Q. 3(b), May 17, 10 Marks, Q. 5(a), Dec. 18, 10 Marks

UQ. 3.5.3 *Draw the circuit diagram of a square waveform generator using op- amp and explain its working with the help of waveforms.*

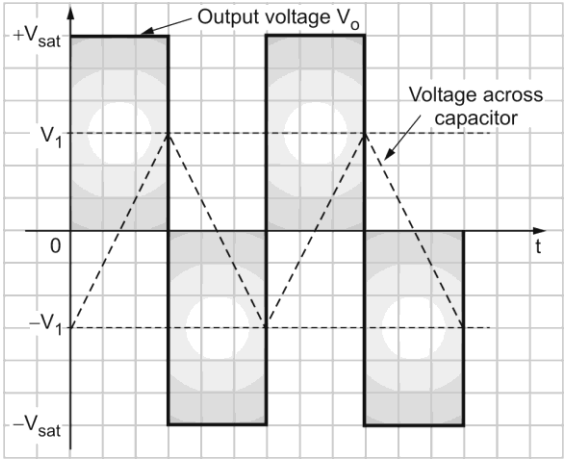
MU - Q. 5(a), May 18, 10 Marks, Q. 3(a), May 19, 10 Marks

- Square wave generator is also called **'free running'** or **'astable multivibrator'**.
- The output of the circuit is + V_{sat} or – V_{sat} depending on whether the differential input voltage 'V_{id}' between inverting and non-inverting terminal is negative or positive.
- Fig. 3.5.1 shows the circuit diagram of square wave generator and Fig. 3.5.2 shows the waveforms across capacitor C and at output.



(1C46) **Fig. 3.5.1 : Circuit diagram of square wave generator**

- Assume that the voltage across capacitor 'C' is zero at the instant d.c. supply voltages + V_{CC} and – V_{EE} are applied.
- This means voltage at inverting terminal $V_2 = 0$
- At the same time, voltage at non-inverting terminal is V_1, due to output-offset voltage, R_1 and R_2.
- Thus the differential input voltage 'V_{id}' is equal to V_1.
- Due to V_1, OP-AMP is driven to saturation and $V_o = + V_{sat}$.



– OP-AMP gain is high.

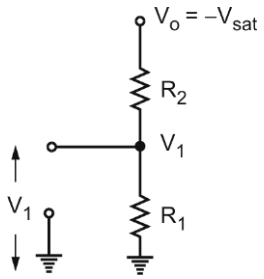
(1C47)**Fig. 3.5.2 : Output voltage waveform**

– With $V_o = + V_{sat}$, capacitor 'C' starts charging towards $+ V_{sat}$ through resistor 'R' as shown in Fig. 3.5.1.

– But as soon as the voltage V_2 across C is slightly more positive than V_1, the output of OP-AMP is forced to switch to a negative saturation, i.e., $– V_{sat}$.

– Voltage V_1 when $V_o = – V_{sat}$ is,

$$V_1 = \left(\frac{R_2}{R_1 + R_2}\right)(– V_{sat})$$



(1C48)**Fig. 3.5.3**

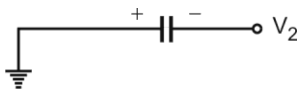
Using voltage divider network, in Fig. 3.5.3.

$R_1 \rightarrow$ Resistor connected to ground

$– V_{sat} \rightarrow$ Total voltage

$R_1 + R_2 \rightarrow$ Total resistance

– Capacitor C discharges and recharges with opposite polarity as shown in Fig. 3.5.4.



(1C49)**Fig. 3.5.4**

– When capacitor voltage becomes more than $– V_1$, the differential voltage V_{id} becomes positive and it drives the output V_o to $+ V_{sat}$. This completes one cycle.

When $V_o = + V_{sat}$, $V_1 = \left(\frac{R_2}{R_1 + R_2}\right)(+ V_{sat})$

The time period of the output waveform is given by,

$$T = \frac{1}{f} = 2\,RC\,ln\left(\frac{1 + \beta}{1 – \beta}\right)$$ where β is feedback factor

$$\beta = \frac{R_1}{R_1 + R_2} \qquad T = 2RC\,ln\left(\frac{R_2 + 2\,R_1}{R_2}\right)$$

and frequency of the output,

$$f_o = \frac{1}{2\,RC\,ln\left[\frac{(R_2 + 2R_1)}{R_2}\right]}$$

– f_o is not only a function of RC time constant but also of the relationship between R_1 and R_2

If $R_2 = 1.16\,R_1$, then $f_o = \frac{1}{2RC}$

i.e., smaller the time constant RC, higher is the output frequency of the square wave generator circuit.

Ex. 3.5.1

Design square wave generator to generate a perfect square wave of 50% duty cycle with an output frequency of

1 kHz. Assume the feedback factor to be 0.1. Also draw the output waveform and waveform across the capacitor using op-amp.

☑ **Soln. :**

Given : f = 1 kHz, $\beta = 0.1$

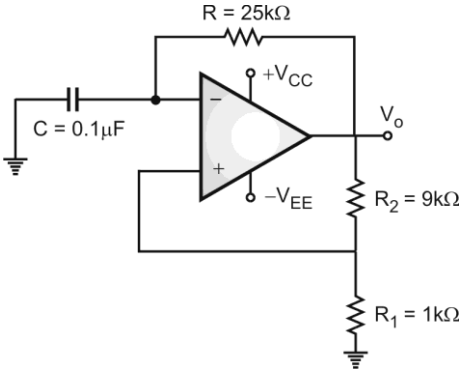


Fig. Ex. 3.5.1 : Circuit diagram of square wave generator with designed values

▶ **Step 1**

$$\text{we know} \quad \beta = \frac{R_1}{R_1 + R_2}$$

$$\text{Let} \quad R_1 = 1\text{k}\Omega$$

$$\therefore \quad \beta = \frac{1000}{R_2 + 1000} = 0.1$$

$$\therefore \quad R_2 = 9\ \text{k}\Omega$$

The frequency of oscillations is given as,

$$T = \frac{1}{f} = 2\,RC\,ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\therefore \quad T = \frac{1}{f} = \frac{1}{1000} = 1\ \text{ms}$$

$$1 \times 10^{-3} = 2\,RC\,ln\left(\frac{1+0.1}{1-0.1}\right)$$

$$\therefore \quad RC = \frac{1 \times 10^{-3}}{2 \times 0.20}$$

$$\text{Let} \quad C = 0.1\ \mu\text{F}$$

$$\therefore \quad R = 25\ \text{k}\Omega$$

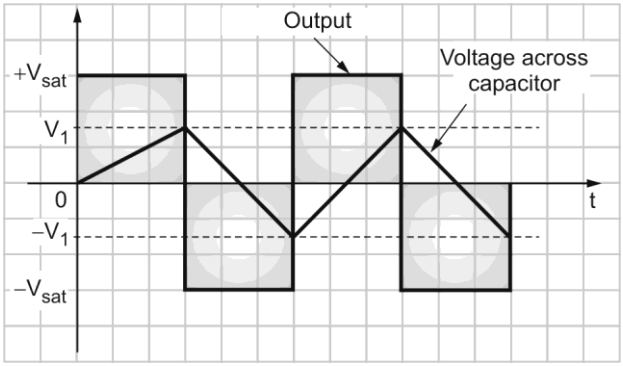


Fig. Ex. 3.5.1(a) : Output waveform and voltage across capacitor C

Ex. 3.5.2

Design the square wave generator so that f_0 = 1kHz. The op-amp is 741 with dc supply voltages = ± 15V.

☑ **Soln. :**

Use $R_2 = 1.16\ R_1$ assumption so that simplified frequency equation can be used

$$\text{i.e.} \quad f_o = \frac{1}{2\,RC}$$

Let $\mathbf{R_1 = 10\ k\Omega}$, then $R_2 = 1.16 \times 10\ \text{k}\Omega$

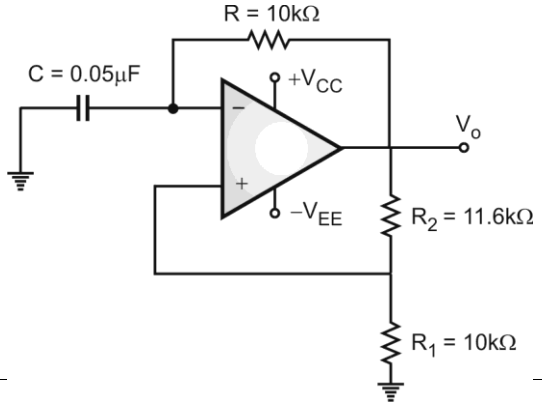
$\mathbf{R_2 = 11.6\ k\Omega}$

also we know,

$$f_o = \frac{1}{2\,RC}$$

Let $\mathbf{C = 0.05\ \mu F}$

$$R = \frac{1}{2\,f_o\,C} = \frac{1}{2 \times (1 \times 10^3)\,(0.05 \times 10^{-6})}$$



$\therefore$ **R = 10 kΩ**

(1C52)**Fig. Ex. 3.5.2 : Square wave generator with designed values**

Syllabus Covered

Triangular Wave Generator and Ex. 3.5.3

3.5.2 Triangular Wave Generator

UQ. 3.5.4 *Draw the circuit diagram for a triangular waveform generator using op-amps. With the help of waveforms at suitable points in the circuit explain it's working. If the duty cycle is to be varied, what modification is required in the circuit. If the output of the square wave is to be clipped to ± V_X how is it obtained ?*

MU - Q. 3(b), Dec. 14, 10 Marks

UQ. 3.5.5 *Draw the circuit diagram of a triangular waveform generator using op-amp. With the help of waveforms at suitable points in the circuit explain its working. Explain how duty cycle can be varied?*

MU - Q. 3(b), May 16, 10 Marks, Q. 3(b), May 17, 10 Marks, Q. 5(a), Dec. 18, 10 Marks

UQ. 3.5.6 *Draw the circuit diagram of a triangular waveform generator using op- amp and explain its working with the help of waveforms.*

MU - Q. 5(a), May 18, 10 Marks, Q. 3(a), May 19, 10 Marks

UQ. 3.5.7 *Write short note on : Triangular wave generator.* **MU - Q. 6(e), Dec. 15, 4 Marks**

Method I

- When square wave is given to the input of integrator, we get triangular wave at its output.
- So we can design triangular wave generator by using square wave generator and the output of square wave generator is given to the input of integrator.
- Thus at the output of integrator, we get triangular wave as shown in Fig. 3.5.5.
- It consists of two circuits :
  - (i) Square wave generator circuit and
  - (ii) Integrator circuit

The frequency of triangular wave is same as frequency of square wave and is given by :

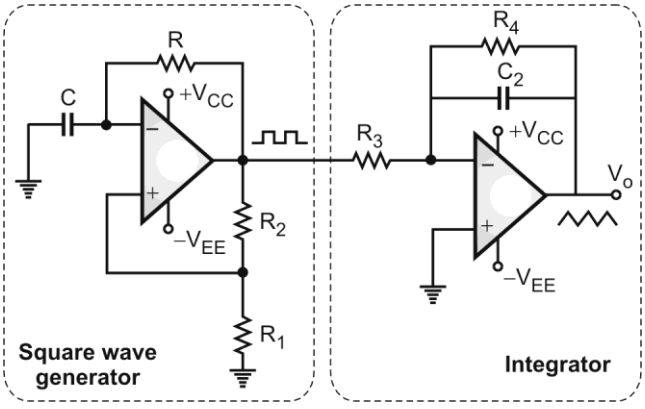


Fig. 3.5.5 : Circuit diagram of triangular wave generator (Method I)

$$T = \frac{1}{f} = 2\,RC\,ln\left(\frac{1+\beta}{1-\beta}\right) \qquad \ldots(3.5.1)$$

where $\beta = \frac{R_1}{R_1 + R_2}$

By putting the value of β in Equation (3.5.1),

$$T = \frac{1}{f} = 2\,RC\,ln\left(\frac{R_2 + 2R_1}{R_2}\right)$$

or $$f = \frac{1}{2\,RC\,ln\left(\frac{R_2 + 2R_1}{R_2}\right)}$$

When, $R_1 = R_2$ and $\beta = 0.5$, then $T = \frac{1}{f} = 2\,RC\,ln\,(3)$ or $f = \frac{1}{2\,RC\,ln\,(3)}$

When $R_1 = 1.16\,R_2$ then $T = \frac{1}{f} = 2\,RC$ and $f = \frac{1}{2\,RC}$

Drawback of method I

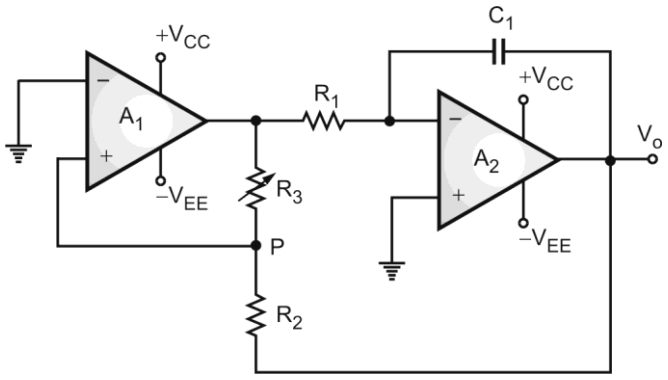
In this circuit, we need two op-amp, two capacitors, and at least five resistors. Thus circuit becomes more bulky due to more number of components.

- **Method II**

Advantage of method II

- This circuit uses few components, as compared to method I.
- This circuit consists of two parts :

  (i) Comparator and (ii) Integrator
- The comparator A_1 compares the voltage at point P, i.e., non-inverting input continuously with the inverting input that is 0V. When the voltage at P, i.e., non-inverting input goes slightly below or above 0V, the output of A_1 is at the negative or positive saturation, i.e., V_{sat} or + V_{sat}.
- When the voltage V_P goes above zero reference level, the output of A_1 will switch to + V_{sat}.



(1C55)**Fig. 3.5.6 : Circuit diagram of triangular wave generator (method II)**

- Now due to positive input given to integrator, the output of A_2 generates a negative going ramp.
- This negative going ramp is connected to resistance R_2 and hence the voltage at 'P' becomes negative, i.e., non-inverting terminal becomes negative.
- Due to negative voltage at non-inverting terminal, the output of A_1 becomes – V_{sat}.

- Due to negative input voltage, output of A_2 will now generate a positive going ramp.
- Again when the voltage at 'P' becomes slightly more than zero, output of A_1 will switch to $+ V_{sat}$.
- This cycle repeats to generate square wave at the output of A_1 and triangular wave at the output of A_2.
- The amplitude of square wave is $\pm V_{sat}$.
- The amplitude of triangular wave is : $V_{o\,(P-P)} = + V_{Ramp} - (- V_{Ramp})$
- $+ V_{Ramp}$, the output of A_2 at which the output of A_1 switches from $- V_{sat}$ to $+ V_{sat}$ is given by,

$$+ V_{Ramp} = \frac{- R_2}{R_3} (- V_{sat})$$

Similarly, $- V_{Ramp} = \frac{- R_2}{R_3} (+ V_{sat})$; $\therefore \quad V_{o\,(p-p)} = (2)\left(\frac{R_2}{R_3}\right) (V_{sat})$

and $T = (2 R_1 C_1) \frac{V_{o\,(P-P)}}{V_{sat}}$; $\therefore \quad T = \frac{4 R_1 C_1 R_2}{R_3}$

and frequency of oscillator is,

$$\mathbf{f_o = \frac{R_3}{4 R_1 C_1 R_2}}$$ f_o increases with increase in R_3.

Ex. 3.5.3

Design the triangular wave generator of method II, so that f_o = 2KHz and $V_{o\,(P-P)} = 7$ V. $\pm V_{CC} = 15$ V.

☑ **Soln. :**

▶ **Step 1**

$V_{o\,(P-P)} = (2) \frac{R_2}{R_3} (V_{sat})$; $V_{sat} = 90\%$ of $V_{CC} = \frac{90}{100} \times 15 = 13.5$ $\therefore \quad V_{sat} = 13.5$ V

$\frac{R_2}{R_3} = \frac{V_{o\,(P-P)}}{2 \times (V_{sat})}$; $\frac{R_2}{R_3} = \frac{7}{(2)(13.5)}$ $\therefore \quad R_2 = \left(\frac{7}{27}\right) R_3$

Let **$R_2 = 10$ kΩ ;** **$\therefore \quad R_3 = 38.57$ kΩ [Use pot. of 50 kΩ]**

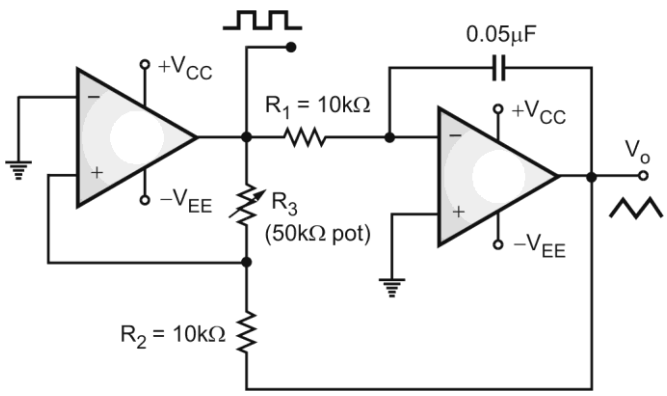
▶ **Step 2**

$$f_o = \frac{R_3}{4 R_1 C_1 R_2}$$

$$2 \times 10^3 = \frac{38.57 \times 10^3}{(4)(R_1 C_1) \cdot (10 \times 10)^3}$$

$$\therefore \quad R_1 C_1 = \frac{38.57 \times 10^3}{(4)(2 \times 10^3)(10 \times 10^3)}$$

$$= 0.48$$



Let $C_1 = 0.05\ \mu F$ then

$R_1 = 10\ k\Omega$

(1C56)**Fig. Ex. 3.5.3 : Circuit diagram of triangular wave generator with designed values**

Thus **$R_1 = R_2 = 10\ k\Omega$, $C_1 = 0.05\ \mu F$ and $R_3 = 38.57\ k\Omega$**

PRECISION RECTIFIER

GQ. 3.6.1 What is the need of precision rectifier ?

UQ. 3.6.2 Write short note on : Precision rectifier. **MU - Q. 6(2), Dec. 14, Q. 6(c), Dec. 19, 5 Marks**

UQ. 3.6.3 What is a precision rectifier ? **MU - Q. 2(a), Dec. 15, Q. 5(a), Dec. 16, 2 Marks**

Precision rectifier is capable to rectify input voltage even if it is less than cut-in voltage of diode; i.e., it rectifies all the range of input voltages including voltages below cut-in voltage of diode.

Unlike p-n junction diode, which remains in off state for the voltages below its cut-in-voltage p-n junction rectifies input voltages, which are above cut-in voltage.

UQ. 3.6.4 Write the advantages of precision rectifier.

MU - Q. 3(b), May 15, 5 Marks

The advantages of precision rectifiers are :

1. It rectifies very small voltages which are less than the diode forward voltage of 0.7 V
2. It has low output impedance.
3. There is no diode forward voltage drop of 0.7 V between input and output voltage.

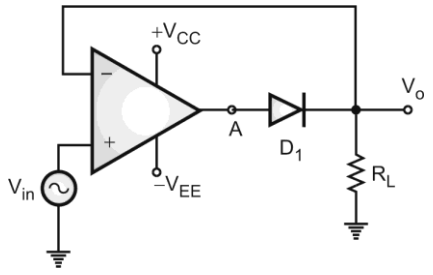
Half Wave Precision Rectifier

Explain half wave precision rectifier along with neat waveforms.

MU - Q. 3(b), May 15, 5 Marks

– Half wave precision rectifier rectifies the half wave of input, which is below cut-in voltage of diode.

– Circuit diagram is shown in Fig. 3.6.1.



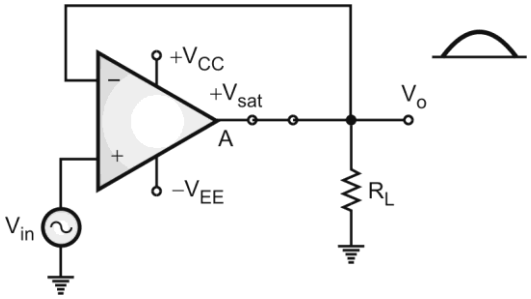
(1C57)**Fig. 3.6.1 : Circuit diagram of half wave precision rectifier**

During positive half cycle

Output is initially zero.

i.e., $V_{inv} = 0$ and when small positive input voltage is applied at non-inverting terminal of op-amp, then $V_{Ninv} > V_{inv}$.

- Output of oP-amp at point of A becomes + V_{sat}.
- Anode of diode D_1 has + V_{sat} voltage and cathode of diode D_1 has 0 voltage. Thus diode becomes forward biased. Circuit behaves as voltage follower.



(1C58)**Fig. 3.6.2 : Voltage follower circuit during positive half cycle**

- Due to voltage follower, output is equal to input because voltage gain of voltage follower is 1, i.e.,

$$A_V = \frac{V_o}{V_{in}} = 1 \quad \therefore V_o = V_{in}.$$

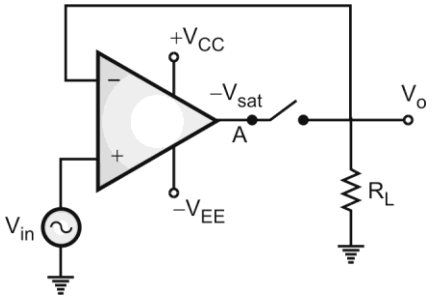
- Thus the entire positive cycle is obtained at the output of the circuit.

During negative half cycle

Output is initially zero.

i.e., $V_{inv} = 0$ and when small negative voltage is applied at non-inverting terminal of op-amp, then $V_{inv} > V_{ninv}$.

- Output of op-amp becomes – V_{sat} .



(1C59)**Fig. 3.6.3 : Open loop circuit during negative half cycle**

- Now anode of diode has – V_{sat} and its cathode is at zero potential and thus diode becomes reverse biased.
- Due to open circuit diode, the output is zero during entire negative cycle. Thus we get only positive half cycle at the output.

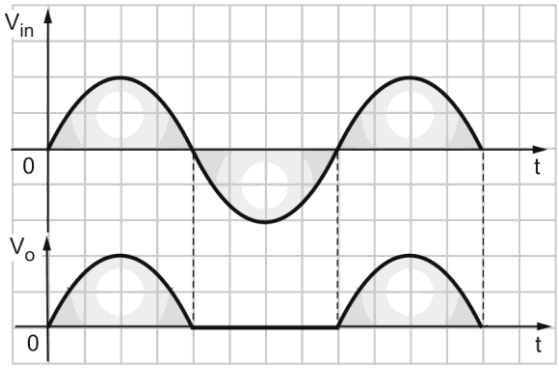


Fig. 3.6.4 : Input and output waveforms

Full Wave Precision Rectifier

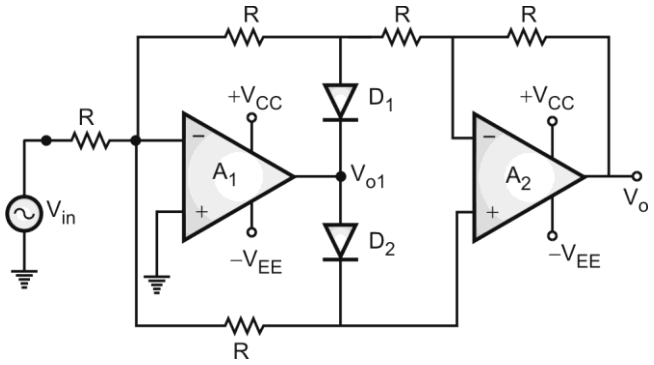
UQ. 3.6.6 *Draw the diagram for a full wave precision rectifier. With the help of waveforms at different points in the circuit explain its working.* **MU - Q. 2(a), Dec. 15, 8 Marks**

UQ. 3.6.7 *Explain working of full wave precision rectifier with the help of neat diagram and waveforms.* **MU - Q. 5(a), Dec. 16, 8 Marks**

In precision full wave rectifier, we get the output voltage for both the cycles. The circuit diagram of full wave precision rectifier is shown in Fig. 3.6.5.

- It consists of two op-amps, A_1 and A_2.

(Refer Fig. 3.6.5)



(1C61)**Fig. 3.6.5 : Circuit diagram of full wave precision rectifier**

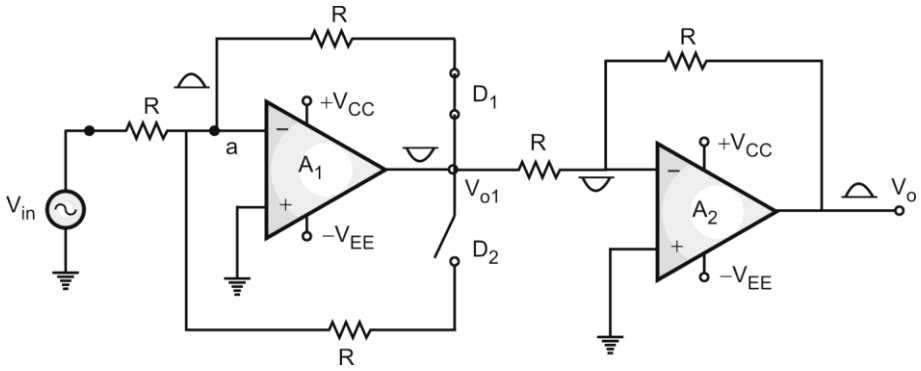
During positive half cycle

- For positive half cycle, $V_{ninv} = 0$, $V_{inv} > 0$.

  Since, $V_{inv} > V_{ninv}$, $V_{o1} = -V_{sat}$

- Diode D_1 is ON, i.e., forward biased and diode D_2 is OFF, i.e., reverse biased.

- For positive half cycle, equivalent circuit is shown in Fig. 3.6.6.



(1C62)**Fig. 3.6.6 : Equivalent circuit when $V_{in} > 0$, i.e., during positive half cycle**

- Both the op-amps A_1 and A_2 operate as inverting amplifiers. It can be seen that,

$$V_{o1} = -\frac{R_f}{R_i}(V_{in}) = -\frac{\cancel{R}}{\cancel{R}}(V_{in}) = -V_{in} \quad \text{and} \quad V_o = -\frac{\cancel{R}}{\cancel{R}}(-V_{o1}); \quad V_o = -(V_{in}) = V_{in}$$

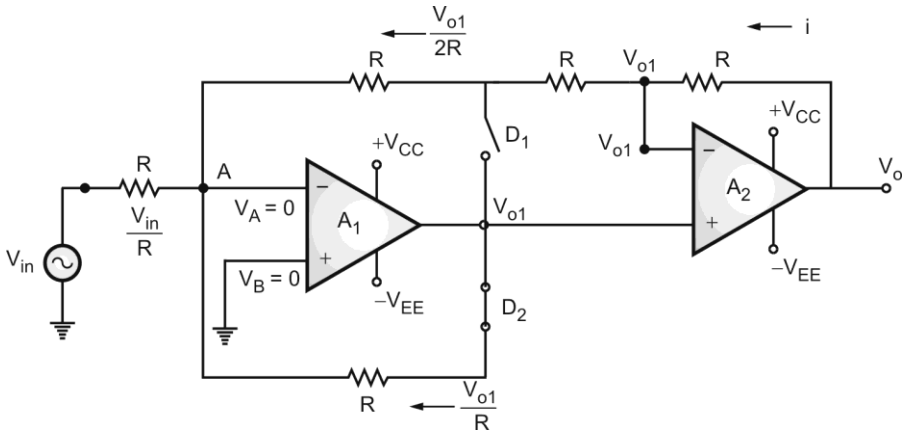
- So for positive half cycle we get, $\mathbf{V_o = V_{in}}$

For negative half cycle

- During negative half cycle, $V_{inv} < 0$ and $V_{ninv} = 0$, $\therefore V_{o1} = +V_{sat}$.

- D_1 is OFF, i.e., reverse biased and D_2 is ON, i.e., forward biased.

- For negative half cycle, equivalent circuit is shown in Fig. 3.6.7.



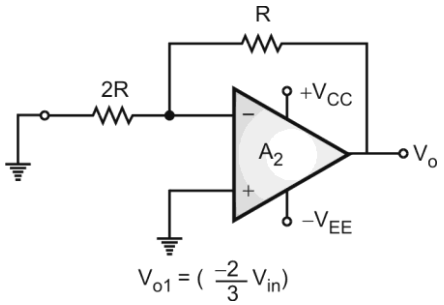
(1C63)**Fig. 3.6.7 : Equivalent circuit when $V_{in} < 0$, i.e., for negative half cycle**

$V_A = V_B \rightarrow$[Due to virtual ground concept]

Apply KCL at node 'A', $\frac{V_{in}}{R} + \frac{V_{o1}}{2R} + \frac{V_{o1}}{R} = 0$

$$\frac{3\,V_{o1}}{2R} = -\frac{V_{in}}{R} \qquad \therefore \mathbf{V_{o1} = -\frac{2}{3}\,V_{in}}$$

The equivalent circuit during negative half cycle is a non-inverting amplifier as shown in Fig. 3.6.8.



(1C64)**Fig. 3.6.8**

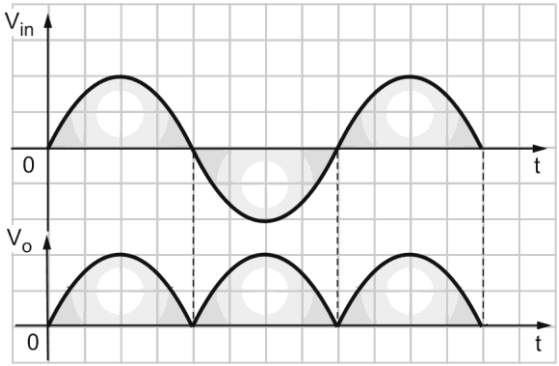
– For non-inverting amplifier,

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_{in} \qquad \therefore V_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} V_{in}\right)$$

$$\therefore V_o = \left(1 + \frac{1}{2}\right)\left(-\frac{2}{3} V_{in}\right) \qquad \therefore V_o = (1.5)\left(-\frac{2}{3} V_{in}\right)$$

$$\therefore \mathbf{V_o = -V_{in}}$$

– Hence during negative half cycle also, we get positive output equal to V_{in}.



(1C65)**Fig. 3.6.9 : Input and output waveforms**

How precision rectifiers are different than simple diode rectifiers.

MU - Q. 1(a), May 18, 5 Marks, Q. 1(B), Dec. 17, 5 Marks

What is the difference between ordinary rectifier and precision rectifier ?

MU - Q. 1(c), Dec. 14, 5 Marks

1. Precision rectifier can rectify the signal of order of mV. i.e. it can rectify the signal below 0.6 V, whereas simple diode rectifiers can rectify the signal after 0.6 V.

2. Precision rectifier consists of op-amp and diode whereas simple diode rectifier consists of ordinary diode.
3. Precision rectifier do not use transformer whereas simple diode rectifier uses transformer at input side in order to step up or step down the voltage.
4. Precision rectifier is more stable than simple rectifier.
5. Precision rectifier has good efficiency as compared to simple rectifiers.
6. Precision rectifier is useful for high precision signal processing whereas simple rectifiers are used in power supply for radio, television and computer.

UNIVERSITY QUESTIONS AND ANSWERS

✳ Dec. 2019

Q. 3.1 If the input to the ideal comparator shown in Fig. Q. 3.1 is a sinusoidal signal of 8 volt peak to peak without any DC component, then the duty cycle of the output comparator is _____. Justify.
i) 33.33% ii) 25% iii) 20% iv) None of these.

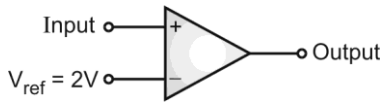


Fig. Q. 3.1

(Ans. : Refer UEx. 3.2.1) **(Q. 1(b), 5 Marks)**

Q. 3.2 Design a Schmitt trigger circuit to convert 5V, 1kHz sinusoidal signal to square wave using 741IC, V_{UT} = 0.8 V, V_{LT} = − 0.8 V and : ± V_{sat} ± 11 V. Draw its transfer characteristics, input and output waveforms. *(Ans. : Refer UEx. 3.4.2)* **(Q. 3(a), 10 Marks)**

Q. 3.3 Short note on : Precision rectifiers *(Ans. : Refer Section 3.6)* **(Q. 6(c), 4 Marks)**

✳ May 2019

Q. 3.4 Explain op-amp as window detector. *(Ans. : Refer Section 3.2.2(B))* **(Q. 1(e), 5 Marks)**

Q. 3.5 With the help of a neat diagram and voltage transfer characteristics, explain the working of an inverting schmitt trigger. Derive the expressions for its threshold levels.
(Ans. : Refer Section 3.4.1) **(Q. 2(a), 10 Marks)**

Q. 3.6 Draw the circuit diagram of a square and triangular waveform generator using op- amp and explain its working with the help of waveforms. *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 3(a), 10 Marks)**

Q. 3.7 Short note on : Peak detector circuit. *(Ans. : Refer Section 3.2.2(C))* **(Q. 6(d), 5 Marks)**

✳ Dec. 2018

Q. 3.8 With neat circuit explain the working of comparator circuit.
(Ans. : Refer Section 3.2) **(Q. 1(a), 5 Marks)**

Q. 3.9 With the help of a neat diagram, input and output waveforms and voltage transfer characteristics explain the working of non-inverting Schmitt trigger. Derive the expressions for its threshold levels. Explain how these levels can be varied? *(Ans. : Refer Section 3.4.2)* **(Q. 4(a), 10 Marks)**

Q. 3.10 Draw the circuit diagram of a square and triangular waveform generator using op-amp. With the help of waveforms at suitable points in the circuit explain its working. Explain how duty cycle can be varied? *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 5(a), 10 Marks)**

✳ May 2018

Q. 3.11 How precision rectifiers are different than simple diode rectifiers ?
(Ans. : Refer Section 3.6.2) **(Q. 1(a), 5 Marks)**

Q. 3.12 With the help of a neat diagram and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expressions for its threshold levels.
(Ans. : Refer Section 3.4.1) **(Q. 4(b), 10 Marks)**

Q. 3.13 Draw the circuit diagram of a square and triangular waveform generator using op-amp and explain its working with the help of waveforms. *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 5(a), 10 Marks)**

Q. 3.14 Short note on : Sample and hold circuit. *(Ans. : Refer Section 3.3)* **(Q. 6(a), 5 Marks)**

✳ Dec. 2017

Q. 3.15 How does precision rectifier differ from conventional rectifier?
(Ans. : Refer Section 3.6.2) **(Q. 1(B), 5 Marks)**

Q. 3.16 Draw a neat circuit diagram and input-output waveforms of an inverting Schmitt trigger. Give the expressions for its threshold levels. *(Ans. : Refer Section 3.4.1)* **(Q. 1(D), 5 Marks)**

Q. 3.17 If the input to the ideal comparator shown in the Fig. Q. 3.17 is a sinusoidal signal of 8 volt peak to peak without any DC component, then check whether the duty cycle of the output of comparator is 33.33 % or 25 % or 20 %. Prove it. *(Ans. : Refer UEx. 3.2.1)* **(Q. 1(E), 5 Marks)**

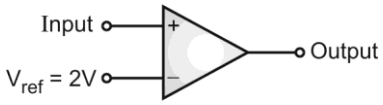


Fig. Q. 3.17

Q. 3.18 Write short note : Sample and Hold Circuit. *(Ans. : Refer Section 3.3)* **(Q. 6(B), 10 Marks)**

✳ May 2017

Q. 3.19 With the help of a neat diagram, input and output waveforms and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expressions for the upper and lower threshold levels. Explain how these levels can be varied.
(Ans. : Refer Section 3.4.1) **(Q. 3(a), 10 Marks)**

Q. 3.20 With the help of a neat diagram and waveforms at appropriate points in the circuit explain the working of a square and triangular waveform generator using op-amps. Explain how the duty cycle of the square and triangular waveforms can be varied. *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 3(b), 10 Marks)**

✳ Dec. 2016

Q. 3.21 Explain working of peak detector. *(Ans. : Refer Section 3.2.2(C))* **(Q. 1(e), 4 Marks)**

Q. 3.22 With the help of a neat diagram, input and output waveforms and voltage transfer characteristics explain the working of non inverting Schmitt trigger. Derive the expressions for the upper and lower threshold levels. Explain how these levels can be varied.
(Ans. : Refer Section 3.4.2) **(Q. 3(b), 10 Marks)**

Q. 3.23 What is precision rectifier ? Explain working of full wave precision rectifier with the help of neat diagram and waveforms. *(Ans. : Refer Sections 3.6 and 3.6.2)* **(Q. 5(a), 10 Marks)**

Q. 3.24 Write short note on : Window detector. *(Ans. : Refer Section 3.2.2(B))* **(Q. 6(a), 4 Marks)**

✳ May 2016

Q. 3.25 Differentiate between inverting and non-inverting comparators.
(Ans. : Refer Section 3.2.1) **(Q. 1(c), 4 Marks)**

Q. 3.26 With the help of a neat diagram and voltage transfer characteristics explain the working of a non-inverting Schmitt trigger. Derive the expressions for the threshold levels and explain how they can be varied. *(Ans. : Refer Section 3.4.2)* **(Q. 3(a), 10 Marks)**

Q. 3.27 Draw the circuit diagram for a square and triangular waveform generator using operational amplifiers. With the help of waveforms at suitable points in the circuit explain its working. Explain how the duty cycle can be varied. *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 3(b), 10 Marks)**

✳ Dec. 2015

Q. 3.28 What is a precision rectifier ? Draw the diagram for a full wave precision rectifier. With the help of waveforms at different points in the circuit explain its working.
(Ans. : Refer Sections 3.6 and 3.6.2) **(Q. 2(a), 10 Marks)**

Q. 3.29 Write short note on : Triangular wave generator. *(Ans. : Refer Section 3.5.2)* **(Q. 6(e), 4 Marks)**

✳ May 2015

Q. 3.30 Design triangular waveform generator for frequency for 5 kHz and V_{opp} = 6 V using op-amp.
(Ans. : Similar to Ex. 3.5.3) **(Q. 2(a), 10 Marks)**

Q. 3.31 Write the advantages of precision rectifier. Explain half wave precision rectifier along with neat waveforms. *(Ans. : Refer Sections 3.6 and 3.6.1)* **(Q. 3(b), 10 Marks)**

Q. 3.32 Explain zero crossing detector with neat diagram.
(Ans. : Refer Section 3.2.2(A)) **(Q. 4(c), 4 Marks)**

✳ Dec. 2014

Q. 3.33 What is the difference between ordinary rectifier and precision rectifier ?
(Ans. : Refer Section 3.6.2) **(Q. 1(c), 4 Marks)**

Q. 3.34 Draw the circuit diagram for a square and triangular waveform generator using op-amps. With the help of waveforms at suitable points in the circuit explain it's working. If the duty cycle is to be varied, what modification is required in the circuit. If the output of the square wave is to be clipped to $\pm V_X$ how is it obtained ? *(Ans. : Refer Sections 3.5.1 and 3.5.2)* **(Q. 3(b), 10 Marks)**

Q. 3.35 Write short note on : Precision rectifier. *(Ans. : Refer Sections 3.6 and 3.6.1)* **(Q. 6(2), 5 Marks)**

Q. 3.36 Write short note on : Schmitt trigger. *(Ans. : Refer Sections 3.4 and 3.4.1)* **(Q. 6(3), 5 Marks)**

Q. 3.37 Write short note on : Sample and hold circuit. *(Ans. : Refer Section 3.3)* **(Q. 6(4), 5 Marks)**

Q. 3.38 Write short note on : Window detector. *(Ans. : Refer Section 3.2.2(B))* **(Q. 6(5), 5 Marks)**

Chapter Ends...

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