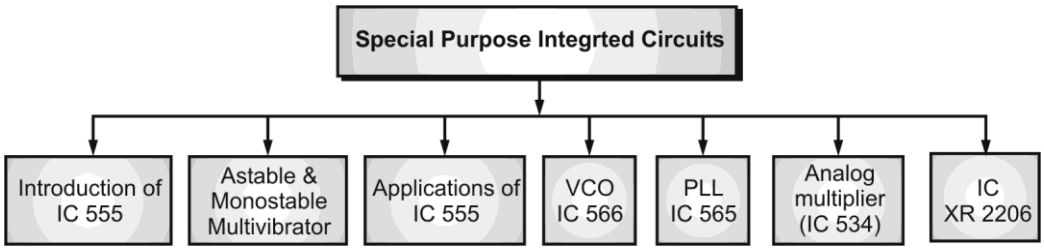
MODULE - **5**

Special Purpose Integrated Circuits

University Prescribed Syllabus

Functional block diagram and working of IC 555, design of astable and monostable multivibrator using IC 555, application of IC 555 as pulse position modulator, pulse width modulator and Schmitt Trigger. Functional block diagram and working of VCO IC 566 and application as frequency modulator, Functional block diagram and working of PLL IC 565 and application as FSK Demodulator, Functional block diagram and working of multiplier IC 534 and application as a phase detector, Functional block diagram and working of waveform generator XR 2206 and application as sinusoidal FSK generator.

This chapter / unit can be divided into seven sections as shown in the chart C5.1.1.



1.1

INTRODUCTION OF IC 555

Draw the pin diagram of IC555 timer DIP 8-pin package.

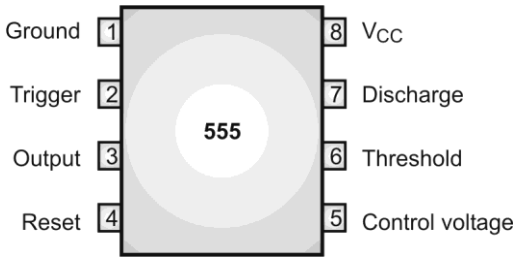


Fig. 5.1.1 : 8-pin DIP package

Explain the function of each pin of 555 timer IC.

Pin 1 : Ground

All voltages are measured with respect to this terminal.

Pin 2 : Trigger

The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3 : Output

Output of the timer is taken from this pin.

Pin 4 : Reset

Timer can be reset or disabled by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{cc}$ to avoid any possibility of false triggering.

Pin 5 : Control voltage

By applying voltage at this pin or by connecting a pot between this pin and ground, the pulse-width of the output waveform can be varied. When not in use, this pin should be bypassed to ground with 0.01 μf capacitor to prevent any noise problem.

Pin 6 : Threshold

This pin is connected to non-inverting terminal of comparator 1 (upper comparator) which monitors the external capacitor. When the voltage at this pin is greater than threshold voltage, i.e., $\left(\frac{2}{3}\right) V_{cc}$, then the comparator 1 output goes high which, in turn, switches the output of timer low.

Pin 7 : Discharge

This pin is connected to the collector of Transistor Q_1. When the output is high, Q_1 is 'OFF' and acts as an open circuit to the external capacitor C connected across it. When the output is low, Q_1 is 'ON' and acts as a short circuit connecting external capacitor C to ground.

Pin 8 : V_{cc}

The supply voltage of + 5V to 18 V is applied to this pin with respect to ground.

Give any five features of IC 555. **MU - Q. 1(a), Dec. 17, 5 Marks**

1. It operates on supply voltage between + 5V to 18 V.
2. It has high temperature stability and is designed to operate in the temperature range of – 55°C to 125°C.
3. It is basically operated in two modes, either as a monostable (one shot) multivibrator or as an astable (free running) multivibrator.
4. 555 timer is reliable, easy to design and is available at low cost.
5. It can source or sink current of 200 mA.

Functional Block Diagram of IC555

Explain the functional block diagram of Timer 555.

MU - Q. 1(d), May 16, Q. 1(d), May 17, 4 Marks

– The circuit consists of :

1. Two comparators
2. One S-R Flip-Flop
3. A transistor Q_1 that operates as a switch
4. One power supply (V_{cc}) with supply voltage of 5V.
5. Three 5 kΩ resistors

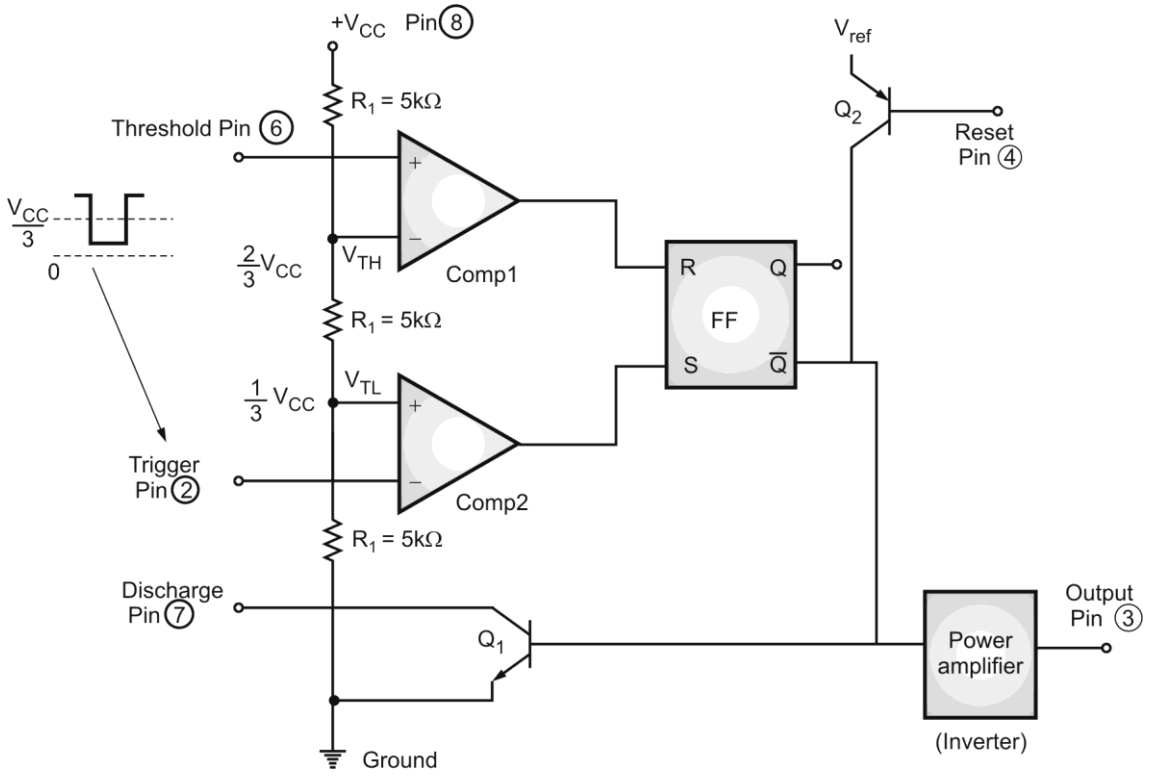


Fig. 5.1.2 : Functional block diagram of Timer 555

- Three resistors are connected across V_{cc} and establish the reference voltage for the two comparators.

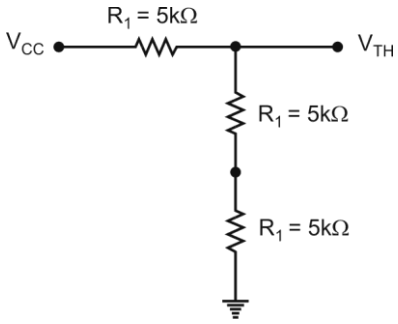


Fig. 5.1.3

- For comparator 1 :

$$V_{TH} = \frac{2R_1}{2R_1 + R_1} \times V_{cc}$$

$$V_{TH} = \frac{2}{3} V_{cc}$$

- For comparator 2 :

$$V_{TL} = \frac{R_1 \times V_{cc}}{2R_1 + R_1}$$

$$\therefore \quad V_{TL} = \frac{1}{3} V_{cc}$$

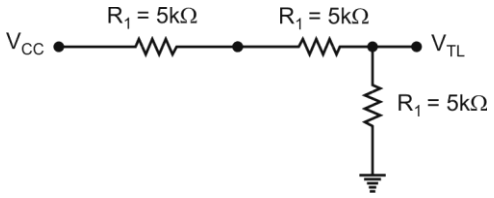


Fig. 5.1.4

- S-R flip-flop is a biastable circuit having complimentary outputs denoted as Q and $\bar{Q}$.
- In the set state, the output at Q is high and $\bar{Q}$ is low.
- In the reset state, the output at Q is low and that at $\bar{Q}$ is high.

- The set and reset input terminals of flip-flop are connected to the output of comparator 1 and comparator 2.
- In the stable state, the output $\bar{Q}$ of the Flip-Flop (FF) is high. This makes the output low because of power amplifier which is an inverted.
- A negative going trigger pulse is applied to pin 2. At the negative going edge of the trigger, as the trigger passes through $\left(\frac{V_{cc}}{3}\right)$, the output of the lower comparator, i.e., comparator 2 goes 'high' and sets the FF ($Q = 1, \bar{Q} = 0$).
- During positive excursion, when the threshold voltage at pin 6 passes through $\left(\frac{2}{3}\right) V_{cc}$, the output of the upper comparator goes 'high' and resets the FF ($Q = 0, \bar{Q} = 1$).
- The reset input (pin 4) provides mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from the lower comparator.
- When this reset is not used, it is returned to V_{cc}.
- The transistor 'Q_2' serves as a buffer to isolate the reset input from the FF and transistor Q_1.
- The transistor 'Q_2' is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

ASTABLE AND MONOSTABLE MULTIVIBRATOR USING IC 555

5.2.1 Monostable Multivibrator using IC 555

Draw the diagram of a monostable multivibrator using timer IC 555 with the help of waveforms at the trigger input across the charging capacitor and at the output explain its working. Design the same for a pulse width of 11 mS.

MU - Q. 5(a), May 17, Q. 2(a), Dec. 16, 10 Marks

With the help of a neat diagram and waveforms at the trigger input, across the capacitor and at the output, explain working of 555 as a monostable multivibrator. Find the values width of 5mS. **MU - Q. 3(a), Dec. 14, 10 Marks**

- In the stable state, FF holds transistor Q_1 in 'ON' state, and connects the capacitor 'C' to ground. The output remains at ground potential, i.e., Low.
- As the trigger passes through $\frac{V_{cc}}{3}$, the FF is set, i.e., $\bar{Q} = 0$. This makes the transistor Q_1 'OFF' and the short circuit across timing capacitor 'C' is released. As $\bar{Q}$ is low, output goes high = V_{cc}.
- The timing cycle now begins. Since 'C' is unclamped, voltage across it rises exponentially through R towards V_{cc} with a time constant RC.
- After a time period T, the capacitor voltage is just greater than $\left(\frac{2}{3}\right) V_{cc}$ and the upper comparator resets the FF, i.e., R = 1, S = 0. This makes $\bar{Q} = 1$ and transistor Q_1 goes 'ON', thereby discharging the capacitor 'C' rapidly to ground potential. The output returns to the ground potential.

– The voltage across the capacitor 'C' is given by,

$$V_c = V_{cc}(1 - e^{-t/RC})$$

At t = T, $V_c = \left(\frac{2}{3}\right) V_{cc}$

Therefore, $\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-T/RC})$

Or $T = RC\, ln\left(\frac{1}{3}\right)$

$\therefore \quad T = 1.1\ RC$ (seconds) …(5.2.1)

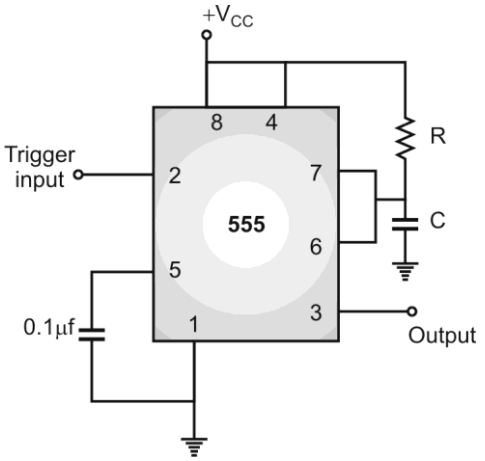


Fig. 5.2.1 : 555 timer connected for monostable operation

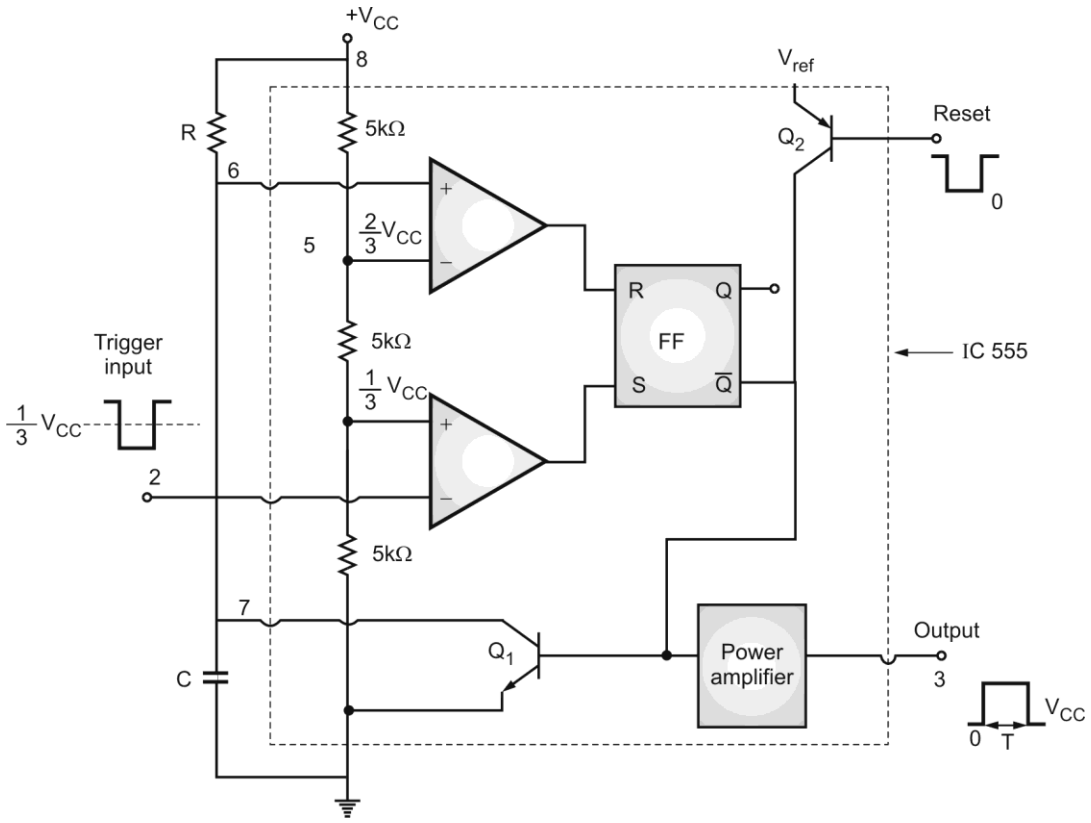


Fig. 5.2.2 : Timer in monostable operation with functional diagram

– From Equation (5.2.1), it is seen that the timing interval is independent of the supply voltage.

– It is also noted that once triggered, the output remains in 'High' state until the time 'T' elapses, which depends on R and C.

– Any additional trigger pulse coming during this time will not change the output state.

Design : Assume R = 10 kΩ, T = 11 mS

We know,

$$T = 1.1\,RC$$

$$\therefore\ C = \frac{T}{1.1\,R} = \frac{11 \times 10^{-3}}{1.1\,(10^4)}$$

$$\mathbf{C = 1\ \mu F}$$

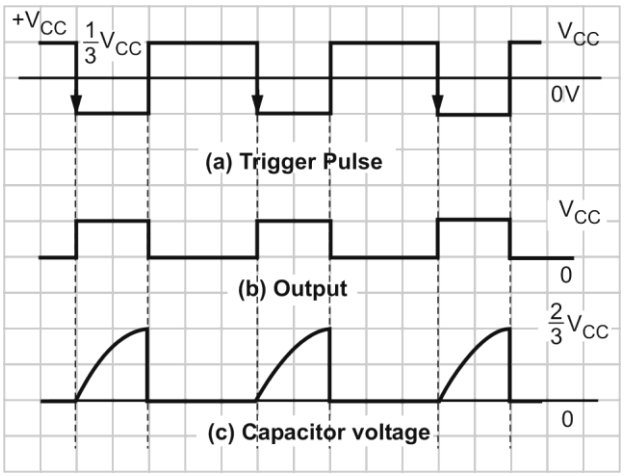


Fig. 5.2.3 : Timing pulses

Astable Multivibrator using IC 555

Draw and explain the functional diagram of IC 555 and explain its operation in astable mode.

MU - Q. 4(a), Dec. 15, Q. 5(a), May 15, 10 Marks

- When the power supply V_{cc} is connected, the external timing capacitor 'C' charges towards V_{cc} with a time constant $(R_A + R_B)C$.
- During this time, output (pin 3) is high (equal to V_{cc}) as Reset R = 0, Set S = 1 and this makes $\overline{Q} = 0$, which has unclamped the capacitor C.
- When the capacitor voltage equals to $\left(\frac{2}{3}\right) V_{cc}$,the upper comparator trigger the control flip-flop so that $\overline{Q} = 1$.

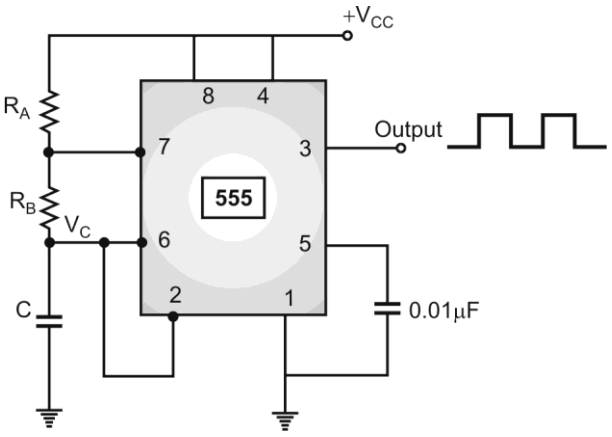


Fig. 5.2.4 : Astable multivibrator using 555 timer

- This makes the Transistor Q_1 'ON' and capacitor C starts discharging towards ground through R_B and Transistor Q_1 with a time constant R_B C.
- During the discharge of capacitor C, as it reaches $\frac{V_{cc}}{3}$, the lower comparator is triggered and at this stage S = 1, R = 0 which turns $\overline{Q} = 0$. $\overline{Q} = 0$ unclamps the capacitor C.

– The capacitor C is thus periodically charged and discharged between $\left(\frac{2}{3}\right) V_{cc}$ and $\left(\frac{1}{3}\right) V_{cc}$.

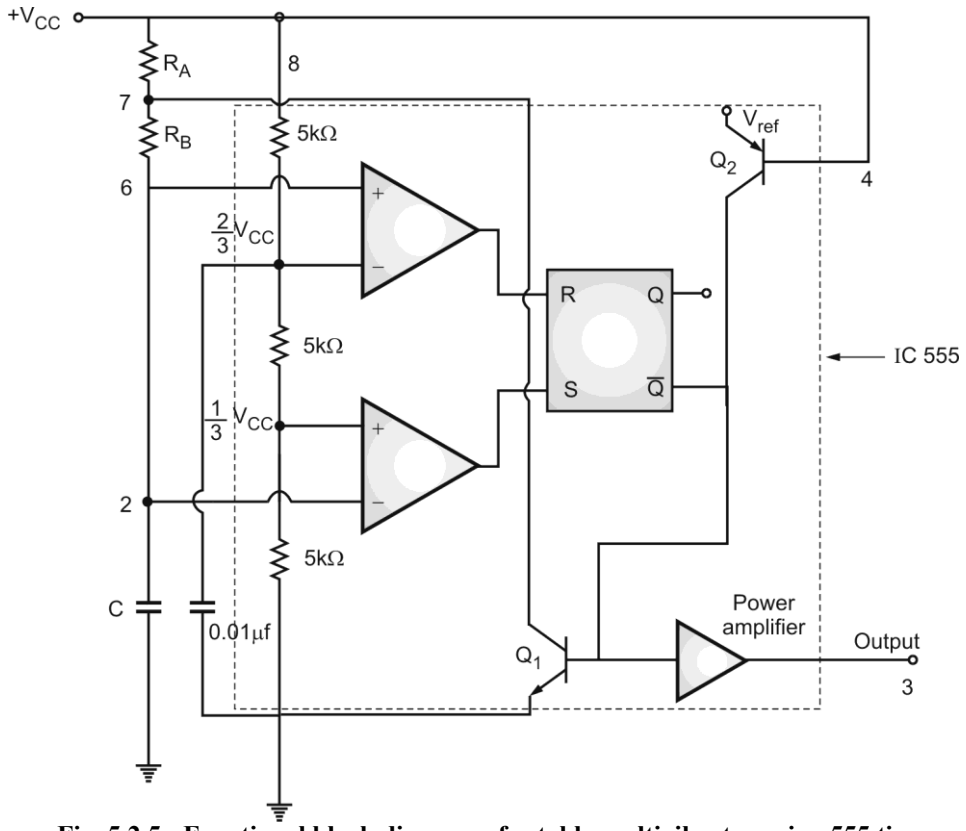


Fig. 5.2.5 : Functional block diagram of astable multivibrator using 555 timer

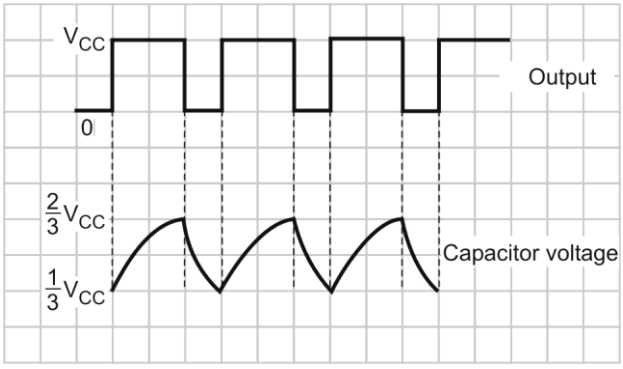


Fig. 5.2.6 : Timing sequence of astable multivibrator

– The capacitor voltage for a low pass RC circuit to a step input of V_{cc} is given by,

$$V_c = V_{cc} (1 - e^{-t/RC})$$

– The time t_1 taken by the circuit to charge from 0 to $\left(\frac{2}{3}\right) V_{cc}$ is,

$$\left(\frac{2}{3}\right) V_{cc} = V_{cc}\,(1 - e^{-t_1/RC})$$

$$\therefore \quad t_1 = 1.09\ RC \qquad \ldots(5.2.2)$$

– The time t_2 to charge from 0 to $\left(\frac{1}{3}\right) V_{cc}$ is,

$$\left(\frac{1}{3}\right) V_{cc} = V_{cc}\,(1 - e^{-t_2/RC})$$

$$\therefore \quad t_2 = 0.405\ RC \qquad \ldots(5.2.3)$$

– So the time to charge from $\left(\frac{1}{3}\right) V_{cc}$ to $\left(\frac{2}{3}\right) V_{cc}$ is,

$$t_c = t_1 - t_2$$

$$\therefore \quad t_c = 1.09\ RC - 0.405\ RC$$

$$\therefore \quad t_c = 0.69\,(R_A + R_B)\,C \qquad \ldots(5.2.4)$$

– The output is low while the capacitor discharges from $\left(\frac{2}{3}\right) V_{cc}$ to $\left(\frac{1}{3}\right) V_{cc}$ and the voltage across the capacitor is given by,

$$\left(\frac{1}{3}\right) V_{cc} = \left(\frac{2}{3}\right) V_{cc} \cdot e^{-t/RC}$$

We get, $t = 0.69\ RC$

$$\therefore \quad t_d = 0.69\,(R_B) \cdot C$$

– Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path.

Therefore Total Time,

$$T = t_c + t_d$$

$$T = 0.69\,(R_A + 2R_B)\,C$$

and frequency of oscillation,

$$f_o = \frac{1}{T}$$

$$= \frac{1.45}{(R_A + 2R_B)\,C}$$

– Duty cycle is the ratio of time t_c during which the output is high to the total time period T. It is generally expressed as a percentage. It is given by,

$$\%\ \text{duty cycle} = \frac{t_c}{T} \times 100$$

$$= \frac{R_A + R_B}{R_A + 2R_B}(100)$$

UEx. 5.2.1 **MU - Q. 5(b), May 18, Q. 5(b), Dec. 18, 10 Marks**

Analyze the circuit given in Fig. Ex. 5.2.1. Draw the waveforms at output terminal V_o and across the capacitor C. Comment on the duty cycle of output waveform. Take diode D as an ideal diode and assume R_A is equal to R_B.

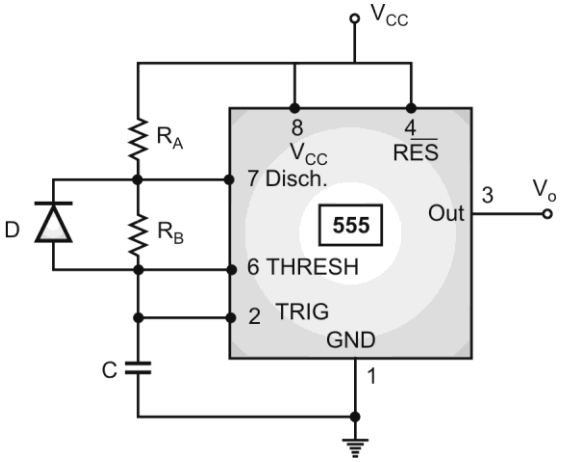


Fig. Ex. 5.2.1

☑ **Soln. :**

– Fig. Ex. 5.2.1 is astable multivibrator with 50% duty cycle. We know that for astable multivibrator % duty cycle is given by,

$$D\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

– For astable multivibrator, charging and discharging time of capacitor is given by,

$$\text{Charging time, } t_c = 0.69 (R_A + R_B) C$$

$$\text{Discharging time, } t_d = 0.69 (R_B) \cdot C$$

$$T = t_c + t_d$$

$$T = 0.69 (R_A + R_B) \cdot C$$

$$\text{and} \quad f = \frac{1}{T} = \frac{1.45}{(R_A + R_B) C}$$

– With this astable multivibrator, it is not possible to have duty cycle equal to 50%.

– Since, $t_c = 0.69 (R_A + R_B) \cdot C$ will always be greater than $t_d = 0.69 R_B C$.

– In order to obtain symmetrical square wave, i.e., D = 50%, the resistance R_A must be reduced to zero.

– If we make $R_A = 0$, then pin 7 will be directly connected to V_{cc} and extra current will flow through Q_1 when it is ON. This may damage Transistor Q_1 and hence the timer. But in the above circuit, diode D is connected across R_B.

- During charging of capacitor C, diode D is forward biased and current will flow through diode and it will short circuit R_B and t_c will be given by,

$$t_c = 0.69\ R_A\ C$$

- During discharging of capacitor C, transistor will be switched 'ON' and it will ground the pin 7 and hence diode D is reverse biased.

Discharging time, $t_d = 0.69\ R_B\ C$

$$\therefore\ T = t_c + t_d = 0.69\ (R_A + R_B) \cdot C$$

$$\text{and}\quad f = \frac{1.45}{(R_A + R_B)\ C}$$

$$\text{and \% duty cycle,}\quad D = \frac{R_A}{R_A + R_B} \times 100$$

When $R_A = R_B$, then

$$\text{\% duty cycle,}\quad \%\ D = \frac{R_A}{R_A + R_A} \times 100$$

$$= \frac{R_A}{2\ R_A} \times 100 = 50\%$$

With this circuit, we can achieve 50% duty cycle.

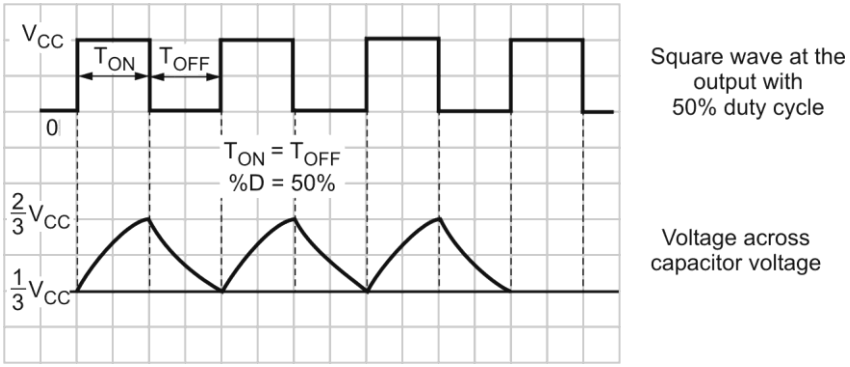
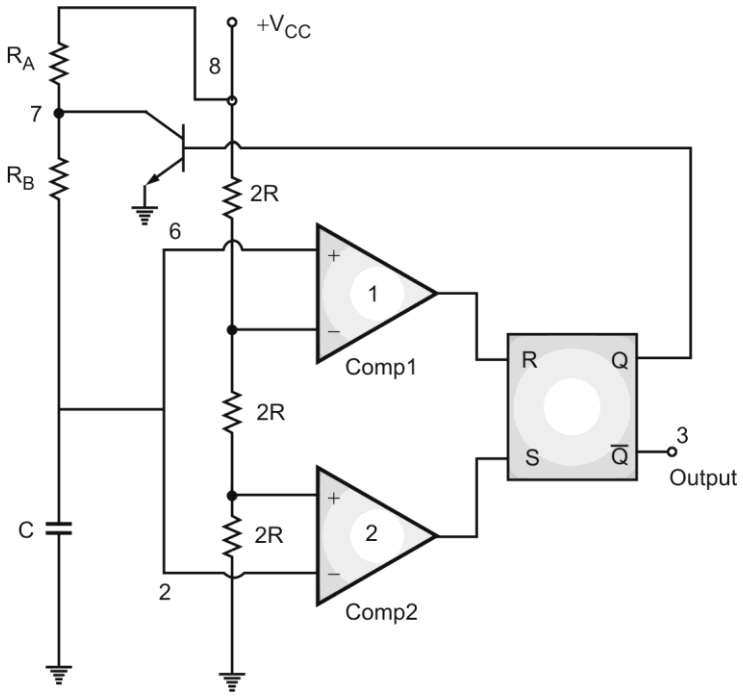


Fig. Ex. 5.2.1(a)

UEx. 5.2.2 **MU - Q. 3(b), May 19, 10 Marks**

The circuit given in Fig. Ex. 5.2.2, is similar to that of internal diagram of IC 555 with slight modifications in the internal resistance to value 2R. Analyze this circuit and draw the waveforms at output terminal V_{out} and across the capacitor C. Comment on the duty cycle of output waveform when :

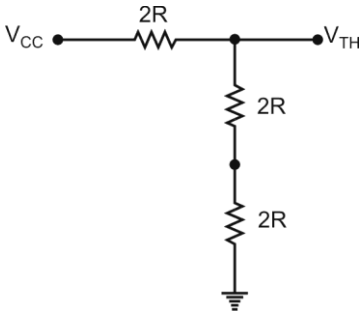
1. R_A is less than R_B.
2. R_A is equal to R_B.
3. R_A is greater than R_B.



(2E15)**Fig. Ex. 5.2.2**

☑ **Soln. :**

- Given circuit is of astable multivibrator using IC 555 timer.
- The value of threshold voltage V_{TH} at inverting terminal of comparator 1 is $\frac{2}{3} V_{cc}$ and threshold voltage V_{TL} at non-inverting terminal of comparator 2 is $\frac{1}{3} V_{cc}$.
- There is no change in these threshold values with change in internal resistance from value R to value 2R.
- This can be proved as follows :



(2E16)**Fig. Ex. 5.2.2(a)**

For comparator 1,

$$V_{TH} = \frac{V_{cc} \times 4R}{4R + 2R} = \frac{V_{cc} \times 4\cancel{R}}{6\cancel{R}} = \frac{4}{6} V_{cc}$$

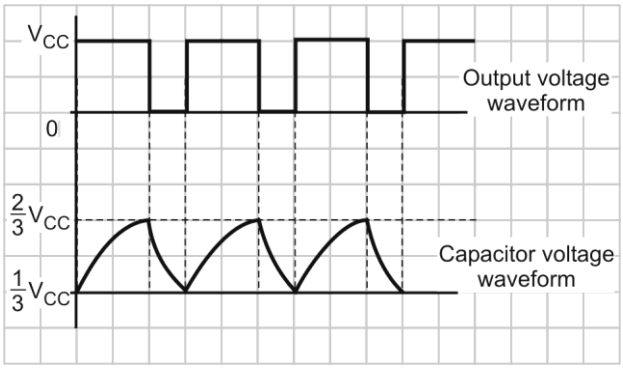
$$V_{TH} = \frac{2}{3} V_{cc}$$

(2E17)**Fig. Ex. 5.2.2(b)**

For comparator 2,

$$V_{TL} = \frac{V_{cc} \times 2R}{2R + 2R + 2R} = \frac{V_{cc} \times 2\cancel{R}}{6\cancel{R}} = \frac{1}{3} \times V_{cc}$$

$$V_{TL} = \frac{1}{3} V_{cc}$$



(2E18)**Fig. Ex. 5.2.2(c)**

Since this circuit is a astable multivibrator,

– We know that, capacitor charges from $\frac{1}{3} V_{cc}$ to $\frac{2}{3} V_{cc}$, when the output is high.

– It discharges from $\frac{2}{3} V_{cc}$ to $\frac{1}{3} V_{cc}$, when the output voltage is low.

Charging time of capacitor is given by,

$$t_c = 0.69 (R_A + R_B) C$$

and discharging time of capacitor is given by,

$$t_d = 0.69 (R_B) \cdot C$$

Total time T is given by,

$$T = t_c + t_d$$

$$\therefore \quad T = 0.69 (R_A + 2R_B) \cdot C$$

and frequency of oscillation is given by,

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B) C}$$

Duty cycle for astable multivibrator is given by,

$$\% \text{ duty cycle} = \frac{t_c}{T} \times 100$$

$$\% \text{ Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B} (100)$$

- **Case 1 :** When R_A is less than R_B, % duty cycle is 60%.
- **Case 2 :** When R_A is equal to R_B, output duty cycle is 66%.
- **Case 3 :** When R_A is greater than R_B, % duty cycle is equal to 75%.

UEx. 5.2.3 MU - Q. 1(c), Dec. 19, 5 Marks

What is the frequency of IC 555 astable multivibrator shown in Fig. Ex. 5.2.3 ?

i) 241 Hz ii) 178 Hz iii) 78 Hz iv) 8 Hz. Justify.

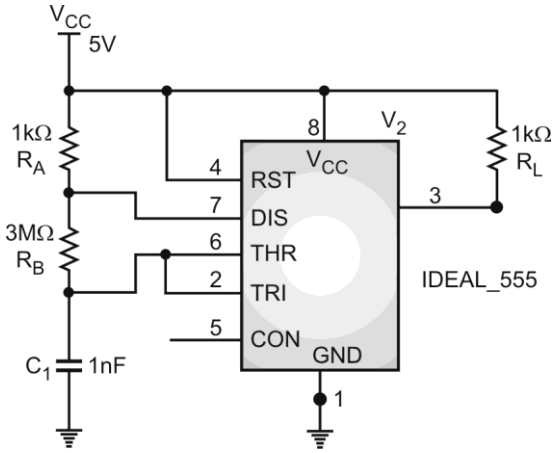


Fig. Ex. 5.2.3

☑ **Soln. : (i) 241 Hz**

The frequency of IC 555 astable multivibrator is given by,

$$f = \frac{1.45}{(R_A + 2R_B)\,C}$$

Given : $R_A = 1\ k\Omega$, $R_B = 3\ \mu\Omega$

$C = 1\ nF$

$$\therefore\ f = \frac{1.45}{(1 \times 10^3 + 2 \times 3 \times 10^6)\ 1 \times 10^{-9}}$$

$$\therefore\ f = \frac{1.45}{0.0060} = \mathbf{241\ Hz}$$

UEx. 5.2.4 MU - Q. 4(a), Dec. 19, 10 Marks

Design an IC 555 astable multivibrator for an output frequency 1 kHz and a duty cycle of 60%.

☑ **Soln. :**

Given : $f_o = 1$ kHz, % Duty cycle = 60 %

▸ **Step 1 :** For astable multivibrator

$$f_o = \frac{1.45}{(R_A + 2R_B)C}$$

and % duty cycle $= \frac{t_c}{T} \times 100$

$t_c = 0.69\ (R_A + R_B) \cdot C = T_{ON}$

$t_d = 0.69\ (R_B) \cdot C = T_{OFF}$

$T = t_c + t_d$

$$T = 0.69 (R_A + 2R_B) C$$

Since % duty cycle = 60 %

$$D = 0.6$$

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$D = \frac{0.69(R_A + R_B)\,C}{0.69 (R_A + R_B)\,C + 0.69\, R_B\, C}$$

$$D = \frac{R_A + R_B}{R_A + 2R_B}$$

$$0.6 = \frac{R_A + R_B}{R_A + 2R_B}$$

$$0.6\, R_A + 1.2\, R_B = R_A + R_B$$

$$1.2\, R_B - R_B = R_A - 0.6\, R_A$$

$$\therefore\ 0.2\, R_B = 0.4\, R_A$$

$$\therefore\ R_B = \frac{0.4}{0.2}\, R_A$$

$$\therefore\ \mathbf{R_B = 0.2\ R_A} \qquad \ldots(1)$$

▸ **Step 2**

$$f_o = \frac{1.45}{(R_A + 2 R_B)C}$$

Assume $C = 0.1\ \mu F$

$$1 \times 10^3 = \frac{1.45}{(R_A + 2 R_B) \times 0.1 \mu F}$$

Put $R_B = 0.2\, R_A$ from (1)

$$1 \times 10^3 = \frac{1.45}{(R_A + 2 \times 0.2\, R_A) \times 0.1 \times 10^{-6}}$$

$$1 \times 10^3 = \frac{1.45}{(1.4\, R_A) \times 0.1 \times 10^{-6}}$$

$$1 \times 10^3 \times 1.4\, R_A \times 0.1 \times 10^{-6} = 1.45$$

$$\therefore\ R_A = \frac{1.45}{1 \times 10^3 \times 1.4 \times 0.1 \times 10^{-6}}$$

$$\therefore\ R_A = \frac{1.45}{0.14 \times 10^{-3}} = 10.35\ k\Omega$$

Since $R_B = 0.2\, R_A$

$$\therefore R_B = 0.2 \times 10.35$$

$$\therefore R_B = 2.07\ k\Omega$$

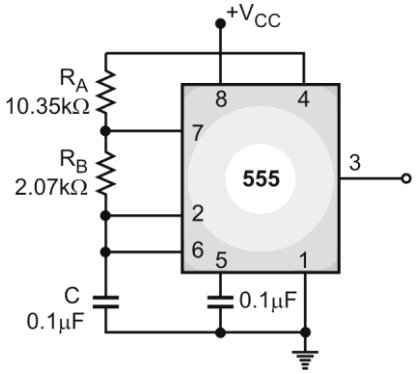
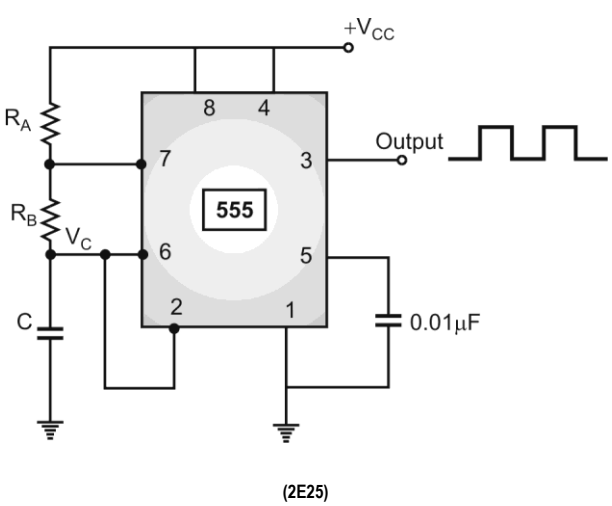
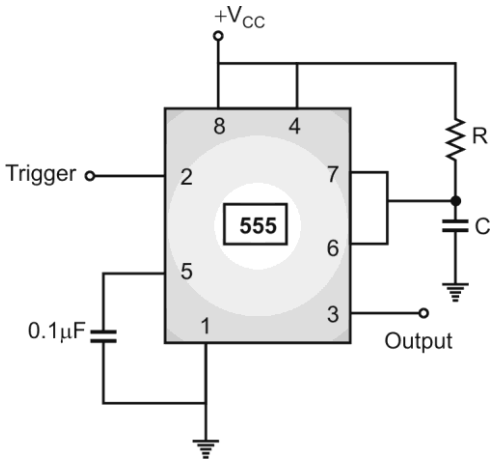


Fig. Ex. 5.2.4

Comparison between Astable and Monostable Multivibrator

Compare astable and monostable multivibrator using IC 555 timer.

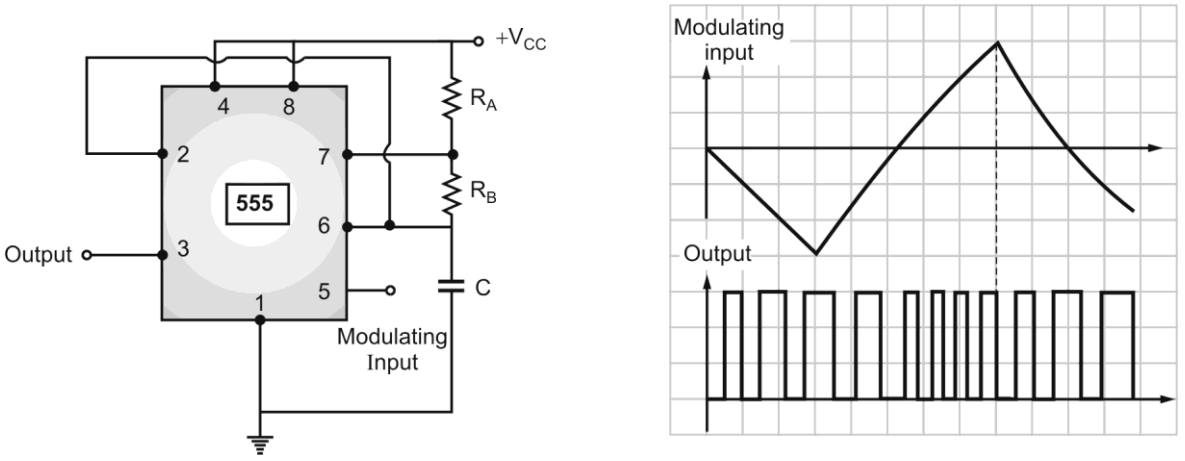
Sr. No.	Astable multivibrator	Monostable multivibrator
1.	Astable multivibrator has two states and neither is stable and will alternate between them without the need for trigger signal, i.e., It has no stable state.	It has single stable state, either high or low level and will switch to the other state, if triggered, but will return to the stable state after the time constant.
2.	$T = 0.69 (R_A + 2R_B) C$	The time delay, $T = 1.1 RC$
3.	**Circuit diagram**  (2E25)	**Circuit diagram**  (2E26)
4.	Frequency of oscillations, $f = \frac{1.45}{(R_A + 2R_B) C}$	Frequency of oscillations, $f = \frac{1}{1.1 \times RC}$
5.	Applications are FSK generator, pulse position modulator.	Applications are missing pulse detector, linear ramp generator, frequency divider and pulse width modulation.

APPLICATIONS OF IC 555

Application of Astable Multivibrator as Pulse Position Modulator

Explain the application of astable multivibrator as pulse-position modulator.

- The circuit consists of
  1. IC 555 timer in astable multivibrator mode.
  2. A modulating signal
- A modulating signal is applied at pin number 5 of IC 555 timer in astable mode.
- Pin number 2, i.e., Trigger pin and pin number 6, i.e., Threshold pin of IC 555 timer are shorted.
- Output pulse is obtained at pin number 3.
- The output pulse position varies with the modulating signal.
- Threshold voltage and hence time delay is varied.
- The modulating signal and the output waveform are shown in Fig. 5.3.1(b).
- We can conclude from the output waveform that the frequency is varying leading to pulse position modulation.



Pulse position modulator using IC 555 timer in astable mode

(b) Pulse position modulator waveform

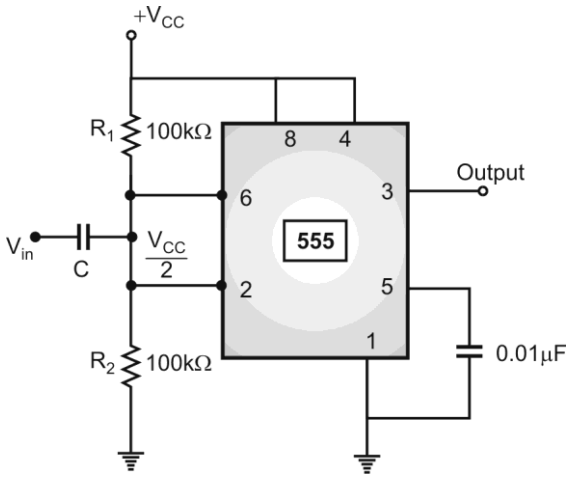
Fig. 5.3.1

Application of IC 555 Timer as Schmitt Trigger

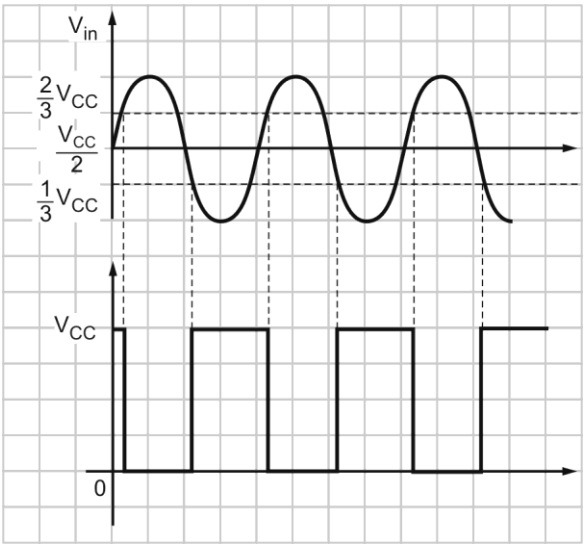
Explain the application of IC 555 timer as Schmitt trigger.

- Schmitt trigger is used to convert sine wave into square wave.
- Schmitt trigger using IC 555 timer is shown in Fig. 5.3.3.
- Here, the two internal comparators are tied together.

- Comparators are externally biased at $\frac{V_{cc}}{2}$ through resistors R_1 and R_2.
- $\frac{V_{cc}}{2}$ is the average voltage of upper comparator voltage, i.e., $\frac{2}{3}V_{cc}$ and lower comparator voltage, i.e., $\frac{1}{3}V_{cc}$.
- $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ voltages are the reference voltage levels.
- A sine wave with amplitude greater than $\left(\frac{2}{3}V_{cc} - \frac{V_{cc}}{2}\right)$ and $\left(\frac{1}{3}V_{cc} - \frac{V_{cc}}{2}\right)$, i.e., $\frac{V_{cc}}{6}$ applied as an input signal.
- Input sine wave amplitude when exceeds the reference levels, causes the internal flip-flop to alternatively set and reset.
- It provides square wave at the output terminal.



Schmitt trigger circuit using IC 555 timer



Input and output waveforms of Schmitt trigger

Fig. 5.3.3

⏭ 5.4 VCO IC 566

GQ. 5.4.1 Draw and explain the block diagram of VCO IC 566.

- The Voltage Controlled Oscillator (VCO) generates an output frequency that is directly proportional to its input voltage.
- The block diagram of VCO IC 566 is shown in Fig. 5.4.1.

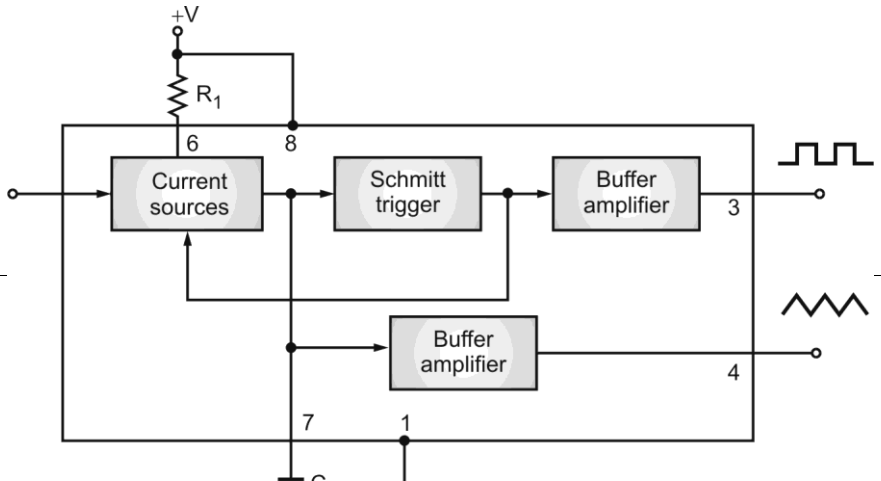


Fig. 5.4.1 : Block diagram of VCO IC 566

- The frequency of oscillation is determined by an external resistor R_1 and capacitor C_1 and the voltage V_C applied to the control terminal 5.
- The triangular wave is generated by alternately charging the external capacitor C_1 by one current source and then linearly discharging it by another.
- The charge discharge levels are determined by Schmitt trigger action.
- The Schmitt trigger also provides the square wave output.
- Both the output waveforms are buffered so that the output impedance of each is 50Ω.
- The typical amplitude of the triangular wave is 2.4 V_{pp} and that of the square wave is 5.4 $V_{P\text{-}P}$.
- Fig. 5.4.2 is the pin diagram of NE/SE 566 VCO.
- Fig. 5.4.3 is typical connection diagram of NE/SE 566 VCO.
- Fig. 5.4.4 shows the output waveform.
- In Fig. 5.4.2, R_1 C_1 combination determines the free running frequency and the control voltage V_C at terminal 5 is set by the voltage divider formed with R_2 and R_3.
- The initial voltage V_C at terminal 5 must be in the range.

$$\frac{3}{4}(+V) \leq V_C \leq +V$$

where + V is the total supply voltage.

- The modulating signal is A.C. coupled with the capacitor C and must be less than 3 $V_{p\text{-}p}$.
- The frequency of the output waveform is given by,

$$f_o = \frac{2\,(+V - V_c)}{R_1\,C_1\,(+V)}$$

- A small capacitor of 0.001 μF should be connected between pins 5 and 6 to eliminate possible oscillations in the control current source.
- Resistance R_1 should be greater than 2kΩ and less than 20 kΩ.

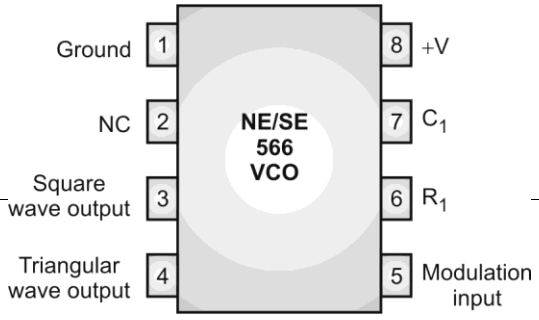


Fig. 5.4.2 : Pin diagram

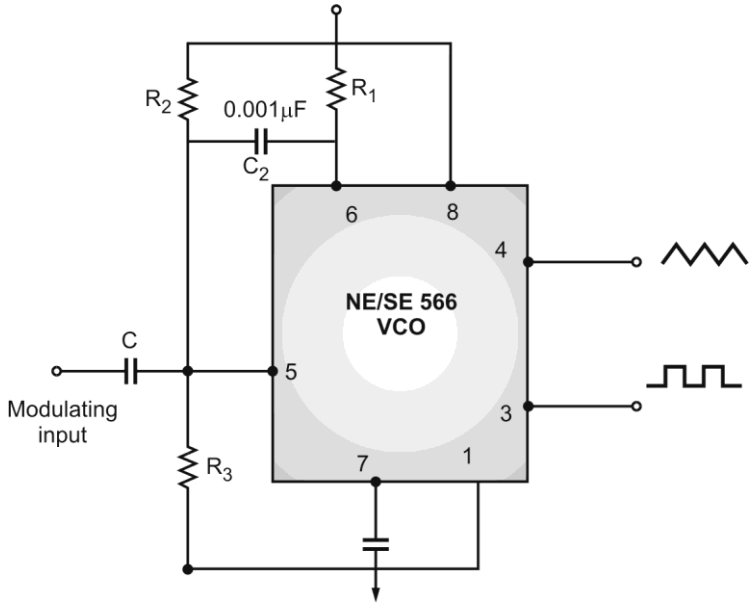


Fig. 5.4.3 : Typical connection diagram

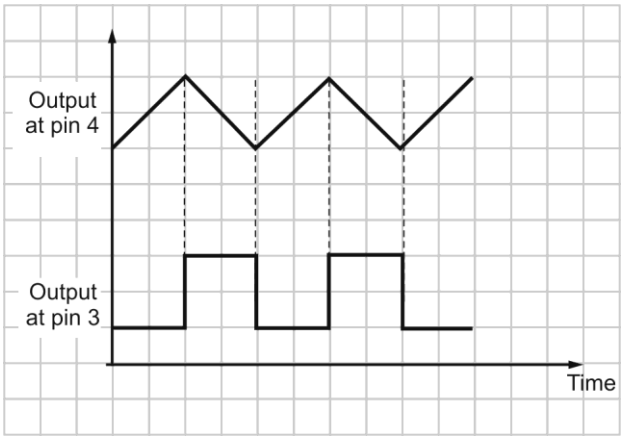


Fig. 5.4.4

– The VCO is commonly used in converting low frequency signals such as EEG (Electroencephalograms) or EKG (electrocardiograms) into an audio frequency range and can be transmitted over telephone lines or two way radio communication for diagnostic purposes.

Application of IC 566 as Frequency Modulator

Explain the application of IC 566 as frequency modulator.

The circuit diagram of frequency modulator is shown in Fig. 5.4.5.

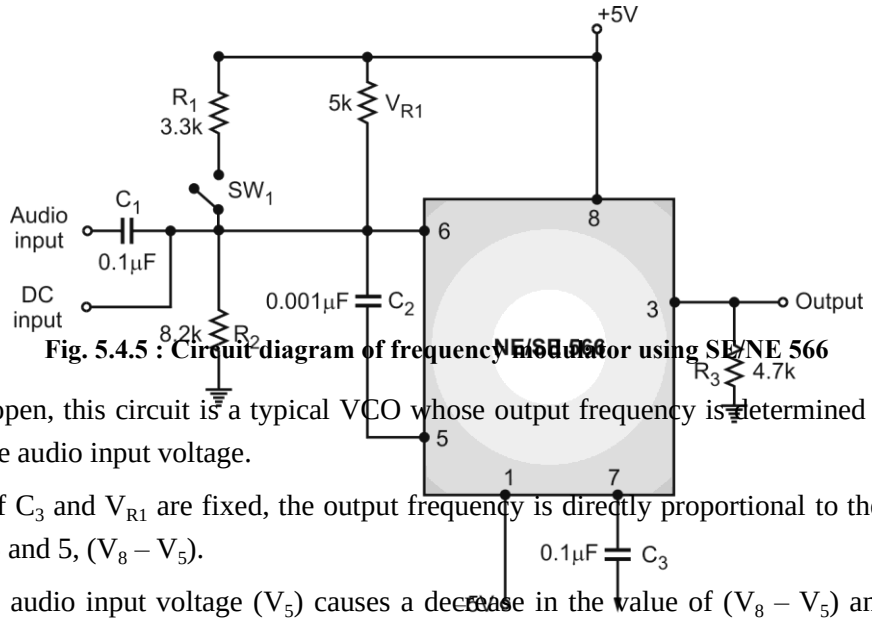


Fig. 5.4.5 : Circuit diagram of frequency modulator using SE/NE 566

- If the SW_1 is open, this circuit is a typical VCO whose output frequency is determined by the values of C_3 and V_{R1} and the audio input voltage.
- If the values of C_3 and V_{R1} are fixed, the output frequency is directly proportional to the voltage difference between pins 8 and 5, $(V_8 - V_5)$.
- An increase in audio input voltage (V_5) causes a decrease in the value of $(V_8 - V_5)$ and a decrease in the output frequency.
- Decreasing the audio input voltage (V_5) will cause the output frequency to increase.
- Output frequency is inversely proportional to the product of V_{R1} and C_3.
- If the SW_1 switch is closed, the voltage divider constructed by R_1 and R_2 provides a dc level to the audio input (pin 5).
- By adjusting V_{R1}, we can easly tune the VCO center frequency f_o .
- When an audio signal is applied to the audio input, the output frequency will generate frequency deviations around f_o in the variation of audio amplitude.
- Thus, a frequency modulated signal is obtained.

PLL IC 565

Define PLL.

Write short note on : Phase locked loop IC 565.

MU - Q. 6(1), Dec. 14, Q. 6(d), Dec. 19, 5 Marks

The phase locked loop, commonly called PLL, is a closed loop feedback system, whose output frequency and phase are in lock with the frequency and phase of the input signal.

What are the general applications of PLL ?

PLL are used in :

(1) Satellite communication systems (2) FM demodulators

(3) Stereo demodulators (4) Tone detectors

(5) Frequency synthesizers (6) Motor speed control

(7) Generation of local oscillator frequency in T.V. and in FM tuners.

Block Diagram of PLL

Explain PLL operation in detail with neat block diagram.

Short note on : Working of PLL IC 565. **MU - Q. 6(e), May 19, 5 Marks**

The basic block diagram of PLL is shown in Fig. 5.5.1. The main elements of PLL are :

(1) Phase detector/comparator (2) A low pass filter

(3) An error Amplifier (A) (4) Voltage controlled oscillator (VCO)

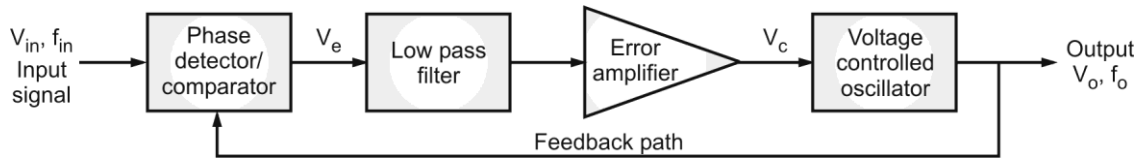


Fig. 5.5.1 : Block diagram of PLL 565

- When no external input signal is applied, voltage controlled oscillator (VCO) oscillates with its natural frequency. This frequency is decided by an external timing capacitor and resistor. This frequency is known as **free running frequency**.
- When input signal V_{in} of frequency f_{in} is applied to PLL, the phase detector compares the phase and frequency of this incoming signal with output signal V_o of frequency f_o.
- If these signals differ in frequency or phase, then an error voltage V_e generates at the output of phase detector. Phase detector produces sum and difference of frequency components, i.e., $(f_{in} + f_o)$ and $(f_{in} – f_o)$ at its output.
- The high frequency component $(f_{in} + f_o)$ is removed by using low pass filter and only low frequency component $(f_{in} – f_o)$ is applied to the amplifier.
- Amplifier amplifies this signal and provides this signal as a control voltage V_c to voltage controlled oscillator (VCO).
- This control voltage V_c shifts VCO frequency in a particular direction to reduce the frequency difference between f_{in} and f_o .
- When this process starts, the signal is said to be in **capture range**.
- VCO continuously changes its frequency till f_o becomes exactly same as f_{in}.When f_o is equal to f_{in}, at this condition, the circuit is said to be in **Locked range**.

  So we can say that :

  (1) Before input is applied, PLL is in free running state.

  (2) When f_{in} is applied, VCO frequency starts to change and PLL is in capture mode.

(3) When $f_{in} = f_o$, PLL is in Lock range.

(1) Phase detector

The phase detector or comparator compares the input frequency f_{in} with feedback frequency f_o. The output of phase detector is proportional to the phase difference between f_{in} and f_o. The two inputs to a phase detector are input voltage V_{in} at frequency f_{in} and the feedback voltage from VCO, i.e., V_o at frequency f_o.

- The phase detector compares these two signals and produces a d.c. voltage V_e which is proportional to the phase difference between f_{in} and f_o.
- The output voltage V_e of phase detector is called as error voltage.

Depending on whether the analog or digital phase detector is being used, the PLL is called either an analog or digital type.

Types of phase detector

(A) Analog

(B) Digital

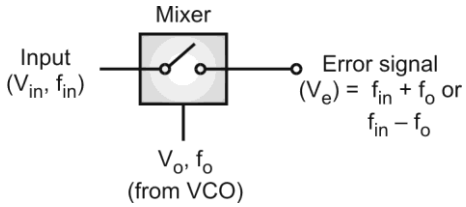


Fig. 5.5.2 : Analog phase detector

(A) Analog Phase Detector

- Here input is applied to the mixer circuit along with the output of VCO.
- Generally VCO output is a square wave. Mixer is operated depending on the output of VCO.
- Mixer generates a sum ($f_{in} + f_o$) and difference ($f_{in} – f_o$) signals at its output. This is known as error voltage.
- Depending on this error, PLL tries to lock the applied frequency.
  (a) When both f_o and f_{in} are in phase, then $V_e = + V_e$.
  (b) When both f_o and f_{in} have phase difference of 90°, then $V_e = 0$.
  (c) When both f_o and f_{in} have phase difference of 180° then $V_e = – V_e$.

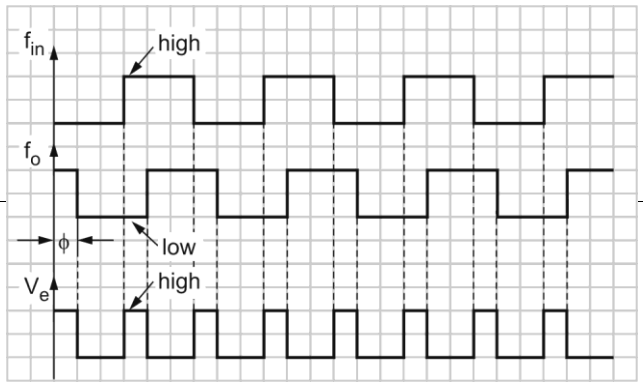
(B) Digital Phase Detector using Ex-OR Gate

Fig. 5.5.3

Truth Table of Ex-OR

f_{in}	f_o	V_e
0	0	0
0	1	1
1	0	1
1	1	0

- We know that output of EX-OR gate is high, only when odd number of inputs are high.
- Thus in Fig. 5.5.4 when either f_{in} or f_o is high, its output is high.



– There is some phase difference between input (f_{in}) and output (f_o).

Fig. 5.5.4 : Input and output waveforms

(2) Low pass filter

– The output of phase detector is given to the low-pass filter.

– The function of low pass filter is to remove the high frequency noise present in the detector output and produces a ripple-free d.c. level.

– The output of low pass filter is applied to the amplifier.

– This d.c. level is amplified to an adequate level by using amplifier and applied to a voltage controlled oscillator (VCO).

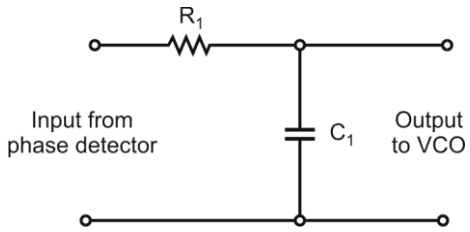


Fig. 5.5.5 : Low pass filter : Passive filter

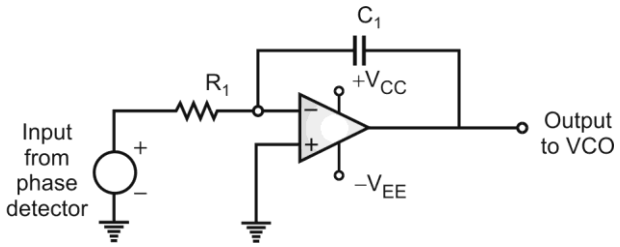


Fig. 5.5.6 : Low pass filter : Active filter

(3) Voltage controlled oscillator (VCO)

– The amplified output of low pass filter is applied to VCO.

– VCO generates an output frequency that is directly proportional to its input voltage.

– The IC used for VCO is SE/NE 566 or its equivalent.

– The block diagram of VCO is shown in Fig. 5.5.7

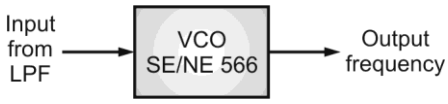


Fig. 5.5.7 : Block diagram of VCO

PLL using IC NE/SE 565

With the help of a neat circuit diagram explain PLL using IC NE/SE 565.

MU - Q. 6(c), May 15, Q. 2(A), Dec. 17, 10 Marks

For PLL IC 565 give expression of free running frequency, lock range and capture range.

MU - Q. 5(a), Dec. 19, 6 Marks

The functional block diagram of PLL using IC NE/SE 565 is shown in Fig. 5.5.8.

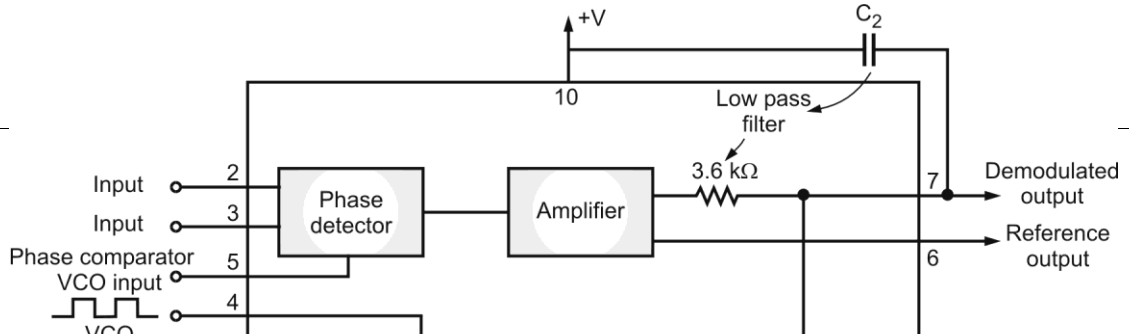


Fig. 5.5.8 : Block diagram of PLL using IC NE/SE 565

- When no input is given, i.e., pin number 2 and 3 are grounded, then the free running frequency of VCO is given by,

$$\mathbf{f_{out} = \frac{1.2}{4R_1C_1}\ Hz}$$

where R_1 and C_1 are an external resistor and capacitor connected to pin 8 and 9, respectively.

- C_1 can be of any value but R_1 must have a value between 2 kΩ to 20 kΩ.
- A capacitor C_2 connected between pin 7 and positive supply pin 10 forms a first order low pass filter with an internal resistance of 3.6 kΩ.
- The VCO free running frequency f_{out} is adjusted externally with R_1 and C_1 to be at centre of the input frequency range.
- The 565 PLL can lock to and track an input signal over typically ± 60 % bandwidth with respect to f_{out} as the centre frequency.
- The lock range for PLL is given by,

$$\mathbf{f_L = \pm \frac{8\ f_{out}}{V}\ Hz}$$

where f_{out} = free running frequency of VCO (Hz) and V = (+ V) – (– V) volts

- The capture range is given by,

$$\mathbf{f_c = \pm \left[\frac{f_L}{(2\pi)(3.6) \times 10^3 \times C_2} \right]^{1/2}}$$

where, C_2 is expressed in farads.

- The lock range usually increases with an increase in input voltage but decreases with an increase in supply voltage.

FSK Demodulator Using IC565

With the help of neat circuit diagram explain application of PLL 565 as FSK de modulator.

MU - Q. 6(c), May 15, Q. 1(vi), Dec. 15, 4 Marks

- In computer peripheral and radio (wireless) communication, the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies.

- Since the carrier frequency is shifted between two preset frequencies, the data transmission is said to use a frequency shift keying (FSK) technique.
- In 565 PLL, the frequency shift is accomplished by driving VCO with the binary data signal. So the two resulting frequencies correspond to logic 1 and logic 0 states of the binary data signal.
- The frequencies corresponding to logic 1 and logic 0 states are commonly called ‘mark’ and ‘space’ frequencies.
- The carrier frequency is shifted either to f_H or f_L depending on whether a binary 1 or 0 is to be transmitted.
- If a ‘1’ is to be sent, the transmitter will transmit a signal frequency f_H and if a ‘0’ is to be sent, then transmitter transmits frequency f_L.
- FSK signal can be demodulated by using PLL as shown in Fig. 5.5.9.

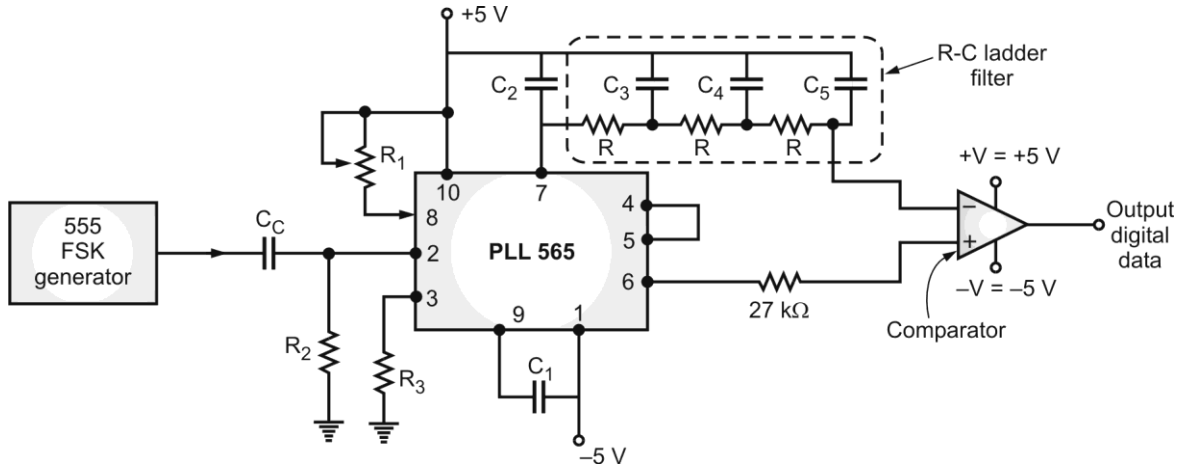


Fig. 5.5.9 : FSK demodulator using PLL

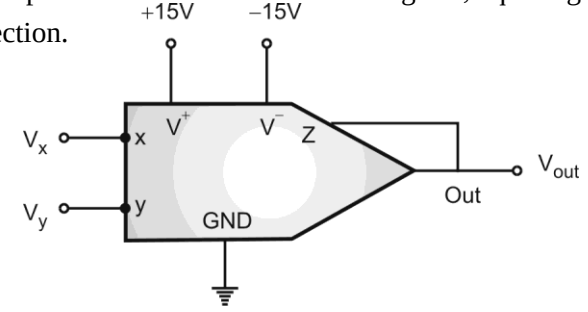
- As shown in Fig. 5.5.9, the output of the 555 FSK generator is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove a d.c. level.
- As the signal appears at the input of the PLL 565, the loop locks to the input frequency and tracks it between two frequencies with a corresponding d.c. shift at the output.
- Resistor R_1 and capacitor C_1 determine the free running frequency of the VCO.
- Capacitor C_2 is a loop filter.
- A three stage RC ladder (low pass) filter is used to remove the carrier component from the output.
- The high cut-off frequency,

  $f_H = \frac{1}{2}\pi$ RC of the ladder filter is chosen between 150 Hz and 2200 Hz.
- Comparator is connected at the output of ladder filter and pin 6 of PLL.

ANALOG MULTIPLIER

Write short note on analog multiplier.

- The circuit which performs the multiplication of the two input voltages is called multiplier circuit.
- Analog multiplier has a number of applications like multiplication and division of two signals, squaring of signal, frequency shifting and doubling, phase angle detection.
- Fig. 5.6.1 is a symbolic representation of an analog multiplier.
- If two signal inputs V_x and V_y are given, then the output is the product of the two inputs divided by a reference voltage V_{ref}.



Hence $V_{out} = \frac{V_x \times V_y}{V_{ref}}$ …(5.6.1)

Normally, V_{ref} is internally set to 10V.

Hence, $V_{out} = \frac{V_x \times V_y}{10}$ …(5.6.2)

(2C1)**Fig. 5.6.1 : Symbol of analog multiplier**

- As long as V_x and $V_y < V_{ref}$, the multiplier does not saturate.
- Equation (5.6.2) can be described in different quadrants as :
  (i) If both inputs V_x and V_y are positive, the multiplier works as one quadrant multiplier.
  (ii) If V_x is held positive and V_y swing between positive and negative, then the multiplier works as two quadrant multiplier.
  (iii) If both inputs V_x and V_y swing between positive and negative, then the multiplier works as four quadrant multiplier.
- One common technique have been applied to multiply two analog signals. This technique uses log-antilog method.
- Let V_x and V_y be the two input signals to be multiplied. Using logarithmic fundamentals, we can write

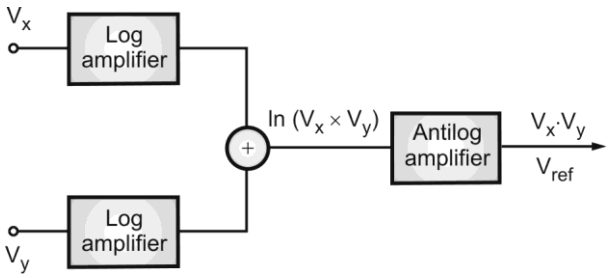
$$\log_e (V_x \times V_y) = \log (V_x) + \log (V_y) \quad \ldots(5.6.3)$$

We can also write,

$$(V_x \times V_y) = 1n^{-1} (V_x - V_y) \quad \ldots(5.6.4)$$

Equation (5.6.3) and (5.6.4) analysed the application of log and antilog amplifiers to construct an analog multiplier as shown in Fig. 5.6.2.

This log-antilog multiplier is set for one quadrant operation. The AD533 and AD534 are multiplier IC chips available in the market.



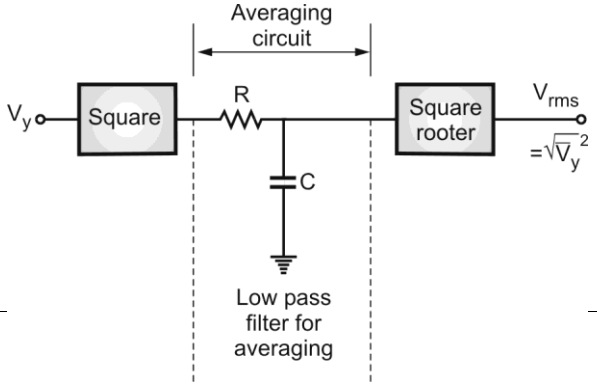
(2C2)**Fig. 5.6.2 : Block diagram of analog multiplier**

How can the true RMS value of voltage signal is measured using analog multipliers ?

MU - Q. 1(e), Dec. 18, 5 Marks

In this measurement, the multiplier can be used as a square and a square rooter.

- The averaging operation can be done by using a low pass filter.
- The rms generating circuit can be used to construct an rms voltmeter. If a d-c voltmeter is connected from the output of the square rooter to the ground.
- This type of r.m.s. measurement is more versatile and accurate than most conventional a-c voltmeters which provide a true r.m.s. value only for sinusoidal voltages.



– A block diagram of a rms converter is shown in Fig. 5.6.3.

Here, $V_{rms} = \sqrt{V_y^{-2}}$

– The Root Mean Square (RMS) value of a signal is given by,

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V_x^2(t)\,dt}$$

where T = period of the input signal.

(2C3)**Fig. 5.6.3 : RMS converter circuit**

– Fig. 5.6.4 shows the circuit diagram of RMS detector. It consists of following stages, namely :

1. Square 2. Integrator 3. Square rooting

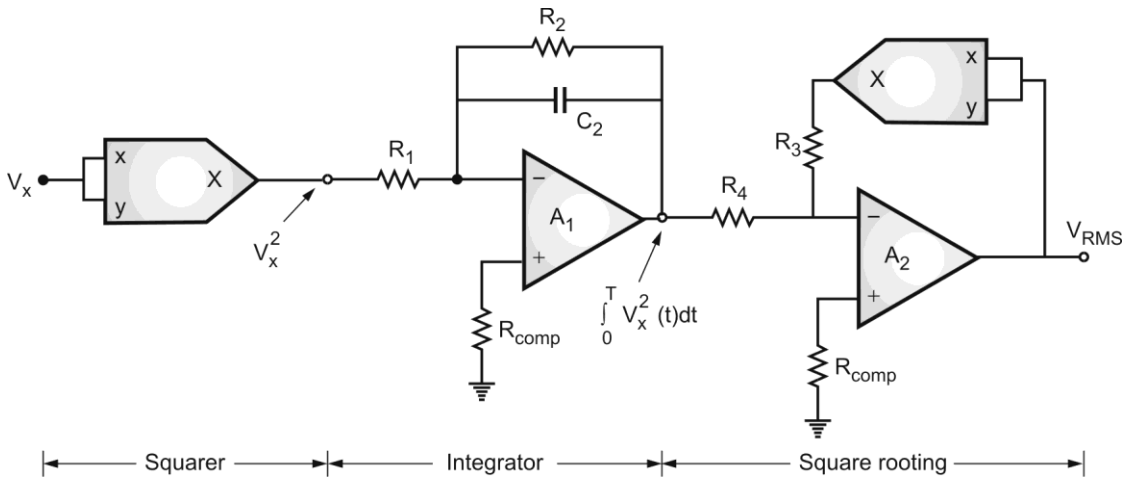


Fig. 5.6.4 : RMS detector circuit

– The operation is performed in the order of squaring, finding the mean i.e. integrated and finally finding the square root.

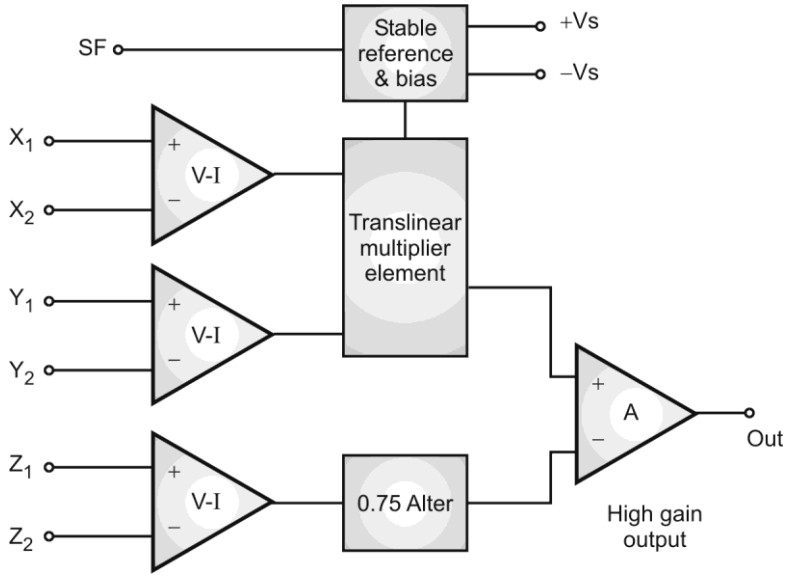
– The squarer is the first stage which gives square of the input.

– OP-amp A, is an integrator which gives the integration of squared input.

– Finally, op-amp A_2 along with the multiplier in its feedback loop performs square rooting operation on the output of op-amp A_1.

– Thus, the final output is the RMS value of the input applied.

GQ. 5.6.3 Draw and explain the functional block diagram and working of multiplier IC 534.



(2E27)**Fig. 5.6.5 : Functional block diagram of the IC 534**

- Fig. 5.6.5 is a functional block diagram of the AD 534.
- Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset.
- The product of the x and y currents is generated by a multiplier cell.
- The difference between XY/SF and Z is then applied to the high gain output amplifier.
- This permits various closed loop configurations and reduces non-linearities due to input amplifiers.
- The generalized transfer function for the AD 534 is given by,

$$V_{out} = A\left[\frac{(x_1 - x_2)(y_1 - y_2)}{SF} - (z_1 - z_2)\right]$$

where, A = open loop gain of output amplifier, typically 700 dB at dc

x, y, z = input voltages (full scale = ± SF, Peak = ± 1.25 SF)

SF = Scale factor, pre-trimmed to 10 V but adjustable by the user down to 3 V.

- In most cases the open loop gain can be infinite, and SF will be 10 V.
- The operation performed by AD 534, can be described in terms of equation\\,

$$(x_1 - x_2)(y_1 - y_2) = 10\ V\ (z_1 - z_2)$$

- The user may adjust SF for values between 10 V and 3 V by connecting an external resistor in series with a potentiometer between SF and $-V_s$.
- The approximate value of total resistance for a given value of SF is given by,

$$R_{SF} = 5.4\ K\ \frac{SF}{10 - SF}$$

- Considerable reduction in noise, bias currents and drift can be achieved by decreasing SF.
- This increases signal gain without increase in noise.
- Peak input signal is always limited to 1.25 SF. So, the overall transfer function will show a maximum gain of 1.25.
- The performance with small input signals is improved by using a lower SF. Bandwidth is unaffected.
- Supply voltages are generally ± 15 V.
- Since all inputs maintain a constant peak input of 1.25 SF, some feedback attenuation will be necessary to achieve output voltage swing in excess of ± 12 V when using higher supply voltages.

What are the applications of multiplier IC AD534?

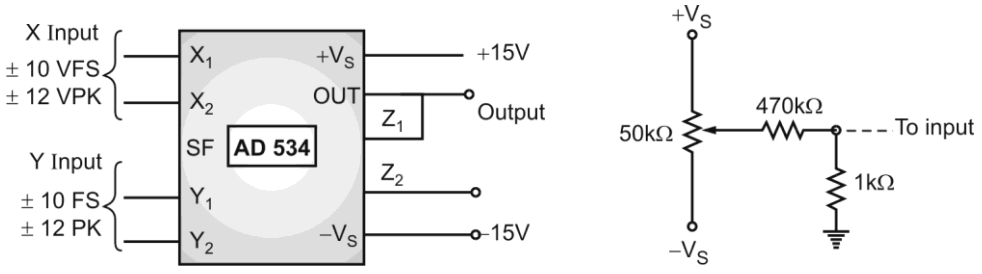
- IC AD534 is used for the following applications :
  1. Multiplier
  2. Squarer
  3. Divider
  4. Square rooter

Explain the application of multiplier IC AD534 as multiplier.

- Fig. 5.6.6 shows the basic circuit arrangement for multiplication.
- The transfer function of the multiplier is given by,

$$\frac{(x_1 - x_2)(y_1 - y_2)}{10\ V} + z_2$$

- The inputs are applied to x and y inputs. The AC signal feed through can be minimized using the optional trimming circuit as shown in Fig. 5.6.6(b) to the x or y input.
- The high impedance terminal z_2 can be used for summing an additional signal into the output. This terminal is referenced to the ground terminal of the system driven.



(a) **(b)**

Fig. 5.6.6 : Basic multiplier connection

XR-2206

Write some features of XR-2206.

1. Low sine wave distortion.
2. Excellent temperature stability.
3. Wide sweep range.
4. Low supply sensitivity, 0.01% V
5. Linear amplitude modulation.
6. TTL compatible FSK controls.
7. Wide supply range, 10 V to 26 V.
8. Adjustable duty cycle, 1 % to 99 %.

Draw and explain the functional block diagram of XR-2206.

– The XR-2206 consists four functional blocks :
  (1) A Voltage Controlled Oscillator (VCO)
  (2) An analog multiplier and sine shaper
  (3) A unity gain amplifier
  (4) A set of current switches

– The block diagram is shown in Fig. 5.7.1.

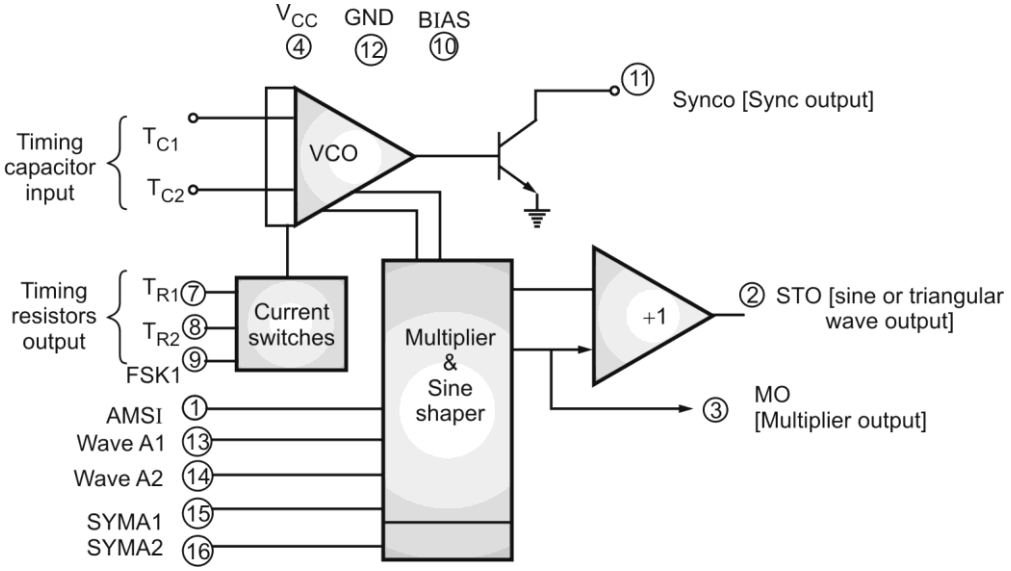


Fig. 5.7.1 : Block diagram of XR-2206

AMSI → Amplitude modulating signal input

Wave A1 → Waveform adjust input 1

Wave A2 → Waveform adjust input 2

Sym A1 → Wave symmetry adjust 1

Sym A2 → Wave symmetry adjust 2

– The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground.

– With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin.

– This input controls the current switches which select one of the timing resistor currents and route it to the VCO.

Applications of XR-2206

Write the applications of XR-2206.

1. Waveform generator
2. Sweep generation
3. AM/FM generation
4. V/F conversion
5. FSK generation
6. Phase-Located Loops (PLL) VCO

Application of XR 2206 as a Waveform Generator

Short note on : XR 2206 waveform generator.

MU - Q. 6(d), May 18, Q. 6(d), Dec. 18, 5 Marks

– The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy.

– The output waveforms can be both amplitude and frequency modulated by an external voltage.

– Frequency of operation can be selected over the range of 0.01 Hz to more than 1 MHz.

– The circuit is ideally suited for communication instrumentation and function generator applications.

– The XR-2206 consists of four functional blocks :

(1) A Voltage Controlled Oscillator (VCO)
(2) An analog multiplier and sine shaper
(3) A unity gain amplifier and
(4) A set of current switches

– The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground.

– With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin.

– This input controls the current switches which select one of the timing resistor currents and route it to the VCO.

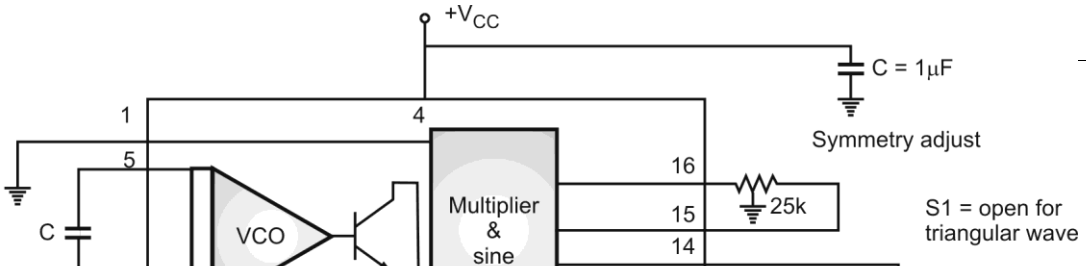


Fig. 5.7.2 : Basic test circuit using IC XR-2206

Short note on : XR2206 waveform generator. ***(Ans. : Refer section 5.7.1(A))*** (Q. 6(d), 5 Marks)

✳ **Dec. 2017**

Q. 5.1 Give any five features of IC 555. *(Ans. : Refer section 5.1)* **(Q. 1(A), 5 Marks)**

Q. 5.2 With the help of a neat circuit diagram explain anyone application of PLL 565. *(Ans. : Refer section 5.5.2)* **(Q. 2(A), 10 Marks)**

✳ **May 2017**

Q. 5.3 Explain the functional block diagram of timer IC 555. *(Ans. : Refer section 5.1.1)* **(Q. 1(d), 4 Marks)**

Q. 5.4 Draw the diagram of a monostable multivibrator using timer IC 555. With the help of waveforms at the trigger input, across the charging capacitor and at the output explain its working. Design the same for a pulse width of 11 ms. *(Ans. : Refer section 5.2.1)* **(Q. 5(a), 10 Marks)**

✳ **Dec. 2016**

Q. 5.5 Draw the diagram of a monostable multivibrator using timer IC555. With the help of waveforms at the trigger input, across the charging capacitor and at the output explain its working. Design the same for pulse width of 11 ms. *(Ans. : Refer section 5.2.1)* **(Q. 2(a), 10 Marks)**

✳ **May 2016**

Q. 5.6 Explain the functional block diagram of timer 555. *(Ans. : Refer section 5.1.1)* **(Q. 1(d), 4 Marks)**

✳ Dec. 2015

Q. 5.7 With the help of neat circuit diagram explain any one application of PLL 565.
(Ans. : Refer section 5.5.3) **(Q. 1(vi), 4 Marks)**

Q. 5.8 Draw and explain the functional diagram of IC555 and explain its operation in astable mode.
(Ans. : Refer section 5.2.2) **(Q. 4(a), 10 Marks)**

✳ May 2015

Q. 5.9 Draw and explain the functional diagram of IC 555 and explain its operation in astable mode.
(Ans. : Refer section 5.2.2) **(Q. 5(a), 10 Marks)**

Q. 5.10 Write short note on : Any two applications of PLL 565.
(Ans. : Refer sections 5.5.2 and 5.5.3) **(Q. 6(c), 5 Marks)**

✳ Dec. 2014

Q. 5.11 Explain any application of waveform generator XR2206 with the help of a neat diagram.
(Ans. : Refer section 5.7.1(B)) **(Q. 1(d), 4 Marks)**

Q. 5.12 With the help of a neat diagram and waveforms at the trigger input, across the capacitor and at the output, explain working of 555 as a monostable multivibrator. Find the values width of 5 mS.
(Ans. : Refer section 5.2.1) **(Q. 3(a), 10 Marks)**

Q. 5.13 Write short note on : Write short note on : Phase-locked loop IC565.
(Ans. : Refer sections 5.5 and 5.5.1) **(Q. 6(1), 5 Marks)**

Chapter Ends

❑❑❑