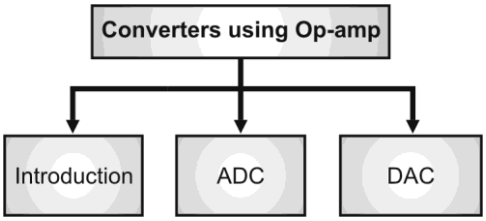
MODULE - 4

Analog to Digital and Digital to Analog Converters

University Prescribed Syllabus

Performance specifications of ADC, single ramp ADC, ADC using DAC, dual slope ADC, successive approximation ADC, Performance specifications of DAC, binary weighted resistor DAC, R/2R ladder DAC, inverted R/2R ladder DAC.

This chapter / unit can be divided into three sections as shown in the chart C4.1.1.



INTRODUCTION

Explain data converters.

The data converters convert one form of data into another form.

- Real world processes produce analog signals like voltage, current, temperature and pressure.
- The rate of flow of such information may be very slow or very fast.
- It is difficult to store, manipulate, compare, calculate and retrieve such data with good accuracy using analog technology.
- Computers can perform these operations quickly and efficiently using digital techniques.
- Therefore it is necessary to convert the analog signals into its equivalent digital data.
- But the computers need to communicate with people and physical processes through the use of analog signals. Therefore digital to analog conversion is necessary.

ADC

Draw and explain the block diagram of A/D converter.

- Analog-to-digital converter converts analog input voltage into digital output.

– Fig. 4.2.1 shows the block diagram of ADC. It accepts input voltage V_a and produces an output binary word $d_1\ d_2\ \ldots..d_n$ of functional value D, so that

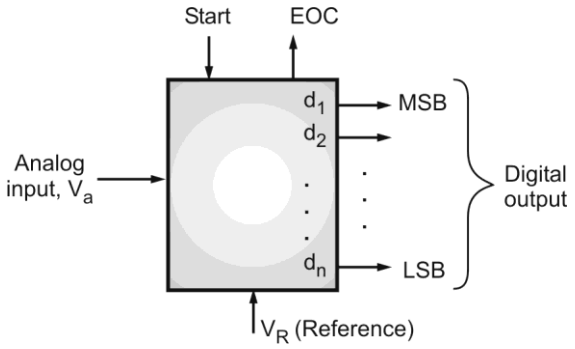
$$D = d_1\ 2^{-1} + d_2\ 2^{-2} + d_3\ 2^{-3} + \ldots.. + d_n\ 2^{-n}$$

where d_1 is the most significant bit and d_n is the least significant bit.

– An ADC has additional two control lines :

(i) Start input to tell the ADC when to start the conversion and

(ii) EOC (End of Conversion) output to announce when the conversion is complete.

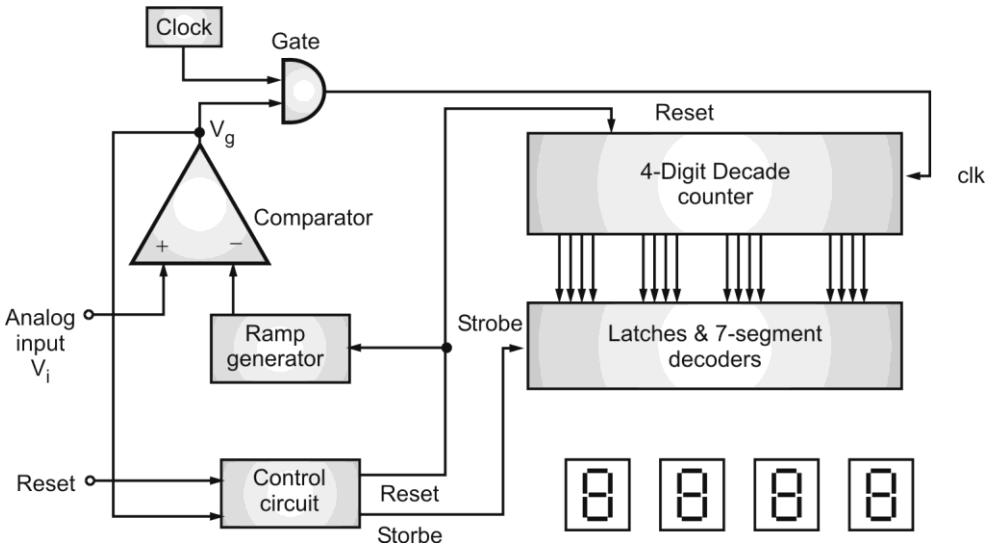


Functional diagram of ADC

Single Slope Type A/D Converter

– This converter technique compares the unknown analog input voltage with a reference voltage that begins at 0V of increases linearly with time. The time required for the reference voltage to reach the value of unknown analog input voltage is proportional to the amplitude of unknown analog input voltage. This time period can be measured using a digital counter.

– The block diagram of single slope type A/D converter is shown in Fig. 4.2.2.



Block diagram of single slope type A/D converter

- Ramp generator, on receiving a RESET signal from the control circuit, increases linearly with time from 0V to a maximum voltage V_m.
- Assume that a positive analog input voltage V_i is applied at the non-inverting input of the comparator.
- When a 'RESET' signal is applied to the control logic, the 4-digit decade counter resets to 0 and the ramp voltage begins to increase.
- Since analog signal 'V_i' is positive the comparator output is high.
- This allows CLK pulse to pass to the input of the 4 digit counter through the AND gate and the counter is incremented.
- This process continues until the analog input voltage is greater than the ramp generator voltage.
- When the ramp generator voltage is equal to the analog input voltage, the comparator output becomes negatively saturated or logic 0 and the clock is prevented from passing through the gate and stops the operation of the counter.
- Then, the control circuit generates a 'STROBE' signal, which latches the counter value in the 4-digit latch, which is displayed on 7-segment displays.
- The displayed value is then equivalent to the amplitude of analog input voltage.

What are the disadvantages of single slope converter ?

1. Single slope converter uses ramp generator circuit, which is integrator circuit. The integrated output voltage is a function of the product of R and C components. i.e.

$$V_o = -\frac{1}{RC}\int_0^t (V_i)\,(dt) + C$$

– Therefore, changes in the value of capacitance and resistance due to temperature affects the integrated output and introduces errors.

2. The drift in clock frequency also causes errors.

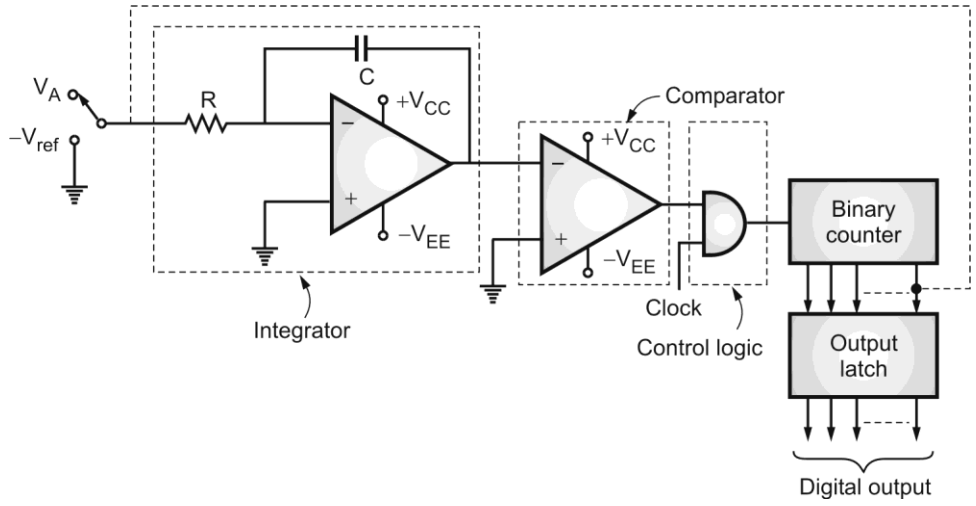
Dual Slope ADC

GQ. 4.2.3 With the help of neat diagram explain the operation of dual slope ADC.

Dual slope type ADC consists of :

1. Integrator 2. Comparator 3. Control logic 4. Binary counter

In dual slope type ADC, the integrator generates two different ramps, one with the unknown analog input voltage V_A and another with a known reference voltage $– V_{ref}$. Hence it is called as dual slope A to D converter. The circuit diagram is shown in Fig. 4.2.3.



(1D26)**Fig. 4.2.3 : Circuit diagram of dual slope ADC**

– The binary counter is initially reset to 0000.

– The input to the integrator is switched to the unknown analog input voltage V_A.

– The analog input voltage V_A is integrated by the inverting integrator and generates a negative ramp output.

– The output of comparator is positive and the clock is passed through the AND gate (i.e., control logic).

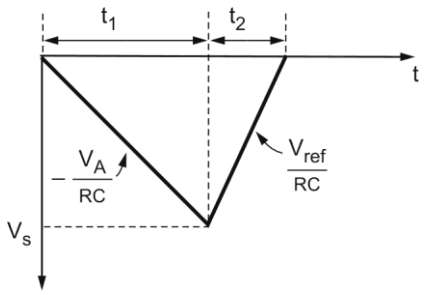
– This results in counting-up of the binary counter.

– The negative ramp continues for a fixed time period t_1, which is determined by a count detector for the time period t_1.

– At the end of the fixed time period t_1, the ramp output of integrator is given by,

$$V_S = \frac{V_A}{R \cdot C} \times t_1 \qquad \ldots(4.2.1)$$

- When the counter reaches the fixed count at time period t_1, the binary counter resets to 0000 and switches the integrator input to a negative reference voltage, $-V_{ref}$.
- Now the ramp generator starts with the initial value V_S and increases in positive direction until it reaches 0V and the counter gets advanced.
- When V_S reaches 0V, comparator output becomes negative (i.e., logic 0) and the AND gate is deactivated.



(1D27)**Fig. 4.2.4 : Output waveform**

- Hence no further clock is applied through AND gate.
- Now, the conversion cycle is said to be completed and the positive ramp voltage is given by,

$$V_S = \frac{V_{ref}}{R \cdot C} \times t_2 \qquad \ldots(4.2.2)$$

where V_{ref} and RC are constant and time period t_2 is variable.

- The dual ramp output waveform is shown in Fig. 4.2.4.
- The amplitude of the negative and ramp voltages can be equated as follows :

$$\frac{V_{ref}}{RC} \times t_2 = \frac{-V_A}{RC} \times t_1 ; \qquad V_A = -V_{ref} \cdot \frac{t_2}{t_1}$$

- Thus the unknown analog input voltage V_A is proportional to the time period t_2, because V_{ref} is known reference voltage and t_1 is the predetermined time period.
- The actual conversion of analog voltage V_A into digital occurs during time period t_2.
- The binary counter gives corresponding digital value for time period t_2.
- The clock is connected to the counter at the beginning of t_2 and is disconnected at the end of t_2.
- Thus the counter counts digital output as,

$$\text{Digital output} = \left(\frac{\text{count}}{\text{sec}}\right) \cdot t_2$$

$$\therefore \text{Digital output} = \left(\frac{\text{count}}{\text{sec}}\right) \left(t_1 \cdot \frac{V_A}{V_{ref}}\right)$$

This can be explained with example as follows :

- Consider the clock frequency is 1 MHz.
- Reference voltage $V_r = -1V$.
- The fixed time period t_1 is 1mS and RC time constant is 1 mS.
- Assume the unknown analog input voltage amplitude $V_A = 5V$.
- During the fixed time period t_1, the integrator output V_S is,

$$V_S = \frac{V_A}{RC} \times t_1 = \frac{(-5)}{1\text{ mS}} \times 1\text{ mS} = -5\text{ V}$$

– During the time period t_2, ramp generator will integrate all the way back to 0V.

$$\therefore \quad t_2 = \frac{V_S}{V_{ref}} \cdot RC = \frac{-5}{-1} \times 1 \text{ mS} = 5 \text{ mS} = 5000 \ \mu S$$

Hence, the 4-bit counter value is 5000 and by activating the decimal point of MSD, seven segment display reads as 5 V.

GQ. 4.2.4 State some advantages of dual slope ADC.

1. High accuracy.
2. Fewer adverse effects from noise.

GQ. 4.2.5 State some disadvantages of dual slope ADC.

1. Slow
2. Accuracy is dependent on the external components.
3. Costly.

Successive Approximation Register (SAR) Method:

Explain analog to digital conversion using successive approximation method.

MU - Q. 3(a), May 18, 10 Marks

Explain the working principle of successive approximation type ADC.

Successive approximation ADC consists of :

1. Successive Approximation Register (SAR)
2. DAC and
3. Comparator

The output of SAR is given to n-bit DAC.

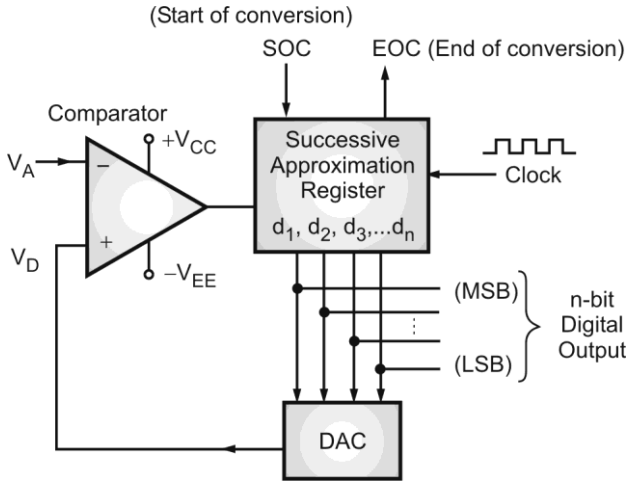
– The equivalent analog output voltage of DAC, V_D is applied to the non-inverting input of the comparator.

– The second input to the comparator is the unknown analog input voltage V_A.

– The output of the comparator is used to activate the successive approximation logic of SAR.

– When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0.

– The digital equivalent voltage is compared with the unknown analog input voltage.



(1D25)Fig. 4.2.7 : Circuit diagram of successive approximation ADC

- If the analog input voltage is higher than the digital equivalent voltage, then the MSB is retained as 1 and the second MSB is set to 1 otherwise, the MSB is set to 0 and the second MSB is set to 1.
- Comparison is made to decide whether to retain or reset the second MSB.

Operation of this method can be explained with the help of an example :

- Let us assume that the 4-bit ADC is used and analog input voltage is $V_A = 11$ V.
- When the conversion starts, the MSB bit is set to 1.

  Now $V_A = 11 > V_D = 8\ V = [1000]_2$
- Since the unknown analog input voltage V_A is higher than the equivalent digital voltage V_D, the MSB is retained as 1 and next MSB bit is set to 1 as follows :

  $V_D = 12\ V = [1100]_2$
- Now $V_A = 11\ V < V_D = 12\ V = [1100]_2$
- Here now, the analog input voltage V_A is lower than the equivalent digital voltage V_D.
- Therefore, the second MSB is set to 0 and next MSB is set to 1 as,

  $V_D = 10\ V = [1010]_2$
- Now again, $V_A = 11\ V > V_D = 10\ V = [1010]_2$
- $V_A > V_D$, hence the third MSB is retained to 1 and the last bit is set to 1.
- The new code is,

  $V_D = 11\ V = [1011]_2$
- Now finally $V_A = V_D$ and the conversion stops.

State some advantages of successive approximation ADC.

1. Conversion time is very small.
2. Conversion time is constant and independent of the amplitude of the analog input signal V_A.

State some disadvantages of successive approximation ADC.

1. Circuit is complex.
2. The conversion time is more as compared to flash type ADC.

State some applications of successive approximation ADC.

It is most widely used in the microprocessor based data acquisition systems.

List various specifications of ADC.

The various specifications of ADC are :

1. Resolution
2. Quantization error
3. Accuracy
4. Gain and offset errors
5. Conversion time
6. Sampling frequency and aliasing phenomenon.
7. Non-linearity or integral non-linearity (INL)
8. Differential Non-Linearity (DNL)

Explain various specifications / characteristics of ADC.

1. Resolution

It is defined as the ratio of a change in value of input voltage needed to change the digital output by 1 LSB.

If the full scale input voltage required to cause a digital output of all 1′s is V_{iFS}, then resolution can be given as,

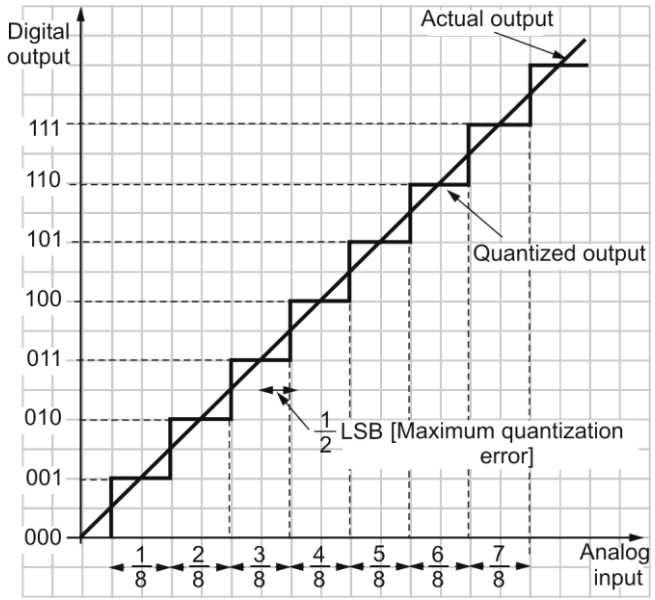
$$\text{Resolution} = \frac{V_{iFS}}{2^n - 1} \qquad \text{where} \quad \text{'n' is the number of bits.}$$

2. Quantization error

For ADC, the digital output is not always the accurate representation of the analog input.

For example, any input voltage between 1/8 to 2/8 of full scale will be converted to a digital word of '001'. This approximation process is called as quantization and the error due to quantization process is called '**quantization error**.'

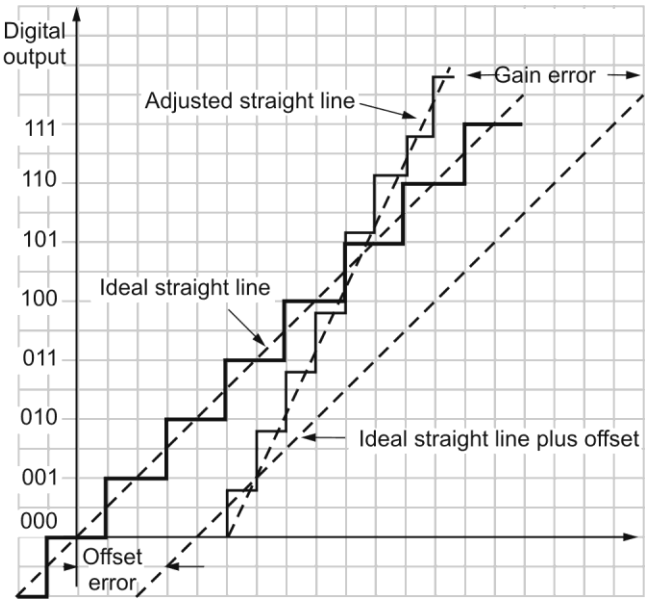
- The maximum value of quantization error is $\pm \frac{1}{2}$ LSB.
- It should be as small as possible.
- It can be reduced by increasing the number of bits.



A graph of input and output voltages of ADC

3. Gain and offset error

- The offset error is the difference between the actual and ideal first transition voltages.
- Gain error is the difference between the actual full scale transition voltage and the ideal full scale transition voltage.



Gain and offset error

4. Sampling frequency and aliasing phenomenon

- According to sampling theorem, the minimum rate at which the analog signal should be sampled must be twice the highest frequency in the analog signal.

  Thus,

  $$f_s \geq 2 f_{max}$$

  With this frequency, it is possible to reproduce analog signal faithfully.
- If the sampling frequency is less than Nyquist rate ($2 f_{max}$), then the faithful reproduction of original signal is not possible.

  In such cases, spurious signals called aliases are produced. The frequency of aliased signal is the difference between the signal frequency and the sampling frequency.

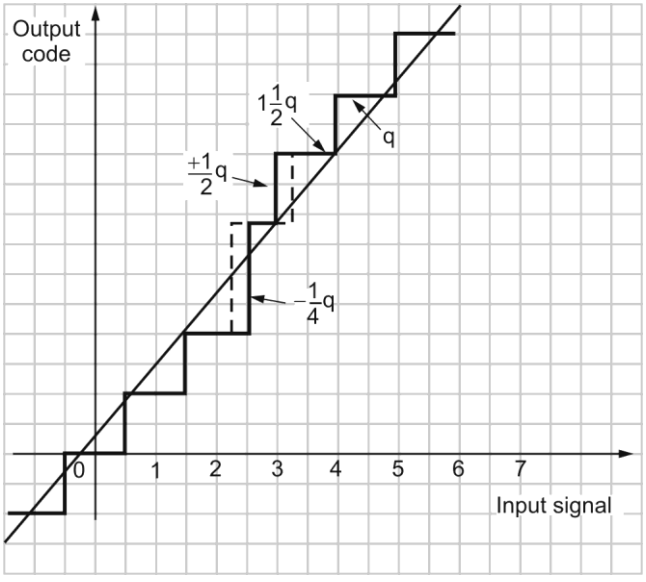
5. Differential non-linearity

Differential non-linearity is a measure of how individual steps may be in error.

It is the difference between the ideal step position and its actual position. A good ADC will hold this error to q/2 where 'q' is the step size.

6. Accuracy

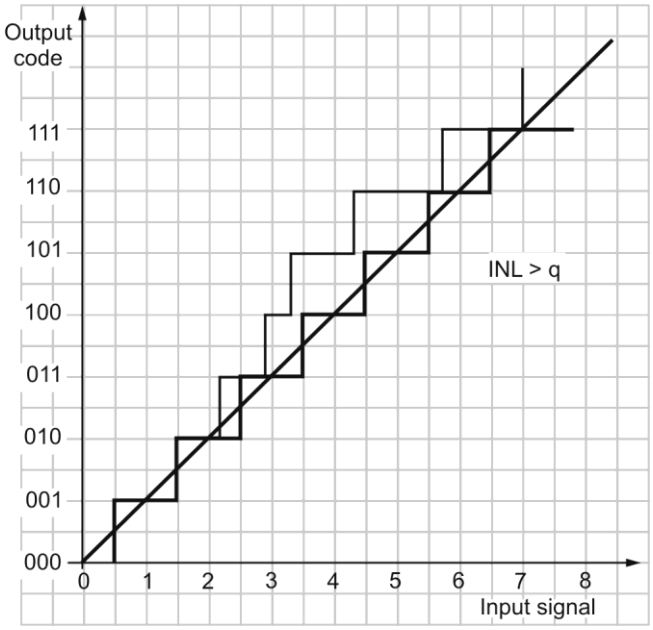
Accuracy is the maximum deviation between the actual converter output and the ideal converter output.



ADC with DNL error

7. Integral non-linearity

Integral non-linearity (INL) is defined as the difference between the actual transition at any level and the ideal transition.



ADC with INL error

8. Conversion time (settling time)

- It is an important parameter for ADC.
- It is defined as the total time required to convert an analog signal into its digital equivalent output.
- It depends on conversion technique used and the propagation delay of circuit components.

Comparison between Different Types of ADC

GQ. 4.2.16 Differentiate between different types of ADC.

Sr. No.	Parameter	Single slop ADC	Dual slope ADC	Counter type ADC	Successive approximation
1.	Speed	Slow	Slowest	Faster than dual slope. Speed is low.	Faster than dual slope.
2.	Accuracy	Poor	Very accurate	Moderately accurate	Moderately accurate
3.	Cost	Low	Low	Low	Moderately high
4.	Advantages	Simple, less complex	High accuracy, low cost.	Simple, less complex	Good speed, high accuracy
5.	Disadvantages	Large conversion time	Slow speed, large conversion time.	Large conversion time	Circuit is complex, conversion time is

					large.
6.	Applications	Applications where low-speed and low power consumption are required	Digital voltmeter	Used in electronics devices and gadgets.	Data acquisition system.

DAC

GQ. 4.3.1 Draw and explain the block diagram of D/A converter.

– Fig. 4.3.1 represents the block diagram of N-bit D/A converter.

– Here, B_{in} is defined to be an N-bit digital word such that,

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots b_N 2^{-N}$$

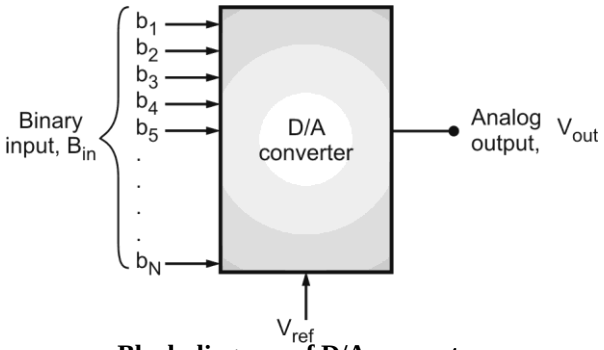
where b_1, b_2, b_3 … b_N may be equal to either zero or one, i.e., (0 or 1) b_1 is most significant bit and b_N is the least significant bit.

– A digital to analog converter produces an output signal of only one polarity, which depends on a sign bit (usually b_1).

– The analog output signal, V_{out} is related to the digital signal B_{in} and V_{ref} as,

$$\mathbf{V_{out} = V_{ref} \cdot B_{in}};$$

where, $B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$



Block diagram of D/A converter

Voltage corresponding to the least significant bit can be expressed as,

$$V_{LSB} = \frac{V_{ref}}{2^N}$$

where 'N' is the number of bits.

– The maximum value of V_{out} is given by,

$$\mathbf{V_{out\ max} = V_{ref}\ (1 - 2^{-N})}$$

Types of DAC

The most commonly used DAC circuits are :

1. Binary weighted resistor DAC.
2. R/2R ladder DAC.

Binary Weighted Resistor DAC

Draw circuit diagram of binary weighted DAC and write its output equation.

With the help of circuit diagram, derive the expression of output analog voltage for a weighted resistor DAC. **MU - Q. 3(b), Dec. 19, 10 Marks**

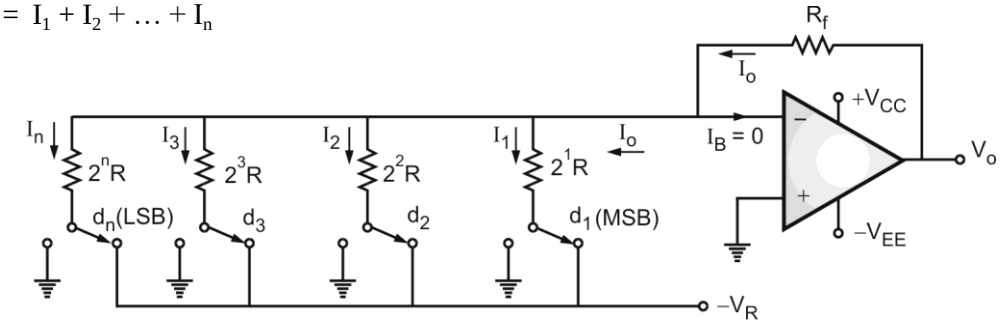
The major components of the binary weighted resistor D/A converter are :

1. The weighted resistor network R to (2^{n-1}) R.
2. n-switches, one for each bit applied to input. Switches are single pole double throw type.
3. A reference voltage V_{ref}.
4. A summing element which sums up the currents flowing in the resistors to give an output proportional to input.

– If the binary input to a particular switch is 1, it connects the resistance to the reference voltage – V_R. And if the input bit is 0, the switch connects the resistor to the ground.

– From Fig. 4.3.2, the output current I_o for an ideal Op-amp can be written as :

$$I_o = I_1 + I_2 + \ldots + I_n$$



(1D8)**Fig. 4.3.2 : Circuit diagram of weighted resistor DAC**

$$I_1 = \frac{V_R}{2^1 R} \cdot d_1$$

$$I_2 = \frac{V_R}{2^2 R} \cdot d_2$$

$$\vdots$$

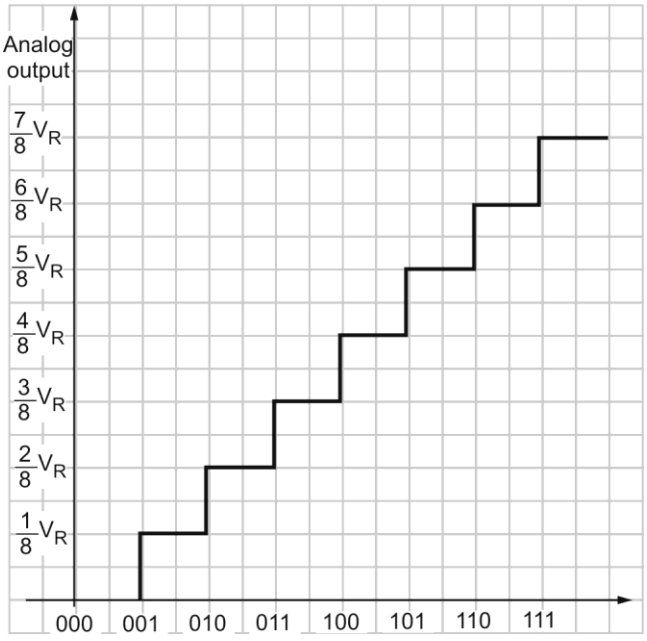
$$I_n = \frac{V_R}{2^n R} \cdot d_n$$

$$\therefore\ I_o = \frac{V_R}{R}[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \ldots + d_n 2^{-n}]$$

Also, $V_o = I_o R_f$

$$\therefore\ \mathbf{V_o = V_R \cdot \frac{R_f}{R}[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \ldots + d_n 2^{-n}]}$$

– The circuit uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 4.3.3.



Transfer characteristics of 3-bit DAC

(Digital Input Code)

What is the advantage of weighted resistor DAC ?

Its circuit is simple to design. Jewelry

What are the disadvantages of weighted resistor DAC ?

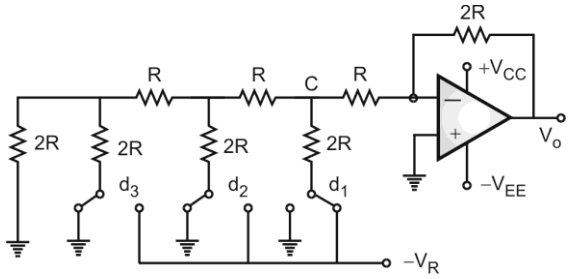
1. Wide range of resistor values are required.

2. For better resolution, the input binary word length should be more.
3. As the number of bit increases, the range of resistance value increases. For 8-bit DAC, the largest resistor value is 128 times the smallest resistor value.
4. Voltage drop across large resistor value, due to bias current, affects the accuracy.

R/2R Ladder DAC

Explain R-2R ladder type digital to analog converter.

- Wide range of resistors are required in binary weighted resistor type DAC.
- This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.
- Fig. 4.3.4 shows the circuit diagram of 3-bit DAC.



Circuit diagram of R-2R ladder DAC

- Here switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100.
- The circuit can be simplified to the equivalent form of Fig. 4.3.5. and finally to Fig. 4.3.8.

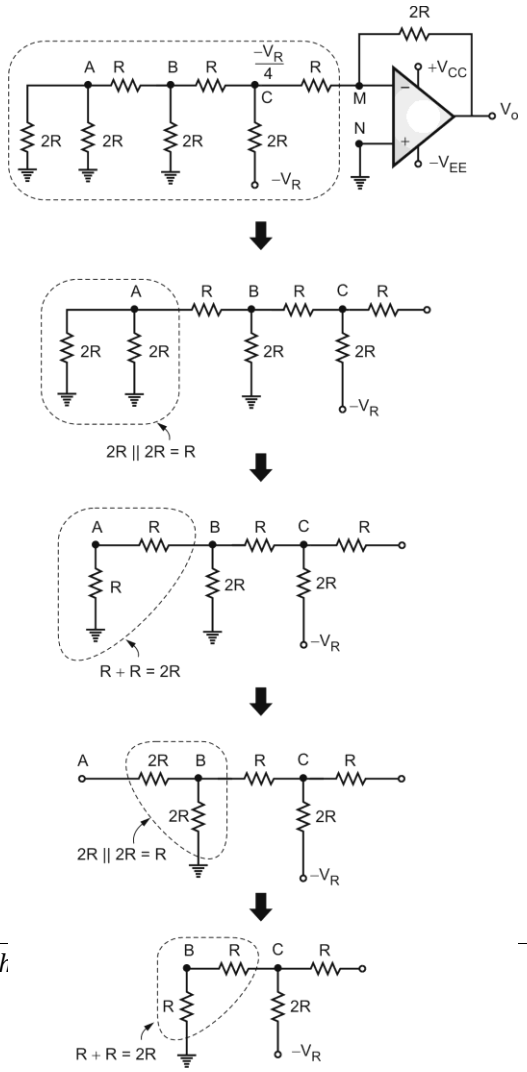


Fig. 4.3.5

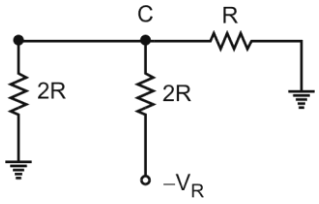


Fig. 4.3.6

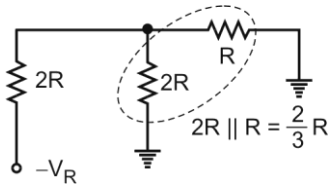


Fig. 4.3.7

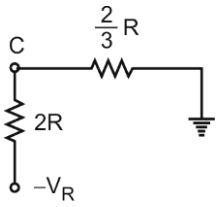


Fig. 4.3.8

In Fig. 4.3.7, $2R \parallel R = \frac{2R \times R}{2R + R} = \frac{2R^{\not 2}}{3\not R} = \frac{2}{3}R$

In Fig. 4.3.8,

Using voltage divider rule,

$$V_C = \frac{-V_R \times \frac{2}{3} \cdot R}{\frac{2}{3}R + 2R}$$

Where, V_R is total voltage

$\frac{2}{3}R \rightarrow$ Resistor connected to ground;

$\frac{2}{3}R + 2R \rightarrow$ Total resistance

$$\mathbf{V_C = \frac{-V_R}{4}} \qquad \ldots(4.3.1)$$

Since it is non-inverting amplifier. Voltage gain is given by,

$A_V = \frac{-R_F}{R_i}$ $\qquad A_V = \frac{V_o}{V_{in}}$, From Fig. 4.3.4.

$V_{in} = V_C$ $\qquad \therefore \; V_o = \frac{-R_F}{R_i} \cdot V_C$ $\qquad \ldots(4.3.2)$

$R_F = 2R$ and $R_i = R$

Put the value of V_C from Equation (4.3.1) in Equation (4.3.2)

$\mathbf{V_o} = \left(\frac{-R_F}{R_i}\right) \cdot V_C$; $\qquad \therefore \; V_o = \left(\frac{-2R}{R}\right) \cdot \left(\frac{-V_R}{4}\right)$

$$\mathbf{V_o = \frac{V_R}{2} = \frac{V_{FS}}{2}}$$

State some advantages of R-2R ladder DAC.

1. We need only two values of resistors. So it is easier to implement the circuit.

2. Number of bits can be increased by adding more sections of R/2R.
3. Due to only two values of resistors, high accuracy and stability can be achieved.

What are the drawbacks of R-2R ladder and weighted resistor types of D/A converters ?

The drawbacks of these methods are :

1. The current flowing through the resistors changes as the input data changes.
2. Power dissipation causes heating.
3. Non-linearity of D/A conversion arises due to varying power dissipation values corresponding to bit pattern. This becomes a serious limitation as the word length increases.

Ex. 4.3.1

An 8-bit DAC converter has a resolution of 10 mV/bit. Find the analog output voltage for the following digital input.

1. 1000 1010 2. 0001 0000

☑ **Soln. :**

▶ **Step 1 :** We know, the decimal equivalent value $D = b_8 2^7 + b_7 2^6 + b_6 2^5 + \ldots + b_1 2^0$

1. For input = 10001010

$$D = (1) \times 2^7 + 0 + 0 + 0 + (1) \times 2^3 + 0 + 1 \times 2^1 + 0 = 128 + 8 + 2 = 138$$

$$\therefore V_o = D \times \text{Resolution}$$

$$V_o = 138 \times 10 \text{ mV/bit}$$

$$\mathbf{V_o = 1.38 \text{ V}}$$

2. For input = 00010000

$$D = 0 + 0 + 0 + (1) \times 2^5 + 0 + 0 + 0 + 0$$

$$D = 32$$

$$\therefore V_o = 32 \times 10 \text{ mV/bit}$$

$$\mathbf{V_o = 0.38 \text{ V}}$$

Ex. 4.3.2

Calculate output voltage of 8-bit DAC for digital input 10000000 and 11011101 with reference voltage of 10V.

☑ **Soln. :**

Given : $V_{ref} = 10\text{V}$

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}; \qquad V_{OFS} = V_{ref} = 10 \text{ V}$$

Also, input is 8 bits so n = 8

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{10}{2^8 - 1}$$

$$\text{Resolution} = \frac{10}{256 - 1}$$

$$\text{Resolution} = \frac{10}{255} = 0.039 \text{ V/bit}$$

$$V_o = \text{Resolution} \times D$$

$$D = b_8 2^7 + b_7 2^6 + b_6 2^5 + \ldots + b_1 2^0$$

1. For digital input 10000000

$$D = 1 \times 2^7 + 0 + 0 + 0 + 0 + 0 + 0 + 0$$

$$D = 128$$

$$\therefore V_o = D \times \text{Resolution} = 128 \times 0.039$$

$$\therefore \mathbf{V_o = 5.01 \text{ V}}$$

2. For digital input 11011101

$$D = 1 \times 2^7 + 1 \times 2^6 + 0 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 + 1 \times 2^0$$

$$D = 128 + 64 + 16 + 8 + 4 + 1$$

$$D = 221$$

$$\therefore V_o = D \times \text{Resolution} = 221 \times 0.039$$

$$\mathbf{V_o = 8.6 \text{ V}}$$

Ex. 4.3.3

What output voltage would be produced by a D/A converter where output range is 0 to 10V and input binary number is :

1. 10 (for 2-bit DAC converter) 2. 0110 (for 4-bit DAC)
3. 10111100 (for 8-bit DAC)

☑ **Soln. :**

1. For input 10 (2-bit D/A converter)

$$V_o = 10 \text{ V} \left(1 \times \frac{1}{2^1} + 0 \times \frac{1}{2^2} \right); \qquad V_o = 10 \left(\frac{1}{2} \right) = \mathbf{5V}$$

2. For input 0110 (for 4-bit DAC)

$$V_o = 10 \left[0 \times \frac{1}{2^1} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4} \right]$$

$$V_o = 10 \left[\frac{1}{4} + \frac{1}{8} \right] = \mathbf{3.75 \text{ V}}$$

3. For input 1011 1100 (for a 8-bit DAC)

$$V_o = 10\text{ V}\left[1\times\frac{1}{2^1}+0\times\frac{1}{2^2}+1\times\frac{1}{2^3}+1\times\frac{1}{2^4}+1\times\frac{1}{2^5}+1\times\frac{1}{2^6}+0\times\frac{1}{2^7}+0\times\frac{1}{2^8}\right]$$

$$V_o = 10\text{ V}\left(\frac{1}{2}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}\right)$$

$$\mathbf{V_o = 7.34\text{ V}}$$

Ex. 4.3.4

The basic step of a 9-bit DAC is 10.3 mV. If 00000000 represents 0V, what output is produced if the input is 101101111 ?

☑ **Soln. :**

The output voltage for input 101101111 is,

$$V_o = 10.3\text{ mV}\,[1\times2^8+0\times2^7+1\times2^6+1\times2^5+0\times2^4+1\times2^3+1\times2^2+1\times2^1\times1\times2^0]$$

$$= 10.3\text{ mV}\,[367] = 3.78\text{ V}$$

$$\therefore\ \mathbf{V_O = 3.78\text{ V}}$$

Ex. 4.3.5

Calculate the values of LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10V range.

☑ **Soln. :**

$$\text{LSB} = \frac{1}{2^8} = \mathbf{\frac{1}{256}}$$

For 10 V range

$$\text{LSB} = \frac{10\text{ V}}{256} = \mathbf{39\text{ mV}}$$

and $$\text{MSB} = \frac{10}{2^1} = \mathbf{5V}$$

Full scale output = (Full scale voltage – 1 LSB)

= 10 V – 0.039V = **9.961 V**

Important parameters or specifications of D/A converter

List and explain the various performance parameters of DAC.

MU - Q. 5(b), Dec. 19, 10 Marks

1. **Accuracy :** It is the error between actual output of a D/A converter to the expected or theoretical output.
2. **Full scale voltage (FSV) :** It represents the maximum output voltage for the D/A converter when all the bits of the digital input are 1.

$$\text{FSV} = V_R\left[1-\frac{1}{2^N}\right]$$

where, V_R is the reference voltage and N is the number of input bits.

3. **Resolution :** It is the smallest change that can occur in the output when the input is changed by 1 LSB.

$$\% \text{ Resolution} = \frac{\text{Step size}}{\text{FSV}} \times 100$$

$$\text{or } \% \text{ Resolution} = \frac{1}{2^N - 1} \times 100$$

% Resolution depends on number of bits and improves as the number of bits increases.

4. **Monotonicity :** It means that the output increases with increase in input or decreases with decrease in input.

5. **Linearity :** It is the maximum deviation from the straight line drawn through input-output plot. Linearity guarantees monotonicity.

6. **Settling time :** It is the time taken by D/A converter to settle in $\pm \frac{1}{2}$ LSB of its final value when a change occurs in the input.

7. **Offset Error :** It is defined as the non-zero level of the output voltage when all inputs are zero. It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.

   It adds a constant value to all output values as shown in Fig. 4.3.10.

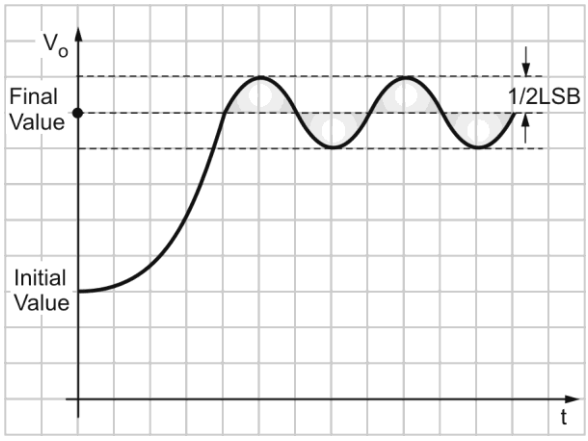


Fig. 4.3.9 : Settling time of D/A converter

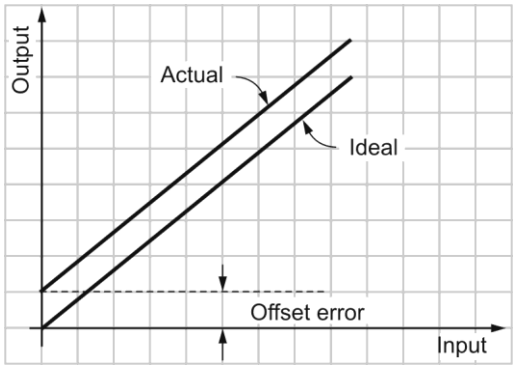


Fig. 4.3.10 : Offset error

Difference between binary weighted and R/2R ladder DAC

GQ. 4.3.11 Differentiate between DAC types, i.e., binary weighted resistor and R/2R ladder DAC.

Sr. No.	Parameter	Binary weighted resistor DAC	R/2R ladder DAC

Sr. No.	Parameter	Binary weighted resistor DAC	R/2R ladder DAC
1.	Speed	Fast	Slower
2.	Construction	Large range of resistors are required.	Only two resistor values are used.
3.	Cost	Expensive	Cheap.
4.	Complexity	Difficult to manufacture, as weighted resistors are used.	Easy to manufacture.
5.	Accuracy	Poor	Good
6.	Applications	Display, data acquisition system.	Motor control

Comparison between DAC and ADC

GQ. 4.3.14 Compare DAC and ADC.

Sr. No.	D/A converter	A/D converter
1.	Input is digital signal.	Input is analog signal.
2.	Output is analog signal.	Output is digital signal.
3.	It produces an analog signal according to its digital form.	ADC samples the analog signal to allow the processor to read it in digital form.
4.	It is an output device.	It is an input device.
5.	DAC is used to generate signal or play speech.	ADC is used to measure voltage or record speech.

UNIVERSITY QUESTIONS AND ANSWERS

✳ **Dec. 2019**

Q. 4.1 With the help of circuit diagram, derive the expression of output analog voltage for a weighted resistor DAC. *(Ans. : Refer section 4.3.1(A))* **(Q. 3(b), 10 Marks)**

Q. 4.2 List and explain the various performance parameters of DAC.
(Ans. : Refer Section 4.3.1(B)) **(Q. 5(b), 10 Marks)**

✳ **May 2018**

Q. 4.3 Explain *R-2R* ladder type digital to analog converter.
(Ans. : Refer section 4.3.1(B)) **(Q. 2(b), 10 Marks)**

Q. 4.4 Explain analog to digital conversion using successive approximation method.
(Ans. : Refer section 4.2.4) **(Q. 3(a), 10 Marks)**

✳ **Dec. 2018**

Q. 4.5 Explain the working principle of successive approximation type ADC.
(Ans. : Refer section 4.2.4) **(Q. 3(b), 10 Marks)**

Chapter Ends…

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