ELEC4123 ELECTIVE TASK REPORT

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PROBLEM STATEMENT

The overarching design problem was collectively perceived by the team to be: "Electronically translating a patient's thoughts into accurate and audible dialogue."

IMPORTANT FEATURES

- Must think about the practicality of the design approach. Is it viable to use in real life? How is it powered? How does it interact with the patient?
- Interfacing between tasks.

FILTRATION

Upon initial research and inspection of the signals provided, it was discovered that EEG signals occupy microvolt level amplitudes. Also, these signals are highly susceptible to noise (such as muscle movements, eye saccades and pink noise).

Key challenges are:

- To amplify the EEG signals to MCU voltage range with low distortion and noise.
- To find a balance with the trade-off between the noise reduction circuitry and minimising component noise. More components means more noise reduction functionality but more components also means more component noise.

SIGNAL PROCESSING

The goal is to achieve a high detection rate in real time. The best algorithms that give good detection rates have higher time complexities, hence they are harder to implement in real time.

Key challenges are:

- Balance the trade-off between real time processing speed and effective detection rate.
- Navigating ambiguities in breaking down a large signal into smaller words to mimic regular human speech, i.e., what is a reasonable 'frame' size?

AUDIO PRODUCTION

Key Challenges are:

- Taking a low voltage analogue signal and amplifying it whilst maintaining a delicate balance between efficiency and THD/spectral characteristics.
- Keeping efficiency high while minimising power consumption which would require a balance between complexity and component count.
- Modelling and accounting for the non-idealities of a realistic speaker.

CONSOLIDATION

It is important to consider how all the tasks will come together to work as one holistic system to ensure outputs remain precise and it is safe to use in a medical environment.

Key Challenges are:

- Condensing all tasks onto a PCB of minimal size so it is practical for real life use
- Minimising signal interference (such as cross talk, ground loops, parasitic capacitance, EMI) for accurate functionality.

BEHAVIOURAL CHALLENGE

- The large breadth of knowledge required to breakdown and complete the task and the difficulty in distributing tasks among the team based on individual expertise and availability

DESIGN CONCEPT AND REASONING

OBJECTIVES & BENCHMARKS-

FILTRATION

The main objective for the filtration part of the circuit is to aim for a balance between noise reduction circuitry and minimizing component noise.

For this part, it is ideal to implement a gain amplifier to make it easier for the microcontroller to sort the input signals into its corresponding bands.

Benchmarks to achieve:

- Realistic noise figure for the filtration part of the circuit is around 2dB-15dB
- ADC selection with high GBP and High slew rate
- Low input referred noise of around 1nV/√Hz
- 3dB cut off at 40Hz for matching the signal bands

SIGNAL PROCESSING

Key objective is to detect the input signals in real time for outputting through a speaker.

Benchmarks to achieve:

- Sampling and Time resolution: Bounded by the Nyquist criterion to avoid aliasing. Sampling rate of at least 256Hz must be chosen.
- Feature extraction scheme: Timing must be real time i.e., processing time on the order of 300ms - comparable to buffer size.
- Detection rate: Must accomplish at least 95% for a usable experience.
- Buffering: Simulate real time audio pause. 300ms pause
- Noise performance: Must still achieve >= 95% detection rate in non-ideal conditions.

AUDIO PRODUCTION

Objective for this part includes creating a Power supply for the first two parts of the circuit as well as making sure the output is relayed through the speaker.

Benchmarks to achieve:

- Bandwidth and flatness: Bandwidth roughly 20k because of limits for human hearing bandwidth 3db drop off should be between low: 20hz, high: 20khz
- Open loop bandwidth: required to be high
- Power delivered: Low as reasonably possible, limit on active biasing etc. Balance with efficiency - 40mW
- THD: the main focus, below 1% and ideally 0.1%. Achieved through a closed loop system that linearizes the output over the crossover distortion period (refer to Deliverable 4)
- AB amplifier choice
- Limit the component count. Zobel network tuning to particular TSP

SOLUTION & REASONING

OVERVIEW OF SOLUTION CONCEPT

Low-noise preamplifier → Microcontroller (feature extraction)

↓

Power amplifier speaker output

FILTRATION

Challenge 1:

To amplify the EEG signals to MCU voltage range with low distortion and noise.

Noise filtration is achieved with a low noise amplifier, low pass filtering and active removal of noise sources. EEG input voltage range is 10-100uV, output range is 0-3.3V.

Key methods to overcome this challenge were:

- Putting op amps in parallel to improve spectral noise characteristics
- Choosing low noise amplifiers
- Performing second order low pass filtering
- Using adjustable gain amplifier to

Meeting objectives:

Through a component choice of low noise precision op amps, an average noise figure of 3.57db was achieved. Furthermore, small resistor values were used to keep component noise low.

Challenge 2:

To find a balance with the trade-off between the noise reduction circuitry and minimizing component noise.

This challenge was met by experimenting with different op amp configurations. Initially only one op amp was used for the preamplification, however, noise at the output was relatively high. Parallelising op amps reduced noise spectral density overall however increased space on the PCB. The optimal number of op amps used to solve this problem were 6. Any less and the output had more noise and any more than 6, and component noise and space increases didn't justify the use.

To simulate component noise, a variety of noise sources were added simulating the effect of an additional component.

Meeting objectives:

Noise was significantly attenuated using low pass filters hence high frequency noise above 40hz was reduced significantly.

SIGNAL PROCESSING

Challenge 1:

Balance the trade-off between real time processing speed and effective detection rate.

In order to meet this challenge effectively, a hybrid implementation of short-time Fourier transform (high speed, lower complexity, mediocre detection rate) and peak detection for detecting false positives for beta band (higher complexity, slower speed). Hence by utilizing this approach a balance was achieved between approach complexity and computational complexity.

Meeting objectives:

Upon implementation of these methods a detection rate of 96% was recorded across all samples and custom test cases. Furthermore, this approach allowed real time processing.

Challenge 2:

Navigating ambiguities in breaking down a large signal into smaller words to mimic regular human speech, i.e., what is a reasonable 'frame' size

For the solution concept to meet this challenge, a literature review was conducted for obtaining lengths of pauses in natural speech. Similarly, the frame size (after research) was chosen to be 1sec to mimic the patterns of user thought. The output between words was buffered using a 0 padded signal with an average buffer size of 0.3seconds, and the processing speed was fast enough to process the next frame whilst buffering was occurring - offering a seamless experience.

Meeting objectives:

Here the frame size, buffer length and sampling rate choices allowed the solution concept to effectively break apart the signal and deliver a user experience worthy of usage.

AUDIO PRODUCTION

Novel features: Adjustable volume control, component minimisation, Zobel network, extremely high bandwidth, outstanding THD, minimizing cross-over distortion

Challenge 1:

Taking a low voltage analogue signal and amplifying it whilst maintaining a delicate balance between efficiency and THD/spectral characteristics.

To meet this challenge a choice was made between class A, B and AB amplifiers. Class A amplifiers have low efficiency and low distortion, AB amplifiers have better efficiency and slightly higher distortion, and class B amplifiers have the highest efficiency and highest distortion.[1] Minimizing THD was the key priority, as THD related to the clarity of produced sounds. Efficiency was the next important metric. To strike a balance between the two, a class AB amplifier configuration was used.

Meeting objectives:

Using this method, a THD of 0.1%, higher efficiency approaching 50% was reported. The solution concept minimized power draw to 40mW by minimizing the number of active components in the design.

Challenge 2:

Modelling and accounting for the non-idealities of a realistic speaker.

The mass of a speaker, inductance, capacitance, force of membrane vibration and other key real-world phenomena require extra attention in order to reproduce a realistic model for audible sound. A Zobel network was implemented to tune these electromechanical parameters also known as Thiele/Small Parameters (TSP).[2] This network serves as a practical method to neutralize instabilities at high frequencies, coil inductance and other realistic non idealities.

Meeting objectives:

The implementation of this section culminated in effective gain and bandwidth (2.51 and 1.061Mhz respectively).

HIGH LEVEL BLOCK DIAGRAM

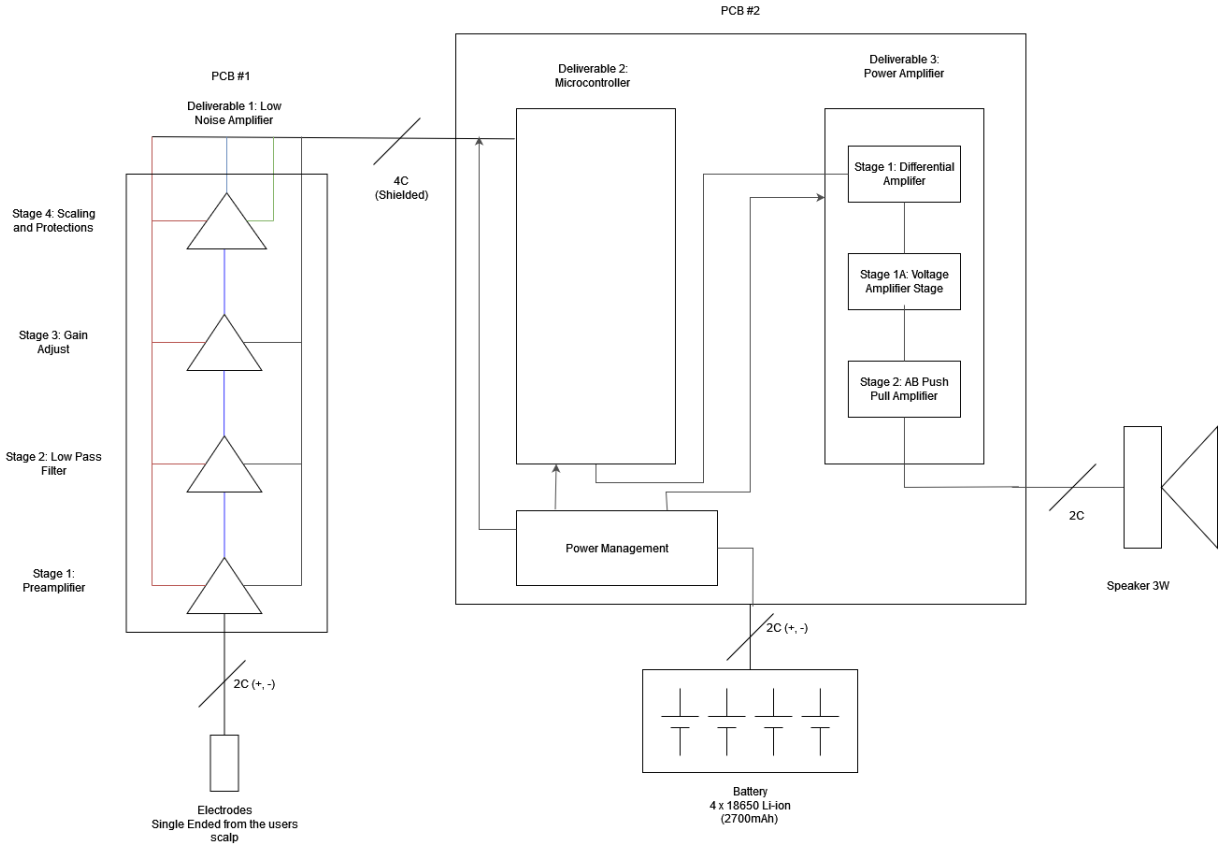


Figure 1 High level block diagram

TASK ALLOCATION

The tasks were allocated based on each member's strength and ultimately what they felt the most comfortable with to maximize productivity and reduce any delays caused by lack of fundamental knowledge for their allocated task.

Although each deliverable was primarily handled by one individual, other team members would be often encouraged to pitch in with any suggestions or ideas relevant to the task at hand.

Primarily, task and time allocation for each deliverable and its subcomponent contributors was done through a Gantt chart as shown below. It can be inferred from the Gantt chart how each deliverable was primarily handled individually by each of the group members.

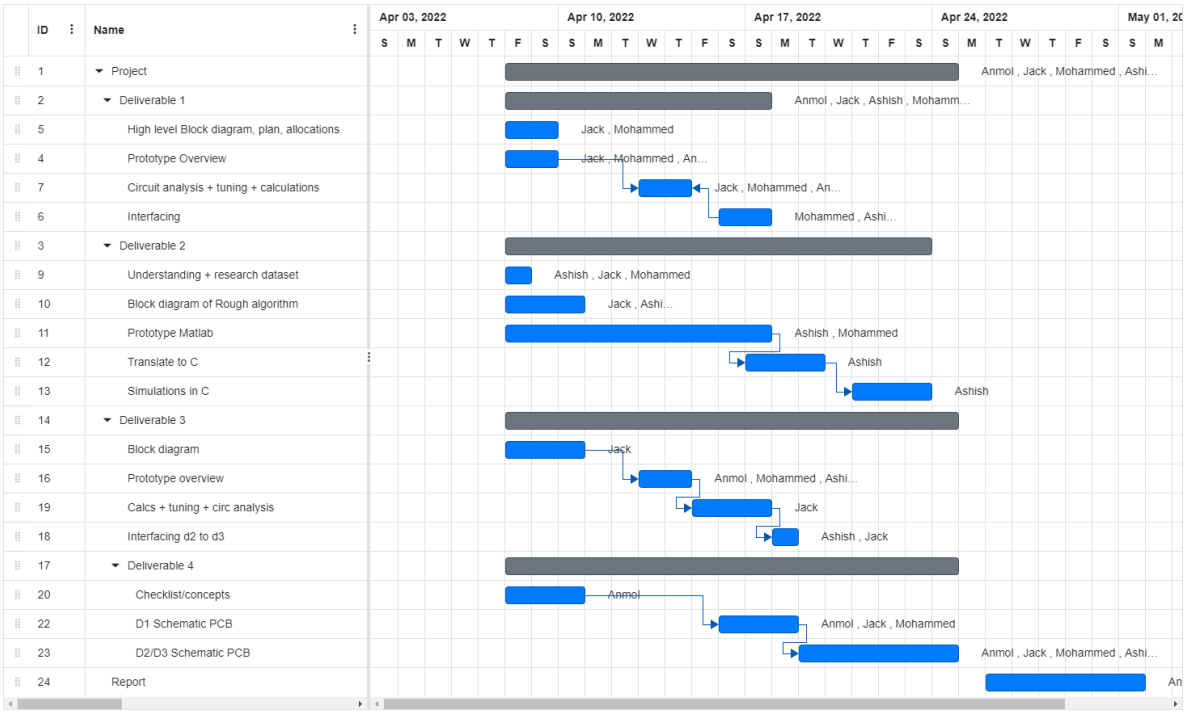


Figure 2 Gantt Chart

TASK DESCRIPTIONS

DELIVERABLE 1

Author: Mohammed Arib

1.1 INTRODUCTION

EEG signals contain a high amount of random and/or repetitive noise which hinders effective analysis of useful information hidden within the signal. This recording circuit is purposed to extract this information by removing redundant noise artifacts through effective filtration techniques while also amplifying the signal so it can be processed on the MCU.

1.2 NOVEL FEATURES

- Parallel pre-amplifier configuration for better noise performance [3]
- Adjustable gain amplifier to record wider variety of signals such as EMG and LFP
- Removing large noise artefacts such as blinking, unstable electrode contacts, swallowing [4]
- Effective bipolar to unipolar signal conversion to minimise component count
- Minimising PCB size by using an even number of op amps to utilise dual package ICs

1.3 STAGE 1: PRE-AMPLIFIER AND DC BLOCKER

Prior to designing the circuit, it was important to determine whether it is better to amplify before filtering or vice versa. Research shows that filtration should be conducted after low noise amplification to achieve the best possible noise figure [3], this is because filtering attenuates the signal bringing the voltage level close to the noise which would then be amplified giving a poor signal to noise ratio.

The first stage of the circuit is a pre-amplifier which allows the amplification of low voltages with low distortion. This was achieved by using a very low noise amplifier (LT1028) with a voltage noise density of 1nV/√Hz at 100Hz. The total noise density of the amplifier stage was significantly improved by implementing a parallel configuration of pre-amplifiers. For a two-level pre-amplifier configuration, the total input referred noise density is reduced by a factor of √2 [5]. This can be shown for a general number of op amps in parallel with the formula:

$$\text{Total noise of op-amps} = N/\sqrt{n}$$

Where N is the noise density of the op-amp, n is the number of op-amps in parallel

Using the above formula for this circuit, the total input referred noise from the op-amps would be:

$$1/\sqrt{2} = 0.7\text{nV}/\sqrt{\text{Hz}}$$

The total noise of this stage is further improved by choosing small feedback resistors to keep the impedance level and component voltage noise as low as possible.

The second part of this stage is a DC blocker which is used to remove any offset voltage present in the EEG signal. The blocker uses a simple topology of consisting an inverting op-

amp followed by a decoupling capacitor at the output to remove the DC offset. It is necessary to remove any offsets in sounds signals to avoid static and crackling noises [6]. The effectiveness of the blocker can be visualised in Figure 2 and 3 showing the original EEG signal and the signal after offset removal.

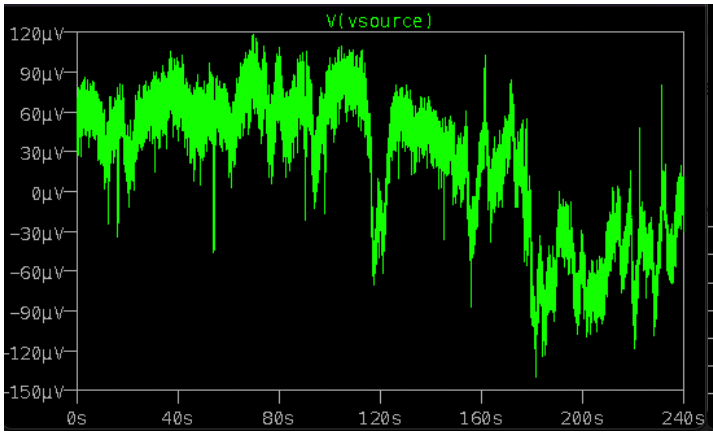


Figure 3 Original EEG signal with 60uV offset

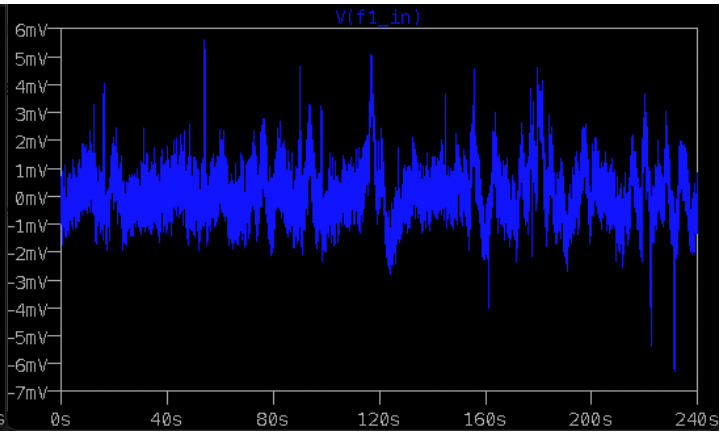


Figure 4 EEG signal after DC blocker with no offset

1.4 STAGE 2: FILTRATION

The next stage of the circuit is a second order Low pass filter tuned to have a 3dB cut off at 40Hz (shown in Figure 4) to match the range of EEG signal bands from delta to beta. A higher order filter has higher attenuation for frequencies above the bandwidth therefore this stage uses a second order filter for a 40dB/dec drop after 40hz which can be seen in Figure 3.

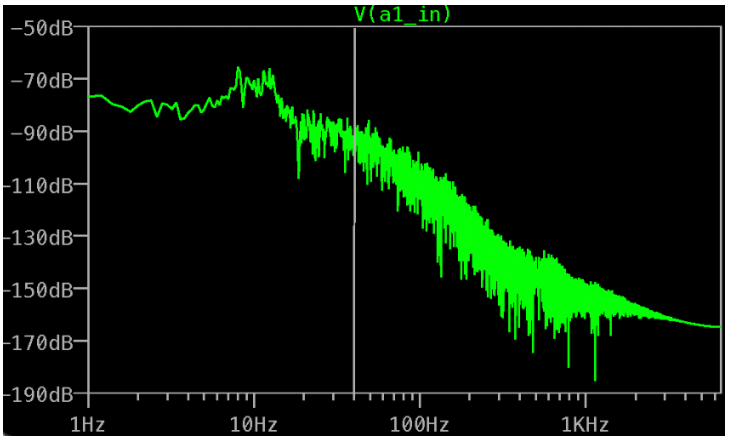


Figure 5 FFT of EEG signal with 40Hz point marked at grey line

A Sallen Key filter topology is used to construct the low pass filter due to its simple design and the ease of cascading RC components to achieve a higher order filter [7], hence reducing component count. This topology also minimizes the gain-bandwidth requirement of the op-amp so the same op-amp can be used as in the Stage 1 to keep a low voltage density and enable the use of the dual package IC available hence minimizing the PCB area and making the device more practical.

1.5 STAGE 3: ADJUSTABLE GAIN AMPLIFIER

The next stage is used to amplify the EEG signal while maintaining its spectral characteristics to increase the resolution up to the ADC voltage level. This is essential to do so that the signal can be accurately quantised and analysed in the MCU. To achieve this an adjustable gain amplifier is implanted using a simple inverting amplifier with a potentiometer as the feedback resistor.

Literature review states that EMG signals are used to record skeletal muscle activity with an amplitude range of 10-20mV [8] putting them at a much higher voltage level than EEG signals. The potentiometer allows the user to change the feedback resistance, in turn changing the gain of the amplifier to accommodate for signals with a greater voltage level.

Due to the high gain required to bring the signal to ADC voltage level of 3V as shown in Figure 5 and 6, the amplifier, LT1630, was chosen based on its high GBP (30Mhz) and slew rate (30V/us) characteristics. This amplifier also maintains it performance at a low supply of 3V which makes it suitable to use for battery powered systems such as this.

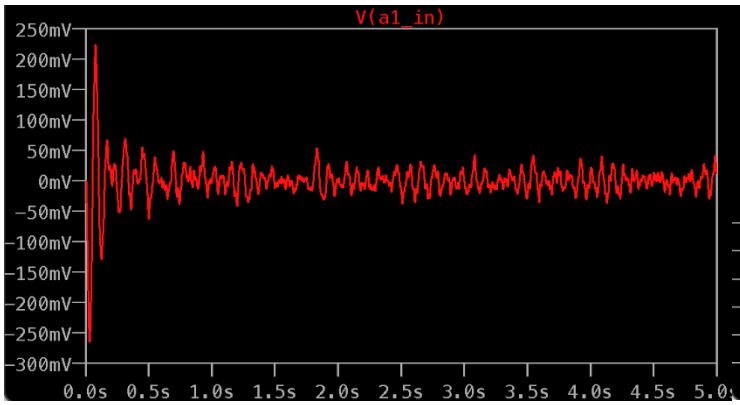


Figure 6 EEG Signal after LPF

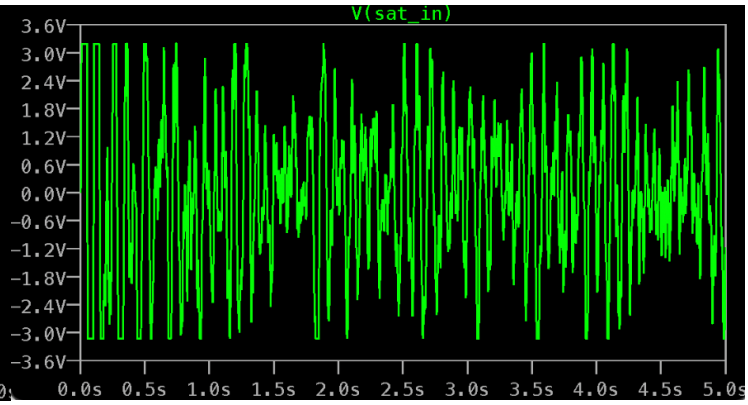


Figure 7 Signal after amplification

1.6 INTERFACING AND ADC SELECTION:

Before explaining the final stage of the circuit, it is important to delve into how this circuit will be interfaced with the MCU and the choices need to be made to achieve that. The analogue signal that this circuits outputs needs to be passed into an ADC before it can be analysed in the MCU. When digitising an analogue signal, parameters such as noise floor and quantisation noise need to be considered.

Noise floor is the sum of the noise each individual component generates in the system [9]. The component noises are accounted for when calculating a noise figure for the system since noise and signal are independently extracted for input and output through LTspice when calculating the noise factor. An ideal noise figure is 0 and through research a realistic noise figure is said to be between 2dB-15dB [10]. The noise figure obtained for this circuit can be seen in the Figure 7 with the peak at approximately 10dB and an average of 3.57dB. Since EEG signals are very susceptible to noise a figure of 3.57dB is acceptable.

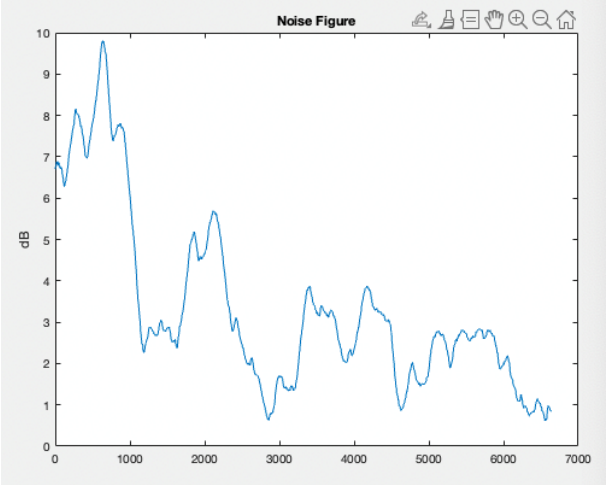


Figure 8 Noise Figure

Quantisation noise is an inevitable effect of converting an analogue signal to a discrete form. It is caused by rounding errors between the real analogue signal and the bit resolution of the ADC [11]. To reduce the quantisation noise level a low pass filter can be used at the output of the ADC which can be implemented digitally on the MCU.

Taking these parameters into consideration, the ADC built into the MCU will be sufficient for interfacing which would also reduce component count and minimise PCB size. The on-board ADC operates within a voltage range of 0-3.3V and has a sufficient resolution of 12 bits giving a dynamic range of 72.4dB for the system. This will appropriately map the analogue signal into the digital domain.

1.7 STAGE 4: SCALING AND PROTECTION

The final stage of this circuit is a unit gain buffer to convert the bipolar signal to a unipolar signal range which the ADC takes. A comparison between the two signals is shown in Figure 8 below, where the green signal is the output of the adjustable gain amplifier, and the blue signal is the output of the unity buffer.

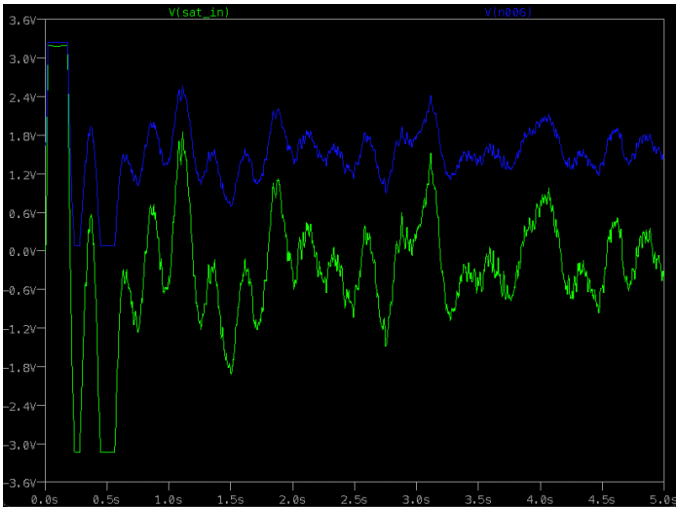


Figure 9 Output of amplifier vs output of buffer

The op-amp used for this stage does not require any new or unique characteristics compared to the previous stage therefore the same op-amp is used. Also, selecting the same op-amp allows for the use of the dual package IC hence making the device more practical by decreasing the size of the PCB.

The second purpose of this stage is to saturate the signal, so it does not exceed 3.3V to protect the ADC and MCU from overheating.

This is a high priority due to the device functioning in an environment that requires human contact. Frequent saturation of the EEG signals is not ideal since op-amps experience a recovery phase when there is signal saturation and if the signal is large if enough in amplitude, information will be lost in the recovery phase.

Therefore, this buffer protection is acts as the last line of defence and the adjustable gain amplifier must be used to adjust the signal amplitude to avoid saturation for best signal output.

DELIVERABLE 2

Author: Ashish Dutta

2.1 INTRODUCTION

Choose simple, effective, and novel approach. Simple designs mean faster processing times (better for real time analysis) less error prone. Effective designs mean a good detection rate. Novel approach to get new performance and improve probability of patenting- which improves market edge (this task is supposed to mimic a real product after all).

2.2 OVERVIEW

D2 interfacing ⇨ Pre-processing data ⇨ Process data/feature extraction ⇨ Output to D3.

2.3 NOVEL FEATURES:

- Filter tuning, memory management and computational optimisation
- Peak detection algorithm – weighting EEG bands differently
- High detection rate: 96%
- Ideas from Short Time Fourier transform (STFT)
- Signal denoising, multiresolution analysis
- Buffering output to reflect natural speech patterns

2.3.1 Algorithm Breakdown and Parameter Choice:

The discrete input signal is broken down into 'windows' or 'frames.' Each frame represents a word. A natural question arises, how long should a frame be?

Frame choice was based on the following reasoning:

- If frame length too long: We miss out on information (i.e., words)
- If frame length too short (then we are not representing user's intentions correctly)
- Correct frame length accurately captures when user thinks of a word.

Based on a paper called "EEG signal processing in brain computer interfaces" by Garces (et al) [13], the rate at which EEG signals fluctuate in **conscious** Brain Computer Interfaces is roughly 1 second. Thus, the signal is broken down into 1 second windows. Obviously, this criterion does not apply completely to Delta waves which are slow and are usually present in deep sleep or meditation.[14]

From here a short time Fourier transform is performed on the windowed signal. From here the powers in each frequency band are calculated using Parseval's theorem [15].

2.3.2 Parseval's Theorem:

$$\sum_{n=0}^{N-1} |x[n]|^2 = \frac{1}{N} \sum_{k=0}^{N-1} |X[k]|^2$$

The maximum of these powers is outputted, and the corresponding wav file is outputted. An important issue to note is the uncertainty principle, governed by the equation below.

$$\Delta t \Delta f \geq \frac{1}{4\pi}$$

Essentially if there is a good time resolution, there cannot be a very good frequency resolution and vice versa. EEG waves are dynamic in nature and not static. STFT is the best for analysing signals with frequency content that is static, [16] but it does not give the frequency component of a signal at a given time. It only gives the frequency component across a timed window. Although the detection rate was very accurate, future iterations could solve this problem by applying ideas from the Wavelet transform. More depth is given in the reflection section of the report.

In this task only Delta (0-4), Theta (4-8), Alpha (8-12) and Beta waves (12-40hz) were considered, practically speaking, delta waves are dominated by 1/f noise at frequencies ranging from 0-0.5hz.[17]

Hence when filtering the signal, filter cut offs were designed in a way to mitigate large sources of 1/f noise. Although this task does not need to detect gamma waves (40-100hz), noise from surroundings 40-50hz also tends to interfere with signals (especially beta signals at the edge of the 40hz). To reduce this noise, filters with sharp cut offs were chosen.

Novel features of filter choice:

- Optimal window choice (Hamming vs Hanning vs Blackman-Harris)
- Sharp attenuation
- Optimising for filter order to avoid excessive memory drain.

2.4 FILTER CHOICE AND DESIGN THINKING

Initially IIR filters were chosen for their lower computational complexity. Linear phase was not exactly an issue as we only care about the magnitude of the filter response for the calculation of the powers. A Chebyshev filter was chosen as: A small passband ripple distributed across a frequency range does not alter relative powers (as the ripple occurs between all frequency bands) and the Chebyshev filter has a maximal drop off (especially important at the edges of frequency bands to avoid confusion and false positives).

However, upon implementing this in python – the internal libraries did not produce the best filter responses. This is due to the mathematical approximations occurring in python not being

able to fully imitate the Chebyshev filter exactly. Hence a quick pivot was done to an FIR approach. A window size of 512 was chosen as:

- Best filter response
- Higher order means more computation and more memory. Higher order approximations did not fare well in terms of this cost benefit.

To further minimise computational complexity, these coefficients were precalculated and stored on the MCU in memory. At run time these coefficients were simply accessed in memory- saving time and speeding up the program.

To further speed up the program even more, powers of 2 were chosen for window lengths; as the internal implementation of many FFT algorithms run faster with vector lengths corresponding to a power of 2.[18]

2.4.1 Window Choice:

The windowing function is essential in smoothing discontinuities in the FFT of a truncated signal [19]. The following criteria were prioritised when choosing the filter window:

- Sharp attenuation
- Passband signal preservation (minimal distortion)
- Small sidelobes in stop band

Examined windows: The following windows were available for use in the in-built python libraries.

Hanning:

Main Lobe: Width of the main lobe is comparable to Hamming window however smaller than Blackman Harris (good thing).[20]

Side Lobe: The first side lobe is bigger than hamming, but the distant sidelobes are smaller.

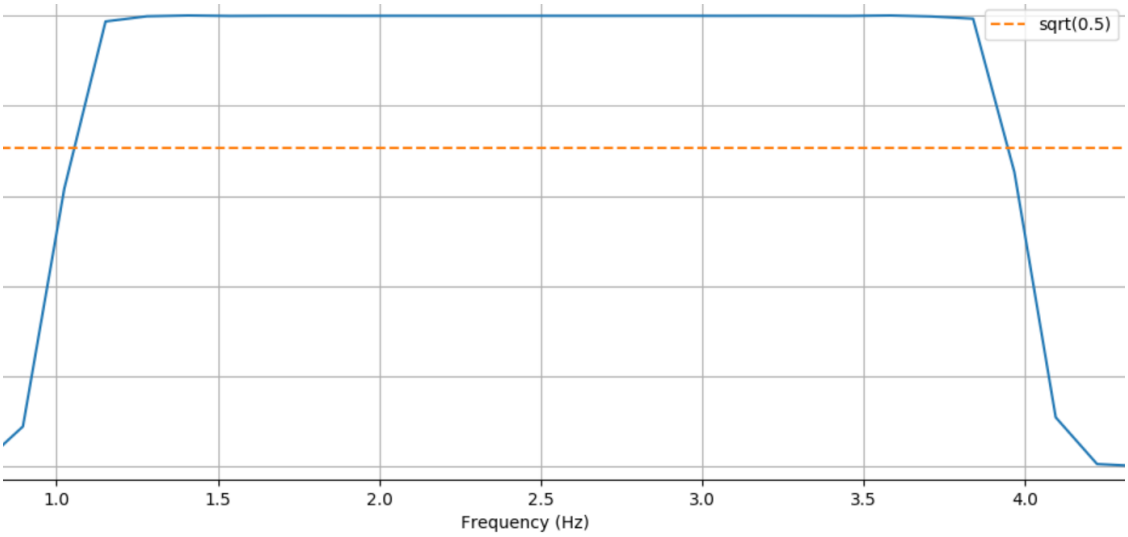


Figure 10 Hanning Window

Blackman Harris:

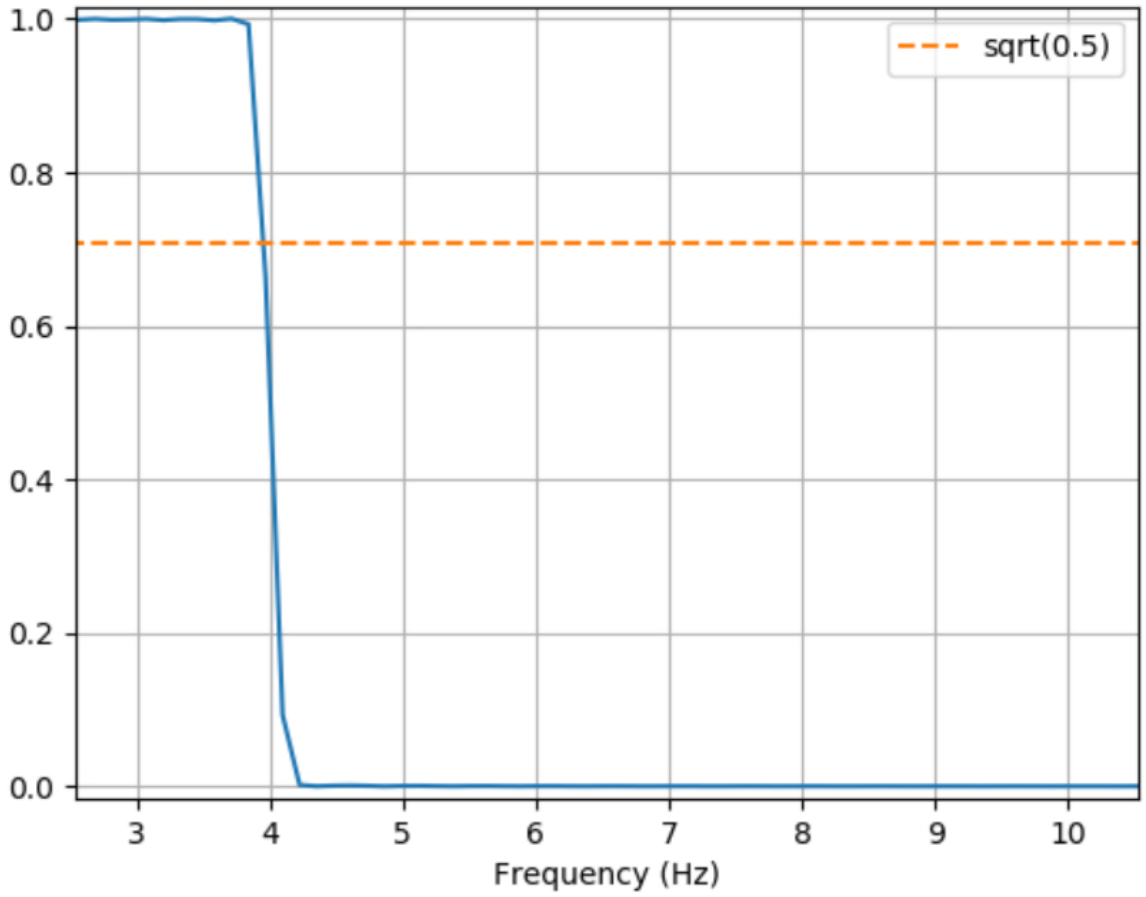


Figure 11 Blackman Harris Window

Main lobe: is wider than Hamming and Hanning (negative).

Side lobe: drop off sharper than both Hamming and Hanning.[20]

Hamming:

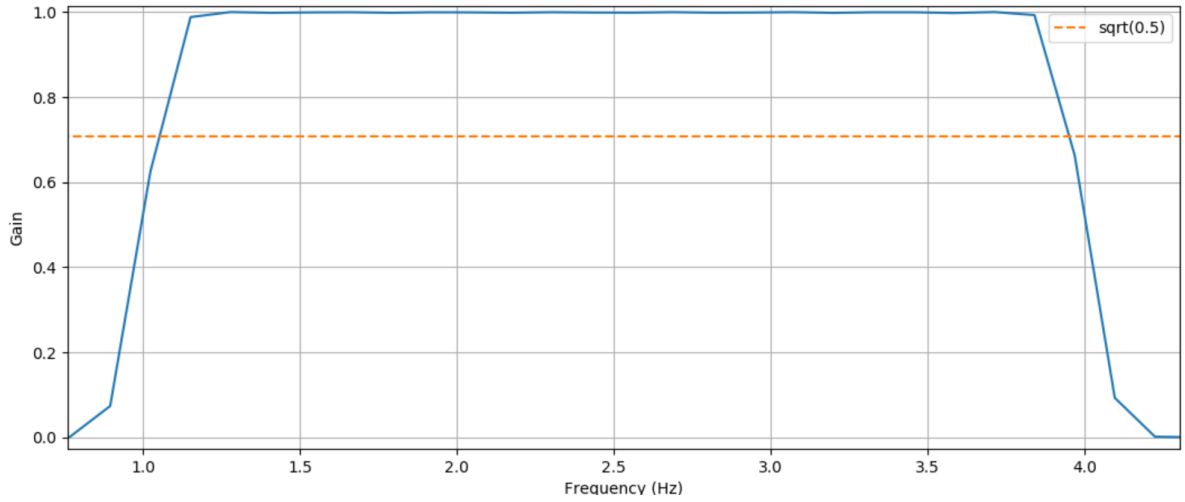


Figure 12 Hamming Window

Main lobe: width is comparable to Hamming, but smaller than Blackman Harris

Side lobe: First side lobe is considerably smaller (good thing) compared to Blackman Harris and Hanning. However, the more distant side lobes are bigger. [20]

Summary:

Blackman is undesirable as there is less signal (due to the width of the main lobe). With signal powers being extremely small it is extremely important to maximise signal content. Hamming has similar lobe width to Hanning (hence similar signal in the pass band). However, the most important thing is the magnitude of the first side lobe (as the distant sidelobes are not as important). Thus, the Hamming window was chosen.

2.5 PERFORMANCE SUMMARY

A summary of the performance characteristics is given below:

Performance Characteristic	Performance Statistic
Detection rate	98% (Averaged detection rate across entire signal spectrum)
Timing/Speed of program	Average of 0.3seconds for 5 words
Time resolution	Sampling rate of 512hz translates to a time resolution of 1.953milliseconds
Noise performance	Effective detection rate is still 96% for signals with added pink noise (1/f), white gaussian noise and noise weighted heavily at the edge of each EEG band.

Figure 13 Performance Characteristics

2.6 TESTING:

Testing was first conducted using the sample sets given in MATLAB, both the noisy and clean synthetic sample sets were utilised. Longer form EEG data was passed to the MCU and MATLAB code to determine the behaviour of the program on practical signals.

2.6.1 Additional Testing:

Data was carefully generated in delta, theta, alpha and beta wavelengths. This was done by taking the difference of the sample data sets in MATLAB to get the common noise. After this a variety of noise sources were added pink, white gaussian noise, high frequency noise, 40-50hz noise. Furthermore, additional test data sets were generated where the main frequency content resided at the edges of the bands. This was done by taking an FFT in MATLAB for each window of the synthetic dataset and then adding more power to the edge frequencies. After this the Inverse Fourier Transform of the signal was taken to map back into the time domain to give the signal.

The results are summarised in the table below.

Note 'frequency edge' data sets still have the noise from the 'custom noise' datasets.

EEG Band	Performance
Delta custom noise	5/5 – 100%
Delta frequency edge	5/5 – 100%
Theta custom noise	5/5 – 100%
Theta frequency edge	5/5 – 100%
Alpha custom noise	4/5 – 80%
Alpha frequency edge	4/5 – 80%
Beta custom noise	5/5 – 100%
Beta frequency edge	4/5 – 100%
Alpha custom noise (II) Re-run with the peak-detection/normalisation of frequency bands	5/5 – 100%
Alpha frequency edge (II)	4/5 – 100%

Figure 14 Additional Testing Results

2.6.2 Comments:

Initially, there were higher delta detection rates in the MCU, the reason for this is that the internal implementation in python of the filters were not completely nulling the offset of the DC – resulting in large delta false detections. To counter this the mean of the signal was subtracted in every window. This resulted in smaller false delta detection, completely eliminating the problem, and boosting the performance significantly.

All test results were run through D1 before D2. The output csv/text file was generated from LTSpice. However, having voltages in the output from 0-3.3V did not result in proper wav file conversion. This is because voltage values above a threshold are saturated at 1 in the wav file. Hence for the purposed of interfacing to D2 a voltage division circuit was used to divide values by 3. This was passed to D2, after which all the aforementioned tests were run.

2.6.3 Tuning the detection algorithm:

Noise is a random process. Hence, since the Beta band has the highest bandwidth (12-40hz) gaussian noise is more prominently weighted in this band. Thus, the number of 'false positives' identifying beta was greater than initially expected. To improve detection rate, the following novel technique was employed:

Peak detection: What distinguished signal from noise in the EEG is conscious thought. Hence a detection mechanism must be employed to give a heuristic prediction of conscious thought (numerically). This peak detection was applied based on realistic values for noise caused by random processes. When the difference between the calculated powers between alpha and beta bands were within the 'noise threshold' [21] – peak detection functions were run to distinguish between the 2 bands more accurately.

2.7 TIME, MEMORY & MICROCONTROLLER CODE:

2.7.1 Microcontroller choice:

Criteria: Low space, high processing speeds, high memory, on board ADC, DAC of reasonable resolution.

2.7.2 Novel choice: Micropython based MCU – esp32. [22]

2.7.3 Reasoning:

The specifications were reasonable for the application and the additional benefit of Micropython meant that additional complexity could be added, with little performance trade-off, to improve the detection algorithm. Micropython comes with a highly specialised subset of python optimised for embedded applications and has the added advantage of highly specialised libraries – reducing code complexity.

2.7.4 MCU Specifications:

Spec Type	Value	Description/Functionality
ROM	448KB	Booting + core functions
SRAM	520KB	Data + instructions
SRAM (Real Time Clock FAST)	8KB	Data storage. CPU accesses during boot from deep sleep mode.
SRAM (Real Time Clock SLOW)	8KB	Data storage. Ultra Low Power coprocessor accesses during deep sleep mode.
Clock speed	8Mhz (Internal)	Synchronise operation of components, instruction execution speed.

Figure 15 MCU Specifications – description taken from datasheet.

2.7.5 Memory Calculations:

A key question to be asked is whether the program can both fit and execute on an ESP-32.

2.7.6 Calculation Methods:

The length of the program is 306 lines:

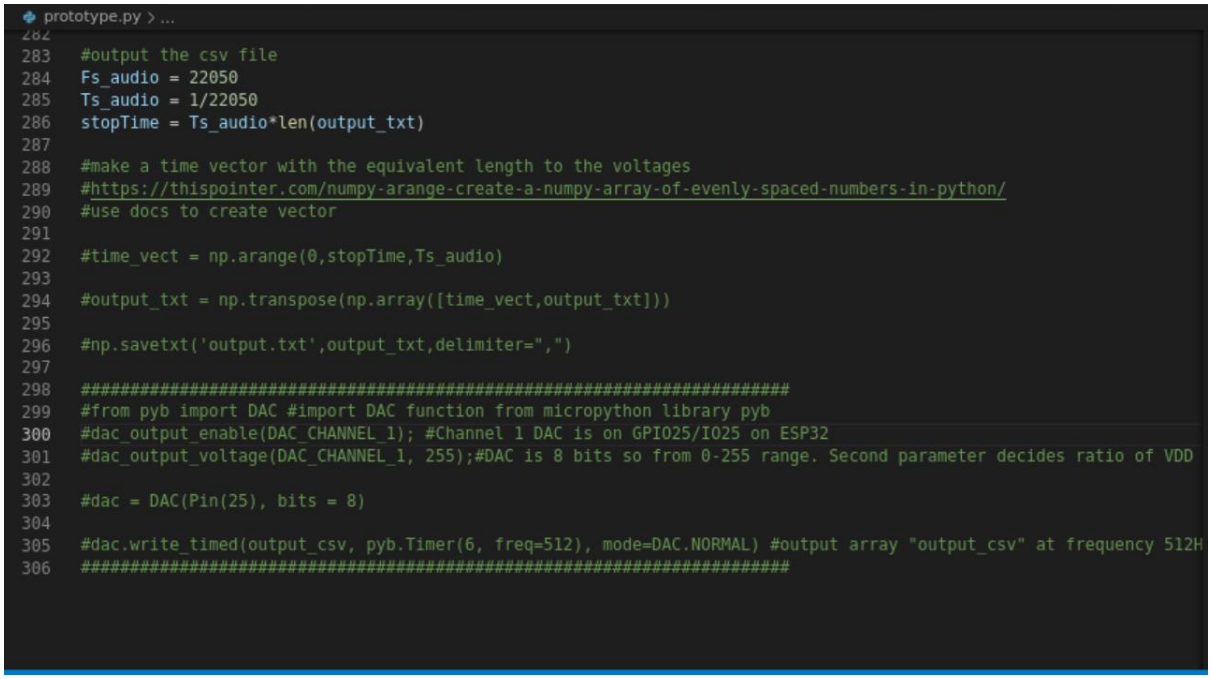


Figure 16 Length of code

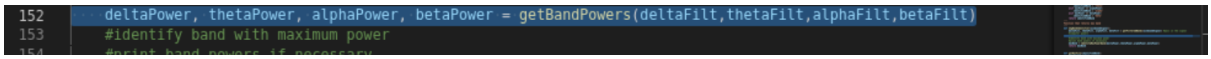


Figure 17 Longest line in code

The length of the longest line is 106 characters. Since a character is stored as 1byte in memory. The size of the total program set is:

106*306 = 32,436B or roughly 32kB << 520kB. Hence the program code fits onto the chip.

The next costly operation is storing the wav files on chip.

The total size of all (uncompressed wav files) is:

Figure 18 Txt files for all bands

Total wav size = 75kB + 120kB + 69kB + 117kB = 381kB

Thus the total size of the data on chip is:

32kB + 381kB = 413kB < 520kB.

2.7.7 Memory (Run time execution):

The most memory intensive operations in the program are:

- Storing FIR filter coefficients at run time.
- Generating wav file at run time.

The order of the FIR filter is 512. Each filter coefficient is represented using a numPy double which is 8bytes. Hence the total size of the filter coefficients at run time is: 8bytes * 512 = 4096 Bytes or 4kB <8kB. Hence these values can fit onto fast access RAM.

Note that since we have 4 bands (and hence 4 filters), it may be tempting to say that the total size of memory related to coefficient usage is 4*4kB, however a memory optimisation is applied to avoid this. Each filter is generated once in a local function. Upon exiting the function, the local variable is 'destroyed' on the stack hence saving memory.

The next biggest bottleneck/problem is generating the wavfile at run time. Storing wav files on the MCU isn't the best idea and a future design would offload the storage to some external chip or device. Loading the entire wav file in one go would result in memory overflow. The smallest wavfile has 6000 double values. Hence 6000*8 = 48kB > 8kB. Hence storing the entire wav file exceeds limits for fast access ram. However, by utilising a principle known as chunking, to essentially load only data that is needed, we can avoid this.

2.7.8 Timing and bitrate calculations:

Host machine: Dell Inspiron – clock speed: 2.5Ghz.

However, this is obviously not the required speed that we want in terms of the MCU, so in order to mimic a real word value a virtual machine hosted in the cloud was used. This firstly, mimics any latency due to any network calls needed to be made, and secondly an environment that somewhat replicates the environment of the MCU can be set up with relative ease. However not perfect this serves as a good estimate of the timing mechanics.

Now in terms of timing when simulating using the virtual machine this program takes 300ms to execute which is the time spent executing in the kernel. Upon executing multiple commands and taking the average, a value of 300ms was achieved.

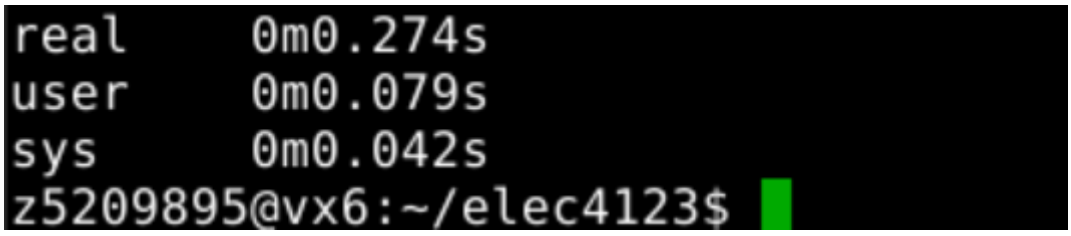
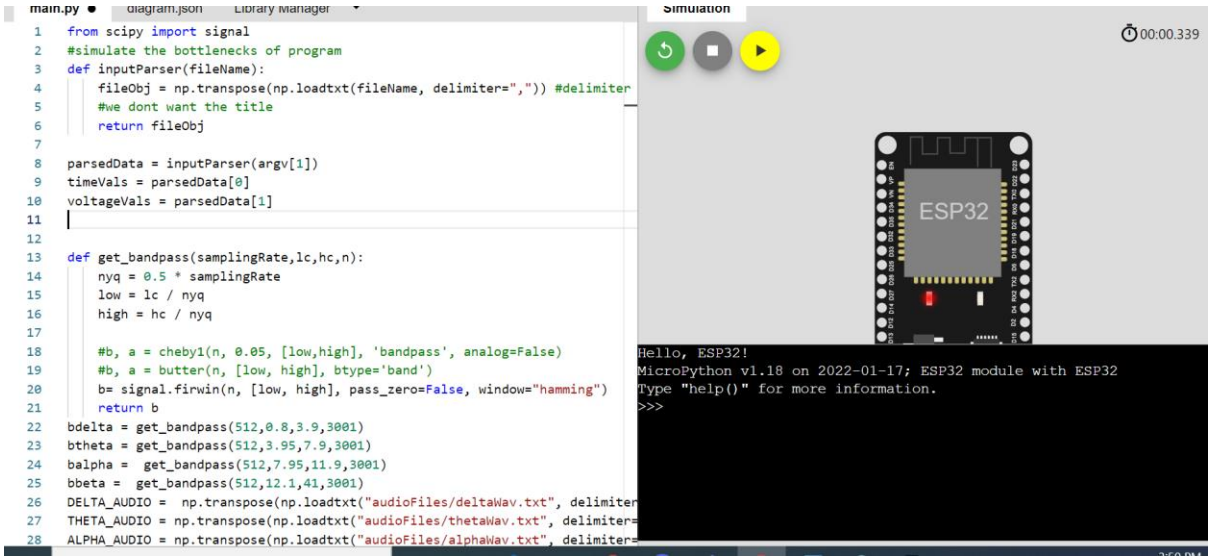


Figure 19 Code Run Time

Now this was done using the above python command. Note that this includes all the time taken to open, read, write, files, concatenating the output which is the biggest bottleneck in the program.

To further verify the nature of the program execution, the program was again run on an online simulator shown below:




```
from scipy import signal
#simulate the bottlenecks of program
def inputParser(fileName):
    fileObj = np.transpose(np.loadtxt(fileName, delimiter=",")) #delimiter
    #we dont want the title
    return fileObj

parsedData = inputParser(argv[1])
timeVals = parsedData[0]
voltageVals = parsedData[1]

def get_bandpass(samplingRate,lc,hc,n):
    nyq = 0.5 * samplingRate
    low = lc / nyq
    high = hc / nyq

    #b, a = cheby1(n, 0.05, [low,high], 'bandpass', analog=False)
    #b, a = butter(n, [low, high], btype='band')
    b= signal.firwin(n, [low, high], pass_zero=False, window="hamming")
    return b
bdelta = get_bandpass(512,0.8,3.9,3001)
btheta = get_bandpass(512,3.95,7.9,3001)
balpha =  get_bandpass(512,7.95,11.9,3001)
bbeta =  get_bandpass(512,12.1,41,3001)
DELTA_AUDIO =  np.transpose(np.loadtxt("audioFiles/deltaWav.txt", delimiter
THETA_AUDIO = np.transpose(np.loadtxt("audioFiles/thetaWav.txt", delimiter=
ALPHA_AUDIO = np.transpose(np.loadtxt("audioFiles/alphaWav.txt", delimiter=
```

Figure 20 Program Running on Online Simulator

2.7.9 Interface between deliverables:

D1-D2:

The ADC outputs 0-4095 to MCU. However, to accurately map these values back into voltages a mapping function was used as shown below:

```
'''
Function that maps values from 0-4095
to actual voltages
'''
def mapValues(windowedSignal):
    resolution = 3.3/(4095)
    windowedSignal = windowedSignal*resolution
    return windowedSignal
```

Figure 21 Mapping Function

From here an interrupt routine was setup to sample the ADC pin at 512hz. From here 512 values (window size) are read into a list representing ADV_VALUES. Pin 2 is set for the 12 bit ADC, and upon calling the interrupt handler a flag is set to signal that sampling is occuring.

```
# isInterrupted = False #flag to see if we are currently reading values from adc
# currentAdcValue = 0 #what sample we are currently reading

# adcPin = ADC(Pin(2))
# ADC_VALUES = [] #initialise a list of certain size

# #we set up a function that is called periodically using an interrupt handler
# def interruptHandler(sysCount):
#     interruptNum = True #increase the interrupt --> gives indication of window

# sysCount.init(period=samplePeriod, callback=interprintruptHandler)

# processRuning = False

# while processRuning:
#     #now we only want the executed code to run
#     #every time there is an interrupt--> i.e we are reading values from the ADC
#     if isInterrupted:
#         ADC_VALUES[currentAdcValue] = adcPin.read()
#         ADC_VALUES = mapValues(ADC_VALUES)
#         state = machine.disable_irq()
#         machine.enable_irq(state) # renable interupts in prep for the next interrup trigger
#         isInterrupted = False
#         currentAdcValue += 1

# The following segment of code parses the input and coverts it into python manipulatable objects
```

Figure 22 Interrupt Handler

D2 – D3:

Upon identifying the most prominent band (delta, theta, alpha, beta etc) a wav file is to be outputted to D3. This is done via an 8bit DAC. The required output wav file is retrieved in chunks and is concatenated to a final output file. In between every word there is a small buffer added to make the words identifiable.

```
else:
    #buffer for X seconds
    #add new identified signal
    output_txt = np.pad(output_txt,(0,pad_length))
    output_txt = np.concatenate((output_txt,getWavFile(identifiedBand)))
```

Figure 23 Addition of Buffer

The size of this buffer is chosen via the subsequent research. According to Jordi Adell (et al.) "Structure of pauses in speech and the classification of speech type," there are multiple pause types between words "acoustic (silent, breath and filled) and syntactic.[23] To simulate realistic pauses, a paper that examined the average differential of pauses between a large data set of human speakers found that 0.3 seconds was a best guess heuristic.[24] Hence, utilising the sampling rate of the output signal, the length of a 0 padded buffer was calculated to give realistic pauses between words.

DELIVERABLE 3

Author: Jack Walsh

3.1 INTRODUCTION

Deliverable 3 required designing a circuit that can amplify small signals to deliver high power to low impedance circuits. The topology of the solution follows a three stage H.C. Lin Amplifier [25].

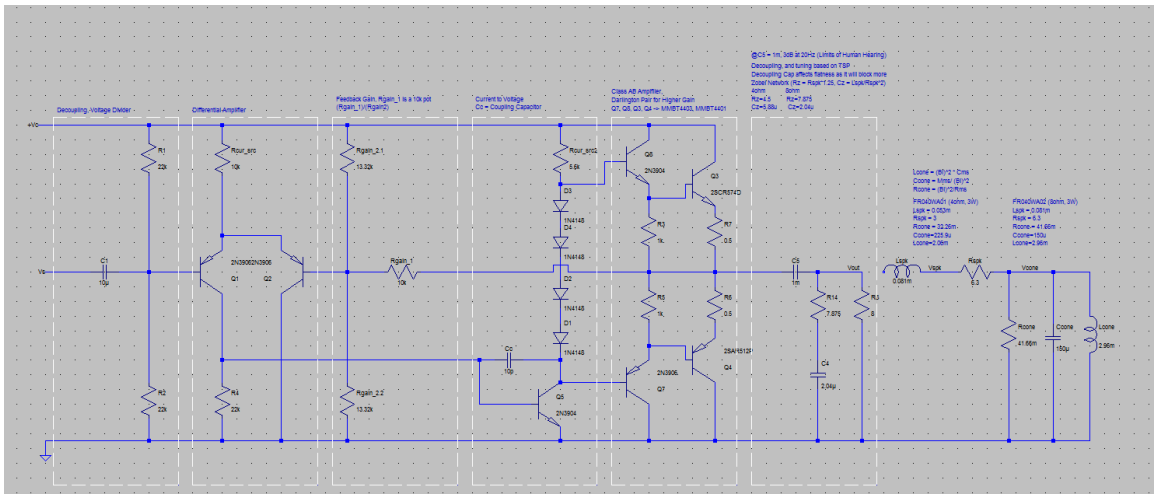


Figure 24 Completed Design in SPICE

3.2 SYSTEM ARCHITECTURE

3.2.1 Input Stage

From Deliverable 2, a signal between [0, +3.3V] is input to the Deliverable 3. This signal is decoupled and offset to the amplifier power supply. This offset is used to ensure that all voltages will have a positive associated current to deliver to the differential amplifier. The differential amplifier acts as high impedance load to DAC while also creating a linear output to the next stage. This property is achieved from comparing the input and output of the entire amplifier as demonstrated in the figure below.

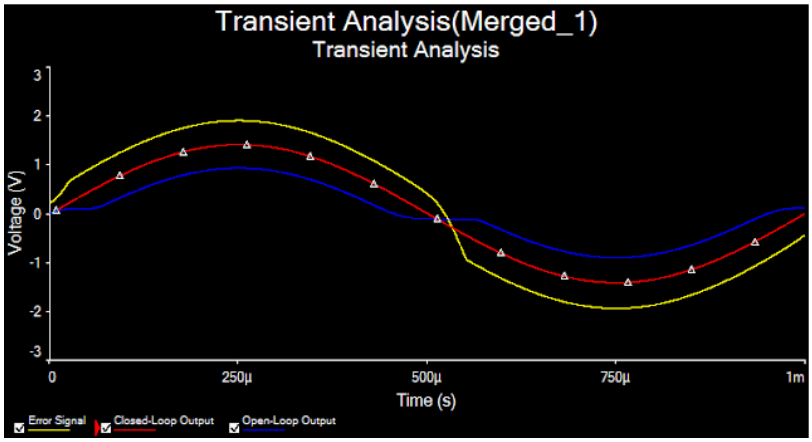


Figure 25 The differential amplifier linearising the output [26]

3.2.2 Voltage Amplifier Stage

The output from the input stage feeds into a BJT with a small compensation capacitor to improve smoothing and create a high frequency pole. This configuration is used to convert the current to a voltage with a gain of set by the beta of the transistor with the fixed current source.

3.2.3 Output Stage

This system takes the output from the voltage amplifier and amplifies the power and current by using a Darlington pair of bipolar transistors. The max power is limited to the supply voltage and the speaker resistance. The push-pull Darlington amplifiers are used to eliminate crossover distortion of a class B and the diodes are implemented to improve the efficiency as the transistors are biased.

3.2.4 Additional Features

The output stage feeds a Zobel Network before outputting to the speaker. The output is also routed back to the differential amplifier to provide negative feedback and create an error signal that will help to linearise the output. The speaker was determined to be an 8Ω 3W speaker as described in the Speaker Choice Section. The Zobel Network is tuned to the TSP data of the specific speaker that was selected, through the following formulas:

$$R_z = R_{spk}^2$$

$$C_z = \frac{L_{spk}}{R_2^2}$$

Adjustable Gain for volume was integrated into the feedback circuit. This allows the consumer to adjust the volume to different dB levels.

3.3 SYSTEM INPUT AND OUTPUT PROOFS

Figure 3 shows the input and output power relative to the signal power to show the amplification to a resistive load

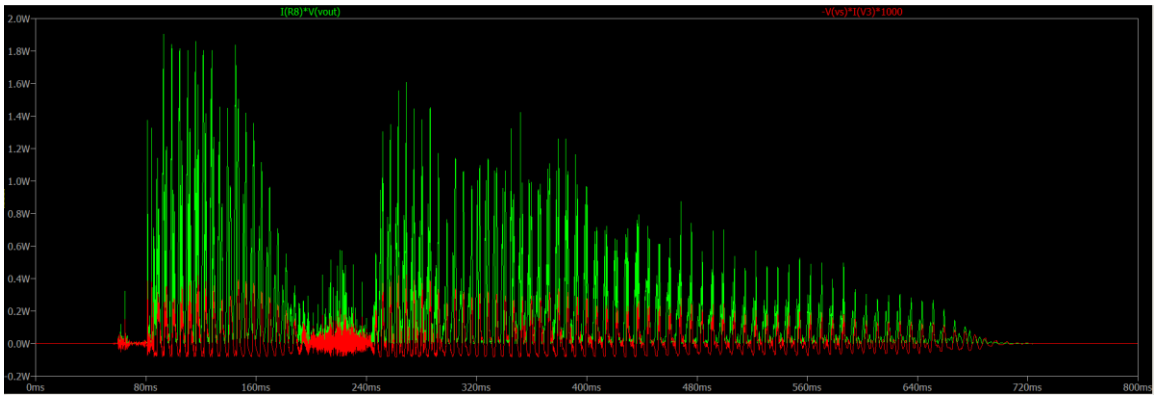


Figure 26 Simple Modelled Speaker Load Response, Input x1000

Figure 4 shows the input and output power relative to the signal power to show the amplification on a "realistic" model. This model accounts for the real-world characteristics such as the moving mass (Mms), mechanical resistance (Rms), suspension compliance (Cms) and force factor (Bl) using the following formulas to translate into electrical components.

$$L_{cone} = Bl^2 * C_{ms}$$

$$C_{cone} = \frac{M_{ms}}{Bl^2}$$

$$R_{cone} = \frac{Bl^2}{R_{ms}}$$

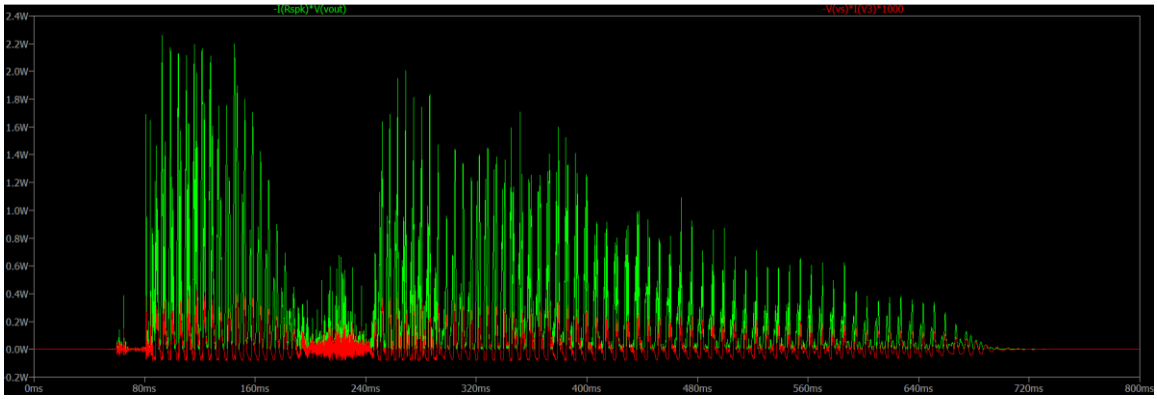


Figure 27 Realistic Modelled Speaker Load Response, Input x1000

3.4 GAIN AND BANDWIDTH

The bandwidth upper limit is dominated by the miller capacitance in the VAS. This is given by the formula

$$f_{upper} = 1/(2\pi 1.5C_c) = 1.061MHz$$

$$f_{lower} = 25Hz$$

This means that the amplifier should have a 3dB drop off at these two bands. In the realistic model, the upper bound pole is closer to 11kHz as seen in Figure 5. This is due to the realistic model of the speaker which has a high pole corner frequency, which can be seen in the SPL Response in Figure 10.

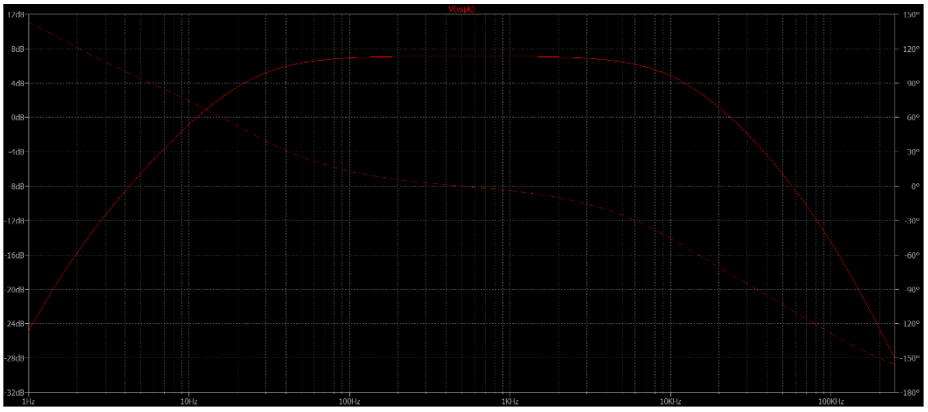


Figure 28 Bandwidth of the Power Amplifier Output

The gain is more obvious in the current, but the voltage is being amplified as well set by the ratio of the gain resistors as seen in Figure 6.

$$g = \frac{G_1}{G_{2.1} || G_{2.2}} + 1 = 2.51$$

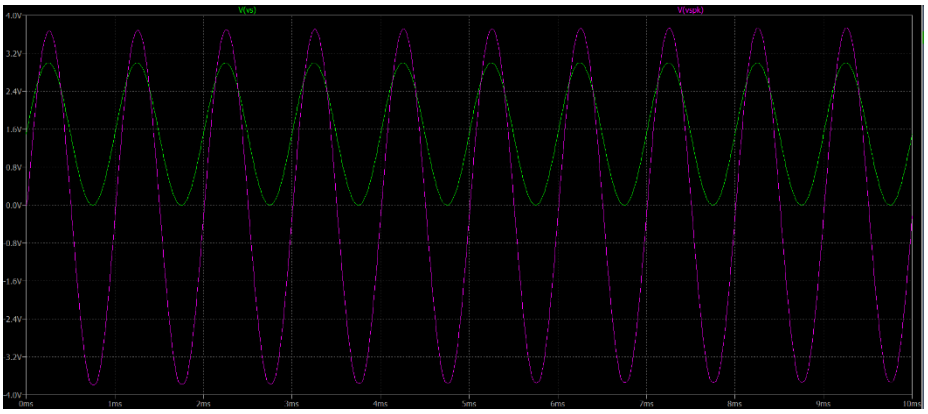


Figure 29 Voltage Gain Referred from Input

This gain is on average around 2.5 but closer to the zero-crossing point there is greater distortion in the relative gains. This is because of the attenuation at lower frequencies causing the output to have spikes at the zero crossing as seen in Figure 7.

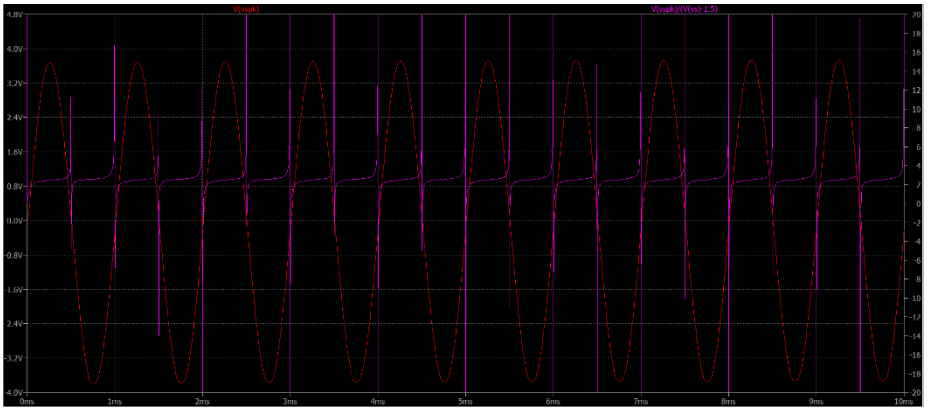


Figure 30 Amplifier Gain Input to Output

3.5 OUTPUT POWER

The output power is limited to the transistor selection on the output stage. The 2SCR574D and the 2SAR512P were selected such that the power is always less than its maximum rating. Since the largest PNP transistor can dissipate 2W, the maximum output power was fixed at 2.2W. The output power can be adjusted through a potentiometer on the gain between 0 - 10k (Gain would be 0 to 2.5).

3.6 TOTAL HARMONIC DISTORTION AND LINEARITY

The Total Harmonic Distortion has been calculated for 3 different signal types (square, triangle, square) at 3 different frequencies (100Hz, 1kHz, 10kHz). The table below summarises the information

Hz	**Sine**	**Triangle**	**Square**
Expected	0%	12.4%	42%
0.1k	0.2%	12.44%	43.2%
1k	0.3%	11.50%	39.82%
10k	0.2%	5.29%	19.1%

It should be noted that square waves have poor THD due to the decoupling that occurs at the input and output stages. The DC can't be passed so it slowly dissipates and causes poor THD. Additionally, the filtering that occurs at the compensation capacitor can cause high frequency signals such as the 10kHz, triangular wave can distort to look more sinusoidal on the output.

Linearity can be discussed in the Gain and Bandwidth Section as the linearity relates to gain. Refer to Figure 7 for the Linearity and Refer to Figure 5 for the Flatness.

3.7 EFFICIENCY

Efficiency of a Class AB Amplifier can range between 50-75%, however there is some power consumed in the other two stages. To calculate the average efficiency over a signal, the output from D2 **that** is correctly scaled by the DAC is fed into the LTSpice simulation. After the sample has run, the RMS Value over the duration of the signal can be displayed (Figure 8). The efficiency can be calculated as follows:

$$\eta = \frac{P_{in}}{P_{out}} = \frac{186.59mW}{717.32mW} = 26.01\%$$

Additionally at a single tone frequency (1kHz) The efficiency is around 52%. The efficiency goes down as the voltage input is reduced, as the overhead power drain is till there, so for lower voltages the system is less efficient.

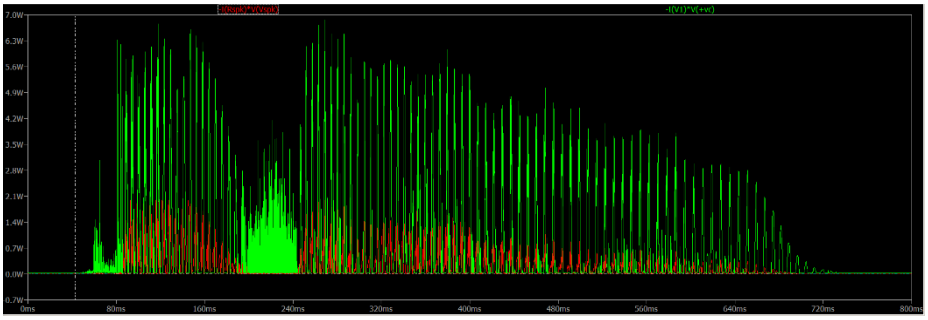


Figure 31 Amplifier Efficiency from Deliverable 2

Power is lost in the main output transistors which are only allowed to dissipate a maximum of 2A at a maximum power rating of 2W for the PNP transistor and 50W for the NPN transistor. The RMS power dissipation is 252.44mW (NPN) and 237.5mW (PNP). The quiescent current draw is 36.18mW due to biasing All other power consumption over the audio is equal to:

$$P_{oth} = P_{in} - (P_{out} + P_{PNP} + P_{NPN}) = 40.79mW$$

The crossover distortion is 8.3us on the rising edge, and 3.6us on the falling edge of Q4. Over a 0.5ms period the total cross over distortion is 2.38% of the time that both BJT's are on. This is what creates distortion at the output and can cause the current through the circuit to momentarily spike.

3.8 SPEAKER CHOICE AND MODEL

The Speaker Choice was determined on the maximum current could be provided without compromising on THD with limited voltage. In addition, some research was conducted on the power required to replicate the human voice which was on average 70dB [27]. An 8Ω, 3W speaker (FR040WA02) has an SPL Profile (Figure 10) that is around 85dB at 1m away driven by 1W. Since our maximum output is 2.2W and this value is already over the average human voice, this speaker fulfilled the conditions needed to use in our design.

Since there was an 8Ω and a 4Ω version, the 8Ω was selected so that the amplifier could have increased power with lower current, since this was a limiting factor in both efficiency and heat dissipation in the power amplifier.

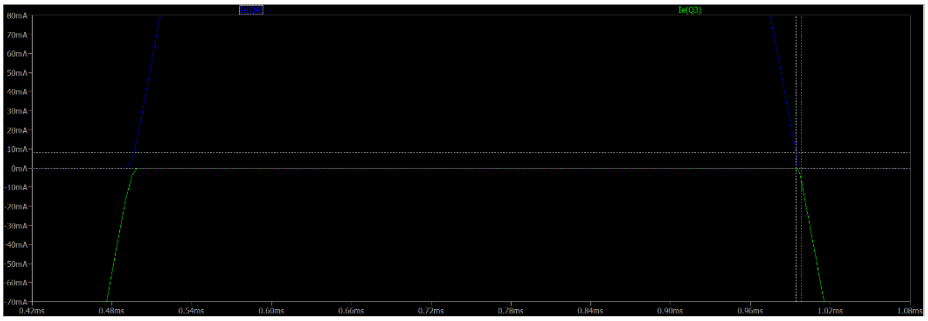


Figure 32 Transistor Switching at the same time

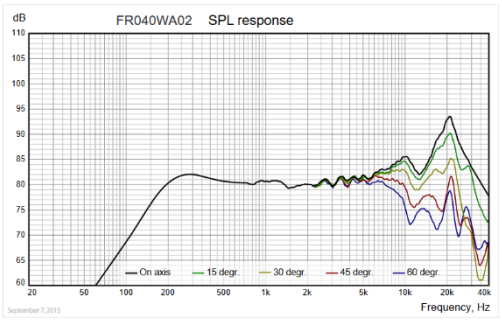


Figure 33 Speaker SPL Response [28]

DELIVERABLE 4

Author: Anmol Yadav

4.1 INTRODUCTION

Creating the PCB is the culmination of all other deliverables in a presentable format that has been thoroughly tested through design rule checks for validity of the PCB design.

4.2 DESIGN DECISIONS

Since the PCB for D1 is separate from the PCB for D2 & D3, they both had to be created on a separate PCB workspace with their own different Stackup and rules.

We had created a set of baseline rules that had to be followed as either of the PCB's design case restrictions along with the restrictions in size of the PCB as mentioned in the task worksheet.

Every capacitor and resistor were chosen based on their tolerance values and their minimum power dissipation while also keeping an eye on the cost side of things.

4.3 NOVEL IDEAS

- Decided to place components on the bottom layer of the PCB 1 to meet the size requirement
- Thought about how to implement shielding (Can't implement in Altium) in an actual real-life setting [29]
- Since we had low frequency our Return Current Path in ground flowed directly from load to source. [30]
- Opted for SOIC type components instead of Through Holes
- Minimalistic Header pins for cost effectiveness
- The BOM total revealed the cost for the components to be $58.645. Best Quality while keeping cost in mind.
- Signal tracks were small (Power tracks take up most of the length!)

4.4 TRACE WIDTH AND VIAS

To determine the trace width and whether it was feasible we used a program called Saturn and input our other parameters which gave us a workable value of around 0.3mW as our allowable power for the circuit for D1 (which is plenty!).

The minimum track width was 0.1mm, preferred track width was 0.15mm and maximum track width was 0.2mm. [31]

This not only enabled us to drastically reduce the size of our PCB but enabled for some easy routing and flexible via placement.

We had 31 vias, most of which were connecting resistors and op amps connecting to ground and power plane since our PCB has 2 layers dedicated for a Power and a Ground plane.

21 of these vias were for signal bus and the other 10 were for getting the power/connecting to the ground plane.

Via diameter is 0.7mm and the signal vias are 'through' vias which go from the top to the bottom layer.

4.5 DELIVERABLE 1 PCB

Since D1 had a lot of op amps and a small workable space area (restrictions!), we opted for a 4-layer PCB design choice as that enabled us to free up some space and barely squeeze in all our components into the PCB.

We changed the design from 4 decoupling capacitors to a single capacitor of equivalent value because of size constraints in the PCB.

Since the frequency of the signals that we were dealing with were small, we went for higher dielectric values for our layers.

4.5.1 Layer stackup for PCB 1

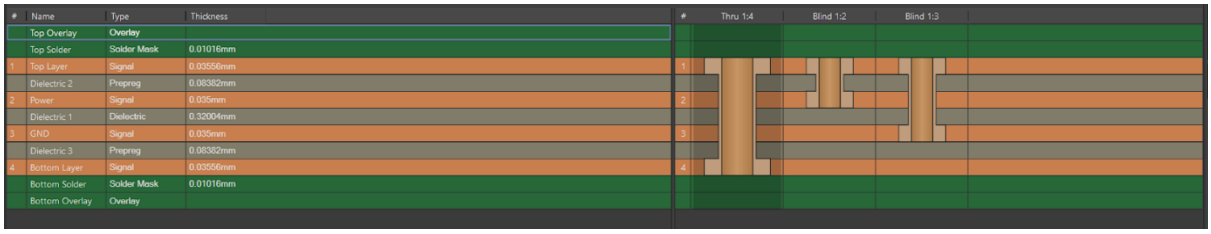


Figure 34 PCB 1 Layer Stackup

4.5.2 Important parameters for D1 PCB

- Longest Track length is 50.32mm.
- Average Track Length is 24.2mm.
- Board Size is 441.66 sq.mm.
- 4 Layers which are namely Top, Power, Ground and Bottom
- Max number of vias on the signal net are 2

4.6 DELIVERABLE 2 & 3 PCB

Since we had a relaxed space for the PCB dimensions there was no point in opting for more than 2 layers for the PCB 2.

Since this PCB had, more power being transmitted to its components, the track width was widened to 0.254mm which was acceptable after calculating the values from the PCB toolkit.

Everything else including the vias remained the same except that we only had vias going from the top to bottom layer

The terminal block (Jout1) in the PCB connects the circuit to the loudspeaker as mentioned in D3 which outputs the audio.

4.6.1 Layer Stackup for PCB 2

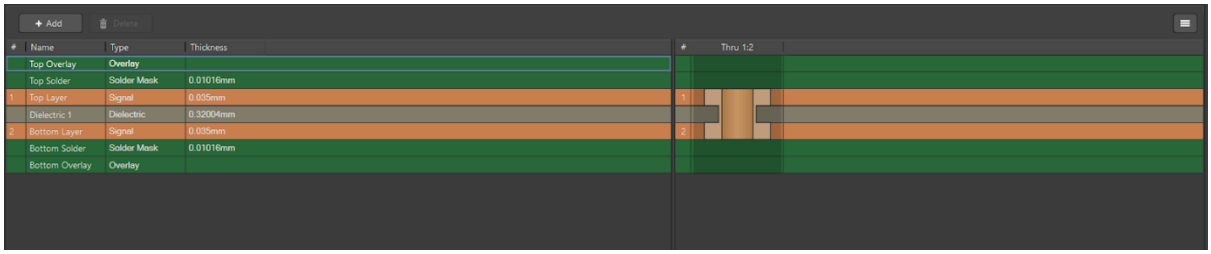


Figure 35 PCB 2 Layer Stackup

4.6.2 Important parameters for PCB 2

- Longest track length is 99.6mm.
- Average Track Length is 51.41mm.
- Board size is 2510.124 sq.mm.
- 2 Layers namely Top and Bottom.
- Max number of vias on the signal net are 2

REFLECTION

THE PLAN

Any project or design that has to be worked upon as a team needs to have proper allocation of tasks for each of its members and a strict timeline.

Our group's plan of action was to first create a Gantt chart to set a basic timeline structure for everyone to work on. This enabled all the team members to be organized and work efficiently.

We distributed the tasks according to every member's strength and the areas that they were comfortable in.

What we hoped to achieve was to get working on D1 as soon as possible and then move onto the other deliverables after some progress and looking back at it now, it turned out well

as we had plenty of time to perform tests and improve upon our ideas for almost every deliverable.

During the long weekends we faced certain difficulties in coordination of the meetings, but we managed to work on individual assigned tasks.

In order to maximize the meetings time with our mentor, Yeoh, we pre formulated questions for each deliverable and the issues that we were facing to get some insight into solving those problems which helped us to minimize idle time during meetings and keep them short and concise.

Since discord has a very good and clean format for working as a team on a task, we opted to create a server in which we collaboratively worked upon. If there were any problems with any deliverable, whoever was available at that point of time would hop on and try to solve the problem. This helped build a sense of bonding within the team and encouraged conversations.

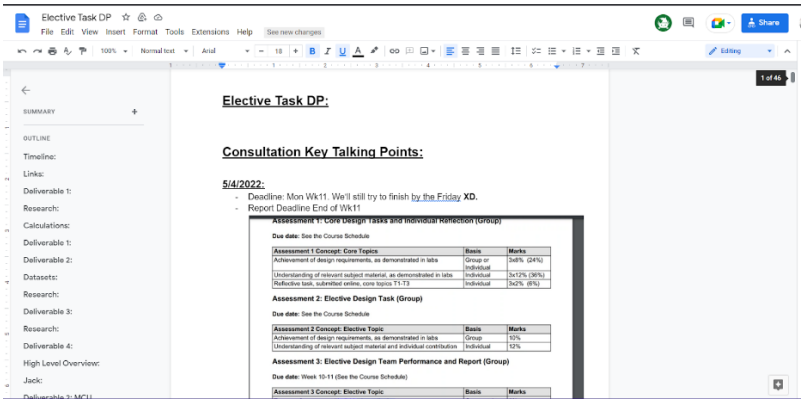


Figure 36 Common Elective Document

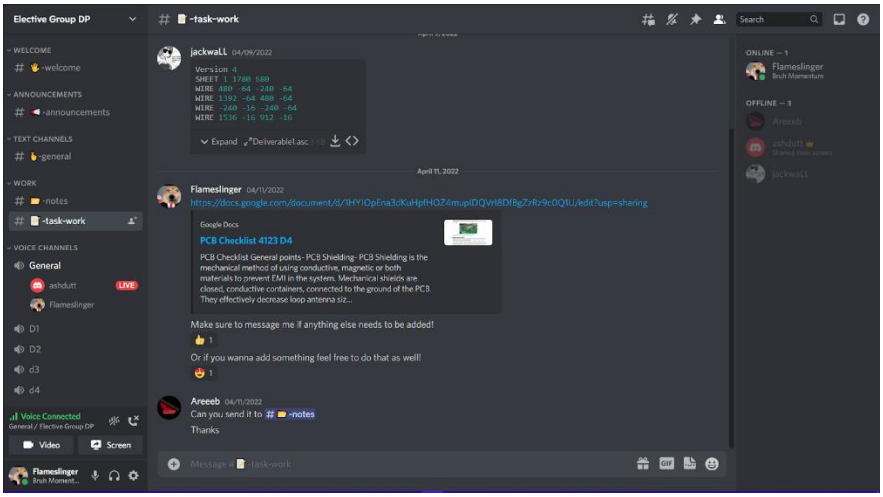


Figure 37 Discord Server

DELIVERABLE SPECIFIC IMPROVEMETNS

Deliverable 1: Some minor improvements for D1 would be:

Tune the low pass filter for a better bandwidth for the higher frequency signal such as Gamma band (40-100Hz) & LFP (100-500Hz).

Deliverable 2:

- Interfacing a 16MB external chip to improve the storage of audio files.
- Implementing a wavelet decomposition allows us to better understand the transient nature of EEG signals. The wavelet transform serves as a generalised Fourier transform that gives the frequency content of a signal at various regions of time by applying a scaling function on a 'wavelet' function – which acts like a windowing function. This is in stark contrast to something like the Short Time Fourier Transform which has a 'fixed' window. By varying window behaviour, the fundamental essence of an EEG signal can better be captured in the mathematics leading to practical detection. [32]

Continuous time wavelet transform:

$$F(\tau, s) = \frac{1}{\sqrt{|s|}} \int_{-\infty}^{+\infty} f(t) \psi^* \left(\frac{t - \tau}{s} \right) d\, t$$

Where, ψ=*continuous function called mother wavelet*

Discrete Time wavelet transform:

$$D[a, b] = \frac{1 \sum_{m=0}^{p-1} f[t_m] \psi[\frac{t_m - a}{b}]}{\sqrt{b}}$$

Where, a= τ

b=s

- Discrete wavelett transform. More efficient for dyadic upper and lower bounds.
- De-noising ECG and MCG signals. [33]

Deliverable 3: For deliverable 3 we didn't have many issues for the most part.

- That being said, we would definitely want to improve on certain aspects of D3 namely the efficiency, better protection and better current biasing.
- We were happy with the efficiency of our overall design but to one up ourselves we would choose better components for the design with a lower ON resistance to improve the efficiency which would also make the THD look better.
- Another thing we wanted to implement would be to add a better protection for our circuit design. Currently we had multiple linear regulators in our design instead of a PMIC which we would have implemented given that we had a bit more time to thoroughly research and choose the best one for the task.
- Active protection is also an integral part of the circuit, and we could improve it by adding an eFuse instead of the traditional fuse that we used in our PCB in D3. Since not only is the eFuse smaller in size but there would be no need to replace the fuse every time in case of a power surge. Also, the user can set a custom value for the eFuse using external resistors.

Deliverable 4: We faced certain challenges such as limited PCB dimensions and the layer stackup for D1 PCB.

- To overcome the limited space for D1 we opted to put the resistors on the bottom of the PCB to incorporate all the components on the PCB. Doing this also enabled us to reduce the op amp trace lengths which in turn would help us reduce the excess noise that would usually develop in longer trace length with a low frequency signal at the input side of the design.
- Since we had to put in a lot of op amps for D1, we opted for a 4-layer PCB to reduce the number of signal vias and to also prevent huge track lengths for individually connecting everything to a common power source.
- However, there was one fatal error/oversight in the design for D1 PCB and that was forgetting to do a polygon pour for the power plane which kind of invalidated the point of having a separate layer for the power plane. To improve on this, we would definitely do a polygon pour on the PCB to minimize power trace lengths and in turn it would make the PCB less complicated as well as more resistant to white noise from EMI or crosstalk.
- One more thing that we would do to improve is to research & implement on the best materials for the components that can be used in our design, for example- we would opt for ceramic capacitors for their paraelectric nature and also being cost effective or using metal film resistors for their lower noise, tighter tolerances and better temperature coefficients.

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APPENDIX

- **BOM for both PCB-**

Line #	Name	Description	Designator	Revision ID	Revision State	Revision Status	Quantity	Manufacturer 1	Manufacturer Part Number 1	Manufacturer Lifecycle 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Subtotal 1
	GRM1885C1H201A01D	Chip Capacitor, 22 pF, +/- 5%, 50 V, -55 to 125 degC, 0603 (1608 Metric), RoHS, Tape and Reel	C1		Unknown server		1	Murata	GRM1885C1H201A01D		Digi-Key	490-1411-1-ND	0.1	0.1
	C0805C103K2RACTU	CAP CER 10000PF 200V X7R 0805	C2, C4		Unknown server		2	KEMET	C0805C103K2RACTU	Volume Production				
	6SVPE150M	CAP ALUM POLY 150UF 20% 6.3V SMD	C3		Unknown server		1	Panasonic	6SVPE150M	Volume Production	Newark	89Y2718	0.221	0.221
	GRM155R61A105KE15D	CAP CER 1UF 10V X5R 0402	C5, C6		Unknown server		2	Murata	GRM155R61A105KE15D		Arrow Electronics	GRM155R61A105KE15D	0.025	250
	UMK105B7471MVHF	None	C7		Unknown server		1	Taiyo Yuden	UMK105B7471MVHF					
	T491A106K010AT	Capacitor, Tantalum, 10 uF, +/- 10%, 10 V, -55 to 125 degC, 2-Pin SMD (1206), RoHS, Tape and Reel	C8		Unknown server		1	KEMET	T491A106K010AT	Volume Production	Newark	57K1635	0.104	0.104
	C0805C100J5GACTU	Capacitor; Ceramic; Cap 10 pF; Tol 5%; Vol-Rtg 50 VDC; SMT; 0805; C0G (NPO); Tape&Reel	C9		Unknown server		1	KEMET	C0805C100J5GACTU	Volume Production	Newark	17H0911	0.005	0.005
	B58035U5205M062	CAP CER 2UF 500V 4SMD	C10		Unknown server		1	TDK EPCOS	B58035U5205M062	Volume Production	Farnell	2991124	13.73	13.73
	1N4148	DIODE GEN PURP 100V 200MA DO35	D1, D2, D3		Unknown server		3	ON Semiconductor / Fairchild	1N4148	Volume Production	Future Electronics	9927732	0.011	0.033
	0451.630MRL	FUSE BOARD MNT 630MA 125VAC/VDC	F1		Unknown server		1	Littelfuse	0451.630MRL	Volume Production	Digi-Key	F2575CT-ND	1.46	1.46
	M22-2510205	CONN HEADER VERT 2POS 2MM	J1, J2, J3		Unknown server		3	Harwin	M22-2510205	Volume Production	Mouser	855-M22-2510205	0.18	0.54
	691103110002	1031 Series 3.5mm Pitch Straight; PCB Terminal Block; Through Hole; 2 Way	Jout1		Not managed		1	Wurth Electronics	691103110002	Volume Production	RSComponents	8267239	0.913	0.913
	620302124022	Male Shrouded Header WR-WTB, SMT, Vertical, pitch 2 mm, 1 x 2 position	P1, P2		Unknown server		2	Wurth Electronics	620302124022	Volume Production	Digi-Key	732-2707-1-ND	1.09	2.18
	61900411021	Male Bottom Locking Header WR-WTB, THT, Right Angled, pitch 2.54 mm, 1 x 4 position	P3		Unknown server		1	Wurth Electronics	61900411021	Volume Production	Digi-Key	732-2701-ND	0.91	0.91

	MMBT3906LT3G	General Purpose Transistor, PNP Silicon, 3-Pin SOT-23, Pb-Free, Tape and Reel	Q3, Q4, Q6, Q7		Unknown server		4	ON Semiconductor	MMBT3906LT3G	Volume Production	Avnet	09R9450	0.128	0.512
	2N4401RLRAG	General Purpose Transistor, NPN Silicon, 3-Pin TO-92, Pb-Free, Tape and Reel	Q5		Unknown server		1	ON Semiconductor	2N4401RLRAG		Avnet	2N4401RLRAG	0.09235	370.05
	CRCW120612R4FKEA		R1, R8		Unknown server		2	Vishay	CRCW120612R4FKEA		Mouser	71-CRCW1206-12.4-E3	0.1	0.2
	CRCW060331K80FKEA	RES Thick Film, 1.8kΩ, 1%, 0.1W, 100ppm/°C, 0603	R2		Unknown server		1	Vishay	CRCW06031K80FKEA	Volume Production	Newark	73T8704	0.002	0.002
	FCD603E50R0BTBST1	RES SMD 50 OHM 0.1% 1/8W 0603	R3, R9		Unknown server		2	Vishay Dale Thin Film	FCD603E50R0BTBST1	Volume Production	Digi-Key	764-FCD603E50R0BTBST1CT-ND	2.93	5.86
	ERJ-2RKF10R0X	RES SMD 10 OHM 1% 1/10W 0402	R4, R10, R14		Unknown server		3	Panasonic	ERJ-2RKF10R0X	Volume Production	Mouser	667-ERJ-2RKF10R0X	0.029	0.29
	CRCW0402390RFKED	RES Thick Film, 390Ω, 1%, 0.063W, 100ppm/°C, 0402	R5, R11		Unknown server		2	Yageo	RC0402FR-07390RL	Volume Production	Newark	12AC2076	0.001	0.002
	ERA-3AEB102V	RES SMD 1K OHM 0.1% 1/10W 0603	R6, R12, R13, R15, R22, R25		Unknown server		6	Panasonic	ERA-3AEB102V	Volume Production	Allied Electronics	70265352	0.08	0.48
	ERJ3EKF1002V	Chip Resistor, 10 KOhm, +/-1%, 0.1 W, -55 to 155 degC, 0603 (1608 Metric), RoHS, Tape and Reel	R7		Unknown server		1	Yageo	RC0603FR-0710KL	Volume Production	Newark	68X3181	0.002	0.002
	ERJ-2RKF2401X		R16		Unknown server		1	Panasonic	ERJ-2RKF2401X	Volume Production	Newark	53W4285	0.003	0.003
	RC0603FR-073K3L	Chip Resistor, 3.3 KOhm, +/-1%, 0.1 W, -55 to 155 degC, 0603 (1608 Metric), RoHS, Tape and Reel	R17		Unknown server		1	Yageo	RC0603FR-073K3L	Volume Production	Newark	85X1797	0.002	0.002
	ERJ-8GEYJ562V		R18		Unknown server		1	Panasonic	ERJ-8GEYJ562V	Volume Production	Newark	53W5018	0.005	0.005
	CRCW08055K00FKTA		R19		Unknown server		1	Vishay Dale	CRCW08055K00FKTA	Volume Production	Arrow Electronics	CRCW08055K00FKTA	0.1418	0.1418
	CRCW060322K0FKEA	RES Thick Film, 22kΩ, 1%, 0.1W, 100ppm/°C, 0603	R20, R27, R28		Unknown server		3	Vishay	CRCW060322K0FKEA	Volume Production	Farnell	1469779	0.05035	0.5035
	CRCW08053K30FKEA	RES Thick Film, 3.3kΩ, 1%, 0.125W, 100ppm/°C, 0805	R21, R29		Unknown server		2	Vishay	CRCW08053K30FKEA	Volume Production	Newark	53K0097	0.118	0.236

	WSLT2512R5000FEA	Chip Resistor, 0.5 Ohm, +/-1%, 1 W, -65 to 275 degC, 2512 (6432 Metric), RoHS, Tape and Reel	R23, R26		Unknown server		2	Vishay Dale	WSLT2512R5000FEA	Volume Production	RSComponents	6836192	1.04	5.18
	CRCW060310R0FKEA	RES Thick Film, 10Ω, 1%, 0.1W, 100ppm/°C, 0603	R24		Unknown server		1	Vishay	CRCW060310R0FKEA	Volume Production	Newark	24W2605	0.006	0.006
	RK09L1120A2S	Potentiometers Flat 15mm 10k	Rpot1		Not managed		1	Alps Electric	RK09L1120A2S	Volume Production	Mouser	688-RK09L1120A2S	2.28	2.28
	OPA2277UA	High Precision Operational Amplifier, 4 to 36 V, -40 to 85 degC, 8-pin SOIC (D8), Green (RoHS & no Sb/Br)	U1, U3		Unknown server		2	Texas Instruments	OPA2277UA	Volume Production	RSComponents	4363052	7.57	15.14
	AD8538ARZ	Single Channel Single-Supply Operation Operational Amplifier, 430 KHz BW, 400 mV/us SR, Industrial, 8-pin SOIC (R-8), Tube	U2, U4		Unknown server		2	Analog Devices	AD8538ARZ	Volume Production	Arrow Electronics	AD8538ARZ	2.93	5.86
	L79L05ACUTR	Negative Voltage Regulator, -5V, 4-Pin SOT-89, Tape and Reel	U5		Unknown server		1	STMicroelectronics	L79L05ACUTR	Volume Production	Newark	45Y5636	0.178	0.178
	NCP1117ST33T3G	Low-Dropout Positive Fixed Voltage Regulator, 1 A, 3.3 V Output Voltage, 0 to 125 degC, 4-Pin SOT-223 (318H-01), Pb-Free, Tape and Reel	Ua1		Unknown server		1	ON Semiconductor	NCP1117ST33T3G	Volume Production	Digi-Key	NCP1117ST33T3GOSCT-ND	0.67	0.67
	LM317LM/NOPB	3-Terminal Adjustable Regulator, 8-pin Narrow SOIC, Pb-Free	Ub1		Unknown server		1	TI National Semiconductor	LM317LM/NOPB	Volume Production	RSComponents	5361293	1.15	1.15
	ESP32-D0WDQ6	IC RF TxRX+MCU BLUETOOTH 48VFQFN	Umain1		Unknown server		1	Espressif Systems	ESP32-D0WDQ6		Mouser	356-ESP32-D0WDQ6	3.26	3.26