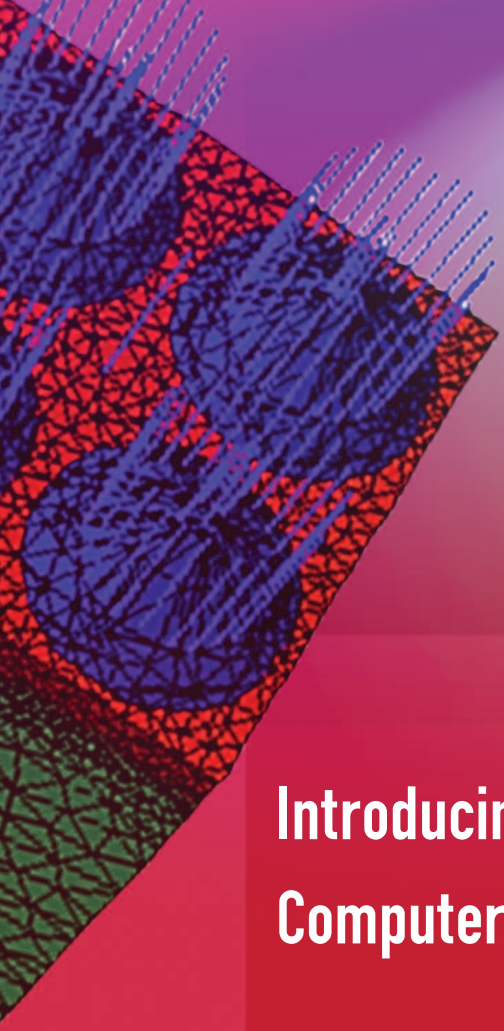

Chinmay K. Maiti

Introducing Technology Computer-Aided Design (TCAD)

Fundamentals, Simulations, and Applications

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Dedicated to

Late Dr. Rakhal Chandra Maiti

and

Dr. Kali Kinkar Das

Contents

Preface

At the beginning of 2015, the fifth-generation Intel Core processor was released, which is built with 14 nm technology containing 1.3 billion transistors. The first processor built with the 14 nm technology is the Intel Core-M processor. Generally speaking, the architecture of transistors has now switched from the planar to the vertical design. To provide the necessary support to keep the semiconductor industry on its technological growth track, heavy emphasis is being placed on technology computer-aided design (TCAD) now for achieving key long-term research results.

Even though the predominant focus of the semiconductor industry in the 1990s and early 2000 was on biaxially strained devices, the current focus has shifted to process-induced uniaxial stress, which is being adopted in all high-performance logic technologies. Uniaxial stress has several advantages over biaxial stress, such as larger mobility and performance enhancements. Encouraged by the strain-enhanced planar metal–oxide–semiconductor field-effect transistors (MOSFETs), researchers recently applied uniaxial stress to multigate devices with a metal gate and high-*k* dielectric as performance boosters. Despite the advantages provided by the manufacture of transistors, introduction and optimization of the mechanical stresses in the channel remain essential.

TCAD simulations provide a comprehensive way to capture the electrical behavior of different devices with different materials and structures for performance assessment. This monograph aims to provide the reader with a comprehensive understanding of the technology development for stress- and strain-engineered device processing. With specific case studies, applications of the process/device simulation programs in process and device development are shown. The aim of this monograph is also to provide device/circuit designers with the ability to predict what impact statistical process variations will have on their designs, as early as possible, using several commercially available tools. As currently, uniaxial strain is being adopted in all high-performance logic technologies

and applications by the industry, we shall focus mainly on process-induced uniaxial stress in this monograph.

Next-generation wireless systems, driven by a vast assortment of rapidly emerging applications operating at radio frequency (RF) and millimeter-wave frequencies, are placing increasingly stringent cost and performance demands upon the supporting microelectronics technologies. On the basis of its performance capabilities, low cost, and capacity for high integration, silicon germanium (SiGe) heterojunction bipolar complementary metal-oxide semiconductor (BiCMOS) technology has established itself as a strong technology contender for a host of such circuit applications, including analog and mixed signals, RF, and millimeter waves. However, as operating frequencies for wireless applications are pushed upward in the spectrum, SiGe heterojunction bipolar transistor (HBT) technologies face significant challenges at the transistor level as operating voltage decreases and performance requirements increase.

Starting with the 90 nm technology node, improved transistor performance has been achieved with the introduction of stress and strain in the transistor. One of the major limitations of the currently available related books is that the most of the design and simulation results presented are obtained using 2D simulations without involving stress. Due to the ultrasmall size of state-of-the-art devices, 3D effects have been dominant. To achieve a better understanding of simulated and fabricated device characteristics, 3D process/device simulation involving stress is necessary. This monograph presents mostly the 3D simulation and analysis of stress- and strain-engineered semiconductor devices for digital, analog/RF, and power applications. Detailed and extensive TCAD simulations are carried out for 3D fin field effect transistors (finFETs), and the key parameters are identified.

TCAD is shown to be an excellent resource for teaching microelectronics. The objective of a laboratory component of any semiconductor fabrication course is to teach the students the unit processes involved in microelectronic fabrication and to introduce the practice of process development. Virtual wafer fabrication (VWF) has become an integral part of the semiconductor industry now. The possibility of teaching semiconductor manufacturing in a university environment in a highly cost-effective manner by taking the advantages of high-speed internet and available TCAD tools has been explored.

Recently, several excellent books and monographs have appeared on multigate MOSFETs, high-mobility substrates and Ge microelectronics, and strained semiconductor physics. Numerous papers have appeared on strained Si and process-induced strain, but there is a lack of a single text that combines both strain- and stress-engineered devices and their design and modeling using TCAD. Attempts have been made to summarize some of the latest efforts to reveal the advantages that strain and stress have brought in the development of strain-engineered devices. We have included important works by the research community, as well as our own research students' works and ideas. The monograph is mainly intended for final-year undergraduate and postgraduate students of electrical and electronic engineering disciplines and scientists and engineers involved in research and development of high-performance devices and circuits. The monograph may serve as a reference on strain-engineered heterostructure devices for engineers involved in advanced device and process design. Instructors involved in teaching microelectronics may also find this monograph useful for laboratory education using remote web-based TCAD laboratories.

After reading the monograph, the students will learn the fundamentals of process and device simulation programs. They will be able to analyze arbitrary device structures to speed up the designing using commercial software. Approaches presented in this monograph are expected also to boost the use of TCAD tools for device characterization and compact model generation.

I am extremely grateful to my research students who made significant contributions to make this monograph a reality. I would also like to express my deep appreciation for the Pan Stanford Publishing team. Finally, I would like to thank my family members (wife, Bhaswati, and sons, Ananda and Anindya) for their support, patience, and understanding during the preparation of the manuscript.

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