



Chinmay K. Maiti

Introducing Technology Computer-Aided Design (TCAD)

Fundamentals, Simulations, and Applications





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Dedicated to
Late Dr. Rakhal Chandra Maiti
and
Dr. Kali Kinkar Das

Contents

Preface

xiii

1. Introduction	1
1.1 The Need	5
1.2 Role of TCAD	6
1.3 TCAD: Challenges	6
1.4 TCAD: 2D versus 3D	9
1.5 TCAD: Design Flow	10
1.6 Extending TCAD	11
1.7 Process Compact Model	13
1.8 Process-Aware Design	13
1.9 Design for Manufacturing	14
1.10 TCAD Calibration	14
1.11 TCAD Tools	15
1.12 Technology Boosters	16
1.13 BiCMOS Process Simulation	17
1.14 SiGe and SiGeC HBTs	17
1.15 Silicon Hetero-FETs	18
1.16 FinFETs	18
1.17 Advanced Devices	18
1.18 Memory Devices	19
1.19 Power Devices	19
1.20 Solar Cells	20
1.21 TCAD for SPICE Parameter Extraction	20
1.22 TCAD for DFM	20
1.23 VWF and Online Laboratory	21
1.24 Summary	22
2. Technology CAD Tools	25
2.1 History of Process and Device Simulation Tools	26
2.2 Commercial TCAD Tools	30
2.3 Silvaco Tool Overview	31
2.3.1 MaskViews	32
2.4 ATHENA	32

2.5	ATLAS	35
2.5.1	Physical Structure	37
2.5.2	Structure Editing	38
2.5.3	Meshing	38
2.5.4	Mesh Definition	39
2.5.5	Regions and Materials	39
2.5.6	Physical Models	40
2.5.6.1	Models	41
2.5.7	Impact Ionization Models	41
2.5.7.1	C-Interpreter functions	42
2.5.8	Gate Current Models	42
2.5.9	Bandgap Narrowing	42
2.5.10	Solution Methods	42
2.5.11	VictoryCell	44
2.5.12	VictoryProcess	45
2.5.13	VictoryStress	47
2.5.13.1	VictoryStress features and capabilities	47
2.5.14	VictoryDevice	48
2.6	Stress Modeling	50
2.6.1	Stress–Strain Relationship	51
2.6.2	Mobility	54
2.6.3	SmartSpice	56
2.7	Synopsys TCAD Platforms	56
2.7.1	Taurus-Device	59
2.7.2	Taurus-Process	60
2.7.3	Device Simulation	60
2.7.4	Carrier Recombination-Generation	61
2.7.4.1	Thin-layer mobility	62
2.7.4.2	High- k degradation mobility	62
2.7.5	Stress Effects	62
2.7.5.1	Band-to-band tunneling leakage current	63
2.8	Atomistic Simulation	63
2.8.1	GARAND	64
2.8.2	MYSTIC	65
2.8.3	RandomSPICE	66
2.9	Summary	66

3. Technology Boosters	69
3.1 Stress Engineering	70
3.1.1 Unintentional Mechanical Stress	70
3.2 Intentional Mechanical Stress	71
3.3 Stress-Engineered Transistors	73
3.3.1 CESL	73
3.3.2 STI Stress	77
3.4 Hybrid Orientation Technology	77
3.5 High- <i>k</i> /Metal Gate	78
3.6 Stress Evolution during Semiconductor Fabrication	82
3.6.1 Stress Modeling Methodology	84
3.6.2 Stress Evolution during Thick Stress Layer Deposition	85
3.6.3 Stress Evolution in Thick Stress Layer Deposition in 3D	90
3.7 Summary	93
4. BiCMOS Process Simulations	95
4.1 Ion Implantation Simulation	97
4.2 Optical Lithography Simulation	101
4.3 Contact-Printing Simulation	105
4.3.1 Nonplanar Lithography	105
4.4 BJT Process Simulation	105
4.4.1 Polysilicon Emitter Bipolar Technology	107
4.5 3D MOS Process Simulation	111
4.5.1 VictoryProcess	114
4.6 Summary	124
5. SiGe and SiGeC HBTs	125
5.1 SiGe HBTs: Process and Device Simulation	131
5.2 High-Speed SiGe HBTs	139
5.3 SiGeC HBTs: Process and Device Simulation	142
5.4 Strain-Engineered SiGe HBTs	155
5.5 n-p-n SiGe HBTs with an Extrinsic Stress Layer	157
5.6 n-p-n SiGe HBT Device Employing a Si ₃ N ₄ Strain Layer	160
5.7 n-p-n SiGe HBT Employing a SiO ₂ Strain Layer	164
5.8 Summary	167

6. Silicon Hetero-FETs	169
6.1 Electronic Properties of Strained Si and SiGe	170
6.1.1 Hole Mobility	176
6.1.2 Electron Mobility	177
6.2 Strained-Si Channel p-MOSFETs	180
6.3 Summary	193
7. FinFETs	195
7.1 Basics of FinFETs	195
7.1.1 Stress-Enhanced Mobility in Embedded SiGe p-MOSFETs	201
7.2 Stress-Engineered FinFETs	202
7.2.1 VictoryCell Process Steps	203
7.2.2 Visualization and Analysis of Simulation Results, Extraction of Average Stresses, and Mobility Enhancement Factors	209
7.3 FinFET Design and Optimization	211
7.3.1 Simulation Setup	214
7.4 Summary	221
8. Advanced Devices	223
8.1 Ultrathin-Body SOI	224
8.2 Gate-First SOI	226
8.3 Gate-Last SOI	227
8.4 3D SOI n-MOSFET	228
8.5 TFT	232
8.6 HEMTs	237
8.6.1 Thermal Optimization Using a Flip-Chip Structure	241
8.7 AlGaIn/GaN HFET	245
8.8 3D SiC Process and Device Simulation	249
8.8.1 Device Simulation	250
8.9 Summary	252
9. Memory Devices	255
9.1 Nanocrystal Floating-Gate Device	261
9.1.1 Advanced Nanocrystal Floating-Gate Devices with High- <i>k</i> Dielectrics	262
9.2 Technology Computer-Aided Design of Memory Devices	264

9.3	Process Simulation of Flash Memory Devices	266
9.4	Device Simulation of Flash Memory Devices	267
9.5	State Transition and Single-Event Upset in SRAM	273
9.6	Nanoscale SRAM	276
9.7	Summary	280
10.	Power Devices	281
10.1	LDMOS	281
10.2	Vertically Diffused MOS Devices	291
10.3	Summary	296
11.	Solar Cells	297
11.1	Solar Cell Simulation	299
11.2	Organic Solar Cells	301
11.3	Tandem Solar Cells	305
11.4	3D Solar Cell Simulation	309
11.5	Summary	312
12.	TCAD for SPICE Parameter Extraction	313
12.1	Compact Model Generation	313
12.2	Compact Modeling of HBTs	318
	12.2.1 VBIC	319
	12.2.2 MEXTRAM	320
	12.2.3 HICUM	321
12.3	Device Characterization	322
	12.3.1 ICCAP Device Modeling: $1/f$ Noise Measurement Configuration	323
12.4	Parameter Extraction Methodology	326
12.5	UTMOST	330
	12.5.1 BSIM3	332
	12.5.2 Parameter Extraction	333
12.6	Summary	338
13.	Technology CAD for DFM	341
13.1	Process-Aware Design for Manufacturing	342
	13.1.1 Seismos	342
	13.1.2 Paramos	343
	13.1.3 Fammos	343
13.2	TCAD for Manufacturing	344
13.3	TCAD for DFM	348

13.4	Process Compact Models	352
13.4.1	Process Parameterization	354
13.4.2	Process Calibration	354
13.4.3	TCAD Validation	355
13.4.4	PCM Simulation	355
13.5	Summary	359
14.	VWF and Online Laboratory	361
14.1	Internet-Based TCAD Laboratory	368
14.2	Microelectronics and VLSI Engineering Laboratory Module	377
14.2.1	Integrated Technology CAD Laboratory	381
14.3	SPICE Parameter Extraction	385
14.4	Summary	387
	<i>Index</i>	389

Preface

At the beginning of 2015, the fifth-generation Intel Core processor was released, which is built with 14 nm technology containing 1.3 billion transistors. The first processor built with the 14 nm technology is the Intel Core-M processor. Generally speaking, the architecture of transistors has now switched from the planar to the vertical design. To provide the necessary support to keep the semiconductor industry on its technological growth track, heavy emphasis is being placed on technology computer-aided design (TCAD) now for achieving key long-term research results.

Even though the predominant focus of the semiconductor industry in the 1990s and early 2000 was on biaxially strained devices, the current focus has shifted to process-induced uniaxial stress, which is being adopted in all high-performance logic technologies. Uniaxial stress has several advantages over biaxial stress, such as larger mobility and performance enhancements. Encouraged by the strain-enhanced planar metal-oxide-semiconductor field-effect transistors (MOSFETs), researchers recently applied uniaxial stress to multigate devices with a metal gate and high- k dielectric as performance boosters. Despite the advantages provided by the manufacture of transistors, introduction and optimization of the mechanical stresses in the channel remain essential.

TCAD simulations provide a comprehensive way to capture the electrical behavior of different devices with different materials and structures for performance assessment. This monograph aims to provide the reader with a comprehensive understanding of the technology development for stress- and strain-engineered device processing. With specific case studies, applications of the process/device simulation programs in process and device development are shown. The aim of this monograph is also to provide device/circuit designers with the ability to predict what impact statistical process variations will have on their designs, as early as possible, using several commercially available tools. As currently, uniaxial strain is being adopted in all high-performance logic technologies

and applications by the industry, we shall focus mainly on process-induced uniaxial stress in this monograph.

Next-generation wireless systems, driven by a vast assortment of rapidly emerging applications operating at radio frequency (RF) and millimeter-wave frequencies, are placing increasingly stringent cost and performance demands upon the supporting microelectronics technologies. On the basis of its performance capabilities, low cost, and capacity for high integration, silicon germanium (SiGe) heterojunction bipolar complementary metal-oxide semiconductor (BiCMOS) technology has established itself as a strong technology contender for a host of such circuit applications, including analog and mixed signals, RF, and millimeter waves. However, as operating frequencies for wireless applications are pushed upward in the spectrum, SiGe heterojunction bipolar transistor (HBT) technologies face significant challenges at the transistor level as operating voltage decreases and performance requirements increase.

Starting with the 90 nm technology node, improved transistor performance has been achieved with the introduction of stress and strain in the transistor. One of the major limitations of the currently available related books is that the most of the design and simulation results presented are obtained using 2D simulations without involving stress. Due to the ultrasmall size of state-of-the-art devices, 3D effects have been dominant. To achieve a better understanding of simulated and fabricated device characteristics, 3D process/device simulation involving stress is necessary. This monograph presents mostly the 3D simulation and analysis of stress- and strain-engineered semiconductor devices for digital, analog/RF, and power applications. Detailed and extensive TCAD simulations are carried out for 3D fin field effect transistors (finFETs), and the key parameters are identified.

TCAD is shown to be an excellent resource for teaching microelectronics. The objective of a laboratory component of any semiconductor fabrication course is to teach the students the unit processes involved in microelectronic fabrication and to introduce the practice of process development. Virtual wafer fabrication (VWF) has become an integral part of the semiconductor industry now. The possibility of teaching semiconductor manufacturing in a university environment in a highly cost-effective manner by taking the advantages of high-speed internet and available TCAD tools has been explored.

Recently, several excellent books and monographs have appeared on multigate MOSFETs, high-mobility substrates and Ge microelectronics, and strained semiconductor physics. Numerous papers have appeared on strained Si and process-induced strain, but there is a lack of a single text that combines both strain- and stress-engineered devices and their design and modeling using TCAD. Attempts have been made to summarize some of the latest efforts to reveal the advantages that strain and stress have brought in the development of strain-engineered devices. We have included important works by the research community, as well as our own research students' works and ideas. The monograph is mainly intended for final-year undergraduate and postgraduate students of electrical and electronic engineering disciplines and scientists and engineers involved in research and development of high-performance devices and circuits. The monograph may serve as a reference on strain-engineered heterostructure devices for engineers involved in advanced device and process design. Instructors involved in teaching microelectronics may also find this monograph useful for laboratory education using remote web-based TCAD laboratories.

After reading the monograph, the students will learn the fundamentals of process and device simulation programs. They will be able to analyze arbitrary device structures to speed up the designing using commercial software. Approaches presented in this monograph are expected also to boost the use of TCAD tools for device characterization and compact model generation.

I am extremely grateful to my research students who made significant contributions to make this monograph a reality. I would also like to express my deep appreciation for the Pan Stanford Publishing team. Finally, I would like to thank my family members (wife, Bhaswati, and sons, Ananda and Anindya) for their support, patience, and understanding during the preparation of the manuscript.

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