R-2R Ladder Circuit Design for 32-bit Digital-to-Analog Converter (DAC) with Noise Analysis and Performance parameters

Sunil S. Parmar, Anuradha P. Gharge

***Abstract*—In modern ICs, signal circuits like ADCs and DACs plays an important role in mixed signal processing. There are thousands of times that you need a signal in analog form. For example to process a signal or data generated by any computer there may be need a signal of an analog form. A simple example of it is a conversion of computer data into Audio-Frequency tones needs for telephony. This function is done by the circuit called DAC. There are numbers of DACs available which may of M-number of bits. In this paper a simple way to design a DAC with register networks (R-2R) is presented. R-2R ladder systems give a straightforward intends to change over digital data to an analog yield. The performance of the R-2R DAC in terms of efficiency or resolution is the major issue of this type of network. Due to mismatching of resistor the performance of R-2R is somehow limited although this type of ladder can be realized as a ICs (Integrated Circuits). Calibration is one of the method by which Integral and Differential Non-Linearities can be reduced. Low noise performance of the resistor ladder (R-2R) DAC, allows it to be used in high performance audio solution. Compensation of DNL and INL nonlinearities are possible somehow even though static distortions are the most often in high end ladder network digital to analog converter. In this paper, 32-bit DAC is presented with noise voltage analysis and other performance parameters, theoretical and simulation in microwind 3.1 with noise voltage analysis is also presented.**

***Index Terms*—ADC, DAC, DNL, INL, Ladder network.**

I. Introduction

ANALOG nature is dominated in real world signal. Interfacing of these analog signals to digital systems is done using Data converter like analog to digital converters (ADCs). Digital to analog converters does the conversion back in analog domain which was converted or initially in analog form. In modern communication and mixed-signal system this conversion is common function. Creating a single

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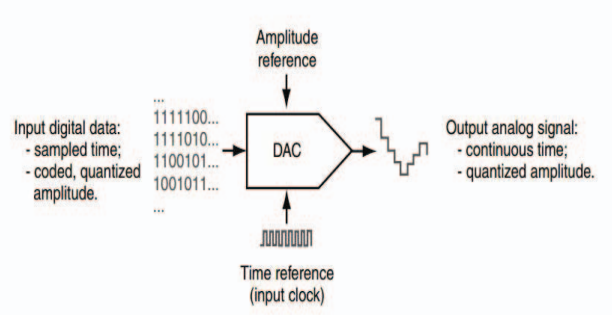

Fig. 1. Block Diagram of system [3]

analog value of set of binary levels is done by DACs. A simple analog value to digital converter, or ADC, performs the previous assignment while a digital to analog converter, or DAC, performs the last mentioned. In the integrated circuits, usage of DACs are most dominated circuit part that exponentially increased since development of digital computers. DACs plays a relevant role in complex system designing Nowadays [1], [2].

Advanced DACs just in part profit by the late improvements of the CMOS IC forms. While designing of DACs, some of the parameters are expected to optimize for example accuracy, sampling rate Fs, speed of DAC and utilization of signal bandwidth also needs to focus on production cost which are problematic design bottlenecks.

The capacity of the DAC considered as an interpretation of the theoretical level of advanced data to solid simple elements there by method for simple static or element portrayal of the yield of the DAC [3].

As we know that, Digital to analog conversion is generally alter the digital input signal into a corresponding analog output signal. Continuous-amplitude and continuous-time analog output signal can be derived from Digital input signal which is identified by discrete-amplitude and discrete-time digital signal [4]. In Fig. 1, a simple block diagram of a DAC, together with the digital input and analog output signals are depicted. Based on various decoding algorithm DACs can be portrayed by three common architecture: binary, thermometer and segmented architectures [5]. For the specific input signals, there are also other types of DAC characterization are available, e.g. sine-weighted DACs. One can specify DACs on the basis of physical implementation according to how an

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element is implemented, architectures are given by: resistor DACs, capacitor DACs and current-steering DACs [5]. These architectures introduces glitches as transformation of more than one bit at a sampling time or it adds noise as resisters are one of eminent noise source. As a result, DAC output results in unpredicted analog output value. It consumes large area as it is dominated by passive components and at the higher resolution it is less accurate to its static characteristics due to high differential non-linearity (DNL). In [4] the merits and demerits of each architecture are figured out by different parameters like integral nonlinearity (INL), differential nonlinearity (DNL), monotonicity.

Current steering [3], [1] and resister ladder are the most prominent construction of DACs because these can be easily implemented in CMOS processes and it gives a better adjustment between covered area, power dissipation, and speed. In this paper R-2R ladder 32-bit DAC has been given with noise performance parameters simulated which gives easy implementation and is cost effective. Next section gives brief of ladder network, In section III performance parameters of DAC has been listed out, in the section IV architecture of 32-bit R-2R DAC and in section V its noise analysis followed by conclusion and references is depicted.

II. RESISTOR LADDER ARCHITECTURE

The resister ladder network is a compact network which is mostly used in digital to analog converters (DACs) and generate binary weighted current or voltage levels [6]. To build an N-bit of passive resistor DAC, it requires 2N resistors of just two distinct qualities R and 2R.

Fig. 2 shows configuration of two different value resistors for R-2R ladder. This R-2R DAC gains inputs from N-bits data. This design comprises of a system of resistors fluctuating in estimation of R and 2R. Starting at the right end of the system, it demonstrates that the resistance looking to one side of any hub to ground is 2R [7].

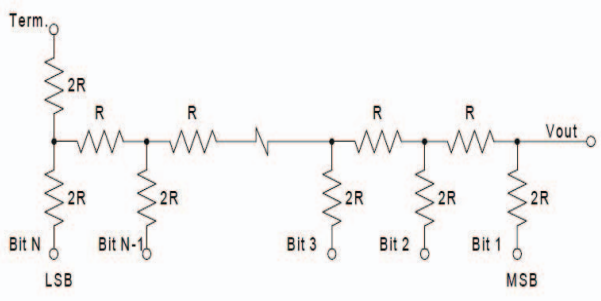

Fig. 2. N-Bit R/2R Ladder [7]

By a binary-weighted relationship caused by the voltage divider rule of the ladder network, each node voltage is related to some reference voltage V_{ref}. Because of the potential at the bottom of each switched resistor is always null, the final current flowing from V_{ref} is constant. This leads to steady node voltage for any value of digital input bits. For the output voltage, V_{ref} is calculated by the (1.1) shown in [8].

$$v_{out} = D \times (\frac{V_{ref}}{2^n}) \tag{1.1}$$

Where D show the digital data word decimal quality, n indicates resolution of DAC, and DAC reference voltage is given by V_{ref} [8].

III. PERFORMANCE PARAMETERS [9], [1]

Resolution, accuracy, linearity, monotonicity, and settling time, etc. are some of the performance characteristic parameters of a DAC.

1) Resolution: The number of bits used to generate the analog output is called resolution. DAC can produce the number of analog output levels that determines resolution which is normally expressed in bits. This is the littlest conceivable change in yield voltage as a portion or rate of the full-scale range [4]. For example, there exist 256 possible analog output voltage level for an 8 bit data converter. Hence the smallest change in the output voltage is 1/255th of the full scale output range. Its resolution is one part in 255.

2) Accuracy: The ADC resolution is defined as the smallest incremental voltage that can be recognized and hence it causes a change in the digital output. It is usually expressed as the number of bits output by the ADC or in terms of a percentage of a full-scale, or maximum output voltage. For example, if a converter has a full-scale output of 10V and the accuracy is ±0.1 %, then the maximum error for any output voltage is (10 V)(0.001) = 0.01V. Ideally, the accuracy should be, at most, 1/2 of an LSB (Least Significant Bit). For a 10-bit converter, 1 LSB is 1/1024 = 0.00097 (0.097% of full scale). The typical value of accuracy is approximately ±0.2%.

3) Linearity: Fig. 3 shows the best review that how we figure out linearity of DACs. In DACs, it is favourable to measure only two linearity: Differential Nonlinearity (DNL) and Integral Nonlinearity (INL).

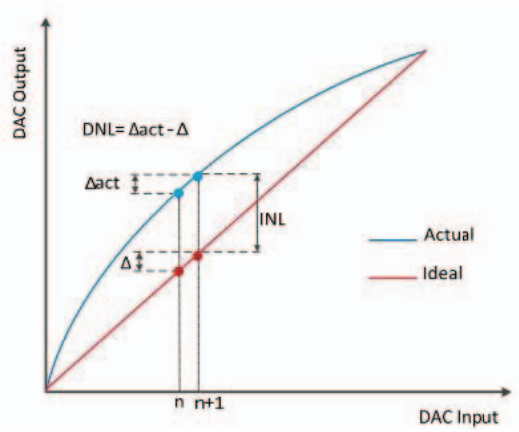

Fig. 3. DNL and INL errors of DAC [10]

DNL can be calculated as the supreme variation of a true analog output step, between adjacent input codes, from the ideal step value Δ. INL is the maximum deviation, at any point in the transfer function, of the true output level from its ideal value. The perfect quality is a straight line drawn between the real zero and full-size of the DAC [10] (see Fig. 3). Any deviation occur in ideal straight line output of the DAC is known as linear error. When all input bits are zero, amount of output voltage is known as offset error.

4) Monotonicity: Increasing in input binary digital value from one step to next step, if output of the DAC is increased then it is said to be monotonic. This outcomes the simple yield of the DAC will never diminish with an expanding in decimal quality relating to the data code, and alternately if the DAC is monotonic.

5) Settling time: Settling time is normally defined as the time it takes a DAC to settle within ±1/2 LSB of its final value when a change occurs in the input code. Being precise for DAC, settling time is the interval between a command to update (change) its output value and the instant it reaches its final value, within a specified percentage. Settling time is influenced by the huge number rate of a yield intensifier and by the measure of speaker ringing and flag overshoot [1], [9].

IV. 32-BIT R-2R DAC

Fig. 4 shows physical layout design of 32 bit R-2R DAC in Microwind 3.1 software. In this simulation results with all voltage source configure to 0V, output voltage is zero which is shown in Fig. 5.

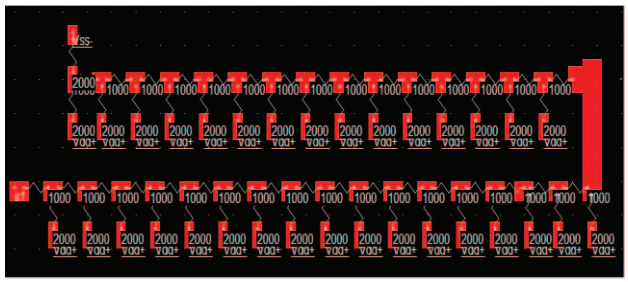

Fig. 4. 32-bit R-2R DAC in Microwind 3.1

If in the case of need, one can have an operational amplifier at the output of the R-2R ladder, it will isolate the output voltage from the operational amplifier´s final output voltage, while always keeping the both voltage at the same value level. 5 V of supply is applied to each bit of DAC which is marked as Vdd+ in Fig. 4. Two types of resistor that used are of 1000 ohm and 2000 ohm here. S1 is output node of the designed ladder DAC and Vss- indicates GND. Only for the simplicity, only few counts of input bits has taken and tabulated in table 1. In the table 1, 32 digital as a binary input is shown. As seen from table when all supply voltage are zero output voltage is zero volt. By that means applying digital inputs continuously conversion to analog can be done and for all supply voltage switched to 5 V maximum of 5 volt output is obtained.

In real time implementation we may need to use either analog or electronic switch for supply voltage that may introduce noise but by using efficient electronic switching noise can be remove or compensate.

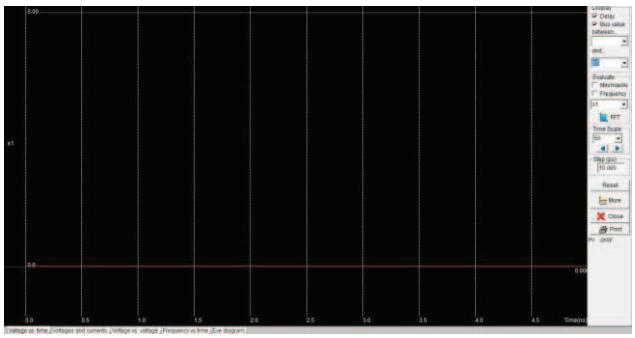

Fig. 5. Simulation results for no source connected to DAC

In any circuit noise plays a very important role. Because of resistor mismatching noise dominates this type of DAC architecture. Error in resolution is noticed, as mismatching of resister values are dominated in R-2R type of DAC. A signal from the DAC can be smoothed by an operational amplifier or low pass filter as a next stage. Accuracy optimization and noise reduction can be achieved by proper switching.

For the accuracy of the data converter noise should be kept within the half of the LSB (Least Significant Bit) size of data converter. LSB size of 32 bit converter is 5.8207 nV for 5 V of reference input voltage. In proposed DAC for some counts INL calculation is given in table 2. The calculated INL is too high that indicates low performance of DAC. This large INL creates large DNL error also, ultimately low performance of DAC. Fig. 6 shows simulation result for all source connected except MSB of designed 32 bit DAC. The output voltage is near about 2.618 V, while all source connected the result is shown in Fig. 7 with output near about 5 V. multisim also provides power consumption, for this all source connected the 11.215 mW power is noticed.

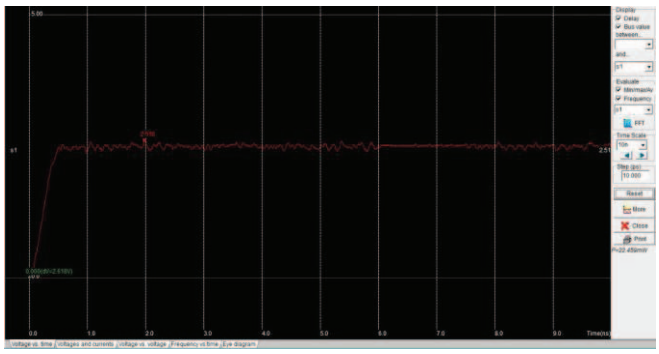

Fig. 6. Simulation results for all source connected except MSB of designed 32 bit DAC

Although resulting in low resolution, this method of converting to analog can be cost effective as compared to usage of DAC ICs. Moreover testing of such a high resolution data converters introduces some limitations or need of time consuming costly processing of signal.

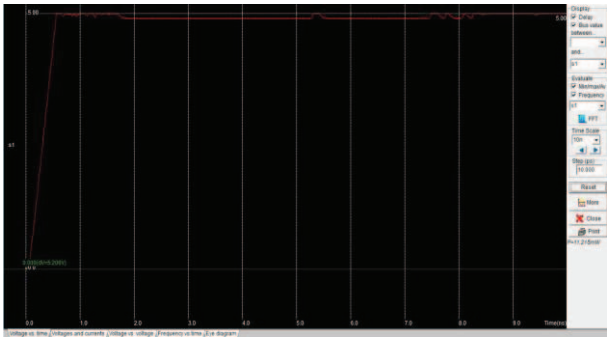

Fig. 7. Simulation results for all source connected to DAC

This low resolution DAC can be used as video DAC or in military radar system where low or moderate resolution can tolerate. Sometimes this types of low resolution DACs are used to generate a high resolution ADC test stimulus for linearity test of ADCs [11].

TABLE I
OUTPUT VOLTAGE FOR SOME COUNT OF DAC

Input Bits	Output Voltage(V)
00000000000000000000000000000000	0
00000000000000000000000000000001	0.010
00000000000000000000000000000011	0.010
00000000000000000000000000000111	0.116
00000000000000000000000000001111	0.060
00000000000000000000000000011111	0.060
00000000000000000000000000111111	0.060
00000000000000000000000001111111	0.060
00000000000000000000000011111111	0.060
00000000000000000000001111111111	0.060
00000000000000000000011111111111	0.083
00000000000000000000111111111111	0.083
00000000000000000001111111111111	0.083
00000000000000000011111111111111	0.083
00000000000000000111111111111111	0.083
00000000000000001111111111111111	0.083
00000000000000011111111111111111	0.092
00000000000000111111111111111111	0.092
00000000000001111111111111111111	0.135
00000000000011111111111111111111	0.122
00000000000111111111111111111111	0.100
00000000001111111111111111111111	0.095
00000000011111111111111111111111	0.100
00000000111111111111111111111111	0.110
00000001111111111111111111111111	0.121
00000011111111111111111111111111	0.119
00000111111111111111111111111111	0.166
00001111111111111111111111111111	0.254
00011111111111111111111111111111	0.412
00111111111111111111111111111111	0.715
01111111111111111111111111111111	1.332
11111111111111111111111111111111	2.618
11111111111111111111111111111111	5

This type of DACs are also popular to generate digital dither signal for ADCs. Also resolution of DAC can be increase by some methods like gain correction etc. In the next section noise analysis in multisim simulation software has been analysed.

TABLE II
INL CALCULATION FOR SOME COUNT OF DAC

Input Bits	Output Voltage(V)	Ideal O/P Voltage (V)	INL
00000000000000000000000000000000	0	0	0
00000000000001111111111111111111	0.122	0.00061035	0.12138964
00000000001111111111111111111111	0.100	0.00488281	0.09511718
00000000011111111111111111111111	0.110	0.00976562	0.10023437
00000111111111111111111111111111	0.412	0.3125	0.0995
00011111111111111111111111111111	0.715	0.625	0.09
00111111111111111111111111111111	1.332	1.25	0.082
01111111111111111111111111111111	2.618	2.5	0.118
11111111111111111111111111111111	5	5	0

V. NOISE ANALYSIS WITH MULTISIM 12.0

Noise analysis plays a very important part in any analog signal processing systems. As ladder circuit is dominated by noise, circuit must provide affordable noise for successive system integration. The whole circuit is implemented with Multisim 12.0 which provides noise figure analysis here it is 40 dB and output noise voltage is 28.677 nV analysed which is shown in Fig. 8.

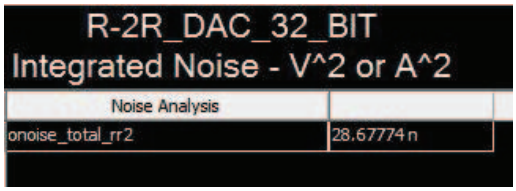

Fig. 8. Noise analysis in multisim 12.0

Also noise spectral density curve at out node of all resistor has been observed and depicted in Fig. 9 and magnified figure of is shown in Fig. 10.

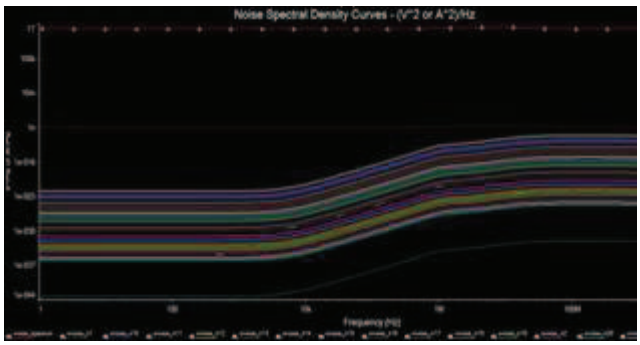

Fig. 9. Noise spectral density curves at output node of each resistor

As from the above figure we can conclude that noise voltage or amplitude fluctuations of the noise signal will increase with the increasing in the signal frequency. For 32 bit DAC with 5 volt input supply which is taken here in multisim simulation LSB size of it will be 5.820 nV. Proposed circuit noise is ≈5.73 LSB of DAC which indicates low output resolution of designed DAC. But as explain earlier it can be modified or it can be used in the application where moderate resolution is

tolerable.

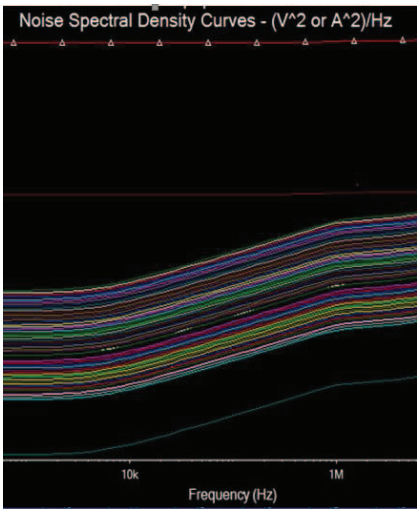

Fig. 10. Magnified image of Fig. 9

VI. Conclusion

In this paper 32-bit R-2R DAC in Microwind 3.1 is presented, and INL for few counts has been calculated. Large INL results in low resolution of DAC and gives low performance. But low cost and easy implementation of this type of DACs is one advantageous part. For the future span the resolution enhancing methods with this type of DACs can be cost effective than traditional available DACs. Physical layout and real implementation can be adopt to test this results.

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