Generic parameterized cell library for logic synthesis with DC-biased RSFQ logic

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# Introduction and setup

## Introduction

This cell library was developed under the IARPA SuperTools/ColdFlux contract via the U.S. Army Research Office grant W911NF-17-1-0120. The aim was to create a generic RSFQ cell library which can be used by circuit designers.

The libraries were developed using open-source tools - *WRspice* and *XIC*.

The RSFQ library is designed with integrated Passive Transmission Line (PTL) drivers and receivers to minimize complexity and, possibly, surface area required when constructing circuits. Separate PTL driver and receiver interconnects are therefore no longer necessary when connecting the cells to PTLs. To indicate the integration of PTL drivers and receivers, the letter ‘T’ is added at the end of the cell name, for example the DFF will be referred to as DFFT.

The RSFQ cell library consists of basic logic gates which, when connected, can be used to construct more complex functions. The following core cells form the generic RSFQ cell library: JTLT, SPLITT, MERGET, DFFT, AND2T, OR2T, NOTT, XORT and NDROT. The cells are currently optimized to run at a maximum of 50 GHz.

The logic cells are tested using *XIC/WRspice* as well as *TimEx* [1]. *TimEx* is used to generate the Mealy Finite State Machine diagram and Verilog files from the cell’s extracted characteristics [2].

## Setup

The cell library is designed to be simulated using *XIC/WRspice* and is stored in the *cir* file format. *XIC* is an *XicTools* software product maintained by Whiteley Research – hosted at <http://wrcad.com/>. The software can be installed on Linux, OS X and Windows devices. The download, installation instructions and the manual can be found on the website.The Josephson Junction (JJ) model for the MIT process should be added to the technology file.

*TimEx* is found on a GitHub repository [1] and should be set up before running the examples provided for the RSFQ library.

## License

The ColdFlux RSFQ generic cell library is free to distribute and/or modify under the terms of the MIT license.

# Cell construction

## The Josephson Junction

The critical current of a Josephson Junction (JJ) is defined through the reference critical current within the JJ model definition and the given area of the JJ. The JJ model definition for the MIT-LL process is:

.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA),

where icrit is the reference critical current. The area of a JJ defined within the netlist is used as a scale factor to represent the ratio of the instance critical current to the reference critical current [3]. The netlist definition of a Josephson junction is:

B0 n+ n- np jjmit area=2.5

where B0 is the unique JJ name,

n+ and n- are the positive and negative element nodes,

np is the phase node and, if specified, should be left unconnected,

jjmit is the model name of the JJ, and

area=2.5 states that the critical current of the JJ is 250uA.

## The *param* function

The generic cell library is constructed using the *param* function within the netlist file available in WRspice. The WRspice manual provides an extensive explanation on how the *param* function can be used [3].

The JJ areas, inductor values, JJ shunt resistor and JJ shunt inductor values are defined in terms of adaptable parameters and equations. An implementation example within the circuit file is shown below:

.param Scaling=1.0

.param B0=1

.param Ic0=0.0001

.param IcRs=100u\*6.859904418

.param B0Rs=IcRs/Ic0\*B0

.param B01rx1=1.047050014928536\*Scaling

.param IB01tx1=0.00012496339862818782\*Scaling

.param RB01rx1=B0Rs/B01rx1

…

B01rx1 3 13 23 jmitll area=B01rx1

…

IB01tx1 0 10 pwl(0 0 5p IB01tx1)

…

RB01rx1 3 14 RB01rx1

…

## Updating parameter values in circuit schematic

The parameter values within the circuit schematic are controlled using a netlist file called the electric netlist, *elecnet*, file. The file automatically incorporates the *param* function into the circuit schematic. Using the electric netlist, the user can change parameter values, import these values into the circuit schematic and test the circuit using *XIC*.

### Generating the electric netlist file

The following steps explain how the electric netlist file can be generated.

* Open *XIC* and open the circuit schematic by selecting *File* → *Open* → *New*. Ensure that all the required files are in the current working directory.
* Go to the electrical view of the *XIC* window before generating the netlist by selecting *View* → *Electrical*.
* In the *XIC* window, select *Extract* → *Dump Elec Netlist*.
* On the Dump Elec Netlist popup window seen in Figure 1a, select the spice checkbox and click *Go*.
* The electric netlist file is created in the current work directory.
* Open the *elecnet* file using a text editor and delete any *save* parameters in the electric netlist file.

### Updating the parameter values in the circuit schematic

* Ensure that the electric netlist file and circuit is in your current working directory.
* Change the value of the desired parameter in electric netlist file using a text editor.
* Delete any *save* parameters in the electric netlist file.
* Delete all the *param* labels in the electrical view of the *XIC* window before updating the parameters of the circuit.
* In the *XIC* window, select *Extract* → *Source SPICE*. The pop-up window in Figure 1b is now seen. Do not select any checkboxes.
* Enter the full name of the *elecnet* file in the *enter name of SPICE file to source* box and click *Go*.

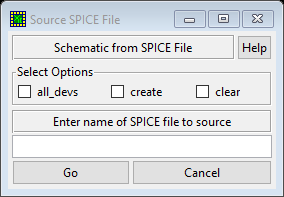
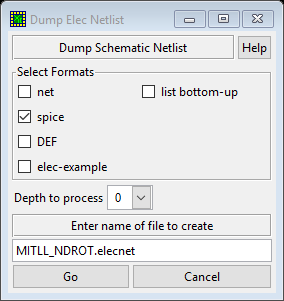


Figure 1. Pop-up windows used for changing circuit schematic parameters. a) The Dump Electric Netlist window (left) and b) the Source SPICE File window (right).

# RSFQ cell library

The integration of the PTL drivers and receivers within the RSFQ cells provides the opportunity to minimize circuit complexity and layout area. The cell library is also load independent due to the PTL interconnects. The RSFQ cells are tested using the test circuit shown in Figure 2. The source, typically a DCSFQ converter, is connected to a PTL driver (TX) followed by a PTL (Z0) and then the device-under-test (DUT).

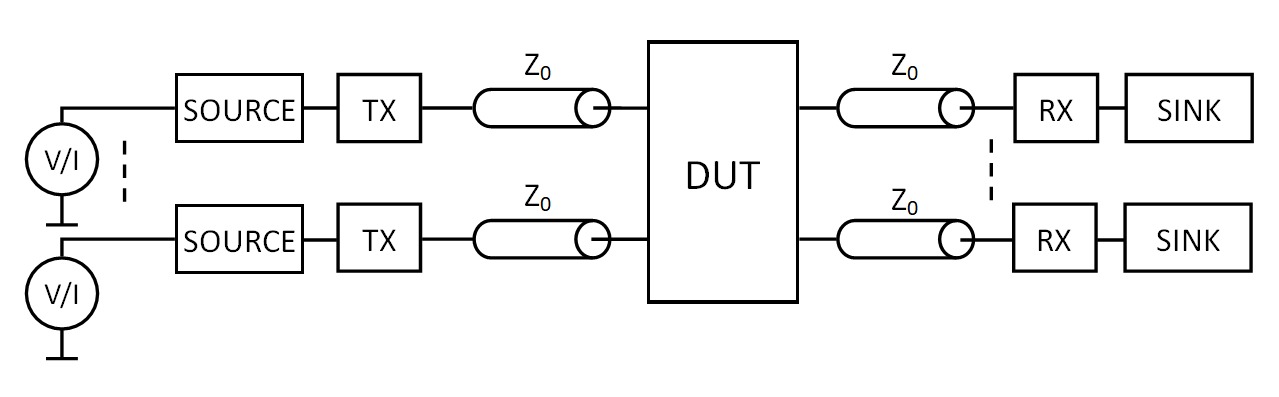


Figure 2. RSFQ test circuit diagram.

The manual includes the schematic, Mealy finite state machine diagram, the simulation graph and the margin analysis for each cell. TimEx is used to construct the state diagram as well as the resulting Verilog file after successful cell testing. The simulation graph typically includes the current through the input inductor(s), the current through the output inductor(s) and the current through the sink resistor(s). The current through the sink resistor is included to show that the pulse generated at the output can successfully travel through a PTL and trigger the connected cell.

Enlarged circuit schematics can be found in Appendix A – Enlarged RSFQ circuit schematics. The parameter values for each RSFQ cell can be found in Appendix A – Parameter values for RSFQ cell library.

## JTLT

The JTLT cell is commonly used to reestablish and propagate SFQ pulses when long PTL connections are required. The state diagram extracted for the JTLT is seen in Figure 3 and is used to describe the functionality of the cell. Figure 4 show the schematic of the designed JTLT cell. P1 is the input port and P2 is the output port. The cell is optimized using the symmetry of the regular JTL cell.

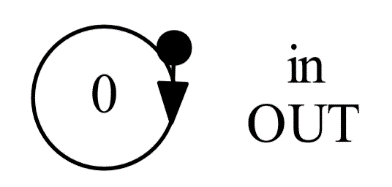


Figure 3. RSFQ JTLT Mealy finite state machine diagram extracted using TimEx.

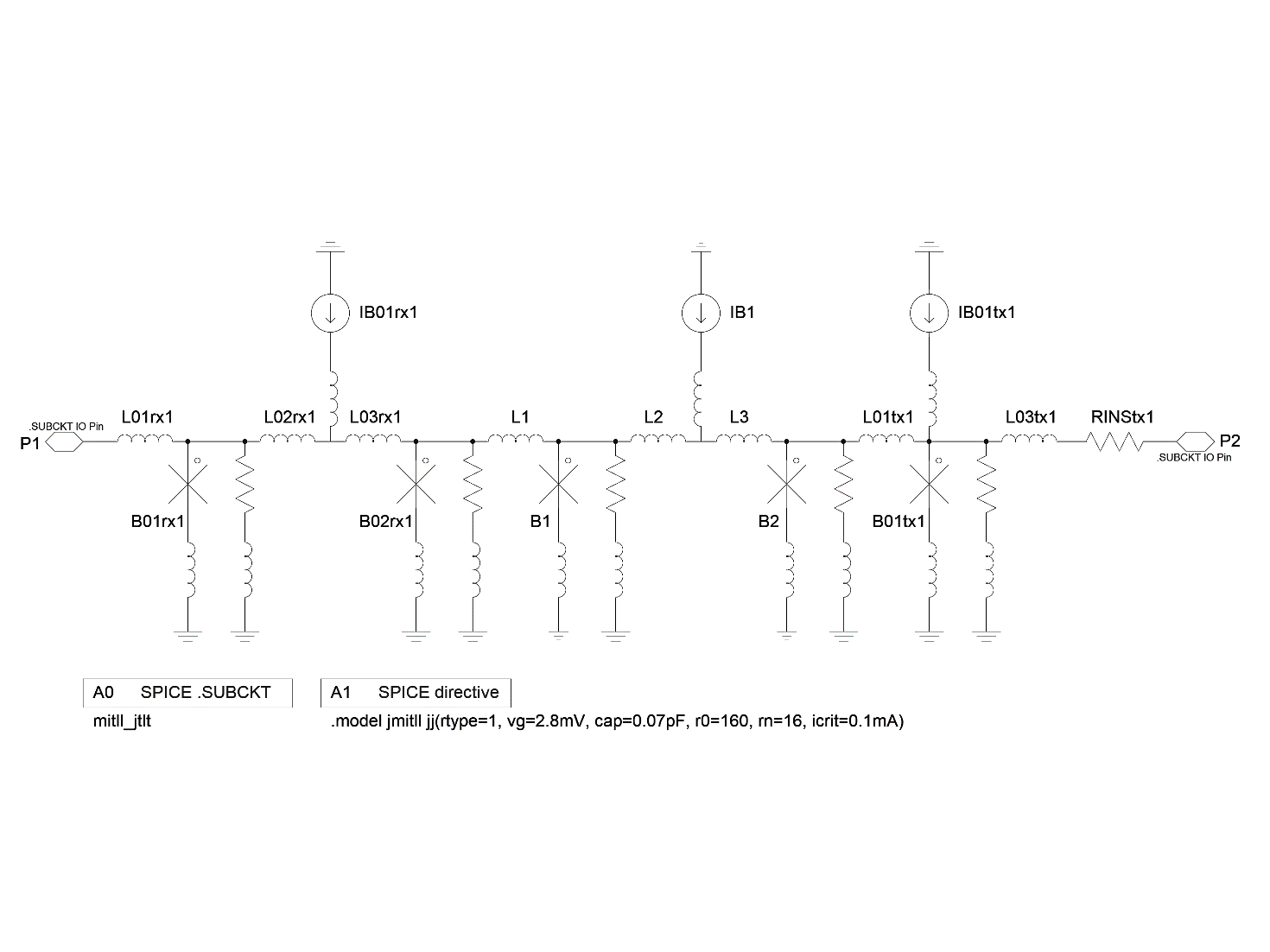


Figure 4. Schematic of RSFQ JTLT cell.

Figure 5 shows how a pulse travels through the RSFQ JTLT through a) the current, in µA, measured through input inductor L01rx1 b) the output current through resistor RINStx1 and c) the current through a sink resistor. Reflection pulses observed in the current through output resistor RINStx1 is caused by the PTL and does not affect the operation of the JTLT.

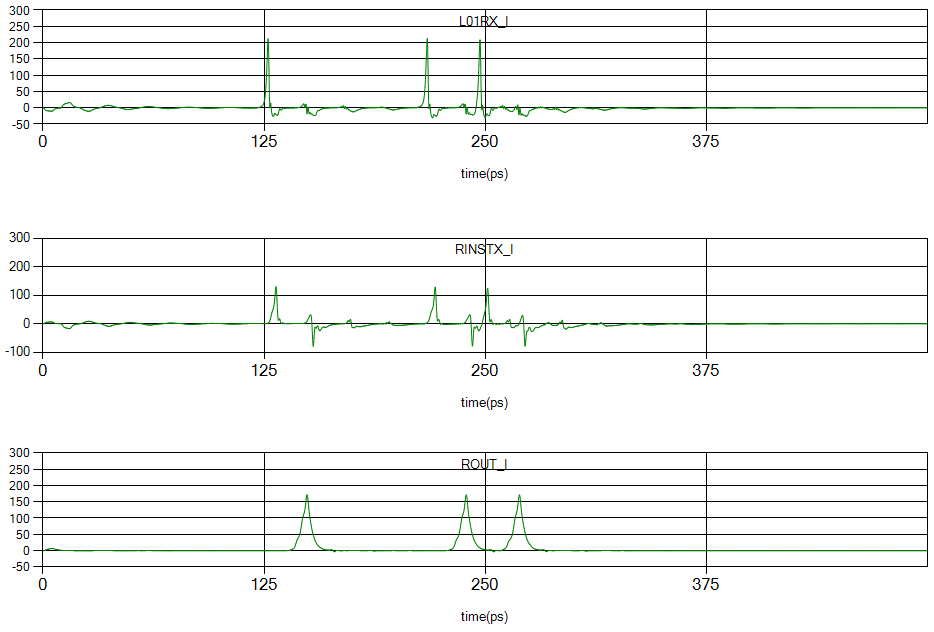


Figure 5. Simulation of the RSFQ JTLT cell showing a) the current through the input inductor, b) the current through the output resistor and c) the current through a sink resistor connected to the JTLT via a PTL with time delay 10 ps.

The margin analysis of the JTLT cell is shown in Figure 6. The critical margin is found with parameter B1tx with margins -62.6% and +73.8%.

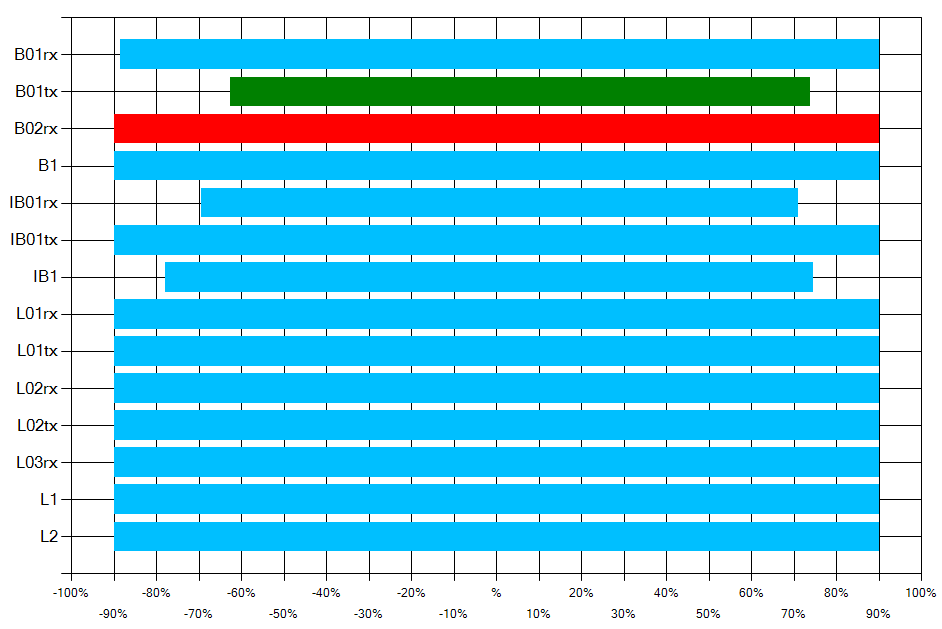


Figure 6. Margin analysis of RSFQ JTLT cell.

## DFFT

The D flip-flop is a basic memory cell which stores the input pulse and only generates an output pulse after the clock signal. If no input signal was received before the clock signal, no output will be generated. Figure 7 shows the functionality of the DFFT through a state diagram. Figure 8 provides the schematic of the designed RSFQ DFFT. P1 is the input port, P2 is the clock port and P3 is the output port.

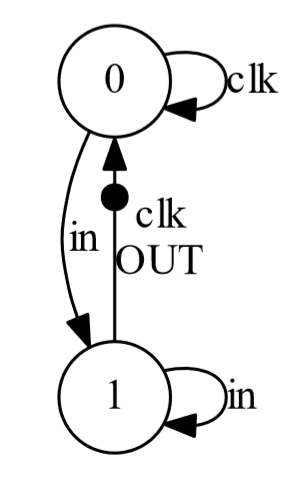


Figure 7. RSFQ DFFT Mealy finite state machine diagram extracted using TimEx.

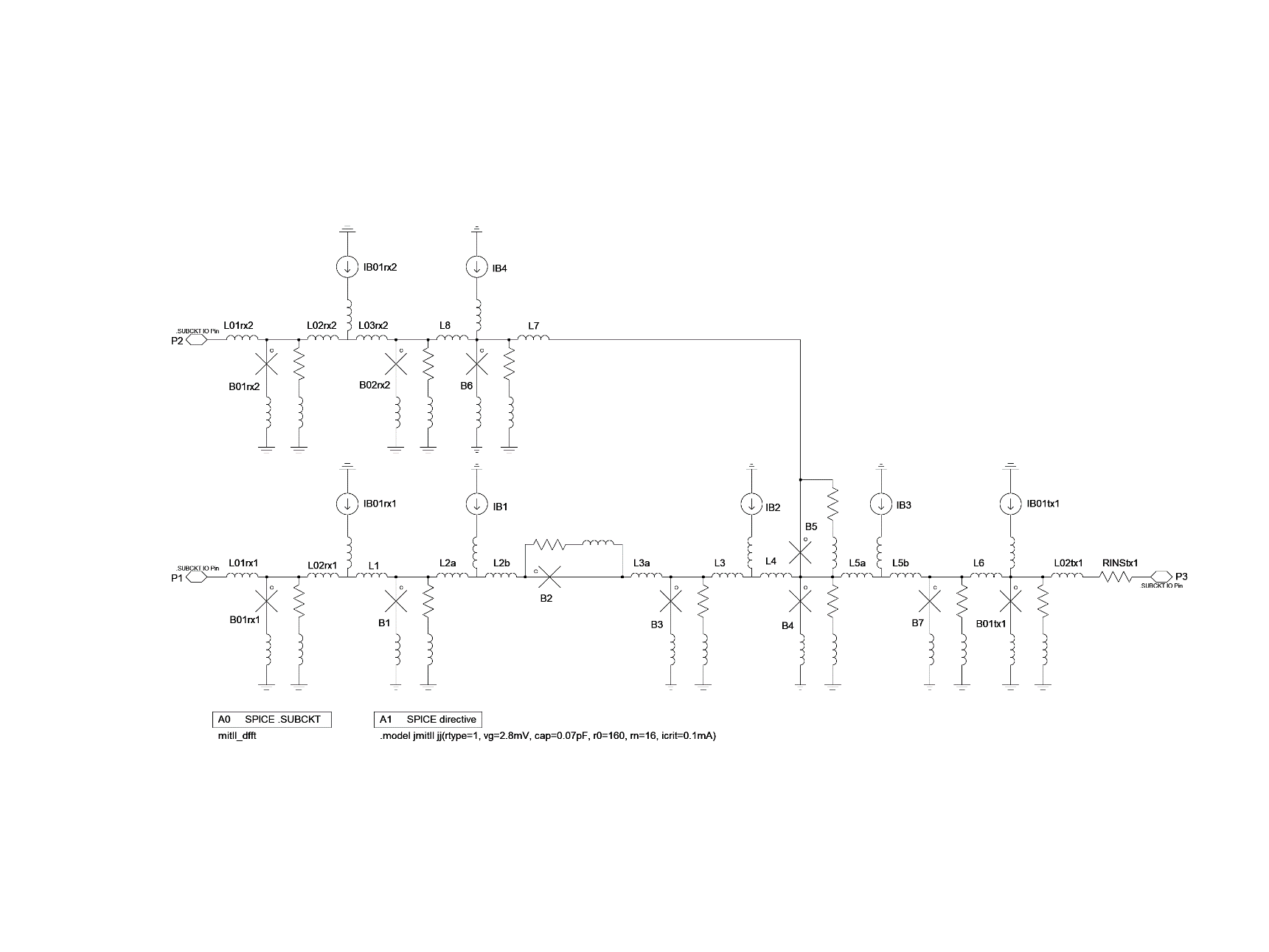


Figure 8. Schematic of the RSFQ DFFT cell.

Figure 9 shows the simulation results from the DFFT. The graph shows current, measured in µA, through a) the input inductor L01RX1, b) clock input inductor L01RX2, c) output inductor L01TX1 and d) the current through a sink resistor.

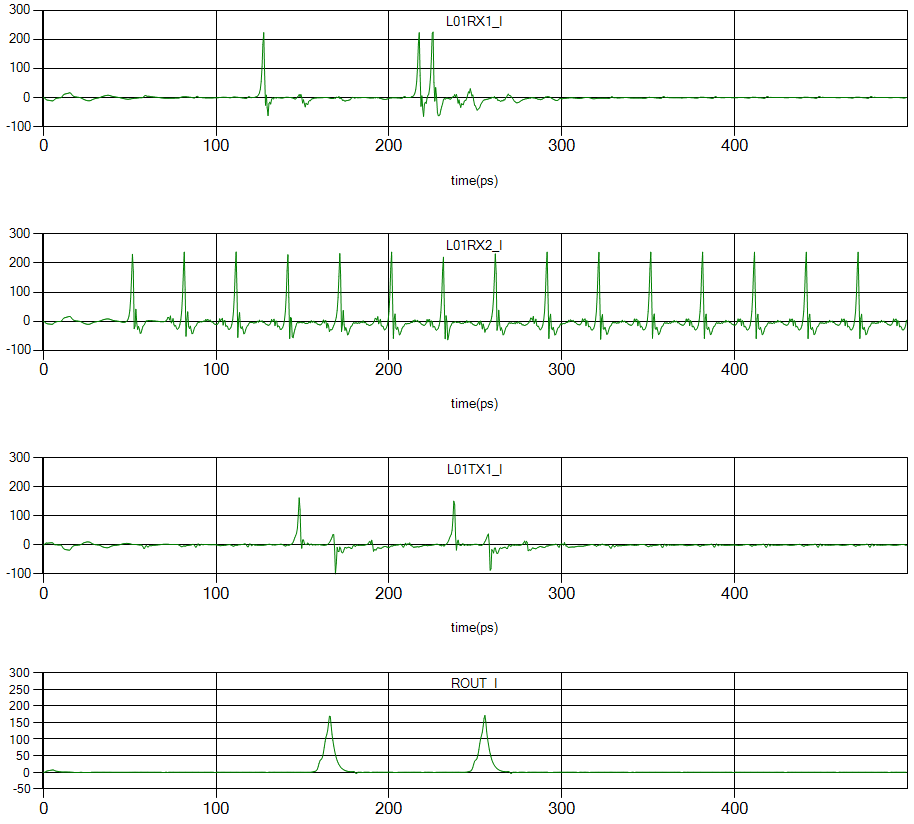


Figure 9. Simulation of the RSFQ DFFT cell showing the currents through a) the input inductor, b) the clock input inductor, c) the output inductor and d) a sink resistor connected through a PTL with time delay 10 ps.

The RSFQ DFFT margin analysis is shown in Figure 10 and the critical margin is determined by B6 with margins -21.8% and +32.3%.

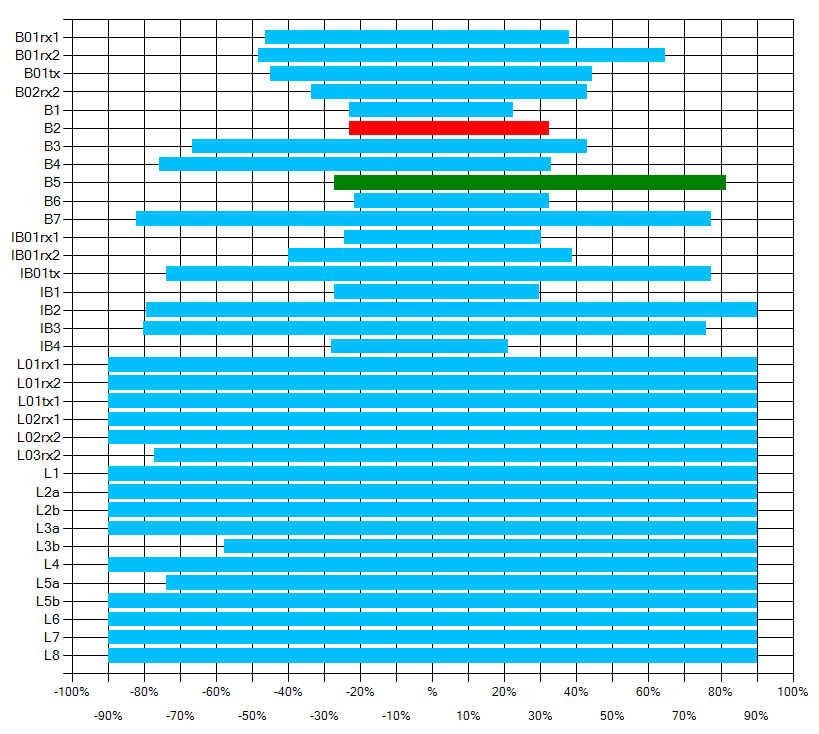


Figure 10. Margin analysis of the RSFQ DFFT cell.

## SPLITT

The splitter cell, as the name suggests, is used to divide a single pulse signal line into two pulse signal lines. Figure 11 shows the functionality of the SPLITT cell using a state diagram extracted using *TimEx*. Figure 12 shows the schematic of the designed RSFQ SPLITT cell. P1 is the input port and P2, P3 are the output ports. The splitter is optimized using the symmetry of the output sub-circuits within the cell.



Figure 11. RSFQ SPLITT Mealy finite state machine diagram extracted using TimEx.

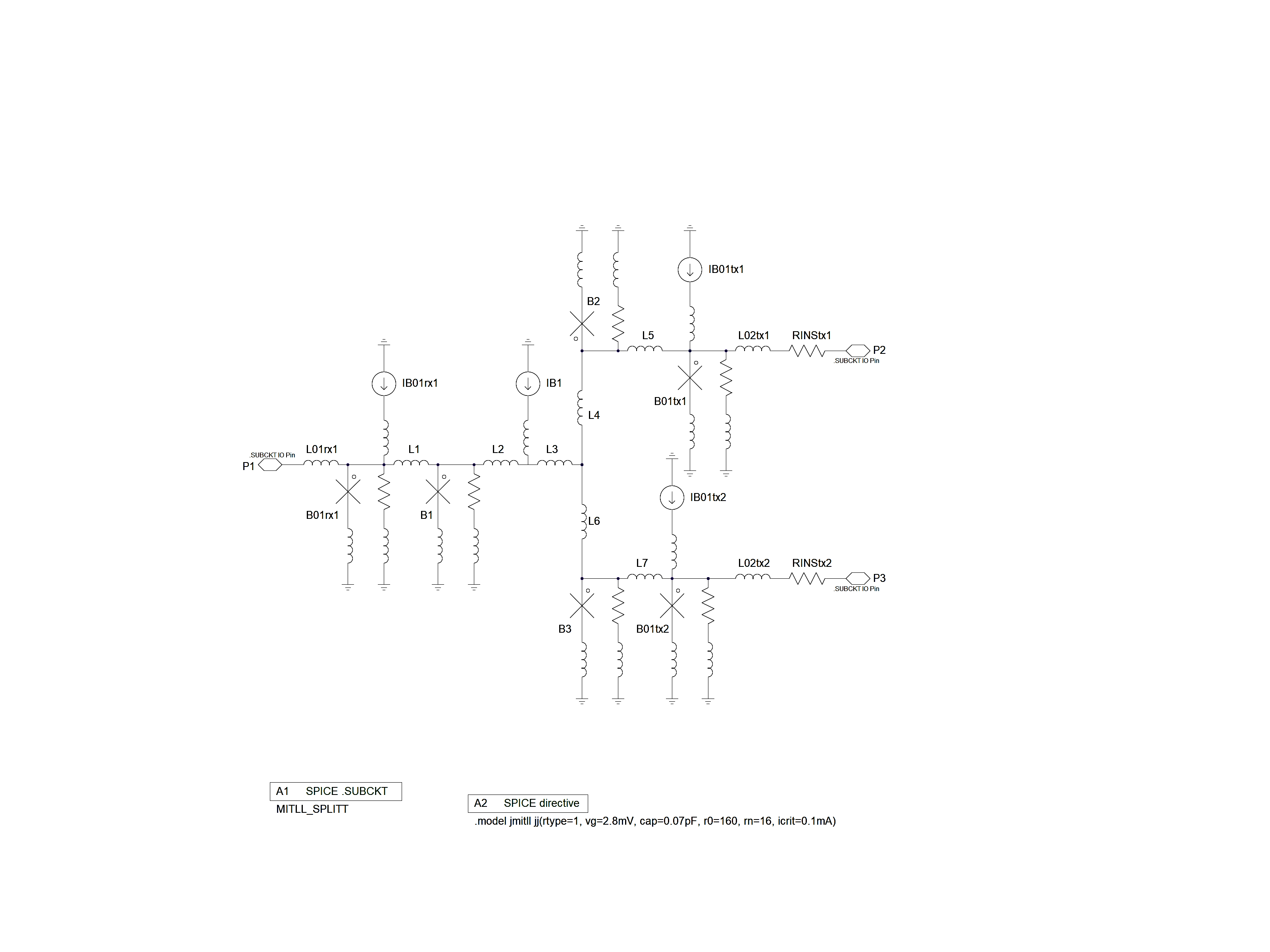


Figure 12. Schematic of the RSFQ SPLITT cell.

Figure 13 shows the simulation results for the RSFQ SPLITT cell. The functionality of the cell is shown by the current, measured in µA, through a) the input inductor L01rx2, b/c) the output inductors L02tx1 and L02tx2 and d) a sink resistor. The currents over both sink resistors are identical.

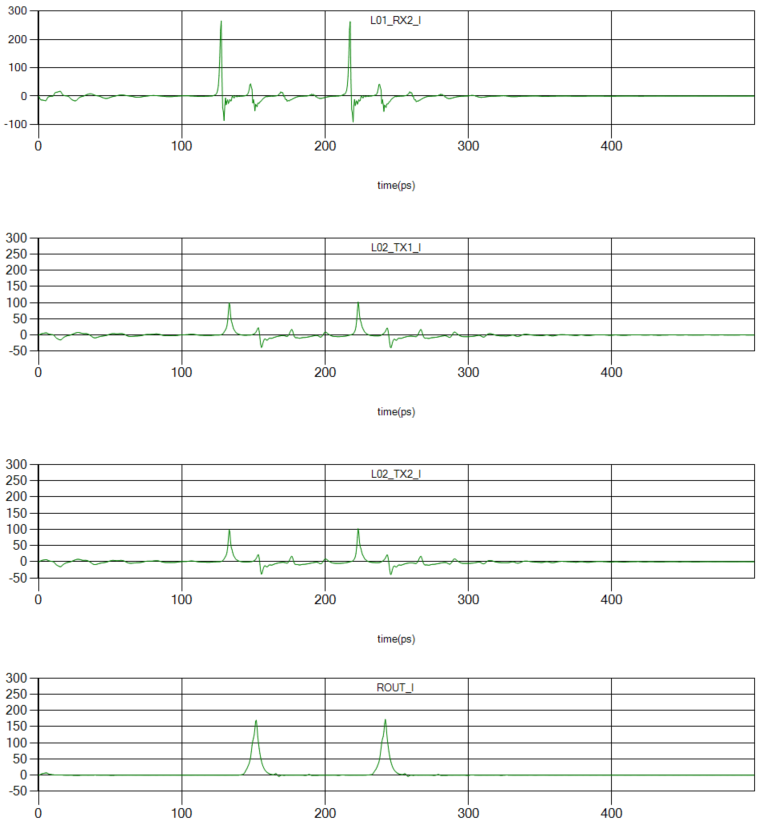


Figure 13. Simulation of the RSFQ SPLITT cell showing the currents through a) the input inductor, b/c) the two output inductors and d) a sink resistor connected through a PTL with time delay 10 ps.

The margin analysis is seen in Figure 14 and shows that the critical margins are determined by IB1 with margins -40.1% and +38.0%.

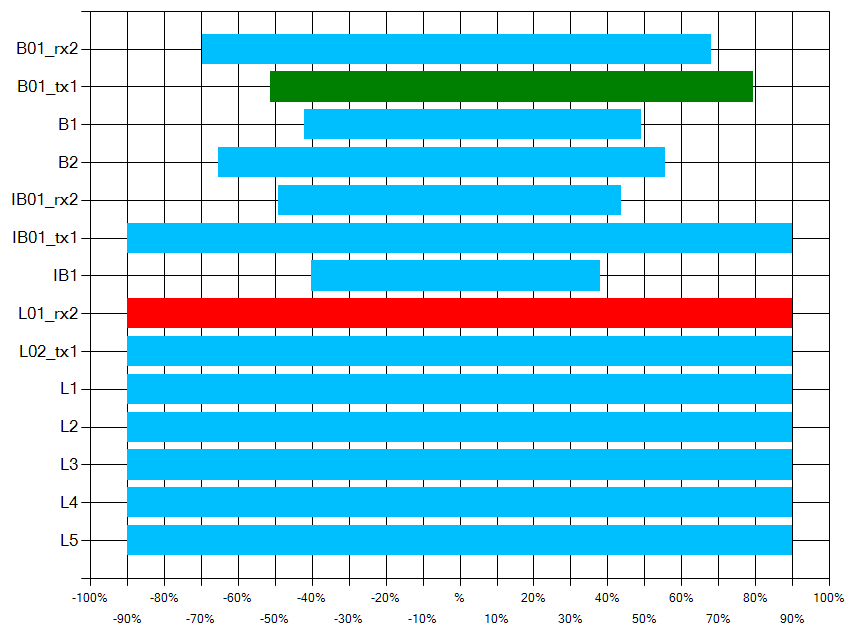


Figure 14. Margin analysis of the RSFQ SPLITT cell.

## MERGET

The RSFQ MERGET joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the MERGET will generate a pulse on the output signal line. Figure 15 illustrates the functionality through a state diagram extracted using TimEx. The schematic of the designed merger is shown in Figure 16. P1 and P2 are the input ports and P3 is the output port. The cell is optimized using the symmetry of the input sub-circuit.

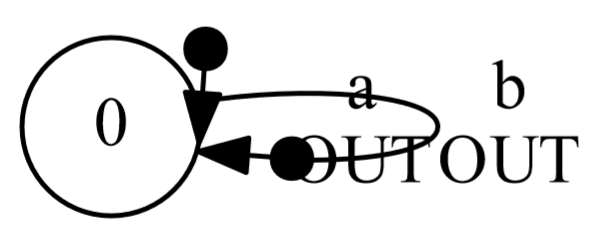


Figure 15. RSFQ MERGET Mealy finite state machine diagram extracted using TimEx.

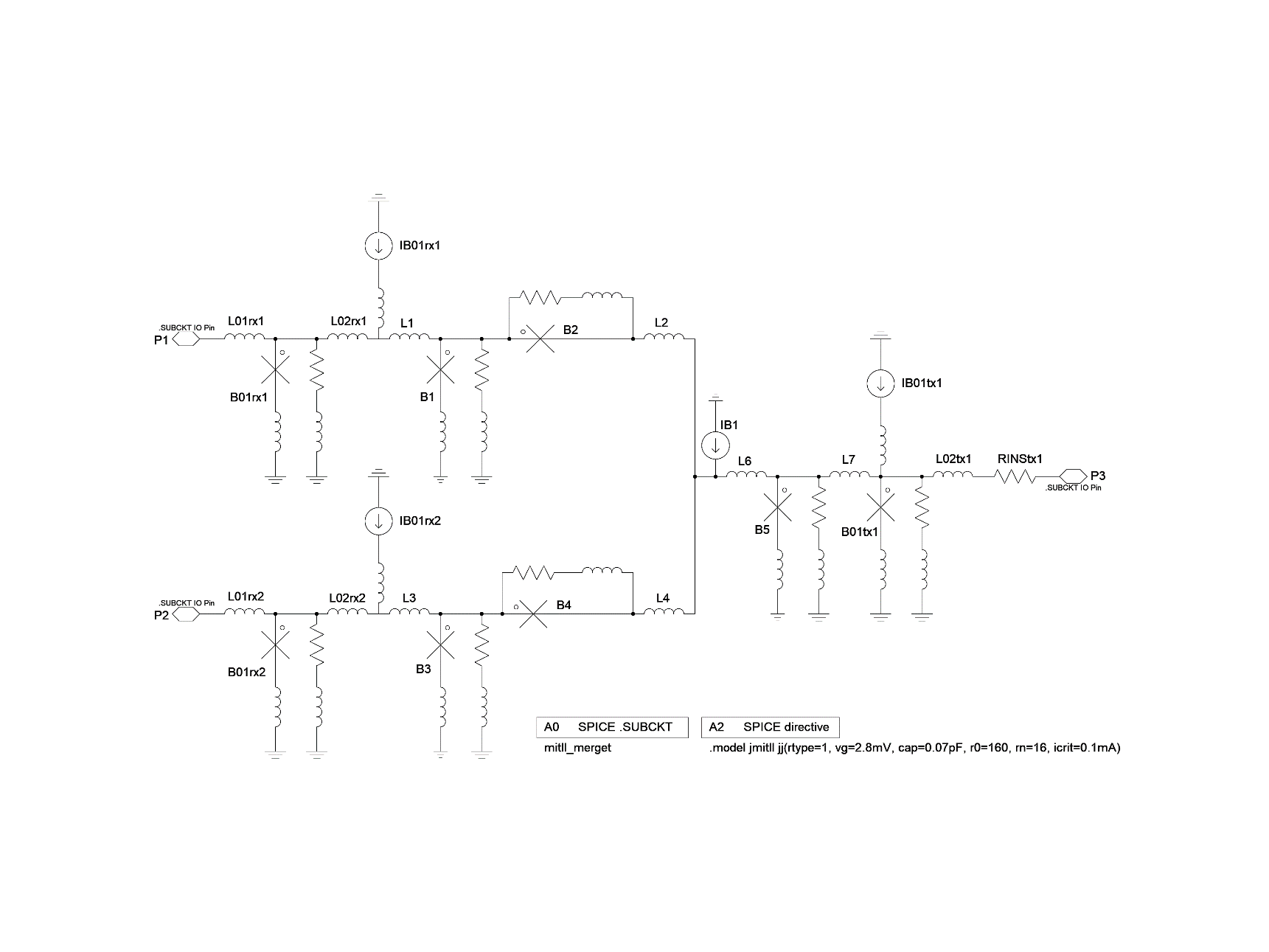


Figure 16. Schematic of the RSFQ MERGET cell.

Figure 17 shows how the MERGET cell functions within a simulation. The graph shows the current, measured in µA, through a/b) the input inductors L01rx1 and L02rx2, c) the output inductor L02tx1 and d) the sink resistor.

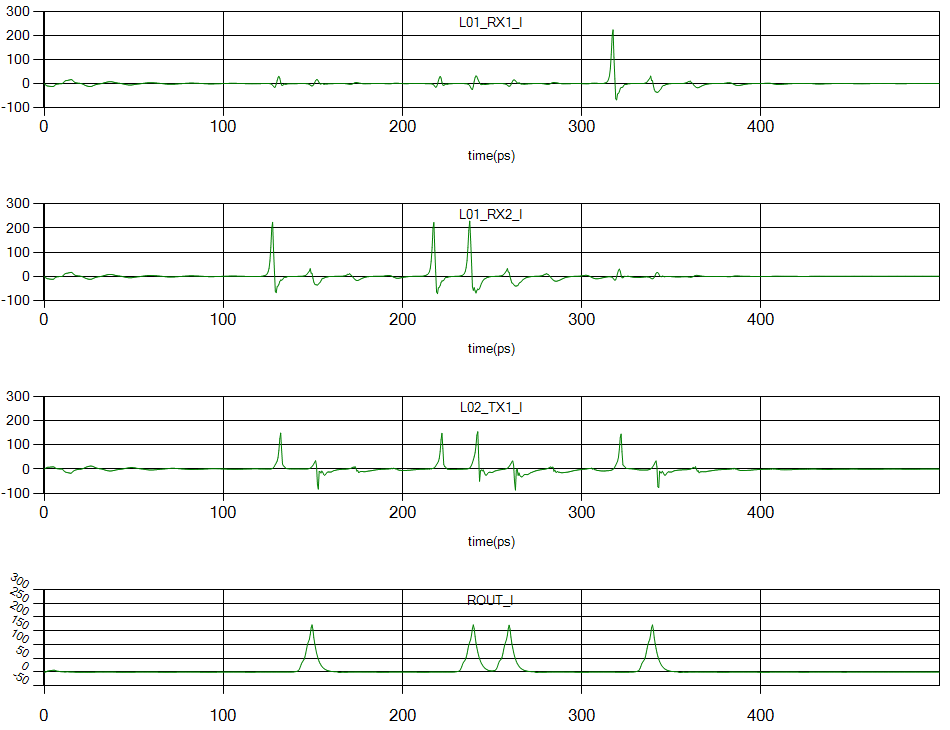


Figure 17. Simulation of the MERGET cell showing the currents through a/b) the input inductors, c) the output inductor and d) the sink resistor connected through a PTL with time delay 10 ps.

The margin analysis of the MERGET cell is shown in Figure 18 and shows that the critical margin is determined by IB1 with margins -31.6% and +30.9%.

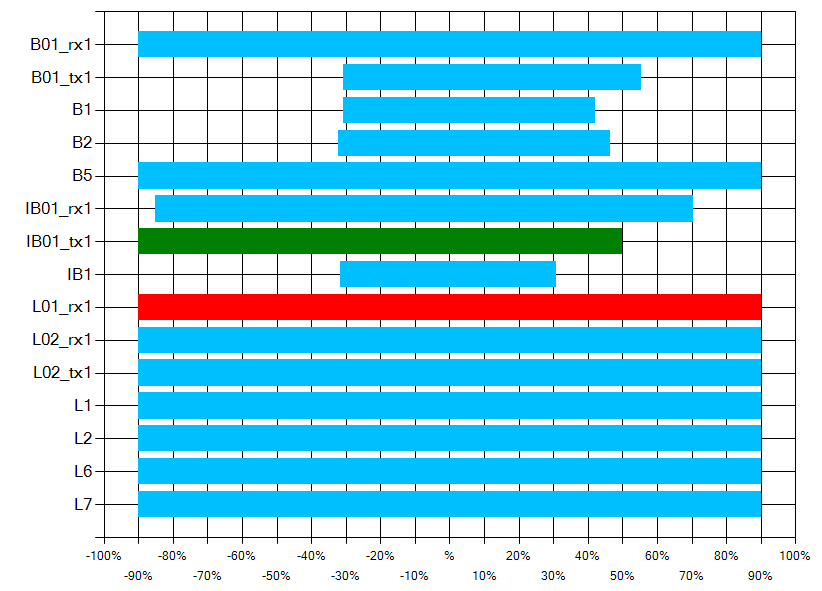


Figure 18. Margin analysis of the RSFQ MERGET cell.

## NOTT

The RSFQ NOTT cell is a signal inverting cell driven by a clock pulse signal line. The functionality is shown in Figure 19 through a Mealy finite state machine diagram. Figure 20 shows the schematic of the designed NOTT cell. P1 is the input signal port, P2 the clock signal port and P3 is the output port.

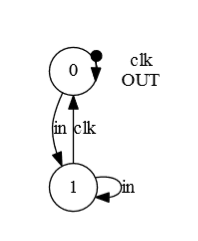


Figure 19. RSFQ NOTT Mealy finite state machine diagram extracted using TimEx.

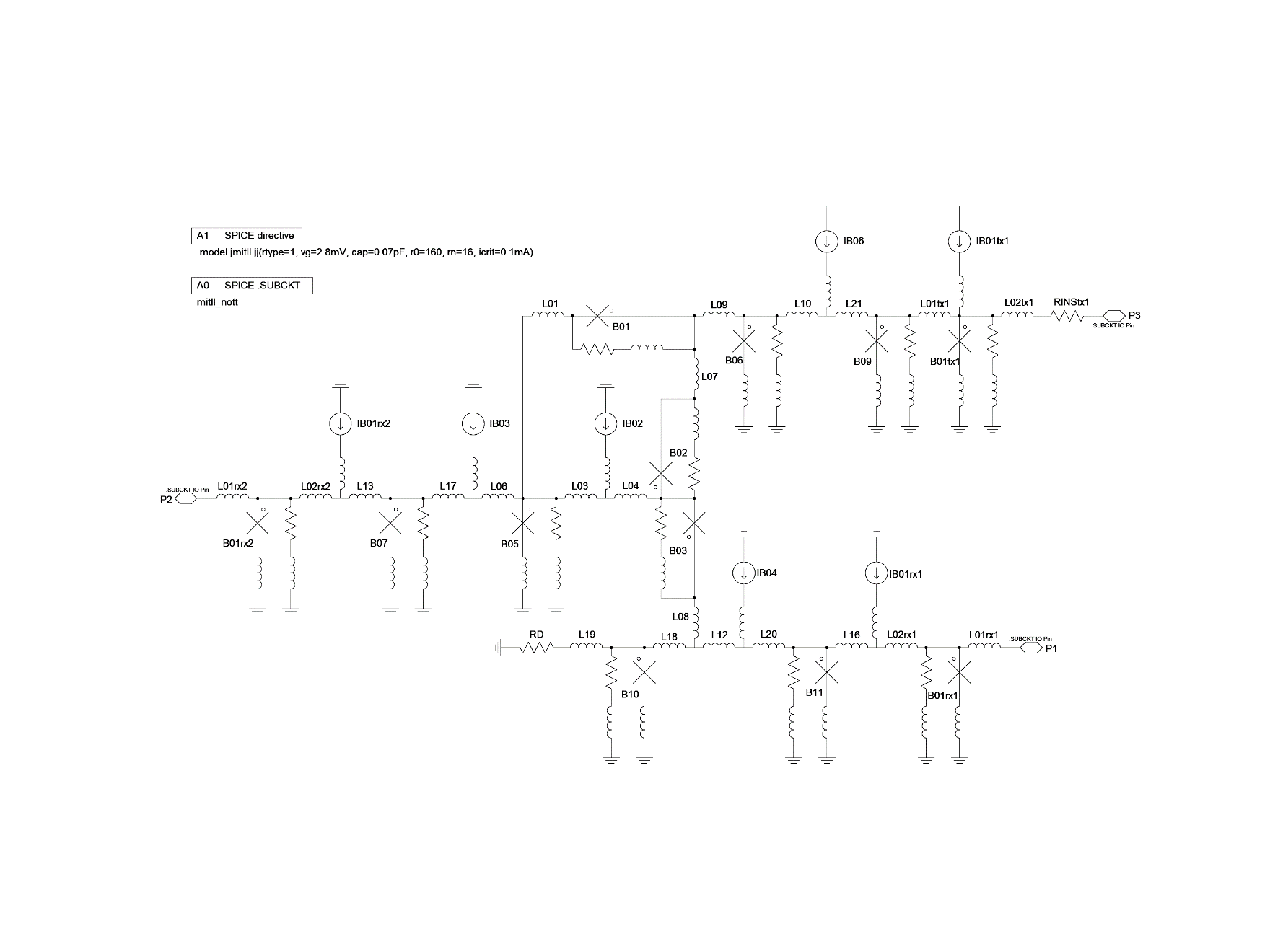


Figure 20. Schematic of the RSFQ NOTT cell.

Figure 21 shows the simulation of the NOTT cell operating at a lower frequency for illustration purposes. The operation of the NOTT cell is shown by the current, measured in µA, through a) the input inductor L01rx1, b) the clock input inductor L01rx2, c) the output inductor L02tx1 and d) the sink resistor.

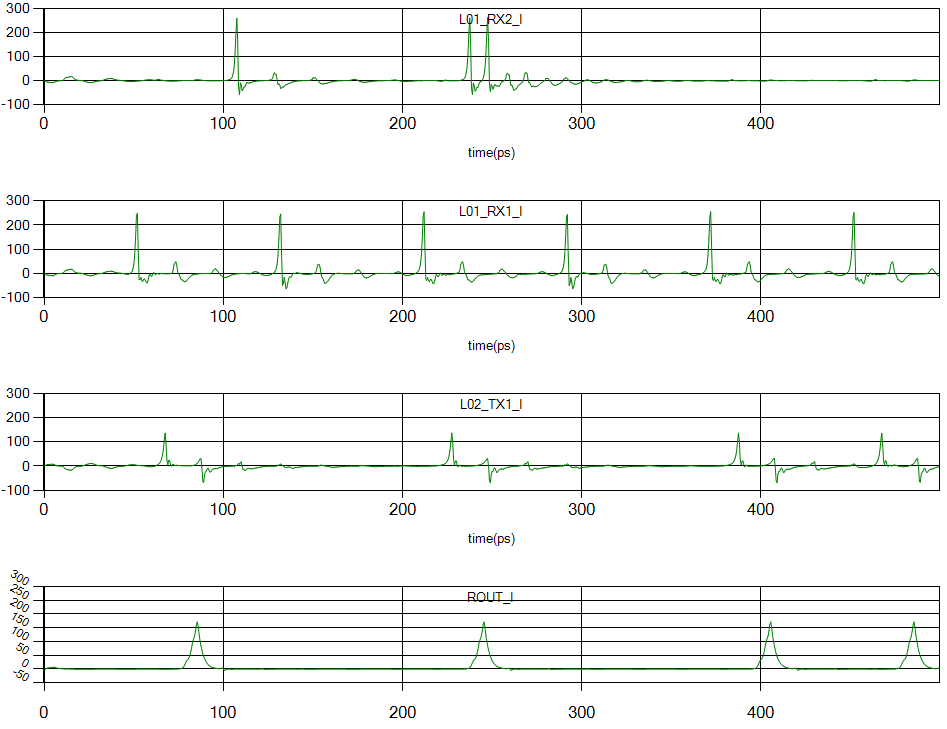


Figure 21. Simulation of the RSFQ NOTT cell showing the currents in a) the input inductor, b) the clock signal inductor, c) the output inductor and d) the sink resistor connected through a PTL with time delay 10 ps.

The margin analysis of the NOTT cell is shown in Figure 22 and shows that the critical margin is determined by B07 with margins -52.7% and +20.4%.

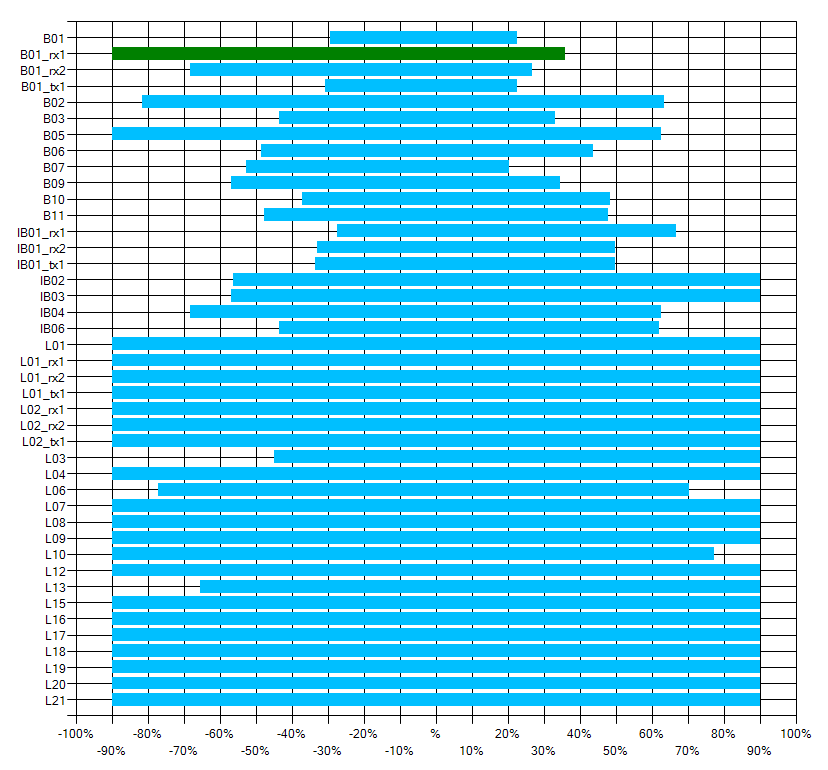


Figure 22. Margin analysis of the RSFQ NOTT cell.

## AND2T

The RSFQ AND2T cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The functionality is shown in Figure 23 through a Mealy finite state machine diagram. Figure 24 shows the schematic of the designed AND2T cell. P1 and P2 are the input signal ports, P3 is the clock signal port and P4 is the output port. The cell is optimized according to the natural symmetry of the input sub-circuits.

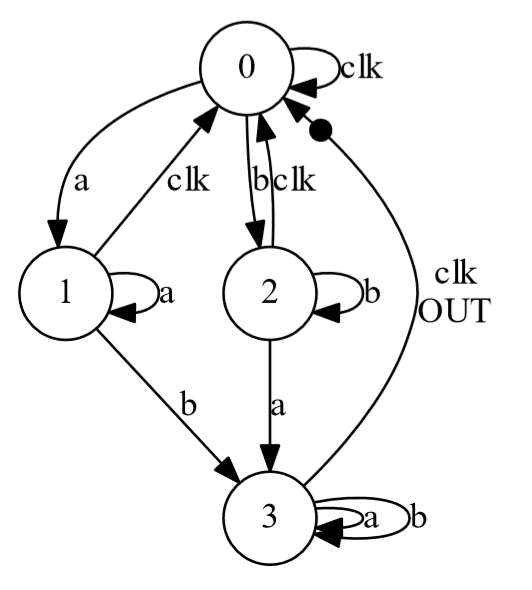


Figure 23. RSFQ AND2T Mealy finite state machine diagram extracted using TimEx.

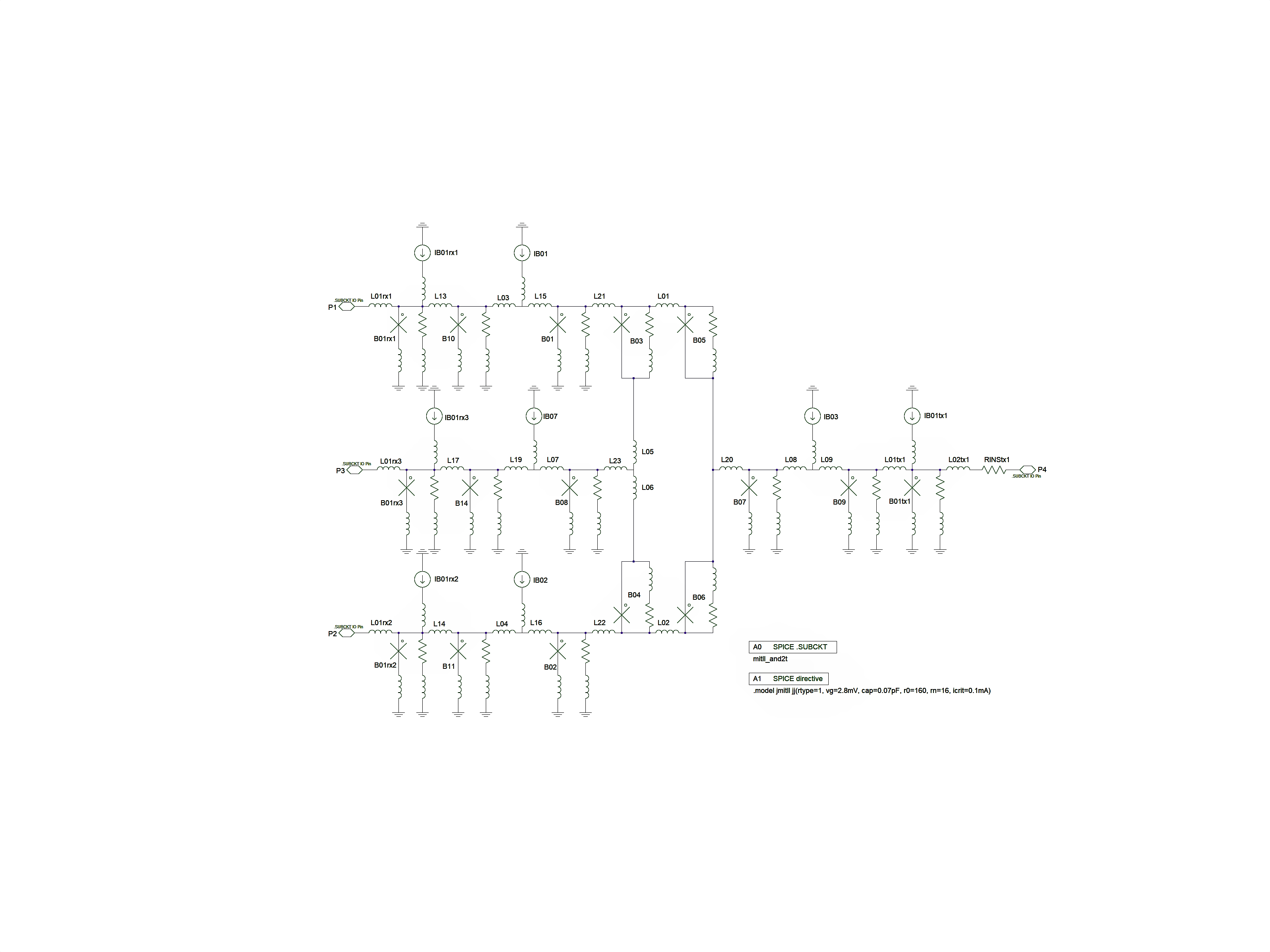


Figure 24. Schematic of the RSFQ AND2T cell.

Figure 25 shows the simulation of the AND2T cell at a lower operation frequency for illustration purposes. The figure shows the current, measured in µA, through a/b) the input inductors L01rx1 and L01rx2 respectively, c) the clock input inductor L01rx3, d) the output inductor L02tx1 and e) the sink resistor.

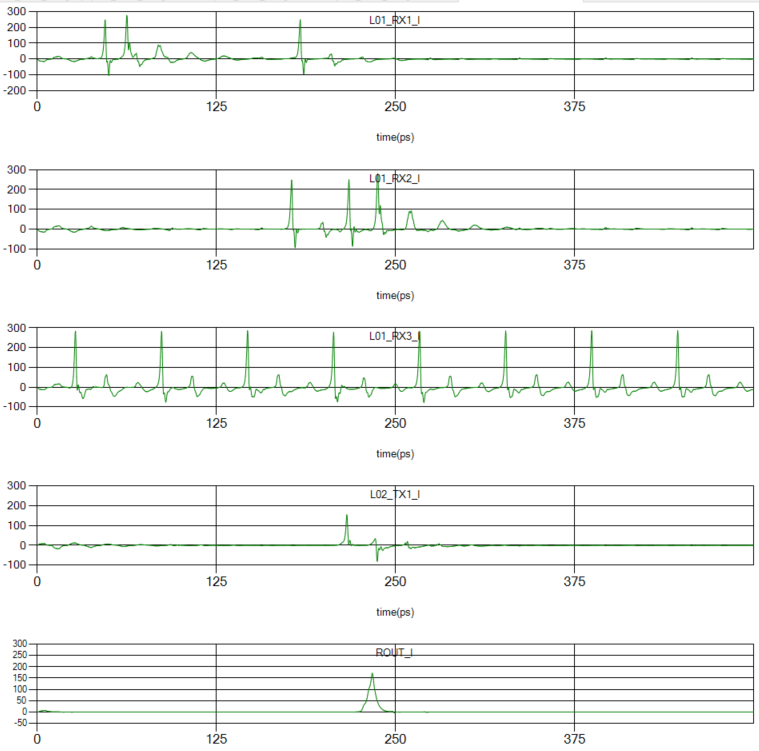


Figure 25. Simulation of the RSFQ AND2T cell showing the currents through a/b) the two input inductors, c) the clock input inductor, d) the output inductor and e) the sink resistor connected through a PTL with time delay 10 ps.

The margin analysis of the RSFQ AND2T cell is shown in Figure 26. The critical margin is determined by B03 with margins -38.0% and +42.2%.

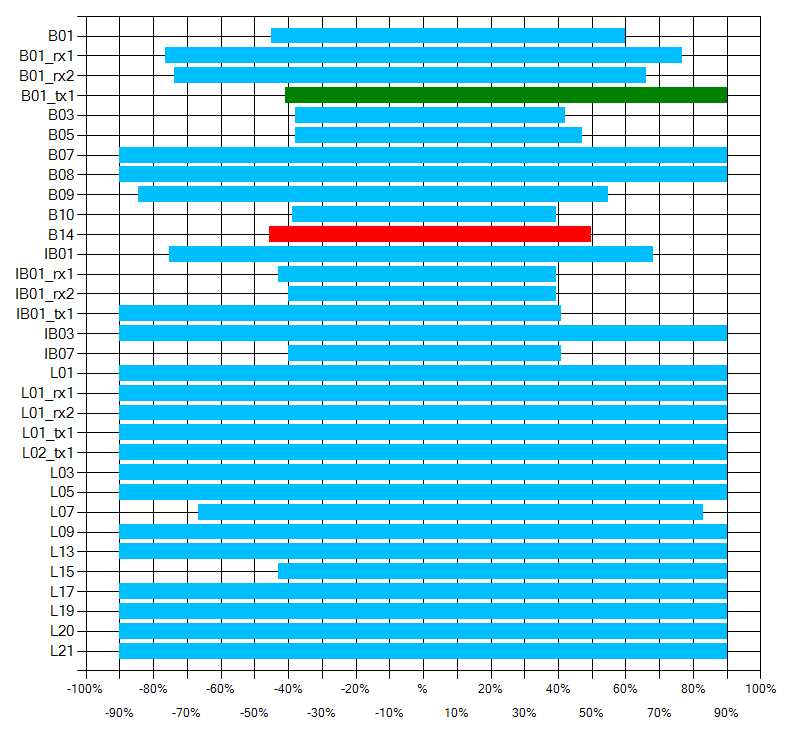


Figure 26. Margin analysis of the RSFQ AND2T cell.

## OR2T

The RSFQ OR2T cell generates an output pulse if an input pulse from either input lines was received before the clock signal. The functionality of the OR2T cell is shown in Figure 27 through a state diagram. The schematic of the designed OR2T cell is shown in Figure 28. P1 and P2 are the two input ports, P3 is the clock signal port and P4 is the output port. The cell is optimized using the natural symmetry of the two input sub-circuits.

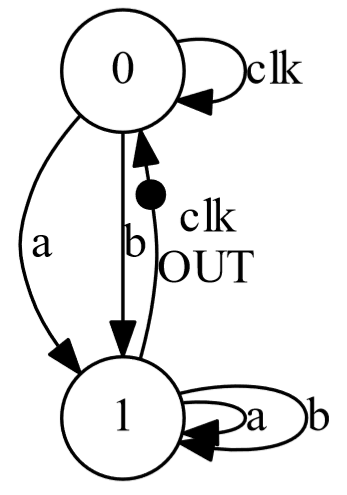


Figure 27. RSFQ OR2T Mealy finite state machine diagram extracted using TimEx.

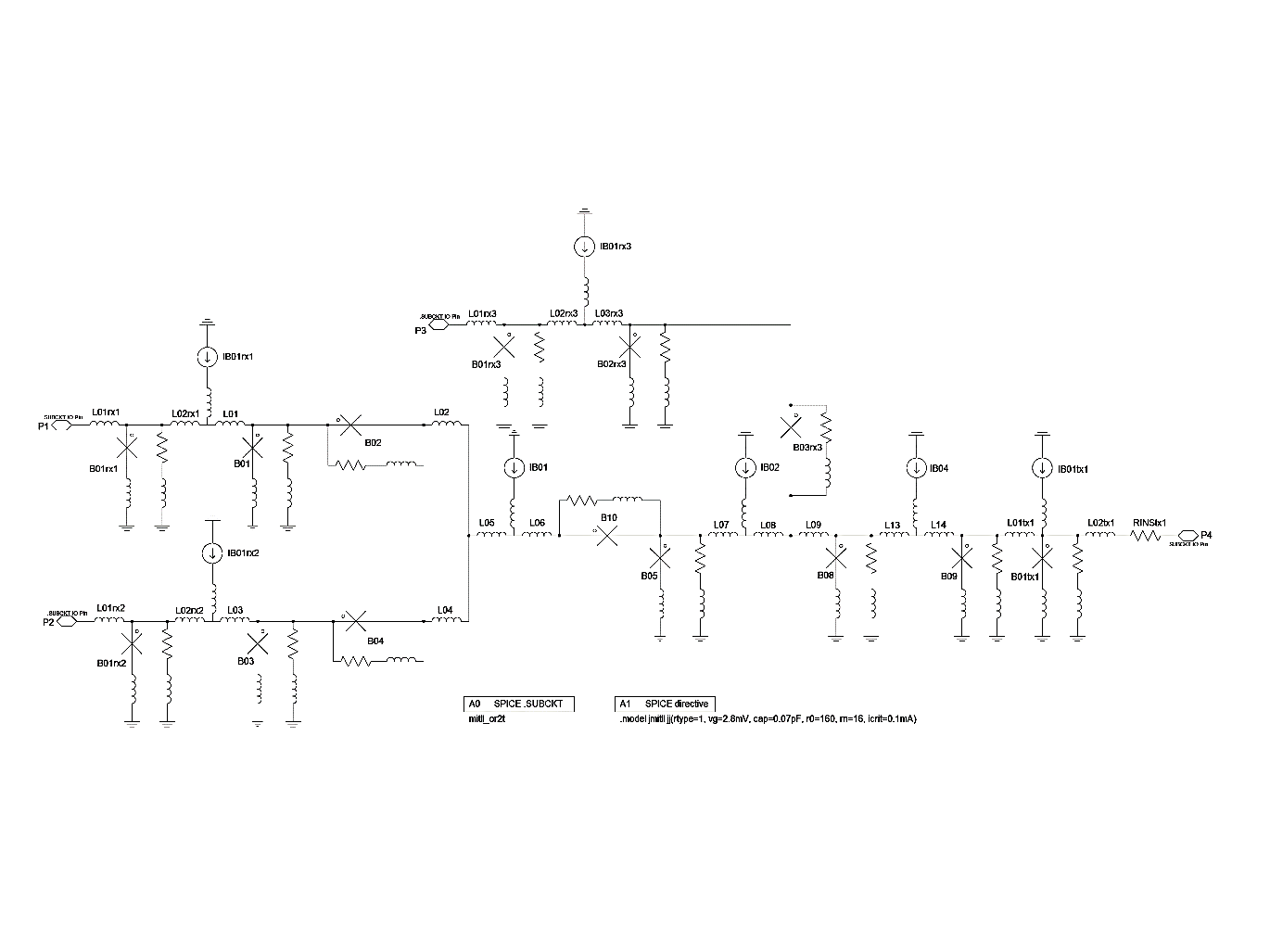


Figure 28. Schematic of the RSFQ OR2T cell.

Figure 29 shows the simulation of the OR2T cell operating at a lower clock frequency for illustration purposes. The figure shows the current, measured in µA, through a) the input inductor L01rx1, b) input inductor L01rx2, c) clock input inductor L01rx3, d) output inductor L02tx1 and e) the sink resistor.

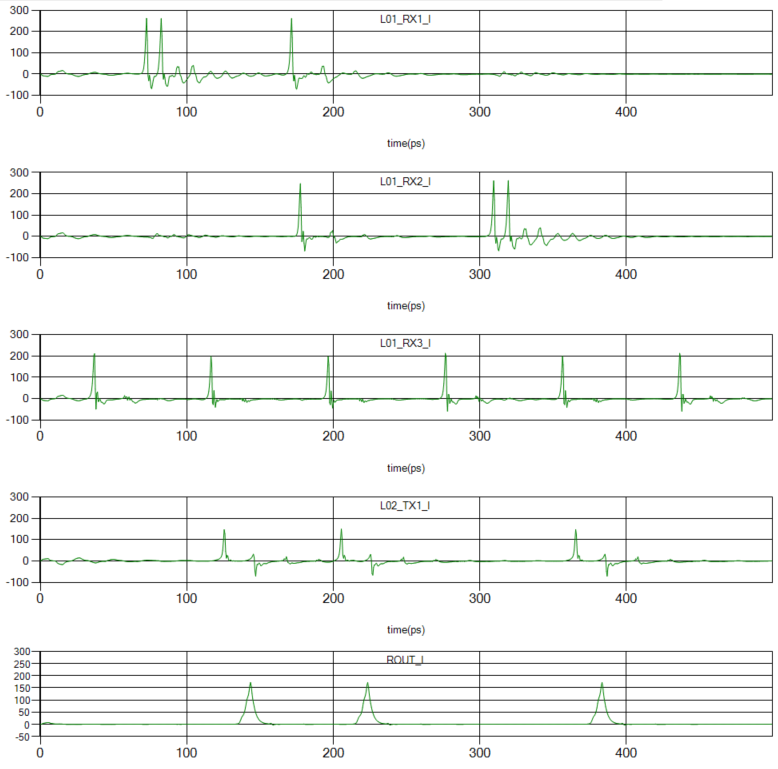


Figure 29. Simulation of the RSFQ OR2T cell showing the current through a/b) the two input inductors, c) the clock input inductor, d) the output inductor and e) the sink resistor connected through a PTL with time delay 10 ps.

The margin analysis for the OR2T cell is shown in Figure 30. The critical margins are determined by B01 with margins -20.4% and +28.1% and B10 with margins -20.4% and +25.3% respectively.

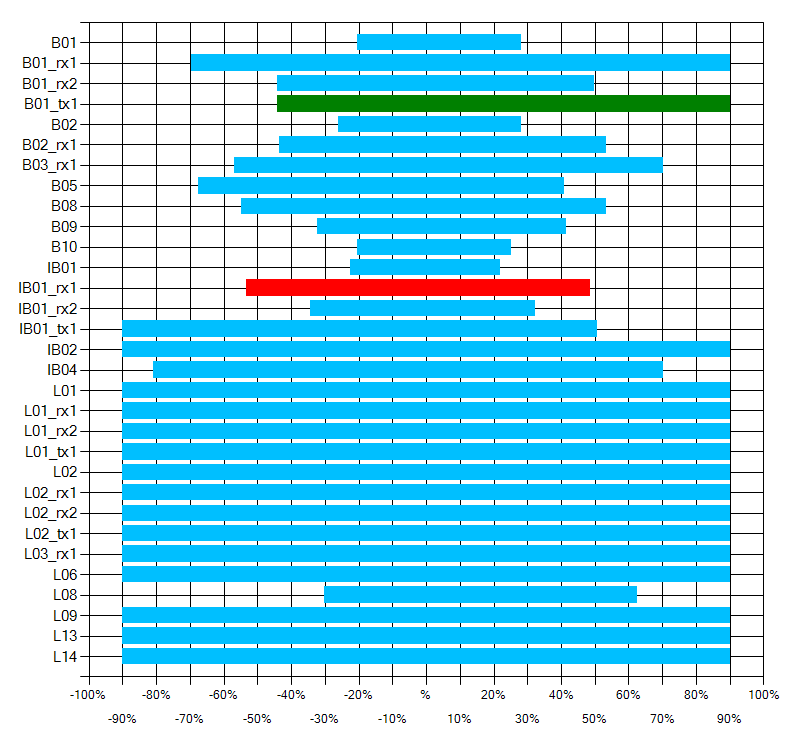


Figure 30. Margin analysis for the RSFQ OR2T cell.

## XORT

The RSFQ XORT cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. Figure 31 shows the functionality of the cell through a Mealy finite state machine diagram. The schematic of the designed XORT cell is shown in Figure 32. P1 and P2 are the two input signal ports, P3 is the clock signal input port and P4 is the output port. The cell is optimized using the symmetry of the two input sub-circuits.

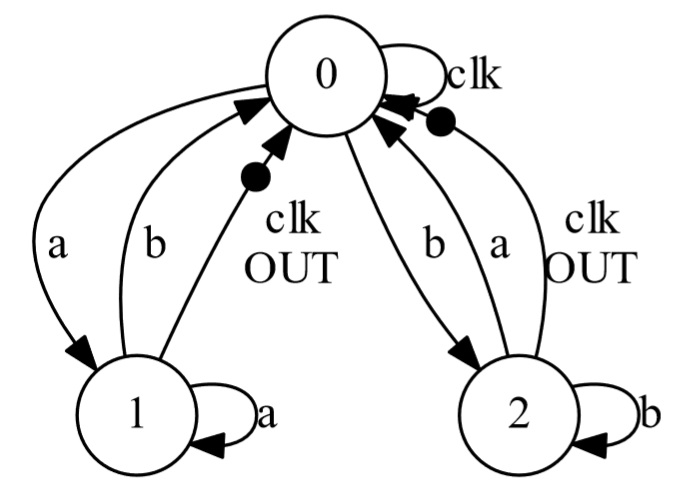


Figure 31. RSFQ XORT Mealy finite state machine diagram extracted using TimEx.

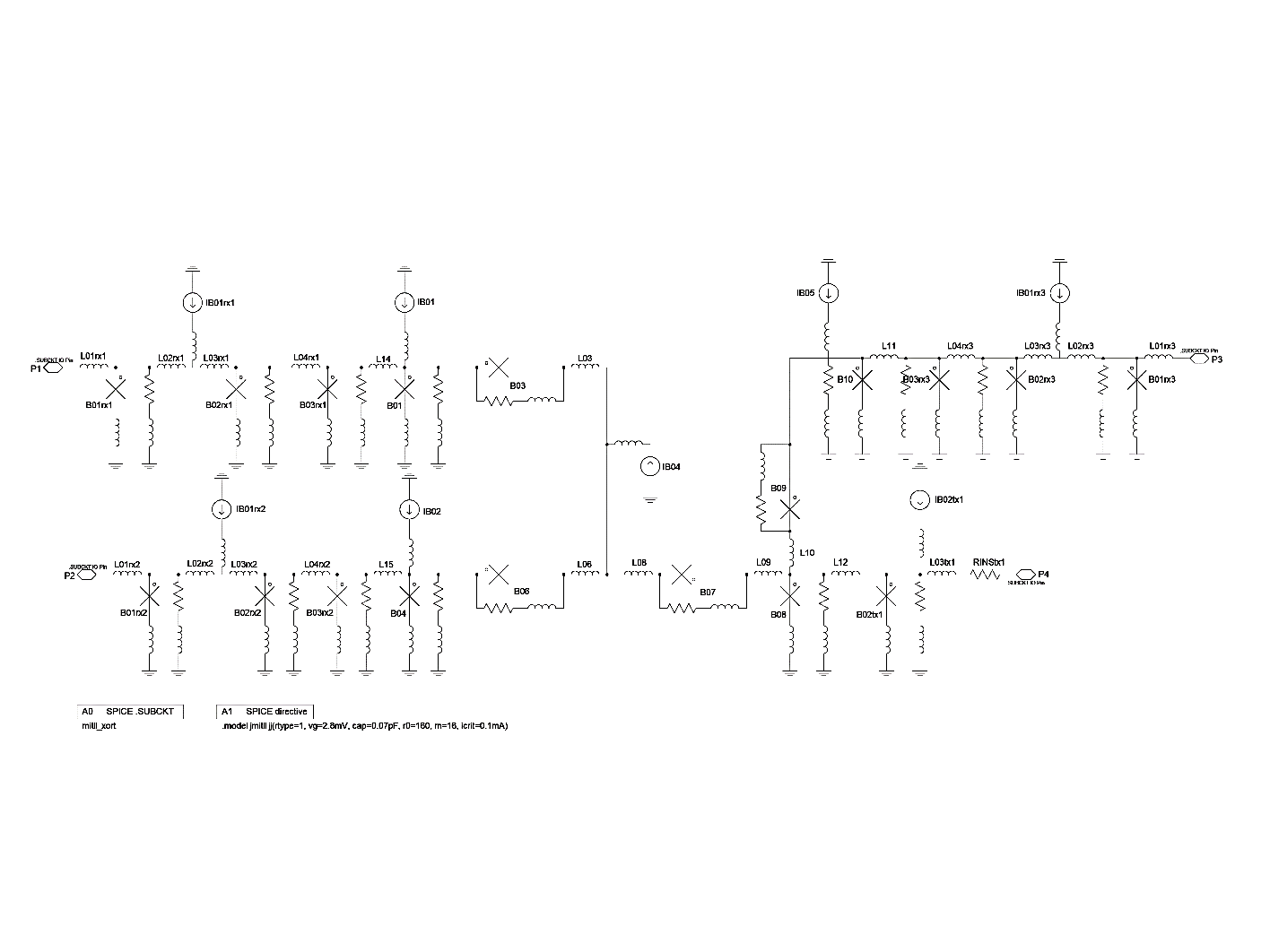


Figure 32. Schematic of the RSFQ XORT cell.

Figure 33 shows the simulation of the XORT cell at a low operation frequency for illustration purposes. The figure shows the currents, measured in µA, through a/b) the input inductors L01rx1 and L01rx2 respectively, c) the clock input inductor L01rx3, d) the output inductor L03tx1 and e) the sink resistor.

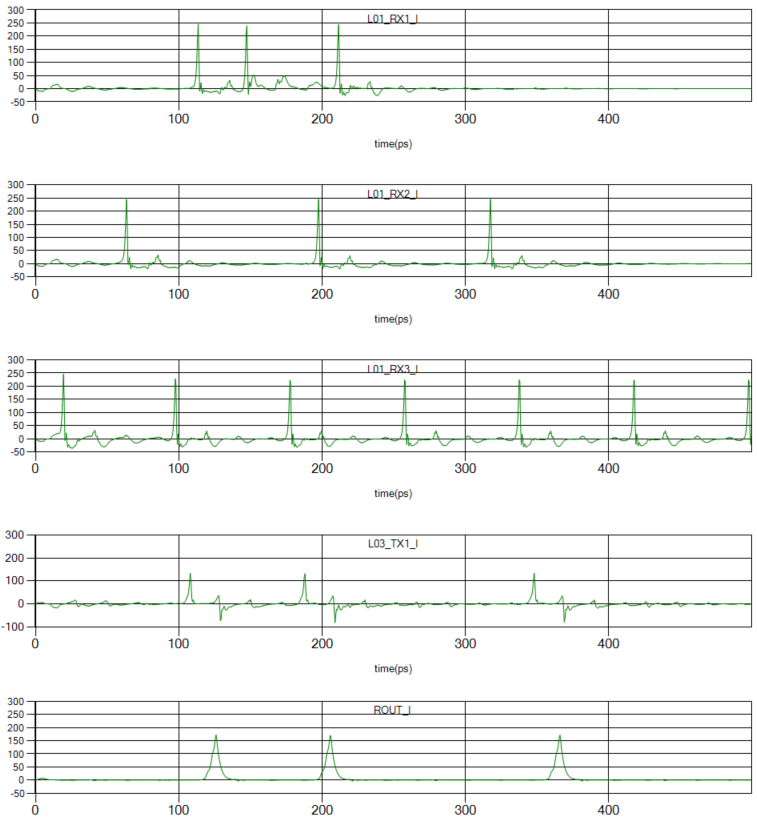


Figure 33. Simulation of the RSFQ XORT cell showing the currents through a/b) the input inductors, c) the clock input inductor, d) the output inductor and e) the sink resistor connected through a PTL with time delay 10 ps.

Figure 34 shows the margin analysis of the RSFQ XORT cell. The critical margins are determined by B03 with margins -25.3% and +26.7%.

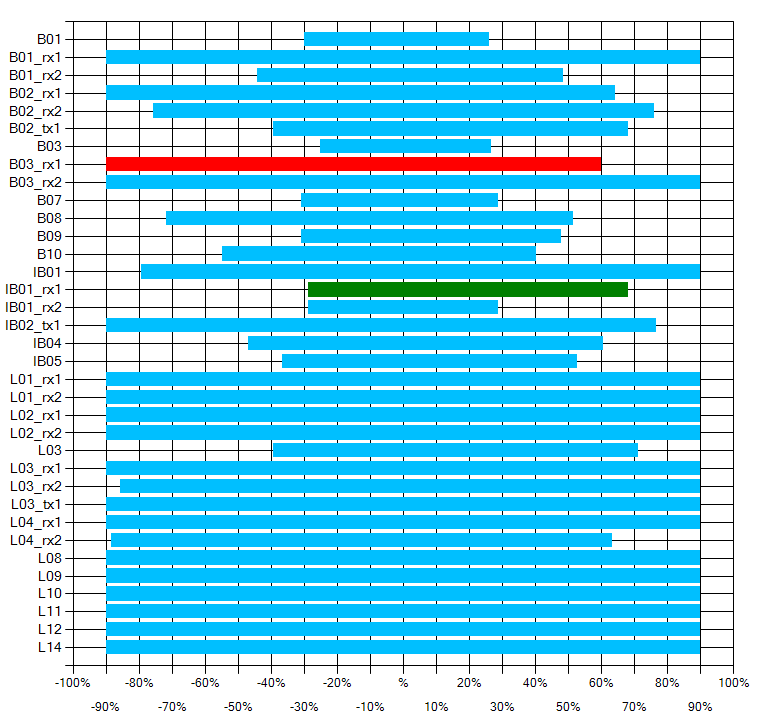


Figure 34. Margin analysis of the RSFQ XORT cell.

## NDROT

The non-destructive readout cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDROT will generate an output pulse after each clock signal until an input reset signal is received. The functionality of the NDROT is shown in Figure 35 through a state diagram. Figure 36 shows the schematic of the designed RSFQ NDROT cell. P1 is the set signal input port, P2 is the reset signal input port, P3 is the clock signal input port and P4 is the output port.

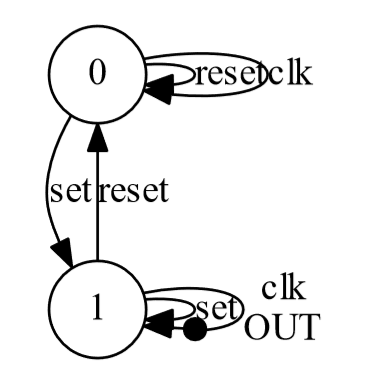


Figure 35. RSFQ NDROT Mealy finite state machine diagram extracted using TimEx.

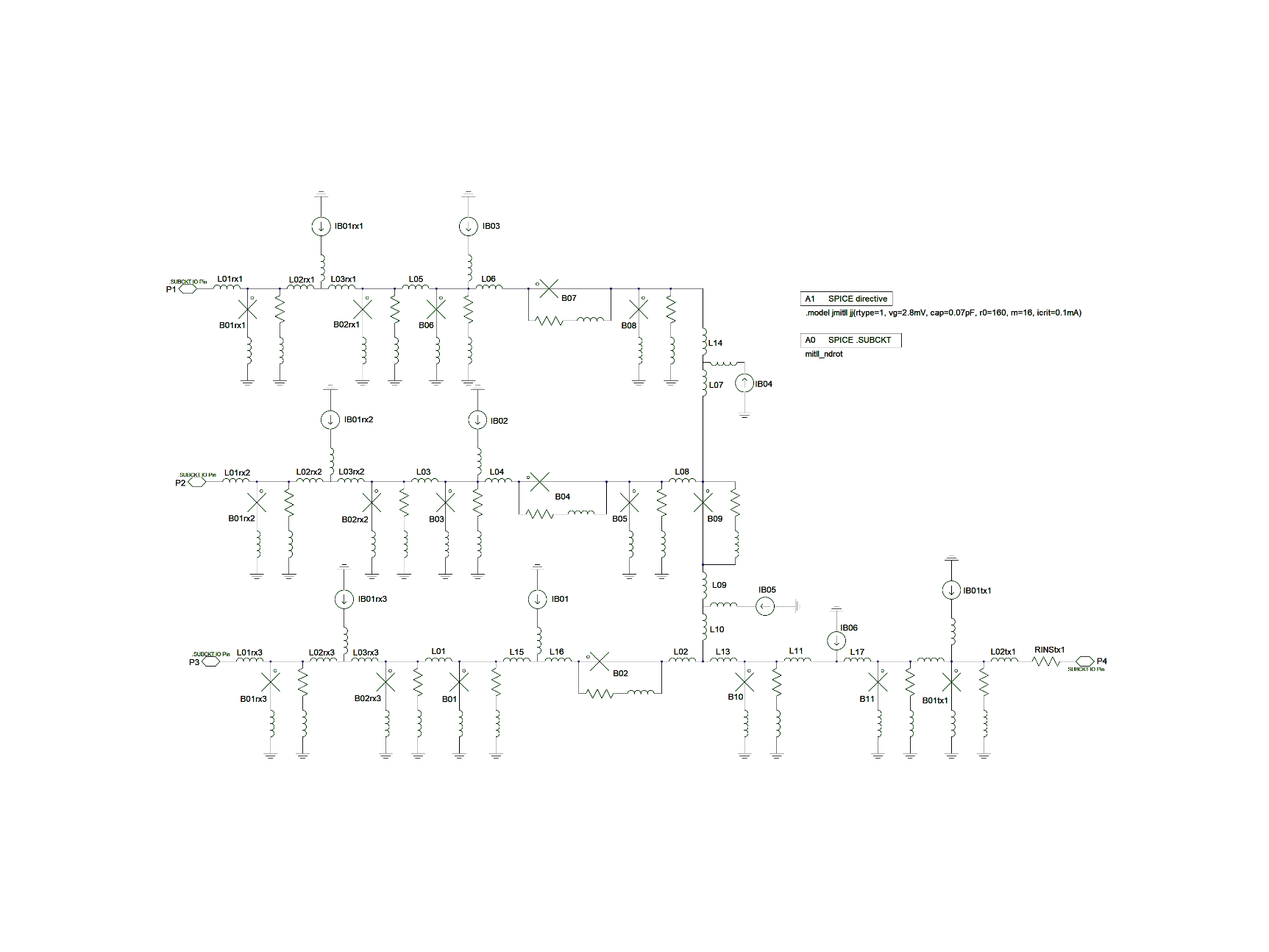


Figure 36. Schematic of the RSFQ NDROT cell.

Figure 37 shows the simulation of the RSFQ NDROT at a lower operation frequency for illustration purposes. The figure shows the currents, measured in µA, through a) the set input inductor L01rx1, b) the reset input inductor L01rx2, c) the clock input inductor L01rx3, d) the output inductor L02tx1 and e) the sink resistor.

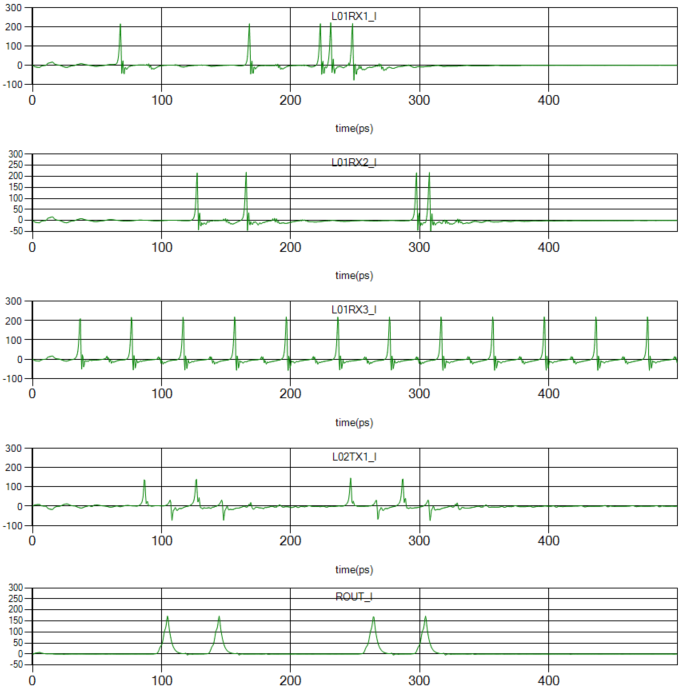


Figure 37. Simulation of RSFQ NDROT cell showing currents through a) the set input inductor, b) the reset input inductor, c) the clock input inductor, d) the output inductor and e) the sink resistor connected through a PTL with time delay 10 ps.

Figure 38 shows the margin analysis of the NDROT cell. The critical margins are determined by B02 with margins -19.7% and +18.3%.

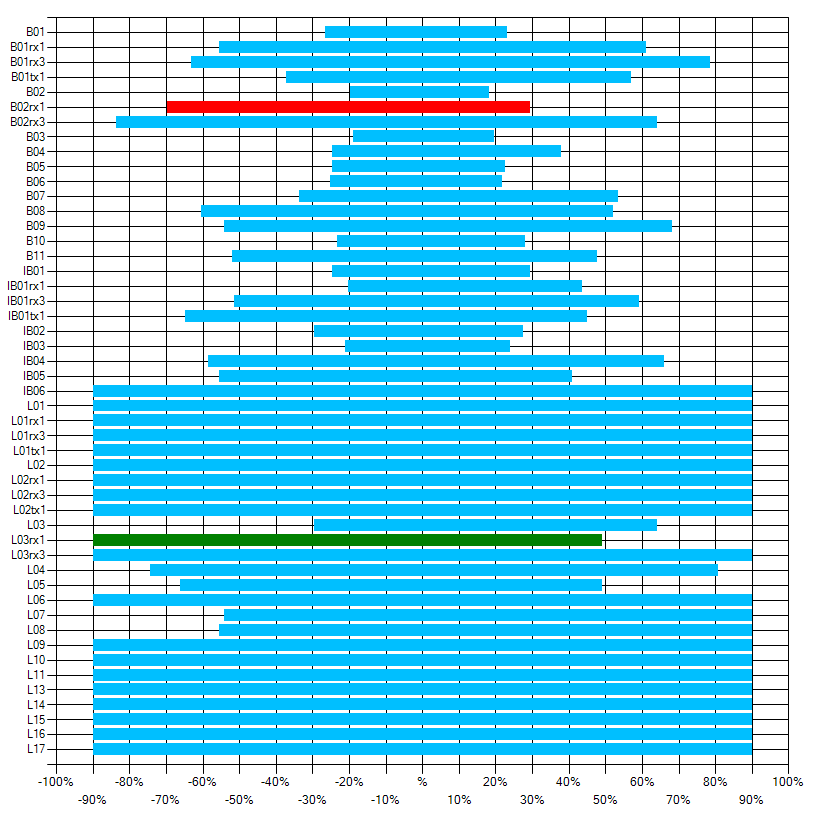


Figure 38. Margin analysis of the RSFQ NROT cell.

# Examples

It is important to test cells with different loads to ensure that the cell is load-independent. Examples are provided to run with TimEx to determine that each cell can drive all the other cells in the RSFQ library. The user can edit and run the provided batch files to test the cells with a load of their choice. This can be done by changing the load definition called within the batch file.

The batch file for the NOTT cell is as follows:

@ECHO OFF

REM run example sequence for TimEx

REM Author: Coenrad Fourie

REM Last mod: 4 May 2018 by Lieze Schindler

REM You need in the path: jsim\_n, iverilog and vvp

@ECHO ON

TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_ptl.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_jtlt.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_dfft.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_splitt.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_merget.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_nott.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_and2t.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_or2t.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_xort.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_ndroset.txt -x

::TimEx .\mitll\_nott\mitll\_nott.js -d .\Definitions\definitions\_ndroreset.txt -x

pause

The comments (denoted through the “::” operator) can be removed to adjust which cell is defined as the load. The output from TimEx when running the above batch file is shown on the next page. The Mealy finite state machine diagram as well as the extracted Verilog file is also generated by *TimEx* and can be found in the Examples folder after execution.

TimEx v2.02.01 (3 Apr 2018). Copyright 2016-2018 Coenrad Fourie, Stellenbosch University.

Definition file read.

Deck for Device-Under-Test read.

Finding all cycles.

Cycles:

[lp06,-b06,l10,l21,b09,-lp09]

[lp06,-b06,l10,l21,l01utx1,b01utx1,-lp01utx1]

[lp06,-b06,-l09,l07,-b02,-b03,-l08,l18,b10,-lp10]

[lp06,-b06,-l09,l07,-b02,-b03,-l08,-l12,-l20,b11,-lp11]

… (*omitted to save space*)

[lp01utx1,-b01utx1,-l01utx1,-l21,-l10,-l09,l07,-b02,-l04,-l03,b05,-lp05]

[lp01utx1,-b01utx1,-l01utx1,-l21,-l10,-l09,b01,-l01,b05,-lp05]

.\mitll\_nott\mitll\_nott.js: Finding all states.

State 0: Input "clk" -> Output "out" after 1.375E-11 s.

States found: 2

.....State 0: No critical timing found in->in. (5 iterations.)

..........State 0: No critical timing found in->clk. (10 iterations.)

...x.xxxx.State 0: Critical timing found clk->in: 7.422E-12 s.

..xxx..x.xState 0: Critical timing found (pulse repulsion) clk->clk: 1.797E-11 s. (Pulse delay at out exceeded MaxDelayChange.)

.....State 1: No critical timing found in->in. (5 iterations.)

..x...x.x.State 1: Critical timing found in->clk: 1.086E-11 s.

..........State 1: No critical timing found clk->in. (10 iterations.)

.....State 1: No critical timing found clk->clk. (5 iterations.)

Writing Verilog and testbench files.

Executing testbench simulations.

The cell library was also used to build a full 2-bit adder. Figure 39 shows the simulation of the adder operating at 20 GHz. The circuit throughput is 3 clock cycles.

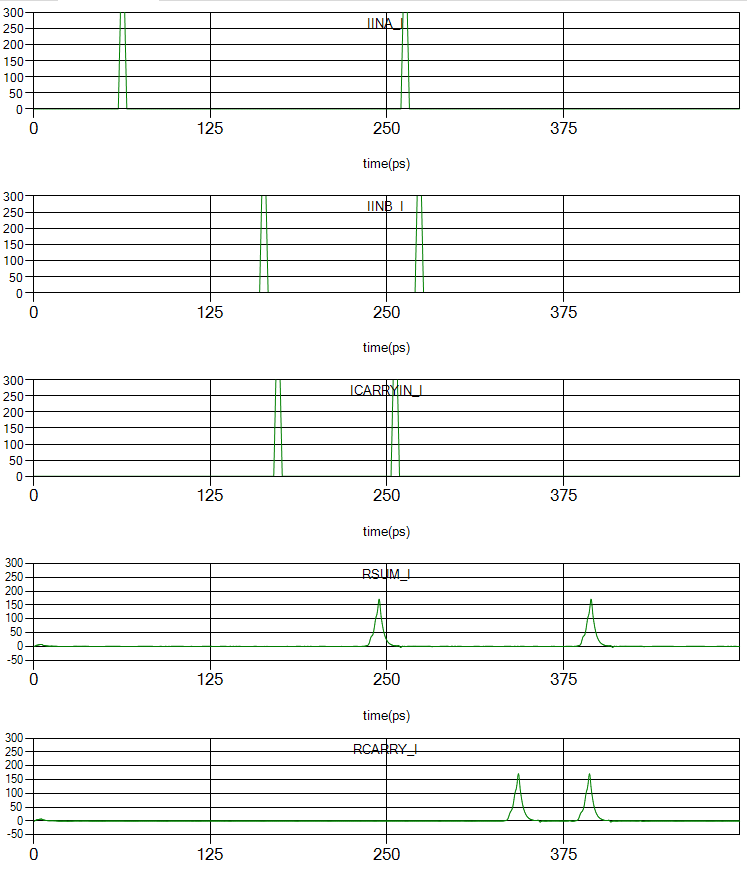


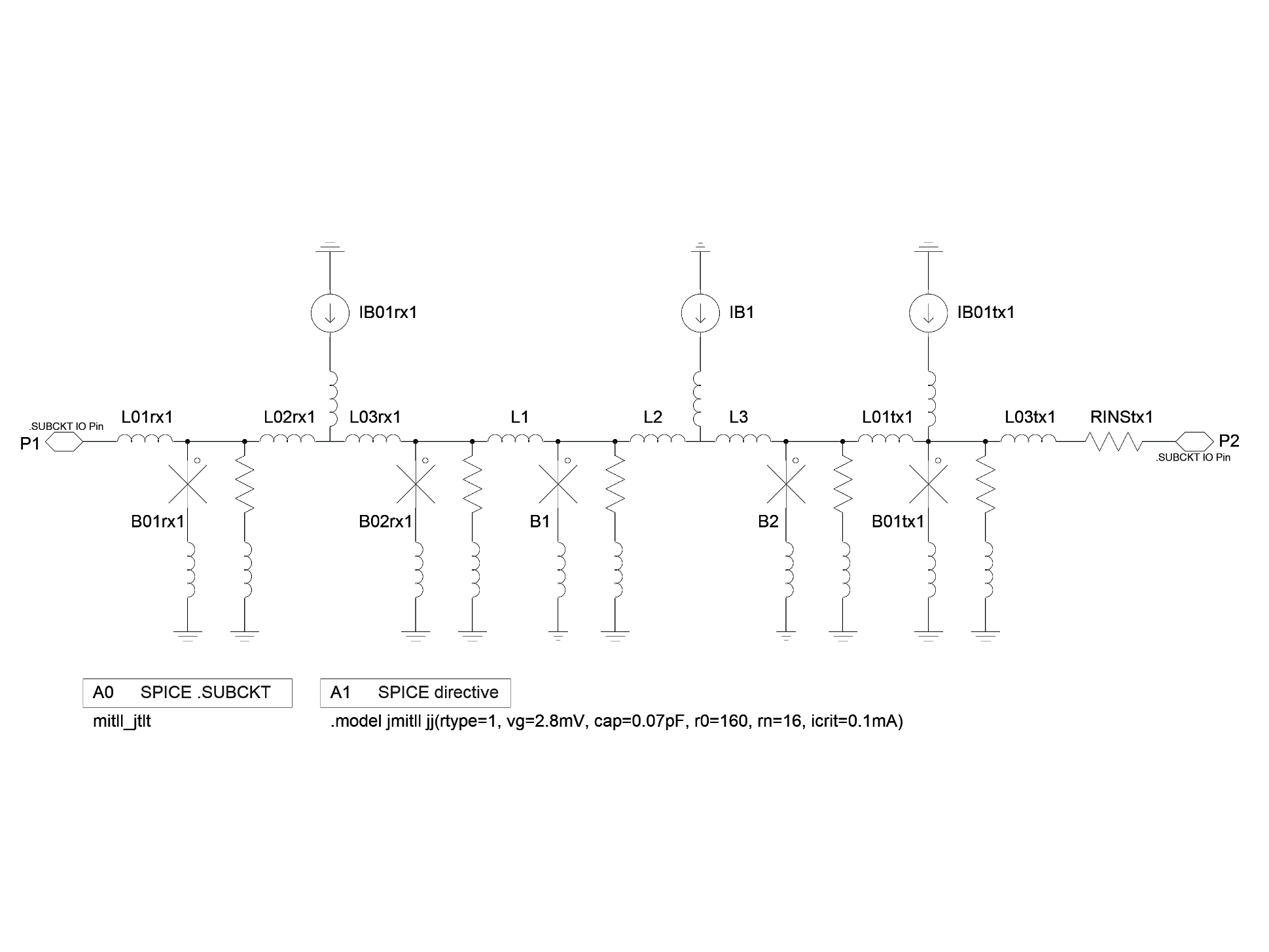
Figure 39. 2-bit full adder example

# References

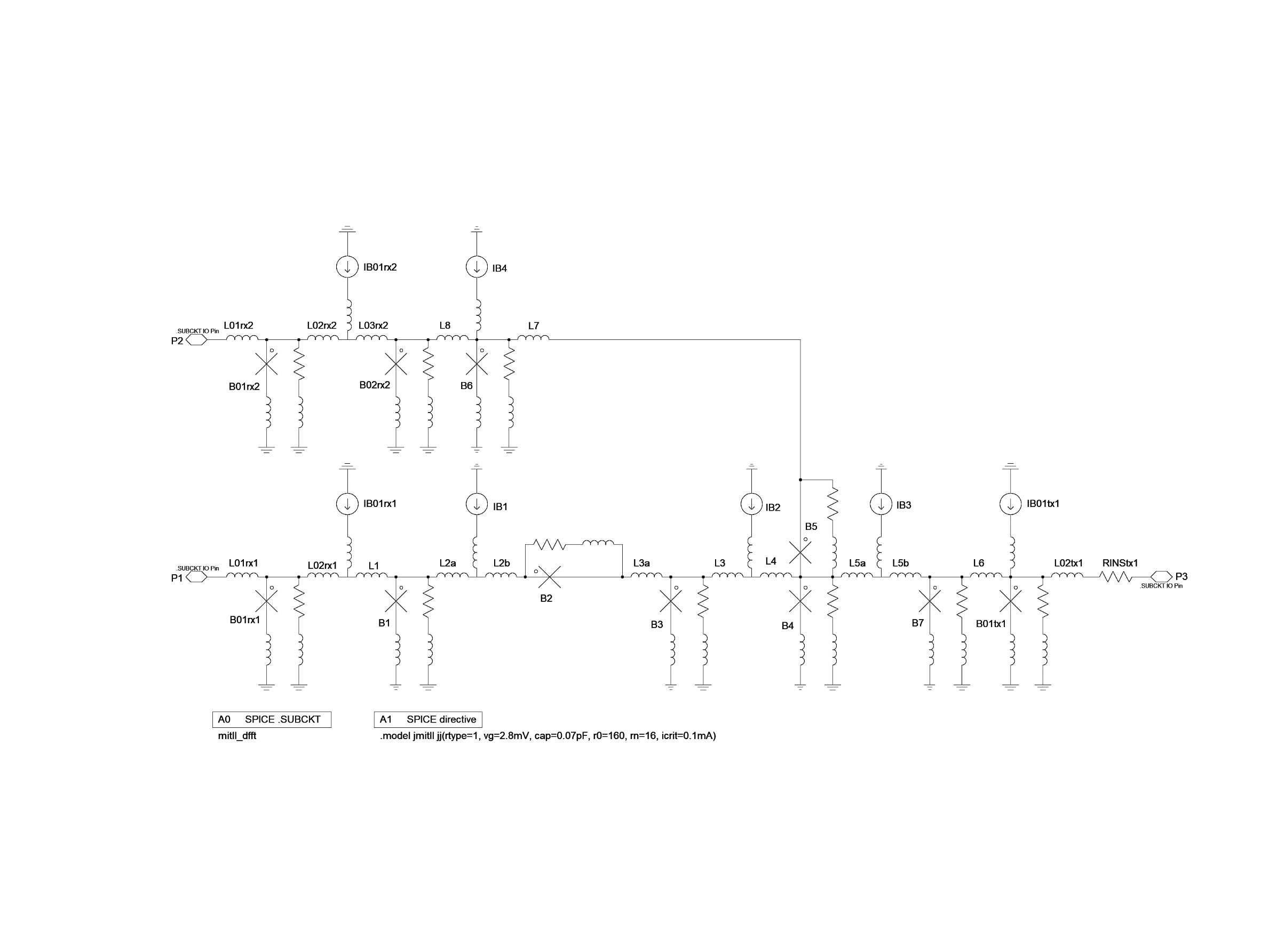
|  |  |
| --- | --- |
| [1] | C. Fourie, TimEx, 2018. [Online]. Available: https://github.com/sunmagnetics/TimEx. |
| [2] | C. Fourie, "Extraction of DC-biased SFQ circuit Verilog models," *IEEE Transactions on Applied Superconductivity,* 2018. |
| [3] | Stephen R. Whiteley, "WRspice Reference Manual," Whiteley Research Incorporated, 22 April 2018. [Online]. Available: http://wrcad.com/manual/wrsmanual/node138.html. [Accessed 27 April 2018]. |

# Appendix A – Enlarged RSFQ circuit schematics

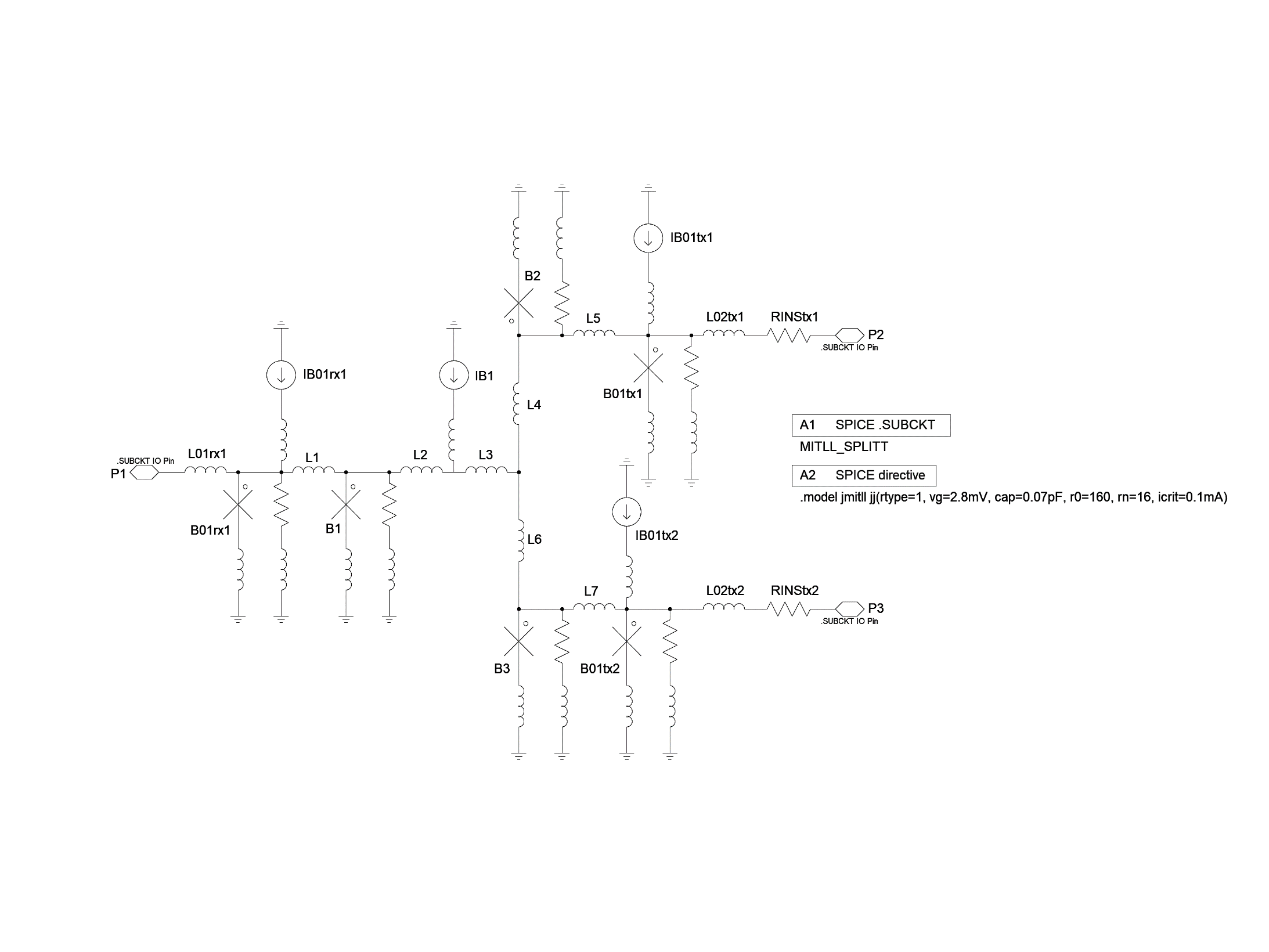
## JTLT



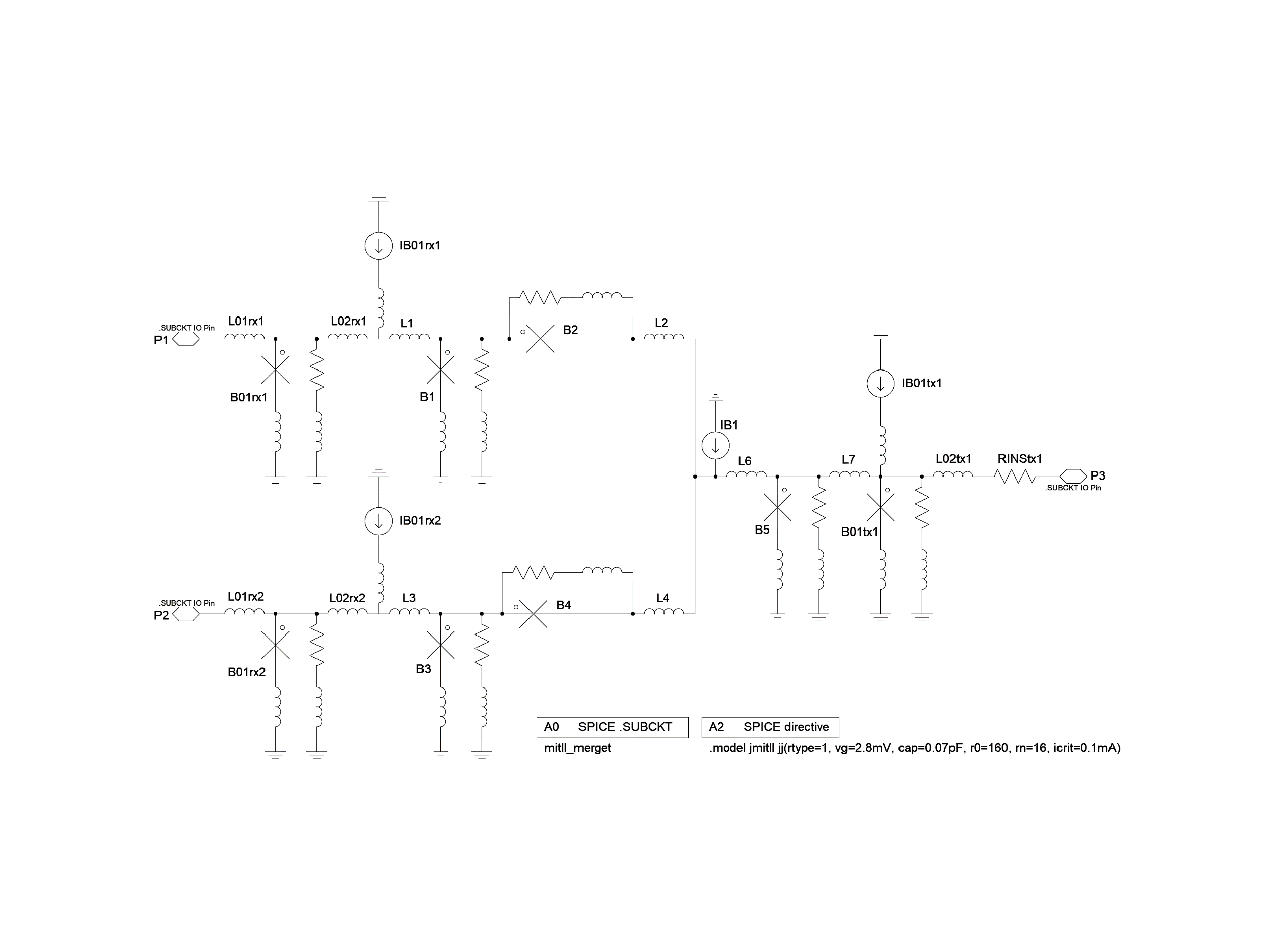
## DFFT



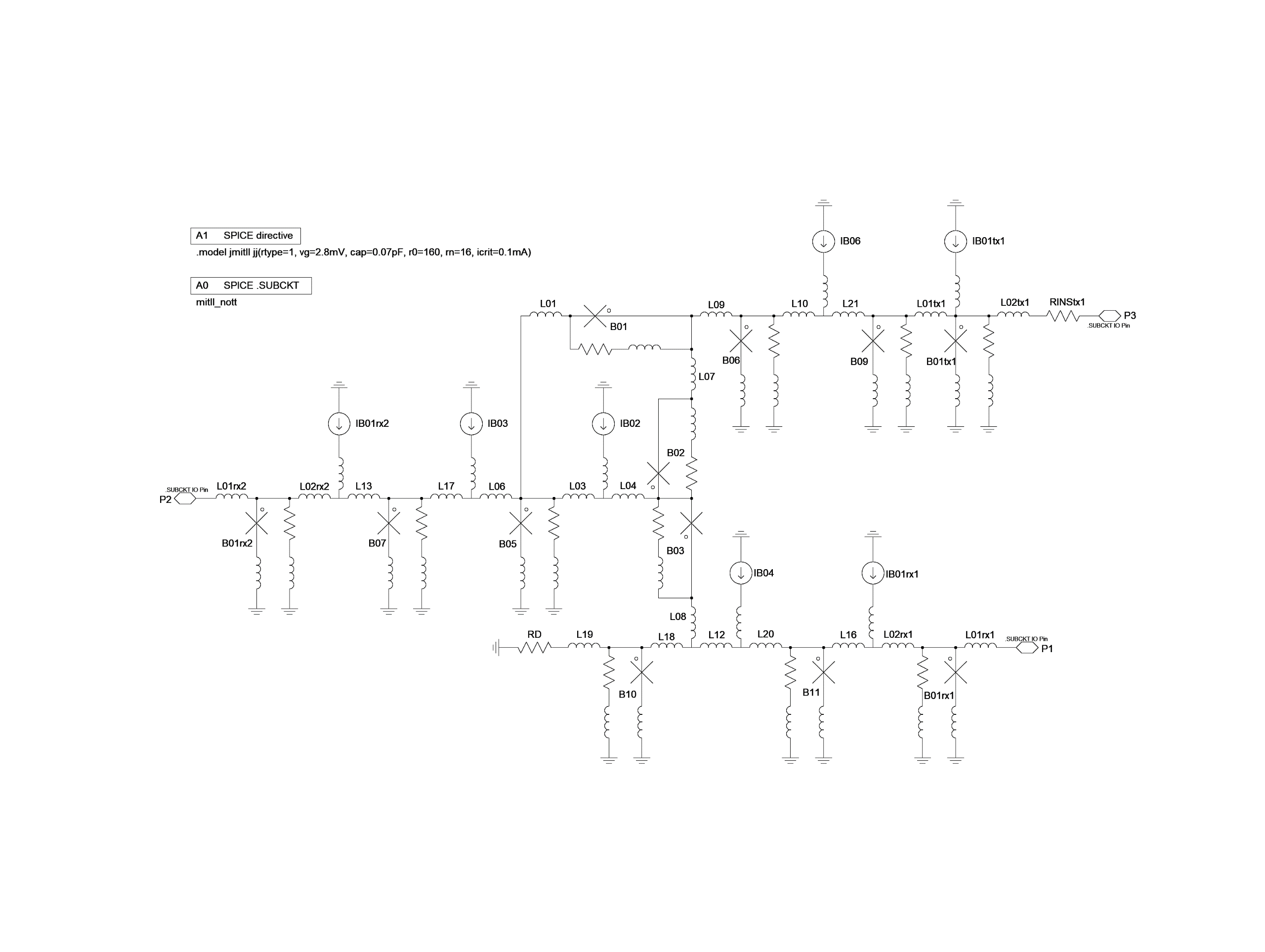
## SPLITT



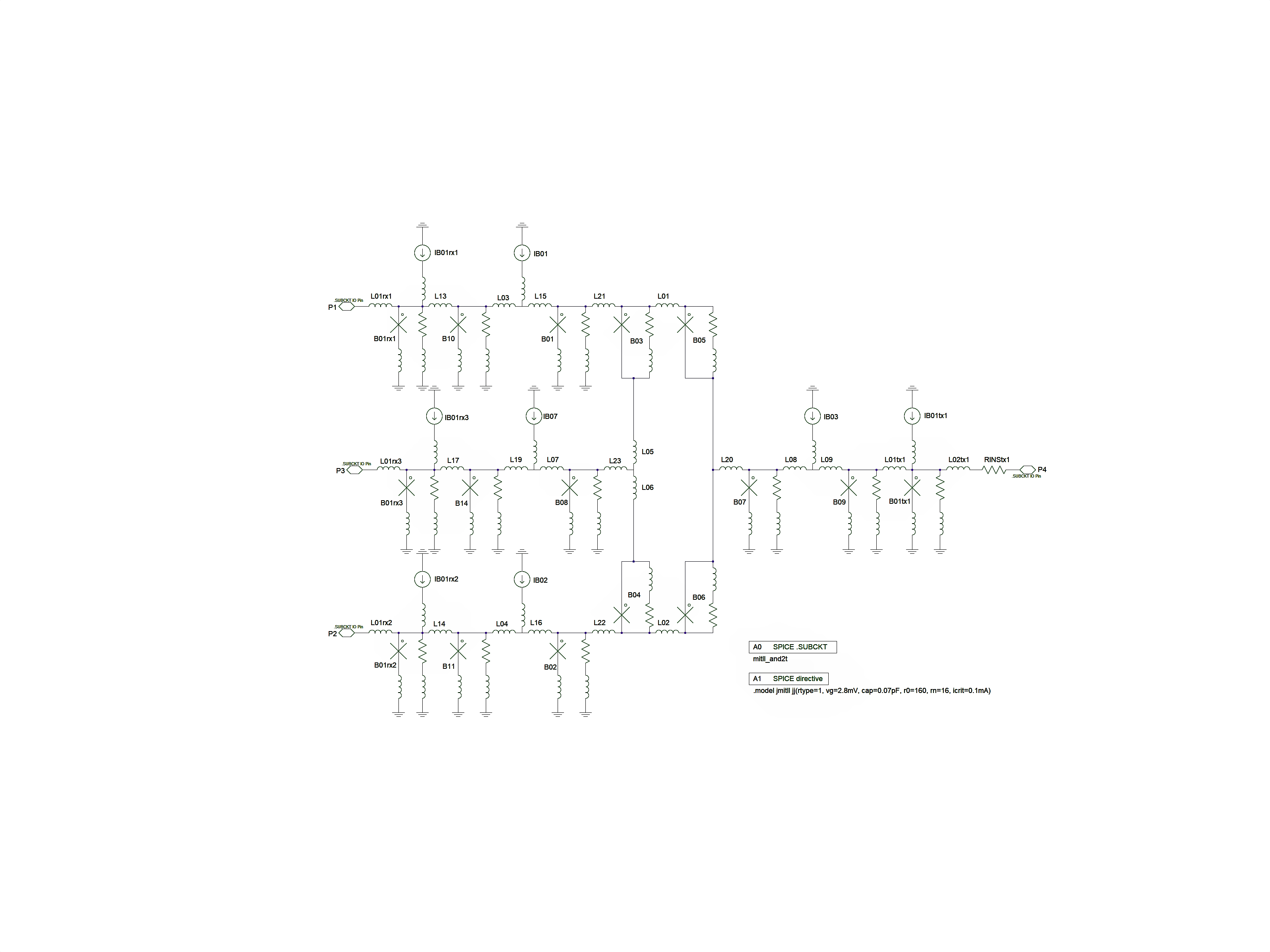
## MERGET



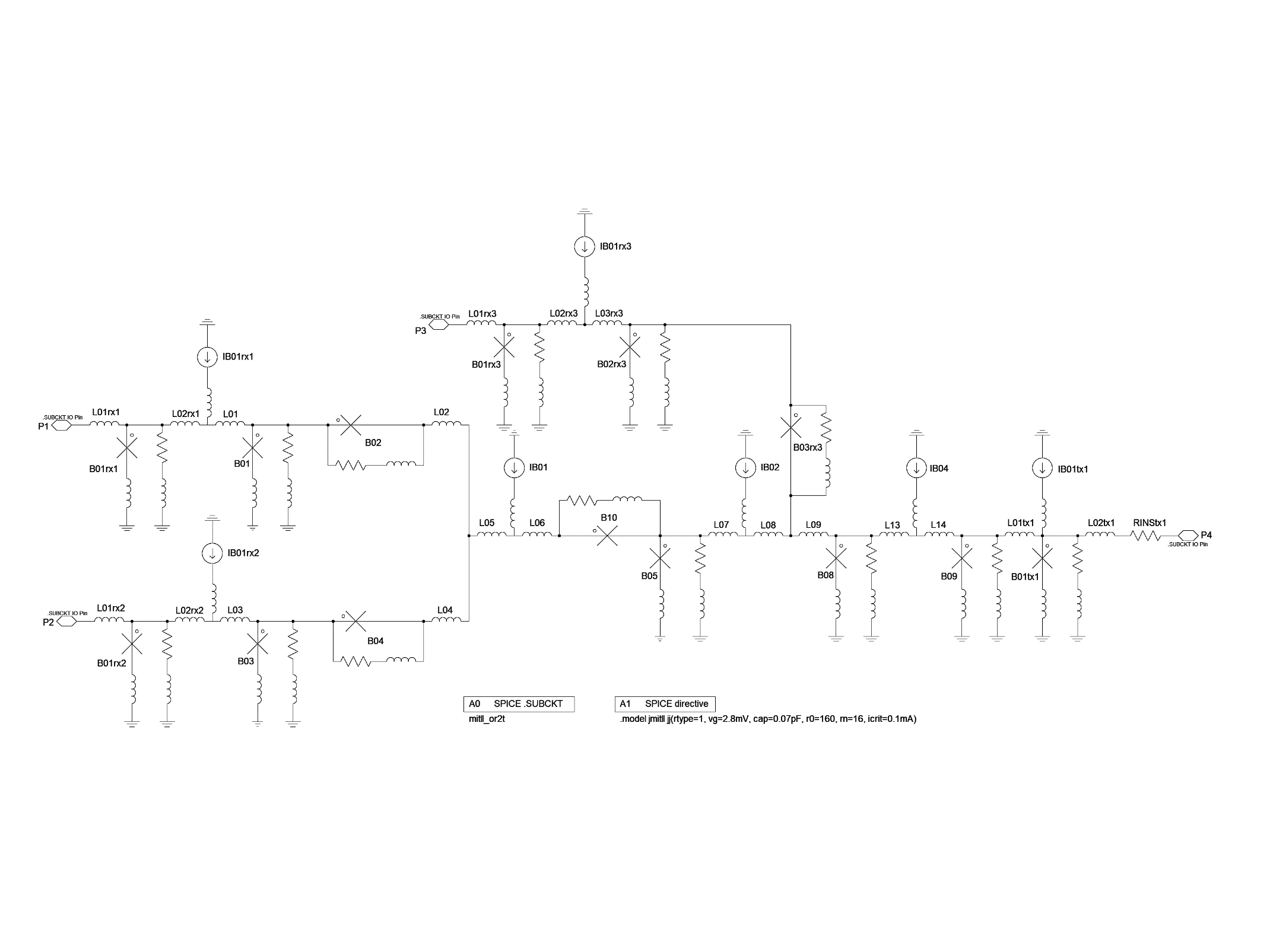
## NOTT



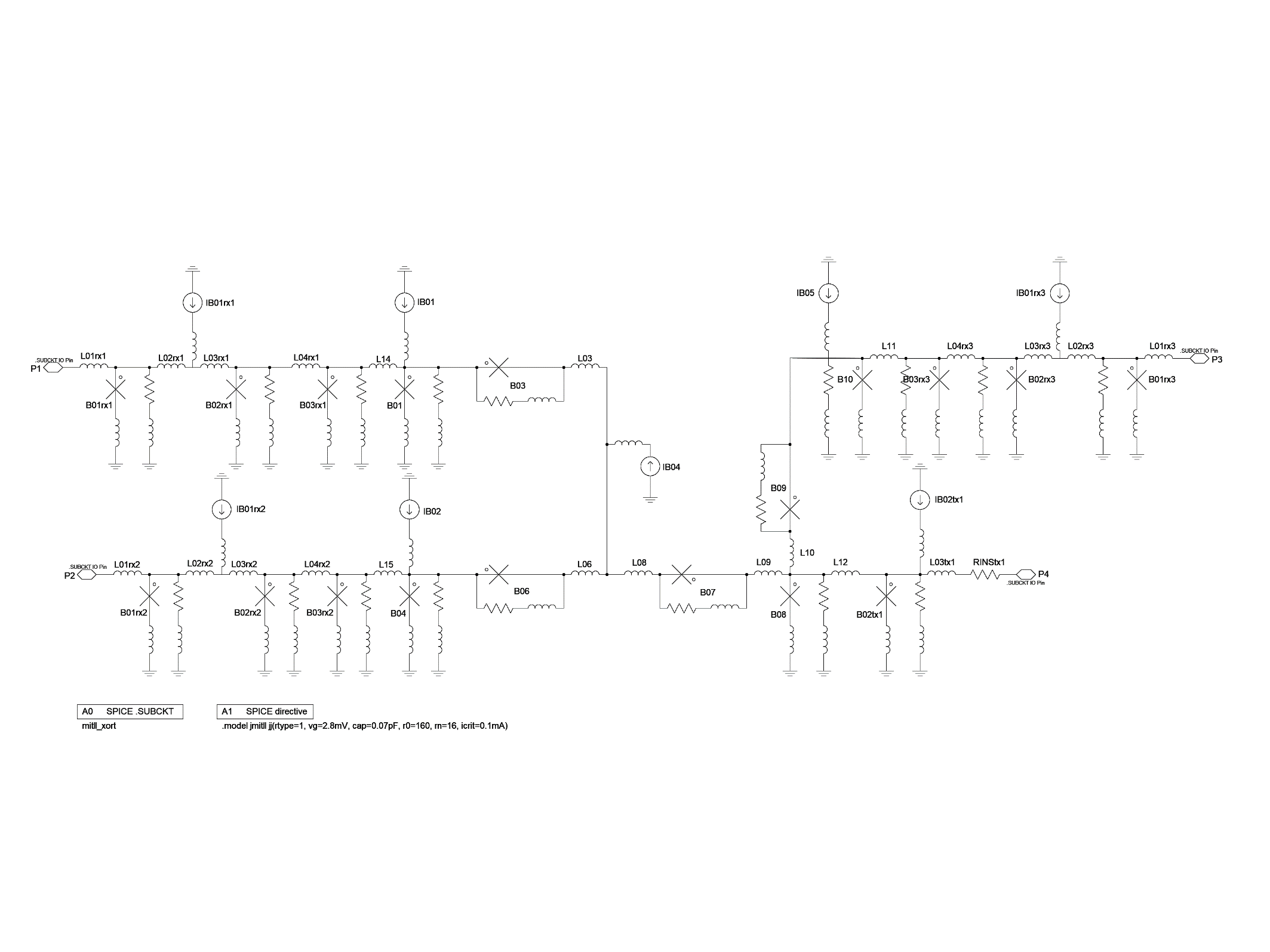
## AND2T



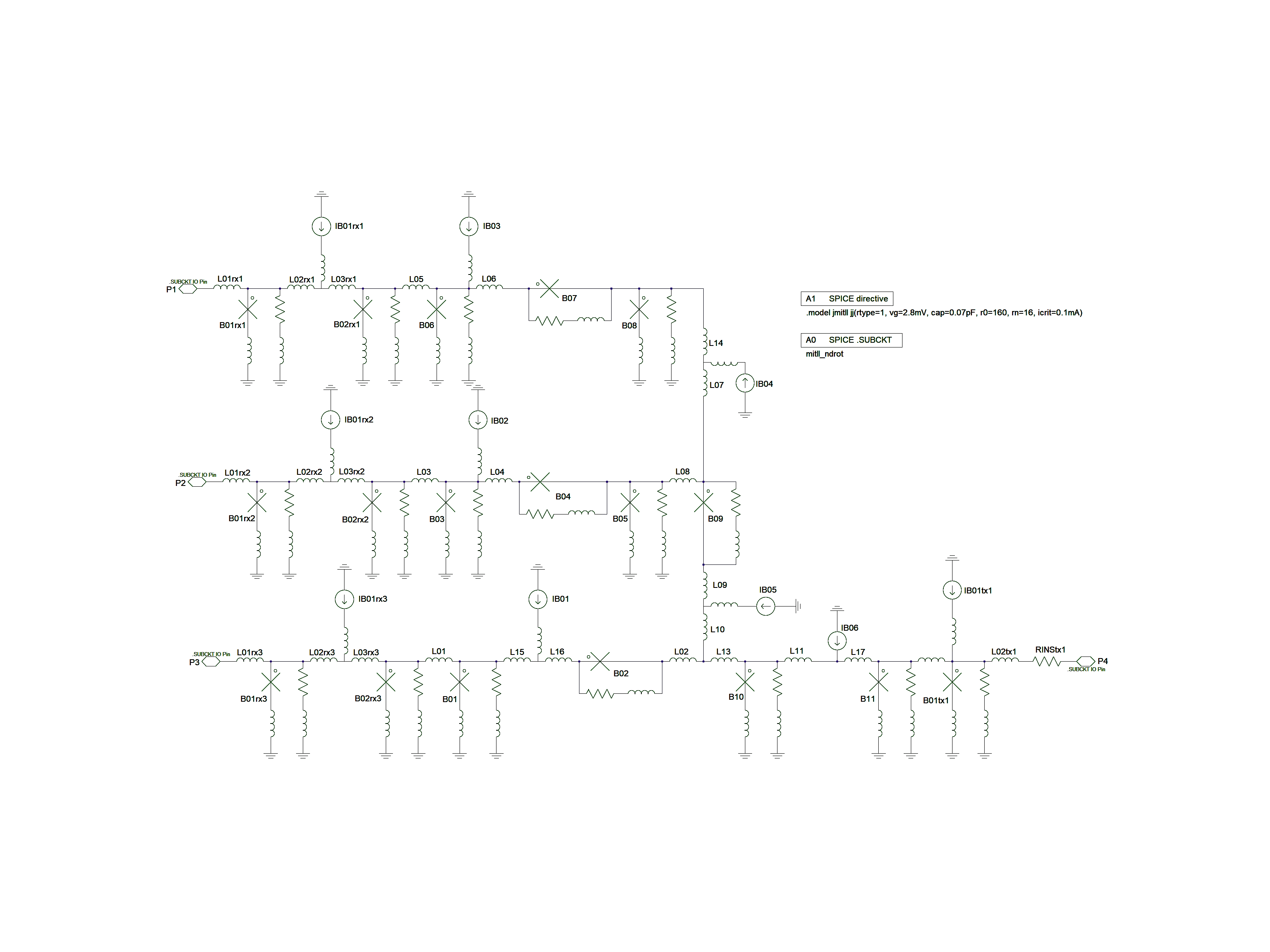
## OR2T



## XORT



## NDROT



# Appendix B – Parameter values for RSFQ cell library

## JTLT

|  |  |
| --- | --- |
| B01rx1 | 0.697897\*Scaling |
| B02rx1 | 0.443156\*Scaling |
| B1 | 0.488052\*Scaling |
| B2 | 0.488052\*Scaling |
| B01tx1 | 1.785104\*Scaling |
| IB01rx1 | 8.645055e-05\*Scaling |
| IB1 | 1.200813e-04\*Scaling |
| IB01tx1 | 5.531224e-05\*Scaling |
| L01rx1 | 3.325159e-13\*(1/Scaling-(1-Scaling)) |
| L02rx1 | 2.403215e-12\*(1/Scaling-(1-Scaling)) |
| L03rx1 | 1.677246e-12\*(1/Scaling-(1-Scaling)) |
| L1 | 2.510910e-12\*(1/Scaling-(1-Scaling)) |
| L2 | 8.665208e-13\*(1/Scaling-(1-Scaling)) |
| L3 | 8.665208e-13\*(1/Scaling-(1-Scaling)) |
| L01tx1 | 2.325626e-12\*(1/Scaling-(1-Scaling)) |
| L03tx1 | 2.363020e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## DFFT

|  |  |
| --- | --- |
| B01rx1 | 0.793833\*Scaling |
| B01rx2 | 0.906104\*Scaling |
| B01tx1 | 3.027087\*Scaling |
| B02rx1 | 0.963766\*Scaling |
| B1 | 1.427775\*Scaling |
| B2 | 1.4987455\*Scaling |
| B3 | 0.960227\*Scaling |
| B4 | 1.695202\*Scaling |
| B5 | 1.173452\*Scaling |
| B6 | 1.364045\*Scaling |
| B7 | 1.499966\*Scaling |
| IB01rx1 | 1.154563e-04\*Scaling |
| IB01rx2 | 1.018892e-04\*Scaling |
| IB01tx1 | 1.814029e-04\*Scaling |
| IB1 | 1.2040155e-04\*Scaling |
| IB2 | 6.347858e-05\*Scaling |
| IB3 | 1.536335e-04\*Scaling |
| IB4 | 1.617296e-04\*Scaling |
| L01rx1 | 1.406653e-12\*(1/Scaling-(1-Scaling)) |
| L01rx2 | 1.231017e-12\*(1/Scaling-(1-Scaling)) |
| L02rx1 | 3.294666e-12\*(1/Scaling-(1-Scaling)) |
| L02rx2 | 2.4403565e-12\*(1/Scaling-(1-Scaling)) |
| L02tx1 | 1.804009e-12\*(1/Scaling-(1-Scaling)) |
| L03rx2 | 3.649437e-12\*(1/Scaling-(1-Scaling)) |
| L1 | 1.128451e-12\*(1/Scaling-(1-Scaling)) |
| L2a | 5.402830e-13\*(1/Scaling-(1-Scaling)) |
| L2b | 1.602892e-12\*(1/Scaling-(1-Scaling)) |
| L3 | 9.453744e-13\*(1/Scaling-(1-Scaling)) |
| L3a | 1.114143e-12\*(1/Scaling-(1-Scaling)) |
| L4 | 4.4400865e-12\*(1/Scaling-(1-Scaling)) |
| L5a | 3.634939e-12\*(1/Scaling-(1-Scaling)) |
| L5b | 5.939354e-13\*(1/Scaling-(1-Scaling)) |
| L6 | 1.323271e-12\*(1/Scaling-(1-Scaling)) |
| L7 | 1.907903e-12\*(1/Scaling-(1-Scaling)) |
| L8 | 1.797636e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## SPLITT

|  |  |
| --- | --- |
| B01rx1 | 1.0070355\*Scaling |
| B01tx1 | 1.699324\*Scaling |
| B01tx2 | 1.699324\*Scaling |
| B1 | 1.695968\*Scaling |
| B2 | 1.209510\*Scaling |
| B3 | 1.209510\*Scaling |
| IB01rx1 | 1.349476e-04\*Scaling |
| IB01tx1 | 7.626697e-05\*Scaling |
| IB01tx2 | 7.626697e-05\*Scaling |
| IB1 | 3.596832e-04\*Scaling |
| L01rx1 | 2.675704e-13\*(1/Scaling-(1-Scaling)) |
| L01tx1 | 9.425321e-12\*(1/Scaling-(1-Scaling)) |
| L01tx2 | 9.425321e-12\*(1/Scaling-(1-Scaling)) |
| L1 | 1.525853e-12\*(1/Scaling-(1-Scaling)) |
| L2 | 2.915385e-12\*(1/Scaling-(1-Scaling)) |
| L3 | 4.813688e-13\*(1/Scaling-(1-Scaling)) |
| L4 | 1.2716425e-12\*(1/Scaling-(1-Scaling)) |
| L5 | 3.257224e-12\*(1/Scaling-(1-Scaling)) |
| L6 | 1.2716425e-12\*(1/Scaling-(1-Scaling)) |
| L7 | 3.257224e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |
| RINStx2 | 1.36 |

## MERGET

|  |  |
| --- | --- |
| B01rx1 | 0.406097\*Scaling |
| B01rx2 | 0.406097\*Scaling |
| B01tx1 | 1.61703\*Scaling |
| B1 | 1.32973\*Scaling |
| B2 | 0.94415\*Scaling |
| B3 | 1.32973\*Scaling |
| B4 | 0.94415\*Scaling |
| B5 | 0.469957\*Scaling |
| IB01rx1 | 5.78131e-05\*Scaling |
| IB01rx2 | 5.78131e-05\*Scaling |
| IB01tx1 | 9.86576e-05\*Scaling |
| IB1 | 2.13019e-04\*Scaling |
| L01rx1 | 1.0229e-13\*(1/Scaling-(1-Scaling)) |
| L01rx2 | 1.0229e-13\*(1/Scaling-(1-Scaling)) |
| L02rx1 | 3.65208e-13\*(1/Scaling-(1-Scaling)) |
| L02rx2 | 3.65208e-13\*(1/Scaling-(1-Scaling)) |
| L02tx1 | 7.96831e-13\*(1/Scaling-(1-Scaling)) |
| L1 | 1.9845e-12 \*(1/Scaling-(1-Scaling)) |
| L2 | 4.25096e-13 \*(1/Scaling-(1-Scaling)) |
| L3 | 1.9845e-12 \*(1/Scaling-(1-Scaling)) |
| L4 | 4.25096e-13\*(1/Scaling-(1-Scaling)) |
| L6 | 3.24979e-12\*(1/Scaling-(1-Scaling)) |
| L7 | 3.11368e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## NOTT

|  |  |
| --- | --- |
| B01 | 1.348788\*Scaling |
| B01\_rx1 | 1.247562\*Scaling |
| B01\_rx2 | 1.261343\*Scaling |
| B01\_tx1 | 2.850960\*Scaling |
| B02 | 0.771808\*(Scaling-0.1) |
| B03 | 1.222667\*Scaling |
| B05 | 1.222101\*Scaling |
| B06 | 1.043226\*Scaling |
| B07 | 2.213909\*Scaling |
| B09 | 1.409949\*Scaling |
| B10 | 1.722710\*Scaling |
| B11 | 1.419310\*Scaling |
| IB01\_rx1 | 1.81215e-04\*Scaling |
| IB01\_rx2 | 1.46094e-04\*Scaling |
| IB01\_tx1 | 1.87178e-04\*Scaling |
| IB02 | 9.697825e-05\*Scaling |
| IB03 | 9.522133e-05\*Scaling |
| IB04 | 1.01564\*e-04Scaling |
| IB06 | 1.08369\*e-04Scaling |
| L01 | 2.2847125e-12\*(1/Scaling-(1-Scaling)) |
| L01\_rx1 | 2.145741e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L01\_rx2 | 1.857050e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L01\_tx1 | 2.3950555e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L02\_rx1 | 2.546748e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L02\_rx2 | 4.471842e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L02\_tx1 | 3.472354e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L03 | 6.596152e-12\*(2/Scaling-(2-Scaling)) |
| L04 | 4.241318e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L06 | 3.285957e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L07 | 4.998546e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L08 | 8.694578e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L09 | 2.841652e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L10 | 5.365068e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L12 | 2.653177e-12\*(0.9/Scaling-(0.9-Scaling)) |
| L13 | 2.156610e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L15 | 2.124466e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L16 | 2.611681e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L17 | 9.918031e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L18 | 2.584239e-13\*(1.5/Scaling-(1.5-Scaling)) |
| L19 | 3.1681135e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L20 | 1.167588e-12\*(1.5/Scaling-(1.5-Scaling)) |
| L21 | 7.461109e-13\*(1.5/Scaling-(1.5-Scaling)) |
| RINS\_tx1 | 1.36 |

## AND2T

|  |  |
| --- | --- |
| B01 | 1.3189865\*Scaling |
| B01rx1 | 0.880630\*Scaling |
| B01rx2 | 0.880630\*Scaling |
| B01rx3 | 0.901389\*Scaling |
| B01tx1 | 2.266253\*Scaling |
| B02 | 1.3189865\*Scaling |
| B03 | 1.134027\*Scaling |
| B04 | 1.134027\*Scaling |
| B05 | 1.527012\*Scaling |
| B06 | 1.527012\*Scaling |
| B07 | 1.2572455\*Scaling |
| B08 | 1.167014\*Scaling |
| B09 | 2.035450\*Scaling |
| B10 | 1.759341\*Scaling |
| B11 | 1.759341\*Scaling |
| B14 | 1.501805\*Scaling |
| IB01 | 1.132685e-04\*Scaling |
| IB01rx1 | 1.314468e-04\*Scaling |
| IB01rx2 | 1.314468e-04\*Scaling |
| IB01rx3 | 1.275400e-04\*Scaling |
| IB01tx1 | 2.136646e-04\*Scaling |
| IB02 | 1.132685e-04\*Scaling |
| IB03 | 6.267584e-05\*Scaling |
| IB07 | 1.792992e-04\*Scaling |
| L01 | 2.579655e-12\*(1/Scaling-(1-Scaling)) |
| L01rx1 | 1.536947e-12\*(1/Scaling-(1-Scaling)) |
| L01rx2 | 1.536947e-12\*(1/Scaling-(1-Scaling)) |
| L01rx3 | 1.774600e-12\*(1/Scaling-(1-Scaling)) |
| L01tx1 | 4.643987e-12\*(1/Scaling-(1-Scaling)) |
| L02 | 2.579655e-12\*(1/Scaling-(1-Scaling)) |
| L02tx1 | 2.742820e-12\*(1/Scaling-(1-Scaling)) |
| L03 | 1.932542e-12\*(1/Scaling-(1-Scaling)) |
| L04 | 1.932542e-12\*(1/Scaling-(1-Scaling)) |
| L05 | 1.146410e-12\*(1/Scaling-(1-Scaling)) |
| L06 | 1.146410e-12\*(1/Scaling-(1-Scaling)) |
| L07 | 1.993193e-12\*(1/Scaling-(1-Scaling)) |
| L08 | 3.900000e-14\*(1/Scaling-(1-Scaling)) |
| L09 | 2.924751e-12\*(1/Scaling-(1-Scaling)) |
| L13 | 2.230395e-12\*(1/Scaling-(1-Scaling)) |
| L14 | 2.230395e-12\*(1/Scaling-(1-Scaling)) |
| L15 | 6.104902e-12\*(1/Scaling-(1-Scaling)) |
| L16 | 6.104902e-12\*(1/Scaling-(1-Scaling)) |
| L17 | 1.942793e-12\*(1/Scaling-(1-Scaling)) |
| L19 | 2.037336e-13\*(1/Scaling-(1-Scaling)) |
| L20 | 3.990105e-13\*(1/Scaling-(1-Scaling)) |
| L21 | 1.290893e-13\*(1/Scaling-(1-Scaling)) |
| L22 | 1.290893e-13\*(1/Scaling-(1-Scaling)) |
| L23 | 1.000000e-14\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## OR2T

|  |  |
| --- | --- |
| B01 | 1.43648\*Scaling |
| B01rx1 | 0.761009\*Scaling |
| B01rx2 | 0.761009\*Scaling |
| B01rx3 | 0.498239\*Scaling |
| B01tx1 | 1.4217\*Scaling |
| B02 | 1.02669\*Scaling |
| B02rx3 | 0.709348\*Scaling |
| B03 | 1.43648\*Scaling |
| B03rx3 | 0.624715\*Scaling |
| B04 | 1.02669\*Scaling |
| B05 | 1.07602\*Scaling |
| B08 | 1.00901\*Scaling |
| B09 | 1.78161\*Scaling |
| B10 | 1.85929\*Scaling |
| IB01 | 2.58575e-04\*Scaling |
| IB01rx1 | 9.93419e-05\*Scaling |
| IB01rx2 | 9.93419e-05\*Scaling |
| IB01rx3 | 6.19356e-05\*Scaling |
| IB01tx1 | 1.24071e-04\*Scaling |
| IB02 | 4.45911e-05\*Scaling |
| IB04 | 7.34836e-05\*Scaling |
| L01 | 1.19917e-12\*(1/Scaling-(1-Scaling)) |
| L01rx1 | 1.0157e-12\*(1/Scaling-(1-Scaling)) |
| L01rx2 | 1.0157e-12\*(1/Scaling-(1-Scaling)) |
| L01rx3 | 1.31862e-12\*(1/Scaling-(1-Scaling)) |
| L01tx1 | 3.33856e-12\*(1/Scaling-(1-Scaling)) |
| L02 | 1.12533e-12\*(1/Scaling-(1-Scaling)) |
| L02rx1 | 1.66138e-12\*(1/Scaling-(1-Scaling)) |
| L02rx2 | 1.66138e-12\*(1/Scaling-(1-Scaling)) |
| L02rx3 | 2.19746e-12\*(1/Scaling-(1-Scaling)) |
| L02tx1 | 2.41485e-12\*(1/Scaling-(1-Scaling)) |
| L03 | 1.19917e-12\*(1/Scaling-(1-Scaling)) |
| L03rx3 | 2.41399e-12\*(1/Scaling-(1-Scaling)) |
| L04 | 1.12533e-12 \*(1/Scaling-(1-Scaling)) |
| L05 | 6.00000e-13\*(1/Scaling-(1-Scaling)) |
| L06 | 2.39701e-12\*(1/Scaling-(1-Scaling)) |
| L07 | 4.00000e-13\*(1/Scaling-(1-Scaling)) |
| L08 | 4.37488e-12\*(1/Scaling-(1-Scaling)) |
| L09 | 1.60915e-12\*(1/Scaling-(1-Scaling)) |
| L13 | 1.86893e-12\*(1/Scaling-(1-Scaling)) |
| L14 | 8.12022e-13\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## XORT

|  |  |
| --- | --- |
| B01 | 2.79835\*Scaling |
| B01\_rx1 | 1.21244\*Scaling |
| B01\_rx2 | 1.21244\*Scaling |
| B01\_rx3 | 0.723632\*Scaling |
| B02\_rx1 | 1.15856\*Scaling |
| B02\_rx2 | 1.15856\*Scaling |
| B02\_rx3 | 0.772041\*Scaling |
| B02\_tx1 | 1.36946\*Scaling |
| B03 | 1.91585\*Scaling |
| B03\_rx1 | 0.89775\*Scaling |
| B03\_rx2 | 0.89775\*Scaling |
| B03\_rx3 | 0.827992\*Scaling |
| B04 | 2.79835\*Scaling |
| B06 | 1.91585\*Scaling |
| B07 | 1.48566\*Scaling |
| B08 | 0.933603\*Scaling |
| B09 | 1.28591\*Scaling |
| B10 | 1.6863\*Scaling |
| IB01 | 8.9218e-05\*Scaling |
| IB01\_rx1 | 2.29789e-04\*Scaling |
| IB01\_rx2 | 2.29789e-04\*Scaling |
| IB01\_rx3 | 1.31858e-04\*Scaling |
| IB02 | 8.92180e-05\*Scaling |
| IB02\_tx1 | 6.64568e-05\*Scaling |
| IB04 | 1.24046e-04\*Scaling |
| IB05 | 1.77629e-04\*Scaling |
| L01\_rx1 | 1.86037e-12\*(1/Scaling-(1-Scaling)) |
| L01\_rx2 | 1.86037e-12\*(1/Scaling-(1-Scaling)) |
| L01\_rx3 | 1.89277e-12\*(1/Scaling-(1-Scaling)) |
| L02\_rx1 | 2.15285e-12\*(1/Scaling-(1-Scaling)) |
| L02\_rx2 | 2.15285e-12\*(1/Scaling-(1-Scaling)) |
| L02\_rx3 | 2.23806e-12\*(1/Scaling-(1-Scaling)) |
| L03 | 2.27926e-12\*(1/Scaling-(1-Scaling)) |
| L03\_rx1 | 1.97288e-12\*(1/Scaling-(1-Scaling)) |
| L03\_rx2 | 1.97288e-12\*(1/Scaling-(1-Scaling)) |
| L03\_rx3 | 2.02047e-12\*(1/Scaling-(1-Scaling)) |
| L03\_tx1 | 2.22608e-12\*(1/Scaling-(1-Scaling)) |
| L04\_rx1 | 2.39660e-12\*(1/Scaling-(1-Scaling)) |
| L04\_rx2 | 2.39660e-12\*(1/Scaling-(1-Scaling)) |
| L04\_rx3 | 2.01777e-12\*(1/Scaling-(1-Scaling)) |
| L06 | 2.27926e-12\*(1/Scaling-(1-Scaling)) |
| L08 | 1.75154e-12\*(1/Scaling-(1-Scaling)) |
| L09 | 1.26199e-12\*(1/Scaling-(1-Scaling)) |
| L10 | 2.22462e-12\*(1/Scaling-(1-Scaling)) |
| L11 | 1.80333e-12\*(1/Scaling-(1-Scaling)) |
| L12 | 1.86580e-12\*(1/Scaling-(1-Scaling)) |
| L14 | 1.63540e-12\*(1/Scaling-(1-Scaling)) |
| L15 | 1.63540e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |

## NDROT

|  |  |
| --- | --- |
| B01 | 2.178840\*Scaling |
| B01rx1 | 0.859672\*Scaling |
| B01rx2 | 0.859672\*Scaling |
| B01rx3 | 0.989203\*Scaling |
| B01tx1 | 2.3613475\*Scaling |
| B02 | 1.649842\*Scaling |
| B02rx1 | 1.000206\*Scaling |
| B02rx2 | 1.000206\*Scaling |
| B02rx3 | 0.942630\*Scaling |
| B03 | 2.346444\*Scaling |
| B04 | 1.959720\*Scaling |
| B05 | 2.836757\*Scaling |
| B06 | 1.907933\*Scaling |
| B07 | 1.7749365\*Scaling |
| B08 | 1.161874\*Scaling |
| B09 | 0.778214\*Scaling |
| B10 | 1.631291\*Scaling |
| B11 | 1.507887\*Scaling |
| IB01 | 2.238515e-04\*Scaling |
| IB01rx1 | 1.341424e-04\*Scaling |
| IB01rx2 | 1.341424e-04\*Scaling |
| IB01rx3 | 1.317977e-04\*Scaling |
| IB01tx1 | 1.955091e-04\*Scaling |
| IB02 | 1.521925e-04\*Scaling |
| IB03 | 1.980858e-04\*Scaling |
| IB04 | 9.8516585e-05\*Scaling |
| IB05 | 9.472815e-05\*Scaling |
| IB06 | 6.367468e-05\*Scaling |
| L01 | 7.583254e-12\*(1/Scaling-(1-Scaling)) |
| L01rx1 | 1.912227e-12\*(1/Scaling-(1-Scaling)) |
| L01rx2 | 1.912227e-12\*(1/Scaling-(1-Scaling)) |
| L01rx3 | 1.786886e-12\*(1/Scaling-(1-Scaling)) |
| L01tx1 | 3.542674e-12\*(1/Scaling-(1-Scaling)) |
| L02 | 1.338136e-12\*(1/Scaling-(1-Scaling)) |
| L02rx1 | 4.048126e-12\*(1/Scaling-(1-Scaling)) |
| L02rx2 | 4.048126e-12\*(1/Scaling-(1-Scaling)) |
| L02rx3 | 4.313534e-12\*(1/Scaling-(1-Scaling)) |
| L02tx1 | 3.526988e-12\*(1/Scaling-(1-Scaling)) |
| L03 | 4.387869e-12\*(1/Scaling-(1-Scaling)) |
| L03rx1 | 3.603585e-12\*(1/Scaling-(1-Scaling)) |
| L03rx2 | 3.603585e-12\*(1/Scaling-(1-Scaling)) |
| L03rx3 | 3.925951e-12\*(1/Scaling-(1-Scaling)) |
| L04 | 3.216968e-12\*(1/Scaling-(1-Scaling)) |
| L05 | 7.2182845e-12\*(1/Scaling-(1-Scaling)) |
| L06 | 3.067698e-12\*(1/Scaling-(1-Scaling)) |
| L07 | 2.559630e-12\*(1/Scaling-(1-Scaling)) |
| L08 | 3.243894e-12\*(1/Scaling-(1-Scaling)) |
| L09 | 3.738166e-13\*(1/Scaling-(1-Scaling)) |
| L10 | 5.299364e-13\*(1/Scaling-(1-Scaling)) |
| L11 | 2.508769e-12\*(1/Scaling-(1-Scaling)) |
| L13 | 9.513657e-13\*(1/Scaling-(1-Scaling)) |
| L14 | 4.752764e-14\*(1/Scaling-(1-Scaling)) |
| L15 | 1.287470e-12\*(1/Scaling-(1-Scaling)) |
| L16 | 1.067767e-12\*(1/Scaling-(1-Scaling)) |
| L17 | 1.279105e-12\*(1/Scaling-(1-Scaling)) |
| RINStx1 | 1.36 |