DSM
IIIT Hyderabad

October 2024

Time: 45 min | *Quiz-2 Exam* | Maximum Marks: 20

Set A

Answer all the questions. Answer in the space provided only. All the best

Roll Number:

Seat Number:

Room Number:

Invigilator signature:

Question number	Marks (a)	Marks (b)	Marks (c)	Marks (d)	Name of TA corrected
1					
2					
3					
4					
5					
6					
Total					

No reading material is allowed to use in the exam hall.

No exchange of material during exam.

Use back sheets for rough work. No additional papers for rough work / answers.

Answer in the space provided only.

1. A stream of bits is given as input, and we need to detect a double zero (two consecutive zeros). You have JK FF and some basic logic gates available.
   (a) Draw a state (transition) diagram [2M]
   (b) Complete state table [2M]
   (c) Implement simplest circuit which will achieve double zero detection [5M]

Question 1 continues on the next page...

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Question 1 continues on the next page...

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2. Describe using a few words or diagram
   (a) Comapre SR latch vs JK flipflop [2 M]
   (b) Shift register vs Parallel register with Pros & Cons. [2M]
   (c) Equivalent states [1M]
   (c) Synchronous reset [1M]

Question 2 continues on the next page...

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Question 2 continues on the next page...

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3. Design a 4-bit universal shift register using T flip-flops and explain its operation. [5 M]

Question 3 continues on the next page...

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Question 3 continues on the next page...

Rough work