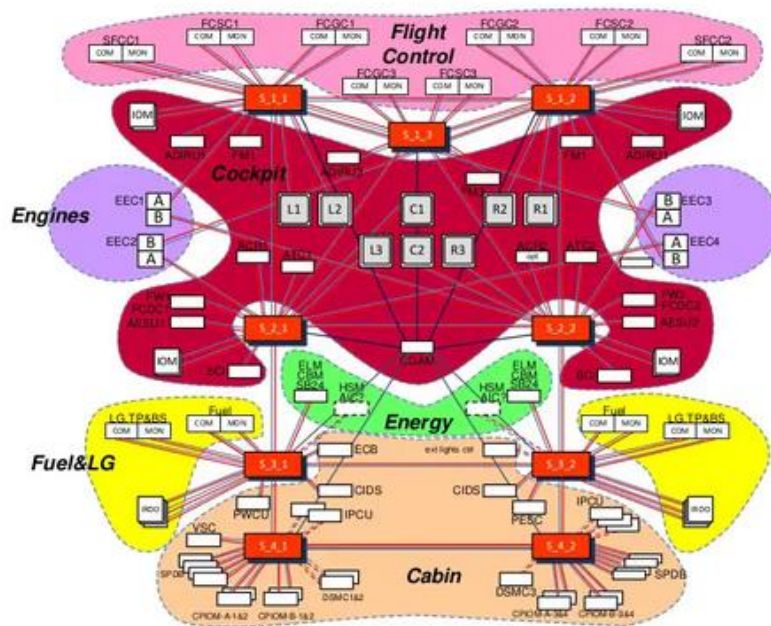


## *System Engineering Report*

# Implementation of a Real-Time Ethernet with Quality-of-Service mechanisms

*AFDX network using P4 language*



**P4FDX**

28/04/2022

EMS 2021/2022 - Integrated Team Project

CHAMPAIN Florian

GRENIER Célestin

ILLI Adil

ZEMZEM Mehdi

## Table of content

Table of content .....	1
Table of figures .....	1
1. Introduction .....	2
1.1 Purpose (context of the project) .....	2
1.2 Documents list (reference documents/applicable documents) .....	2
1.3 Glossary/Acronyms .....	2
2. System presentation .....	3
2.1 Purpose, Mission, Objectives .....	3
2.2 System life-cycle .....	4
2.2.1 Stakeholder Needs Definition .....	4
2.2.2 Requirement Analysis .....	4
2.2.3 Functional & Physical Design .....	4
2.2.4 Implementation .....	4
2.2.5 Integration .....	4
2.2.6 Verification .....	5
2.2.7 Validation .....	5
2.2.8 Operational & Maintenance .....	5
2.2.9 Disposal .....	5
2.3 Stakeholders and associated satisfaction analysis .....	6
3. System analysis .....	7
3.1 Functional analysis .....	7
3.2 Physical analysis .....	8
3.3 Verification and Validation .....	9

## Table of figures

Figure 1 : System life-cycle .....	4
Figure 2 : Octopus diagram functional analysis .....	7
Figure 3 : System hierarchical decomposition .....	8
Figure 4 : Architecture interfaces diagram .....	8
Figure 5 : Function breakdown .....	9

# 1. Introduction

## 1.1 Purpose (context of the project)

The main aim of the project is the implementation of a Real-time Ethernet network with quality-of-service mechanisms. For embedded systems, Real-time communications are a necessity. More specifically for avionics systems, real-time networks are the prominent form of communications due to baud rate, latency, and overall system weight.

The current situation in IRIT-ENSEEIH is that all the research related to Real-time networks, is only implemented on simulation tools (such as Mininet). Hence, the implementation of such a network in the labs of ENSEEIH, will have a significant impact on the progress of research in this field. At the end, it will serve as a base ground for future work related to Real-time networking.

This document will outline the system engineering aspect for the implementation of a Real-time Ethernet network with quality-of-service mechanisms.

## 1.2 Documents list (reference documents/applicable documents)

- “*Implementation of a Real-Time Ethernet with Quality-of-Service mechanisms*” - Jérôme Ermont (11/10/2021): Document presenting the project context and objectives
- “P416 Language Specification version 1.0.0” - The P4 Language Consortium (22/05/2017)
- “Avionics networks lecture” - Katia Jaffrès-Runser (ENSEEIH 2021-2022)

## 1.3 Glossary/Acronyms

<i>AFDX</i>	Avionics Full-Duplex Switched Ethernet
<i>TSN</i>	Time sensitive networking
<i>P4</i>	Programming Protocol-independent Packet Processors
<i>P4C</i>	P4 compiler
<i>P4PI</i>	P4 on Raspberry Pi
<i>DPDK</i>	Data Plane Development Kit
<i>T4P4S</i>	Target-independent Compiler for P4
<i>QoS</i>	Quality of service
<i>SPQ</i>	Static priority queue
<i>WRR</i>	Weighted round robin
<i>DRR</i>	Deficit round robin
<i>CBS</i>	Credit Based Shaper

## 2. System presentation

### 2.1 Purpose, Mission, Objectives

The purpose of the project is to demonstrate the feasibility of an AFDX network implemented on classic lab hardware (PC and Raspberry PI) with quality-of-service mechanisms.

The mission of the project is split in two main parts:

- Implement a functional AFDX network using :
  - specific hardware furnished by the IRT lab: Linux PC with ethernet Cards and Raspberry PI 3 and PI4
  - P4 abstraction language (as required by the main stakeholder)
- Implement QoS mechanisms algorithms such as SPQ, WRR and DRR

The objectives of the project have been defined as:

- Mandatory : Implementation of P4 on Raspberry (using P4Pi) and on computer (using DPDK)
- Mandatory : Implementation of QoS using WRR and SPQ mechanisms
- Facultative : Implementation of DRR QoS mechanism
- Facultative : Study and implementation of Ethernet 802.1 TSN mechanisms such as CBS

## 2.2 System life-cycle

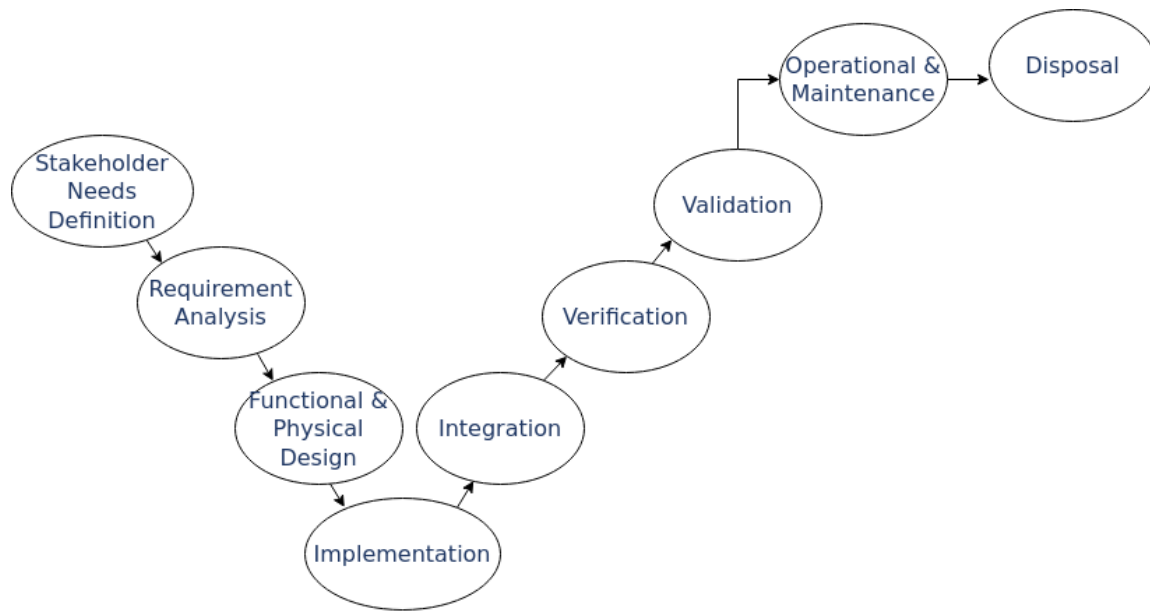


Figure 1 : System life-cycle

### 2.2.1 Stakeholder Needs Definition

See §2.3

### 2.2.2 Requirement Analysis

See §2.3

### 2.2.3 Functional & Physical Design

See §3.1 and §3.2.

### 2.2.4 Implementation

The implementation is divided into 2 work packages:

- WP1: Implementation of QoS mechanisms and simulation under Mininet
- WP2: AFDX hardware architecture implementation

### 2.2.5 Integration

The integration is defined in work package 3 (WP3: Integration of QoS on hardware network).

It will be done in the Enseeiht IT lab with computers and Raspberry provided by the Enseeiht.

### 2.2.6 Verification

See §3.3

### 2.2.7 Validation

See §3.3

### 2.2.8 Operational & Maintenance

A technical documentation and a files package will be delivered to the stakeholder to provide all the tools needed for the installation and execution of an AFDX network based on computers and raspberry with QoS strategies.

The file package will include, the setup tools, all the technical files (P4, DPDK, P4PI files) and the validation tools.

### 2.2.9 Disposal

Usage of whole system at the end of the project.

## 2.3 Stakeholders and associated satisfaction analysis

The main stakeholder of this project is the ENSEEIHT IT laboratory and, specifically, the project tutor, Jérôme Ermont, who provided the project objectives, requirements and specifications.

The satisfaction will be determined by 2 categories of objectives defined by the main stakeholder (as defined in §2.1 and §2.2): Mandatory objectives and optional objectives.

From these stakeholders needs, the following requirements are defined:

R1 - The system shall simulate an AFDX real time network using only PC and Raspberry as host and programmable switches

R1.1 (Mandatory) - The system shall run a programmable switch on a computer

R1.2 (Mandatory) - The system shall run a programmable switch on a Raspberry PI

R2 - The system shall provide QoS mechanisms

R2.1 (Mandatory) - The system shall provide QoS using WRR mechanisms

R2.2 (Mandatory) - The system shall provide QoS using SPQ mechanisms

R2.3 (Optional) - The system shall provide QoS using DRR mechanisms

R3 (Optional) - The system shall provide Ethernet 802.1 TSN mechanisms

The secondary stakeholders are the project management and systems engineering tutors. Their satisfaction is determined by the on-time delivery and the quality of both reports.

R4 (Mandatory) - Deliver a Project Management Report

R5 (Mandatory) - Deliver a System Engineering Report

### 3. System analysis

#### 3.1 Functional analysis

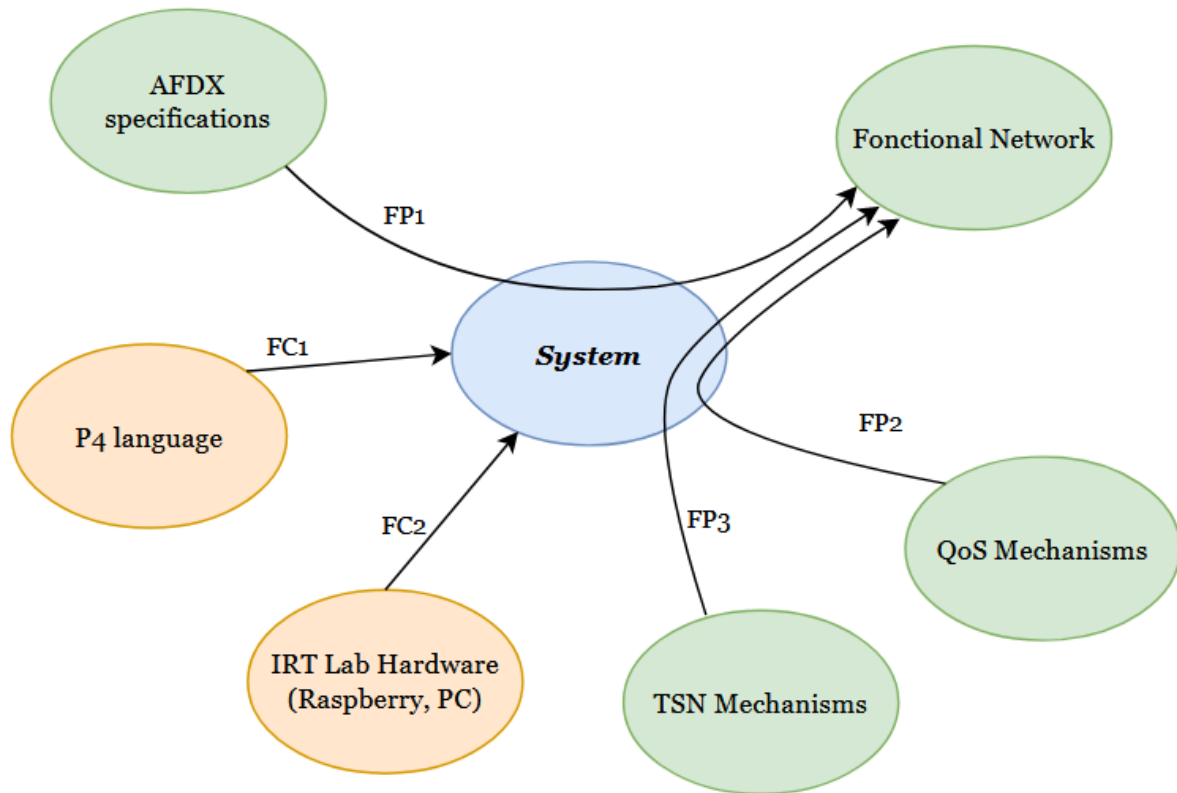


Figure 2 : Octopus diagram functional analysis

Main functions:

- FP1 is the implementation of the AFDX specifications in a functional network.
- FP2 is the implementation of QoS mechanisms in a functional network
- FP3 is the implementation of TSN mechanisms in a functional network

Constraint functions:

- FC1 : P4 abstraction language has to be used by the system
- FC2 : The system has to use the hardware furnished by the IRT lab



### 3.2 Physical analysis

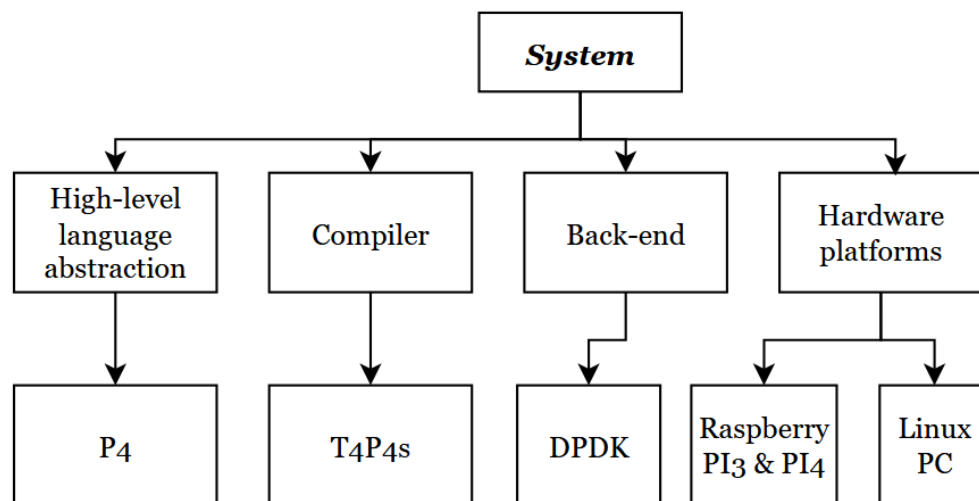


Figure 3 : System hierarchical decomposition

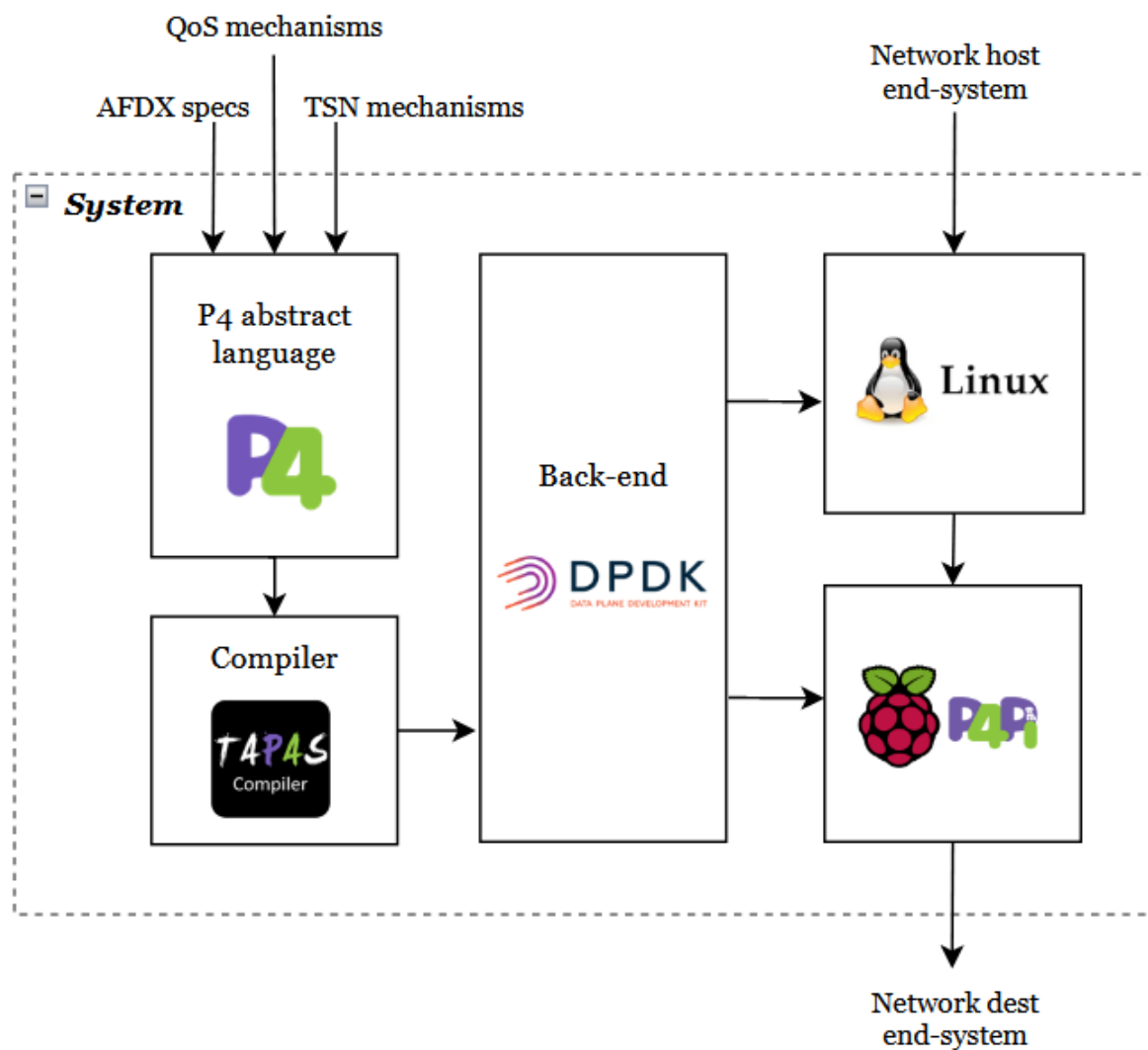


Figure 4 : Architecture interfaces diagram

### 3.3 Verification and Validation

The validation will be performed using specific tools developed for verification phase. For each requirements group, the validation criteria are the followings:

- R1: The system is able to transfer a packet from a host to other hosts through switches using AFDX protocol (virtual links)
- R2: The system is able to transfer a large number of network packets while respecting the selected QoS strategy.
- R3: The system is able to transfer a large number of network packets while respecting the TSN protocol.

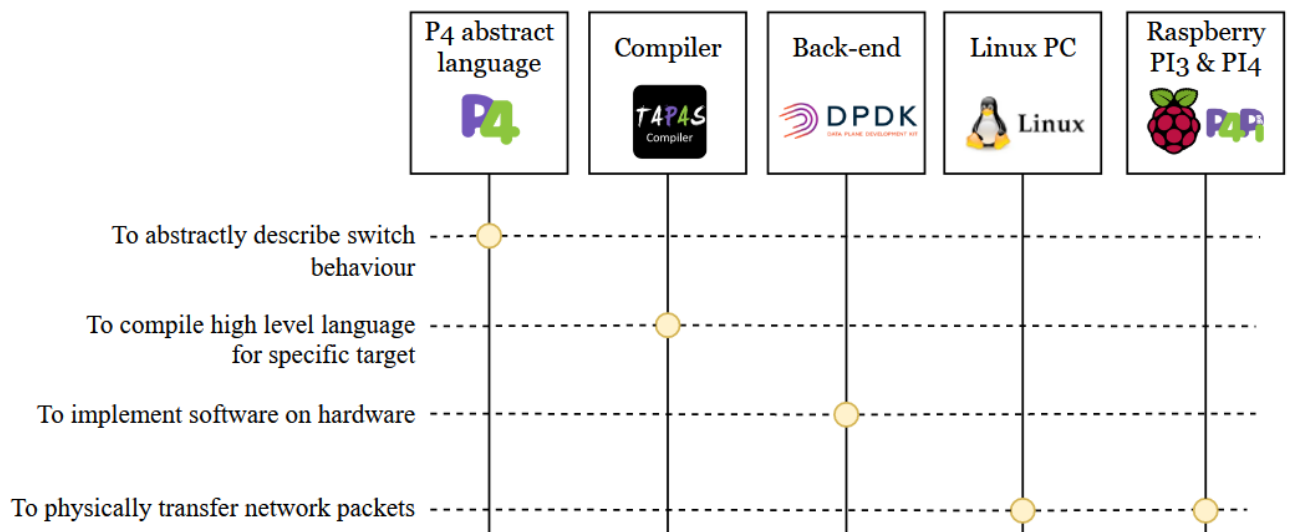


Figure 5 : Function breakdown