Prototyping a Secure Controller for Trusted Heterogeneous Disaggregated Architectures

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Motivation

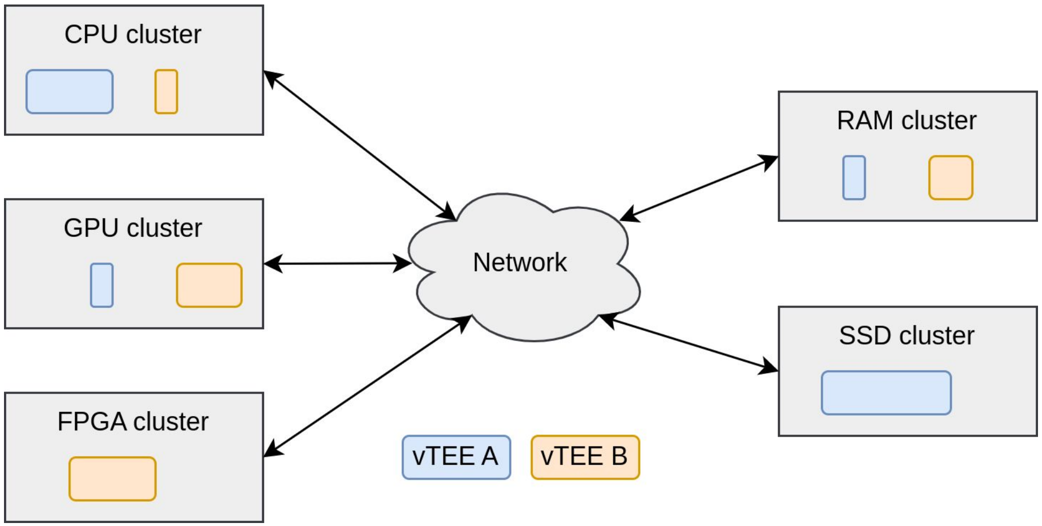
- Data center architectures are becoming more
  - Heterogeneous: CPUs, GPUs, FPGAs, ASICs, …
  - Disaggregated: Devices in racks connected to the network
- Workloads involve sensitive data
- New security challenges
- Trusted isolated environment?

State-of-the-art

- Trusted Execution Environments
  - CPU-centric and vendor-specific (Intel SGX/TDX, AMD SEV, ARM TrustZone)
  - Device-specific (Graviton [1], ShEF [2])
- Distributed operating systems
  - LegoOS [3]: Supports Linux applications, CPU-centric
  - FractOS [4]: Own programming model, execution graph
- Distributed TEEs
  - HETEE [5]: Centralized security controller, limited to one rack
  - [6]: Similar to HETEE with multiple security controllers

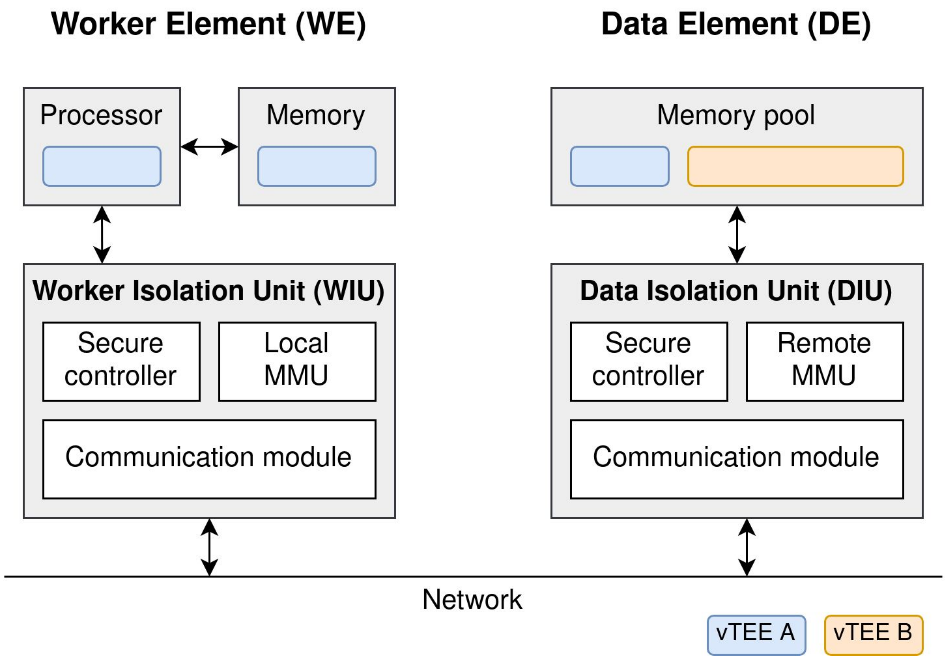
Research gap

How to establish virtual Trusted Execution Environments spanning multiple heterogeneous disaggregated resources?



Problem statement

Develop a prototype of a secure controller for trusted heterogeneous disaggregated architectures



Background

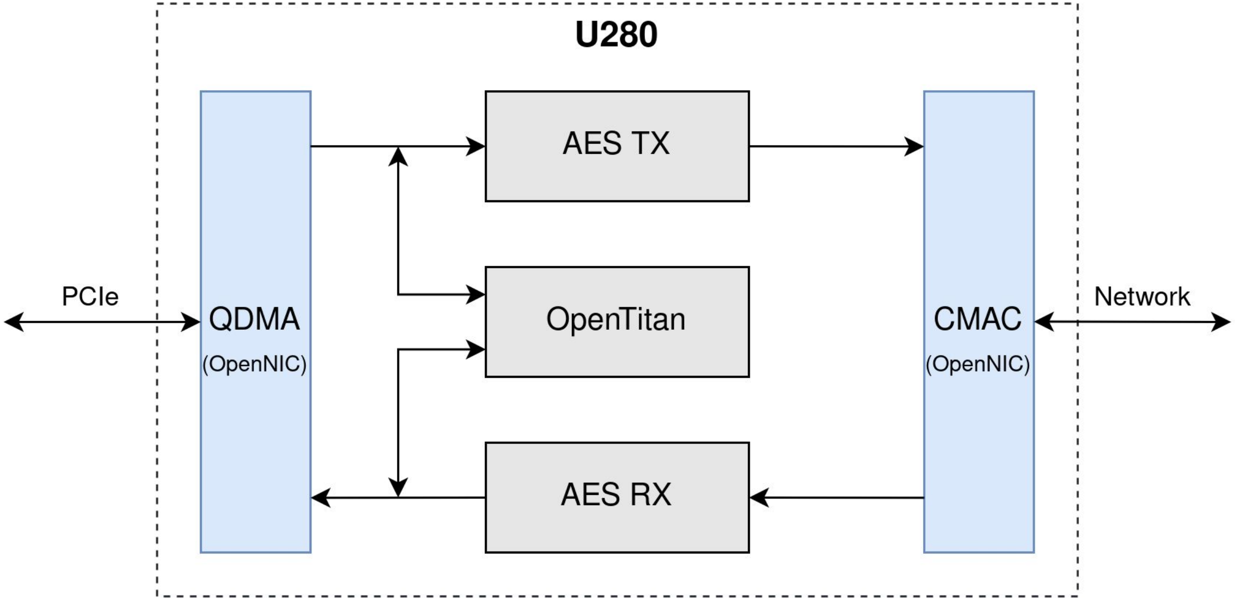
- OpenTitan
  - Open-source silicon Root of Trust
  - Officially supports one FPGA development board
- AES accelerator
  - Performance of the OpenTitan AES module is insufficient
  - Two modes: communication with OpenTitan and passthrough
- Xilinx Alveo U280
  - PCIe FPGA card
  - 100 Gbit/s network interface

Design Goals

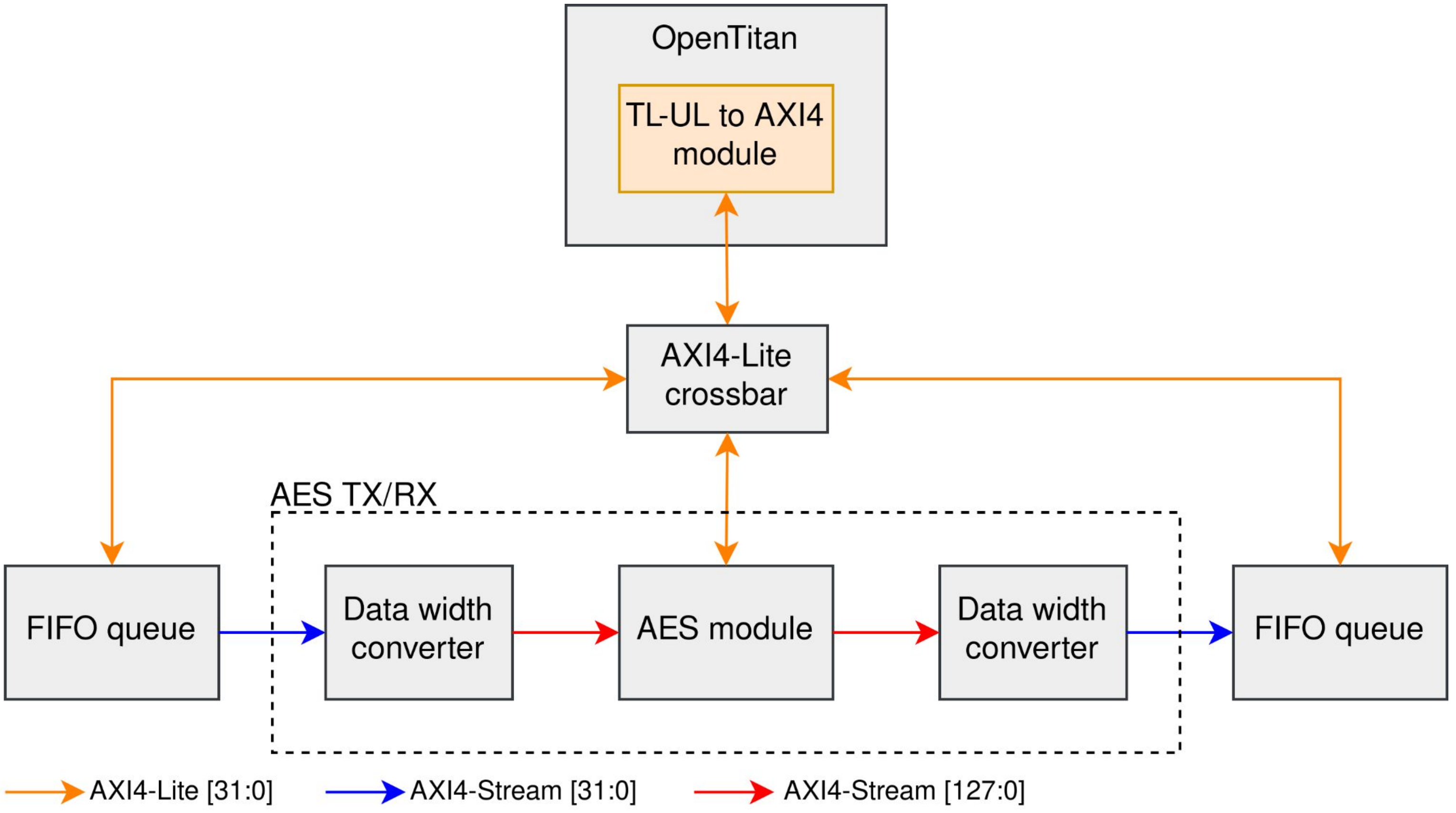
- Implementation on the U280
- OpenTitan as Root of Trust and main CPU
- High-speed symmetric encryption
  - vTEE management (OpenTitan ⇔ OpenTitan)
  - vTEE execution (passthrough, e.g. CPU ⇔ GPU)

Design

- OpenTitan as Root of Trust
- OpenNIC for communication via PCIe and network
- AES modules controlled by OpenTitan



Implementation



Implementation

- Porting the OpenTitan to U280
  - Change config files and constraints
  - Package as Vivado IP ⇒ easy integration into a larger project
- OpenTitan AXI4 module
  - Based on ToAXI4 module from Rocket Chip project[1]
  - Converts internal TL-UL bus to external AXI4 bus
- AXI4-Lite crossbar to connect multiple modules to OpenTitan

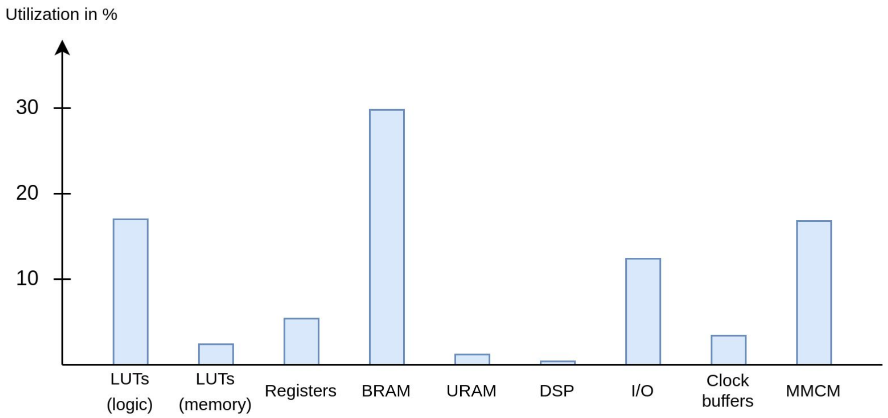
[1] https://github.com/chipsalliance/rocket-chip/blob/master/src/main/scala/tilelink/ToAXI4.scala

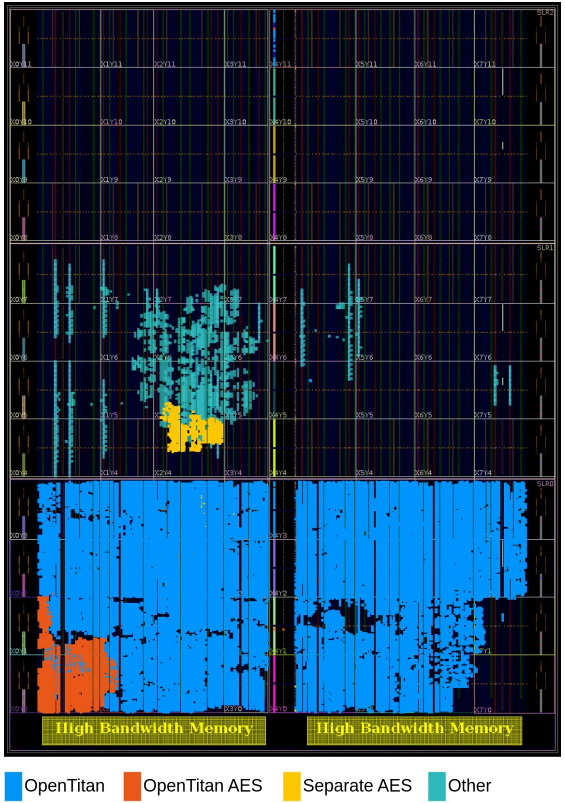
Implementation

- AES module
  - Based on AES module form Xilinx Vitis RTL kernel tutorial[1]
  - Operates on AXI4-Stream traffic
  - AES function only ⇒ ECB mode!
- Data width converters
  - AXI4-Stream data widths: FIFOs 32 bit, AES 128 bit

[1] https://github.com/Xilinx/Vitis-Tutorials/blob/2021.2/Hardware_Acceleration/Design_Tutorials/05-bottom_up_rtl_kernel/doc/krnl_aes.md

Evaluation: FPGA Utilization

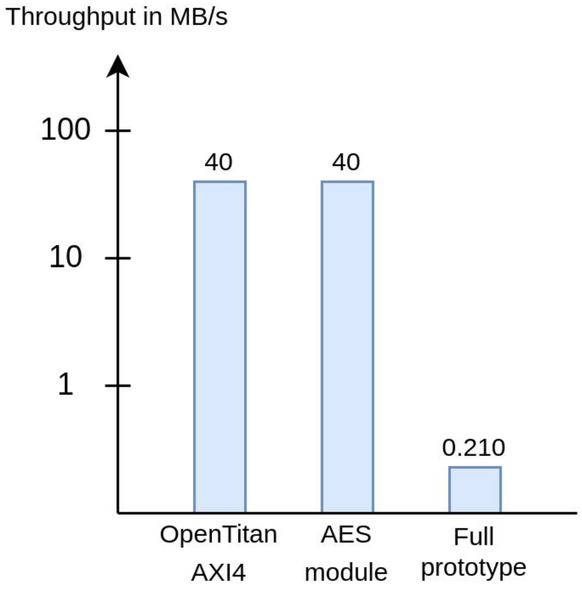




Utilization is low enough to add additional modules (e.g. OpenNIC)

Evaluation: Performance

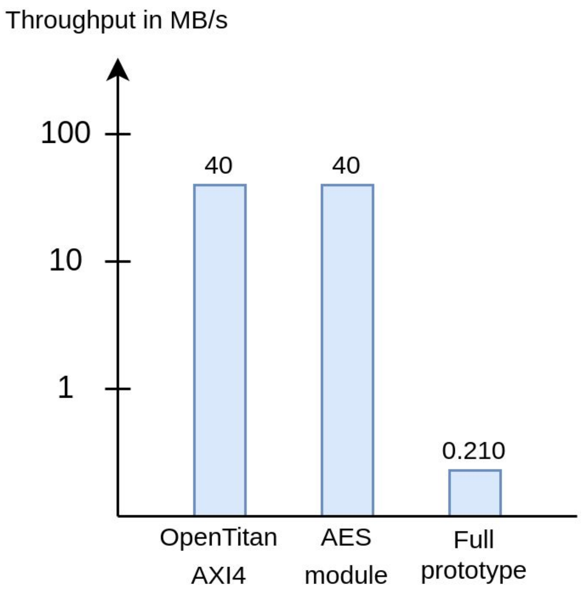
- OpenTitan AXI4 module: 40 MB/s
  - Limited by 10 MHz TL-UL bus
  - Sufficient for intended use case
- AES module: 40 MB/s
  - Limited by 10 MHz AXI4 clock
  - Too slow for high-speed network traffic
  - Xilinx benchmark with higher clock: 390 MB/s



AES performance is sufficient for OpenTitan but insufficient for communication between worker elements

Evaluation: Performance

- Full prototype: 210 KB/s
  - OpenTitan ⇒ FIFO ⇒ AES ⇒ FIFO ⇒ OpenTitan
  - Extrapolated from 4 KB per run
  - Limited by
    - AXI4 clock
    - Data width converters
    - FIFO copying



Full prototype performance limited by multiple factors, greatly lags behind raw AES module performance

Summary

Data center architectures are becoming more heterogeneous and disaggregated

- Goal: distributed virtual Trusted Execution Environments (vTEEs)

Secure controller prototype

- Root of Trust OpenTitan ported to U280 & extended with AXI4 module
- AES module for encrypting network traffic controlled by OpenTitan
- Evaluation: resource utilization low, AES performance lacking

Code

- OpenTitan: https://github.com/TUM-DSE/TDA-opentitan
- Full prototype: https://github.com/TUM-DSE/TDA-testbed

References

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