AN2948

Configuration Registers of LAN743x

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INTRODUCTION

The LAN743x can be configured:

- Via One-Time Programmable (OTP) Memory
- Via External EEPROM

OTP Memory: The LAN743x device's registers may be configured via the hub's internal OTP memory. Any register may be given a new default value. It has a capacity of 1 kB arranged as 1K x 8 bits. The OTP supports single bits write and 8-bit reads and each byte within the OTP memory may be written only once. The OTP memory may be programmed via the PCIe interface.

External EEPROM: The device may use an external EEPROM to store the default values for the PCIe controller and the MAC address. The EEPROM controller supports most "93C56 or 93C66" type 256/512 byte EEPROMs. A total of nine address bits are used. A Microwire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation must be used. After a system-level reset occurs, the device loads the default values from EEPROM. The device is connected to the PCIe bus but responds with CRS until this process is completed. The EEPROM controller also allows the Host to read, write and erase the contents of the Serial EEPROM.

SECTIONS

This document includes the following topics:

REFERENCES

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *LAN7430 Data Sheet*
- *LAN7431 Data Sheet*

1.0 REGISTER MAP

1.1 Introduction

This application note provides the device register map, summarizing the various directly addressable Control and Status Registers (CSRs). CSRs are categorized into two major groups–PCIe configuration registers and Device registers. PCIe configuration registers are mapped into PCI configuration space. Device registers are mapped into memory space based on the contents of the PCIe configuration registers.

Table 1 provides a summary of the memory mapped CSRs and their corresponding address offsets. Detailed descriptions of the CSRs are provided in the later sections. The PCIe configuration registers are described in Section 2.0, PCIe Configuration Registers.

TABLE 1: DEVICE REGISTER MAP

Address	Register
0000h through 009Fh and 0700h through 070Fh and 0900h through 09FFh	Miscellaneous System Configuration and Status Registers
0040h through 0047h	EEPROM Controller Registers
00A0h through 00FFh	FCT Controller Registers
0100h through 03FFh and 0600h through 06FFh and 1200h through 12FFh	MAC Registers
0780h through 07FFh	Interrupt Controller Registers
0400h through 05FFh	RFE Controller Registers
0A00h through 0AFFh	1588 Registers
0C00h through 0FFFh	DMA Controller Registers

TABLE 1: DEVICE REGISTER MAP (CONTINUED)

1000h through 11FFh	OTP Control and Status Registers
1400h-1FFBh	RESERVED
1FFCh-1FFFh	unused

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

2.0 PCIE CONFIGURATION REGISTERS

This section details the PCIe Configuration registers that comprise the PCIe configuration space. The PCIe configuration space is separate from the memory mapped CSR register space. See Table 2.

TABLE 2: PCIE CONFIGURATION REGISTER MAP

Section	Byte Offset	Byte 3	Byte 2	Byte 1	Byte 0
Configuration Space	000h	Device ID		Vendor ID	
	004h	Status		Command	
	008h	Class Code			Revision ID
	00Ch	BIST	Header Type	Master Latency Timer	Cache Line Size
	010h	Base Address 0			
	014h	Base Address 1			
	018h	Base Address 2			
	01Ch	Base Address 3			
	020h	Base Address 4			
	024h	Base Address 5			
	028h	CardBus CIS Pointer			
	02Ch	Subsystem ID		Subsystem Vendor ID	
	030h	Expansion ROM Base Address			
	034h	Reserved			Capabilities Pointer
	038h	Reserved			
	03Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line
Power Management Capability	040h	Power Management Capabilities		Next Capability Pointer for PM	Capability ID for PM
	044h	Data	Bridge Support Extensions	Power Management Control/Status	
MSI Capability	050h	Message Control for MSI		Next Pointer for MSI	Capability ID for MSI
	054h	Message Lower Address for MSI			
	058h	Message Upper Address for MSI			
	05Ch	Reserved		Message Data for MSI	
	060h	Mask Bits for MSI			
	064h	Pending Bits for MSI			

TABLE 2: PCIE CONFIGURATION REGISTER MAP (CONTINUED)

PCI Express Capability	070h	PCI Express Capabilities	Next Pointer for PCIe	Capability ID for PCIe
	074h	Device Capabilities		
	078h	Device Status	Device Control	
	07Ch	Link Capabilities		
	080h	Link Status	Link Control	
	084h	Reserved		
	088h	Reserved	Reserved	
	08Ch	Reserved	Reserved	
	090h	Reserved		
	094h	Device Capabilities 2		
	098h	This field is Read Only if the LTR Mechanism Supported field in Device Capabilities 2 is cleared.	Device Control 2	
	09Ch	Link Capabilities 2		
	0A0h	Link Status 2	Link Control 2	
	0A4h	Reserved		
	0A8h	Reserved	Reserved	
MSI-X Capability	0B0h	Message Control for MSI-X	Next Pointer for MSI-X	Capability ID for MSI-X
	0B4h	Table Offset/BIR for MSI-X		
	0B8h	PBA Offset/BIR for MSI-X		
Advanced Error Reporting Capability	100h	Advanced Error Reporting Extended Capability Header		
	104h	Uncorrectable Error Status		
	108h	Uncorrectable Error Mask		
	10Ch	Uncorrectable Error Severity		
	110h	Correctable Error Status		
	114h	Correctable Error Mask		
	118h	Advanced Error Capabilities and Control		
	11Ch	Header Log		
	120h			
	124h			
	128h			
Device Serial Number Capability	148h	Device Serial Number Extended Capability Header		
	14Ch	Serial Number		
	150h			
Latency Tolerance Reporting (LTR) Capability	158h	LTR Extended Capability Header		
	15Ch	Max No-Snoop Latency	Max Snoop Latency	
L1 PM Substates Extended Capability	160h	L1 PM Substates Extended Capability Header		
	164h	L1 PM Substates Capabilities		
	168h	L1 PM Substates Control 1		
	16Ch	L1 PM Substates Control 2		

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

2.1 Configuration Space

2.1.1 VENDOR ID

Offset: 000h
Size: 16 bits

This register identifies the manufacturer of the device. See Table 3.

TABLE 3: VENDOR ID SPECIFICATIONS

Bit	Description	Type	Default
15:0	**Vendor ID** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	1055h

2.1.2 DEVICE ID

Offset: 002h
Size: 16 bits

This register identifies the particular device. See Table 4.

TABLE 4: DEVICE ID SPECIFICATIONS

Bit	Description	Type	Default
15:0	**Device ID** This field identifies the particular device.This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.(See **Note 1**.)	RO (DBI – W/STKY)	7430h 7431h 743Fh

Note 1: The device ID depends upon the SKU.

2.1.3 COMMAND

Offset: 004h
Size: 16 bits

This register provides coarse control over a device's ability to generate and respond to PCIe cycles. When a “0” is written to this register, the device is logically disconnected from the PCIe bus for all access except configuration access. See Table 5.

TABLE 5: COMMAND SPECIFICATIONS

Bit	Description	Type	Default
15:11	**RESERVED**	RO	—
10	**Interrupt Disable** When this field is set, the function is disabled from generating legacy interrupt messages. Any INTx emulation interrupts already asserted by the function must be deasserted when this field is set.	R/W	0b
9	**Fast Back-to-Back Enable** This field is not used by PCIe.	RO	0b

Note 1: This device does not support I/O space access.

TABLE 5: COMMAND SPECIFICATIONS (CONTINUED)

8	**SERR# Enable** When set, this field enables reporting of Non-fatal and Fatal errors detected by the function to the Root Complex. Note that errors are reported if enabled either through this field or through the PCI Express specific bits in the Device Control register.	R/W	0b
7	**IDSEL Stepping/Wait Cycle Control** This field is not used by PCIe.	RO	0b
6	**Parity Error Response** This field controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status Register.	R/W	0b
5	**VGA Palette Snoop** This field is not used by PCIe.	RO	0b
4	**Memory Write and Invalidate Enable** This field is not used by PCIe.	RO	0b
3	**Special Cycles** This field is not used by PCIe.	RO	0b
2	**Bus Master** This field controls the ability to issue memory and I/O read/write requests. When this field is set, the function is allowed to issue memory or I/O requests. When this field is clear, the function is not allowed to issue any memory or I/O requests. Note that as MSI/MSI-X interrupt messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt messages as well. Requests other than memory or I/O requests are not controlled by this field.	R/W	0b
1	**Memory Space** Controls the function's response to memory space access. A value of 0 disables the function response. A value of 1 allows the function to respond to memory space access.	R/W	0b
0	**I/O Space** Controls the function's response to I/O space access. A value of 0 disables the function response. A value of 1 allows the function to respond to I/O space access. (See **Note 1**.)	RO	0b

Note 1: This device does not support I/O space access.

2.1.4 STATUS

Offset: 006h
Size: 16 bits

This register is used to record status information for PCIe bus-related events. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 6.

TABLE 6: STATUS SPECIFICATIONS

Bit	Description	Type	Default
15	**Detected Parity Error** This field is set when the function receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register.	R/W1C	0b
14	**Signaled System Error** This field is set when the function sends an ERR_FATAL or ERR_NONFATAL Message and the SERR# Enable bit in the Command register is 1.	R/W1C	0b
13	**Received Master Abort** This field is set when the function receives a Completion with Unsupported Request Completion status.	R/W1C	0b
12	**Received Target Abort** This field is set when the function receives a Completion with Completer Abort Completion status.	R/W1C	0b
11	**Signaled Target Abort** This field is set when the function completes a Posted or Non-posted request as a Completer Abort error.	R/W1C	0b
10:9	**DEVSEL Timing** This field is not used by PCIe.	RO	00b
8	**Master Data Parity Error** This field is set by the function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: • Endpoint receives a Poisoned Completion • Endpoint transmits a Poisoned Request If the Parity Error Response bit is 0b, this field is never set.	R/W1C	0b
7	**Fast Back-to-Back Transactions Capable** This field is not used by PCIe.	RO	0b
6	**RESERVED**	RO	—
5	**66 MHz Capable** This field is not used by PCIe.	RO	0b
4	**Capabilities List** Indicates the presence of an Extended Capability list item. All PCI Express device functions are required to implement the PCI Express Capability structure.	RO	1b
3	**Interrupt Status** When set, this indicates that an INTx emulation interrupt is pending internally in the function.	RO	0b
2:1	**RESERVED**	RO	—

Note 1: This device does not support immediate readiness.

TABLE 6: STATUS SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
0	**Immediate Readiness** When set, this indicates the function is guaranteed to be ready to successfully complete valid configuration access at any time following any reset that the host is capable of issuing configuration requests to this function. (See **Note 1**.)	RO	0b

Note 1: This device does not support immediate readiness.

2.1.5 REVISION ID

Offset: 008h
Size: 8 bits

This register identifies the device revision. See Table 7.

TABLE 7: REVISION ID SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Revision ID** This field identifies the device revision. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	(**Note 1**)

Note 1: The value will track the device revision.
For the initial revision of the device (mask set A0), this value defaults to 00h.
For silicon version mask set B0, this value defaults to 10h.
For silicon version mask set B1, this value defaults to 11h.

2.1.6 CLASS CODE

Offset: 009h
Size: 24 bits

This register identifies the function class and sub-class. See Table 8.

TABLE 8: CLASS CODE SPECIFICATIONS

Bit	Description	Type	Default
23:16	**Base Class Code** This field classifies the function as a Network Controller. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	02h
15:8	**Sub-Class Code** This field classifies the function as an Ethernet Controller. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	00h
7:0	**Programming Interface** There are no register-level programming interfaces defined. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	00h

2.1.7 CACHE LINE SIZE

Offset: 00Ch
Size: 8 bits

This register indicates system cache line size. This field is implemented as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior. See Table 9.

TABLE 9: CACHE LINE SIZE SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Cache Line Size** This field indicates system cache line size. This field is implemented as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.	R/W	00h

2.1.8 MASTER LATENCY TIMER

Offset: 00Dh
Size: 8 bits

This register does not apply to PCIe. See Table 10.

TABLE 10: MASTER LATENCY TIMER SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Latency Timer** This field is not used by PCIe.	RO	00h

2.1.9 HEADER TYPE

Offset: 00Eh
Size: 8 bits

This register identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and whether or not the device contains multiple functions. See Table 11.

TABLE 11: HEADER TYPE SPECIFICATIONS

Bit	Description	Type	Default
7	**Multi-Function Device** This field indicates that the device is a single function. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY **Note 1**)	0b
6:0	**Header Type** These bits identify the layout of the second part of the predefined header. The encoding 00h specifies the layout shown in Table 2.	RO	0000000b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.10 BIST

Offset: 00Fh
Size: 8 bits

This register is used for control and status of BIST. See Table 12.

TABLE 12: BIST SPECIFICATIONS

Bit	Description	Type	Default
7	**BIST NOT Supported** This field indicates that the device does not support BIST.	RO	0b
6	**Invoke BIST** This field is not used by this device.	RO	0b
5:4	**RESERVED**	RO	—
3:0	**BIST Status** This field is not used by this device.	RO	0000b

2.1.11 BASE ADDRESS 0

Offset: 010h
Size: 32 bits

This register identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and whether or not the device contains multiple functions. See Table 13.

TABLE 13: BASE ADDRESS 0 SPECIFICATIONS

Bit	Description	Type	Default
31:13	**Base Address[31:13]** These bits specify the middle bits of the starting address.	R/W	00000h
12:4	**Base Address[12:4]** These bits specify the lower bits of the starting address.	RO	000h
3	**Prefetchable** This field indicates if the memory space allocated can be prefetchable.	RO (DBI – W)	0b
2:1	**Memory Type** This field indicates the function uses 64 bit addressing.	RO (DBI – W **Note 1**)	10b
0	**Memory or I/O** This field specifies the function uses memory mapped space.	RO (DBI – W **Note 1**)	0b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.12 BASE ADDRESS 1

Offset: 014h
Size: 32 bits

This register along with Base Address 0 specifies the system starting address for the Control and Status registers. See Table 14.

TABLE 14: BASE ADDRESS 1 SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Base Address[63:31]** These bits specify the upper bits of the starting address.	R/W	00000000h

2.1.13 BASE ADDRESS 2

Offset: 018h
Size: 32 bits

This register along with Base Address 3 specifies the system starting address for the MSI-X Table. The MSI-X Table occupies 256 bytes of memory mapped space as indicated by the RO bits in the Base Address[7:4] field. See Table 15.

TABLE 15: BASE ADDRESS 2 SPECIFICATIONS

Bit	Description	Type	Default
31:8	**Base Address[31:8]** These bits specify the middle bits of the starting address.	R/W	000000h
7:4	**Base Address[7:4]** These bits specify the lower bits of the starting address.	RO	0h
3	**Prefetchable** This field indicates if the memory space allocated can be prefetchable.	RO (DBI – W)	0b
2:1	**Memory Type** This field indicates the function uses 64 bit addressing.	RO (DBI – W **Note 1**)	10b
0	**Memory or I/O** This field specifies the function uses memory mapped space.	RO (DBI – W **Note 1**)	0b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.14 BASE ADDRESS 3

Offset: 01Ch
Size: 32 bits

This register along with Base Address 2 specifies the system starting address for the MSI-X Table. See Table 16.

TABLE 16: BASE ADDRESS 3 SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Base Address[63:31]** These bits specify the upper bits of the starting address.	R/W	00000000h

2.1.15 BASE ADDRESS 4

Offset: 020h
Size: 32 bits

This register along with Base Address 5 specifies the system starting address for the MSI-X PBA. The MSI-X PBA occupies 256 bytes of memory mapped space as indicated by the RO bits in the Base Address[7:4] field. See Table 17.

TABLE 17: BASE ADDRESS 4 SPECIFICATIONS

Bit	Description	Type	Default
31:8	**Base Address[31:8]** These bits specify the middle bits of the starting address.	R/W	000000h
7:4	**Base Address[7:4]** These bits specify the lower bits of the starting address.	RO	0h
3	**Prefetchable** This field indicates if the memory space allocated can be prefetchable.	RO (DBI – W)	0b
2:1	**Memory Type** This field indicates that the function uses 64-bit addressing.	RO (DBI – W **Note 1**)	10b
0	**Memory or I/O** This field specifies the function uses memory mapped space.	RO (DBI – W **Note 1**)	0b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.16 BASE ADDRESS 5

Offset: 024h
Size: 32 bits

This register along with Base Address 4 specifies the system starting address for the MSI-X PBA. See Table 18.

TABLE 18: BASE ADDRESS 5 SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Base Address[63:31]** These bits specify the upper bits of the starting address.	R/W	00000000h

2.1.17 CARDBUS CIS POINTER

Offset: 028h
Size: 32 bits

This register is not used by this device. See Table 19.

TABLE 19: CARDBUS CIS POINTER SPECIFICATIONS

Bit	Description	Type	Default
31:0	**CardBus CIS Pointer** This field is not used by this device. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY **Note 1**)	00000000h

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.18 SUBSYSTEM VENDOR ID

Offset: 02Ch
Size: 16 bits

This register identifies the manufacturer of the add-in card or subsystem. See Table 20.

TABLE 20: SUBSYSTEM VENDOR ID SPECIFICATIONS

Bit	Description	Type	Default
15:0	**Subsystem Vendor ID** This field identifies the manufacturer of the add-in card or subsystem. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	1055h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.1.19 SUBSYSTEM ID

Offset: 02Eh
Size: 16 bits

This register identifies the particular device of the add-in card or subsystem. See Table 21.

TABLE 21: SUBSYSTEM ID SPECIFICATIONS

Bit	Description	Type	Default
15:0	**Subsystem ID** This field identifies the particular device of the add-in card or subsystem. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	7430h 7431h 743Fh (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.1.20 EXPANSION ROM BASE ADDRESS

Offset: 030h
Size: 32 bits

This register is not used by this device. See Table 22.

TABLE 22: EXPANSION ROM BASE ADDRESS SPECIFICATIONS

Bit	Description	Type	Default
31:11	**Address** This field is not used by this device.	RO	000000h
10:1	**RESERVED**	RO	—
0	**Enable** This field is not used by this device.	RO	0b

2.1.21 CAPABILITIES POINTER

Offset: 034h
Size: 8 bits

This register points to the linked list of capabilities implemented by this device. See Table 23.

TABLE 23: CAPABILITIES POINTER SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Capabilities Pointer** This field points to the linked list of capabilities implemented by this device. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	40h

2.1.22 INTERRUPT LINE

Offset: 03Ch
Size: 8 bits

The Interrupt Line register is an 8-bit register used to communicate interrupt line routing information. Values in this register are programmed by system software and are system architecture specific. The function itself does not use this value, rather the value in this register is used by device drivers and operating systems. See Table 24.

TABLE 24: INTERRUPT LINE SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Interrupt Line** This field is used to communicate interrupt line routing information.	R/W	FFh

2.1.23 INTERRUPT PIN

Offset: 03Dh
Size: 8 bits

This register identifies the legacy interrupt message the function uses.

The function itself does not use this value, rather the value in this register is used by device drivers and operating systems. See Table 25.

TABLE 25: INTERRUPT PIN SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Interrupt Pin** This field identifies the legacy interrupt message the function uses	RO (DBI – W **Note 1**)	01h

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.1.24 MIN_GNT

Offset: 03Eh
Size: 8 bits

This register does not apply to PCIe. See Table 26.

TABLE 26: MIN_GNT SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Min_Gnt** This field is not used by PCIe.	RO	00h

2.1.25 MAX_LAT

Offset: 040h
Size: 8 bits

This register does not apply to PCIe. See Table 27.

TABLE 27: MAX_LAT SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Max_Lat** This field is not used by PCIe.	RO	00h

2.2 Power Management Capability

2.2.1 CAPABILITY ID FOR PM

Offset: 040h
Size: 8 bits

This register indicates that the data structure currently being pointed to is the PCI Power Management data structure. See Table 28.

TABLE 28: CAPABILITY ID FOR PM SPECIFICATIONS

Bit	Description	Type	Default
7:0	**PM Capability ID** This field identifies the linked list item as being the PCI Power Management registers.	RO	01h

2.2.2 NEXT CAPABILITY POINTER FOR PM

Offset: 041h
Size: 8 bits

This register describes the location of the next item in the function's capability list. See Table 29.

TABLE 29: NEXT CAPABILITY POINTER FOR PM SPECIFICATIONS

Bit	Description	Type	Default
7:0	**PM Next Pointer** This field provides an offset into Configuration Space pointing to the location of next item in the function's capability list.	RO (DBI – W)	50h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Section 4.1.5, EEPROM User Initialization Table.) in order to bypass any of the capability structures that follow.
Valid values are:
050h (MSI Capability – default)
070h (PCI Express Capability)
0B0h (MSI-X Capability)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.

2.2.3 POWER MANAGEMENT CAPABILITIES

Offset: 042h
Size: 16 bits

This register provides information on the capabilities of the function related to power management. See Table 30.

TABLE 30: POWER MANAGEMENT CAPABILITIES SPECIFICATIONS

Bit	Description	Type	Default
15:11	**PME_Support** This field indicates the power states in which the function may generate a PME. A value of 0b for any bit indicates that the function is not capable of signaling PME while in that power state. bit(11) X XXX1b – PME can be signaled from D0. bit(12) X XX1Xb – PME can be signaled from D1. bit(13) X X1XXb – PME can be signaled from D2. bit(14) X 1XXXb – PME can be signaled from D3hot. bit(15) 1 XXXXb – PME can be signaled from D3cold. (See **Note 5** and **Note 6**.)	RO (DBI – W)	**Note 1**

Note 1: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 19h. When VAUX_DET is low, the default is 09h.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

3: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 111b. When VAUX_DET is low, the default is 000b.

4: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

5: Even if overwritten to a 1, bit 15 will always read back as a 0 when VAUX_DET is low.

6: Even if overwritten to a 1, bits 12 and 13 will always read back as a 0 if D1_Support or D2_Support, respectively, is low.

7: Based on the contents of the OTP or EEPROM, the EEPROM Loader could set the upper bit of the PME_-Support field to 0 and illegally set this field to a non-zero value.

TABLE 30: POWER MANAGEMENT CAPABILITIES SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
10	**D2_Support** This field indicates if the function supports the D2 Power Management State. 0 – No support 1 – Supported	RO (DBI – W, **Note 4**)	0b
9	**D1_Support** This field indicates if the function supports the D1 Power Management State 0 – No support 1 – Supported	RO (DBI – W, **Note 4**)	0b
8:6	**Aux_Current** This field reports the 3.3V auxiliary current requirements for the PCI function. When the device does not support PME generation from D3cold (as indicated by the upper bit of the PME_Support field), this field should contain a value of “000b” when read. Otherwise the following encodings are used: 111 – 375 mA 110 – 320 mA 101 – 270 mA 100 – 220 mA 011 – 160 mA 010 – 100 mA 001 – 55 mA 000 – 0 (self powered) (See **Note 7**.)	RO (DBI – W)	**Note 3** **Note 4**
5	**DSI** This field indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A “1” indicates that the function requires a device-specific initialization sequence following transition to the D0 uninitialized state.	RO (DBI – W)	1b
4	**Immediate Readiness on Return to D0** This field indicates whether the function is immediately ready when it returns to D0 from D3hot.	RO (DBI – W)	1b (**Note 1**)
3	**PME Clock** This field is not used by PCIe.	RO	0b

Note 1: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 19h. When VAUX_DET is low, the default is 09h.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

3: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 111b. When VAUX_DET is low, the default is 000b.

4: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

5: Even if overwritten to a 1, bit 15 will always read back as a 0 when VAUX_DET is low.

6: Even if overwritten to a 1, bits 12 and 13 will always read back as a 0 if D1_Support or D2_Support, respectively, is low.

7: Based on the contents of the OTP or EEPROM, the EEPROM Loader could set the upper bit of the PME_-Support field to 0 and illegally set this field to a non-zero value.

TABLE 30: POWER MANAGEMENT CAPABILITIES SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
2:0	**Version** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.	RO (DBI – W)	011b

Note 1: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 19h. When VAUX_DET is low, the default is 09h.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

3: The default depends upon the value of the VAUX_DET pin. When VAUX_DET is high, the default is 111b. When VAUX_DET is low, the default is 000b.

4: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

5: Even if overwritten to a 1, bit 15 will always read back as a 0 when VAUX_DET is low.

6: Even if overwritten to a 1, bits 12 and 13 will always read back as a 0 if D1_Support or D2_Support, respectively, is low.

7: Based on the contents of the OTP or EEPROM, the EEPROM Loader could set the upper bit of the PME_-Support field to 0 and illegally set this field to a non-zero value.

2.2.4 POWER MANAGEMENT CONTROL/STATUS

Offset: 044h
Size: 16 bits

This register is used to manage the PCI function's power management state as well as to enable/monitor PMEs. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will be cleared. See Table 31.

TABLE 31: POWER MANAGEMENT CONTROL/STATUS SPECIFICATIONS

Bit	Description	Type	Default
15	**PME_Status** This field is set when the function would normally assert the PME signaling independent of the state of the PME_En bit. When this device is consuming auxiliary power (VAUX_DET pin is high), then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. This field is "Sticky" in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/STKY	0b (Indeterminate at time of initial operating system boot if function supports PME from D3cold.)
14:13	**Data_Scale** This field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field. This device does not support the use of the Data register.	RO	00b

Note 1: Although this field is writable via the DBI, it is not recommended to use this method.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

3: If software attempts to write an unsupported, optional state to this field, the write operation completes normally on the bus. However, the data is discarded and no state change occurs.

TABLE 31: POWER MANAGEMENT CONTROL/STATUS SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
12:9	**Data_Select** This field is used to select which data is to be reported through the Data register and Data_Scale field. This device does not support the use of the Data register.	RO	0h
8	**PME_En** This field enables the function to assert a PME. When “0”, PME assertion is disabled. When this device is consuming auxiliary power (VAUX_DET pin is high), then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b (Indeterminate at time of initial operating system boot if function supports PME from D3cold.)
7:4	**RESERVED**	RO	—
3	**No_Soft_Reset** When set, this field indicates that the device transitioning from D3hot to D0 because of PowerState commands does not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (“0”), the device does perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this field, the device transitioning from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only the PME context preserved.	RO (DBI – W **Note 1**)	1b (**Note 2**)
2	**RESERVED**	RO	—
1:0	**PowerState** This field is used to both determine the current power state of the function and set the function into a new power state. The definition of the field values is given below. 00 – D0 01 – D1 – not supported 10 – D2 – not supported 11 – D3hot (See **Note 3**.)	R/W	00b

Note 1: Although this field is writable via the DBI, it is not recommended to use this method.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

3: If software attempts to write an unsupported, optional state to this field, the write operation completes normally on the bus. However, the data is discarded and no state change occurs.

2.2.5 BRIDGE SUPPORT EXTENSIONS

Offset: 046h
Size: 8 bits

This register is used to support PCI bridge specific functionality. It is not used by this device. See Table 32.

TABLE 32: BRIDGE SUPPORT EXTENSIONS SPECIFICATIONS

Bit	Description	Type	Default
7	**Bus Power/Clock Control Enable** This field indicates that the bus power/clock control mechanism is enabled.	RO	0b
6	**B2/B3 support for D3hot** This field determines the action that is to occur as a direct result of programming the function to D3hot.	RO	0b
5:0	**RESERVED**	RO	—

2.2.6 DATA

Offset: 047h
Size: 8 bits

This register provides a mechanism for the function to report state-dependent operating data. It is not implemented by this device. See Table 33.

TABLE 33: DATA SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Data** This field reports the state-dependent data requested by the Data_Select field. The value of this register is scaled by the value reported by the Data_Scale field.	RO	00h

2.3 MSI Capability

2.3.1 CAPABILITY ID FOR MSI

Offset: 050h
Size: 8 bits

This register indicates that the data structure currently being pointed to is the MSI data structure. See Table 34.

TABLE 34: CAPABILITY ID FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
7:0	**MSI Capability ID** This field identifies the linked list item as being MSI.	RO	05h

2.3.2 NEXT POINTER FOR MSI

Offset: 051h
Size: 8 bits

This register describes the location of the next item in the function's capability list. See Table 35.

TABLE 35: NEXT POINTER FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
7:0	**MSI Next Pointer** This field provides an offset into Configuration Space pointing to the location of next item in the function's capability list.	RO (DBI – W)	70h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
070h (PCI Express Capability – default)
0B0h (MSI-X Capability)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.

2.3.3 MESSAGE CONTROL FOR MSI

Offset: 052h
Size: 16 bits

This register describes the location of the next item in the function's capability list. See Table 36.

TABLE 36: MESSAGE CONTROL FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**MSI Per-vector Masking Capable** This field indicates the function supports MSI per-vector masking.	RO	1b
7	**MSI 64 Bit Address Capable** This field indicates the function is capable of sending a 64-bit message address. If this field is cleared or if the Message Upper Address for MSI is zero, 32-bit format messages are used. Otherwise, 64-bit format messages are used.	RO (DBI – W)	1b
6:4	**MSI Multiple Message Enable** This field is use to indicate the number of allocated vectors. 000 – 1 001 – 2 010 – 4 011 – 8 100 – 16 101 – 32 110 – Reserved 111 – Reserved This device supports up to 8 vectors.	R/W	000b

TABLE 36: MESSAGE CONTROL FOR MSI SPECIFICATIONS (CONTINUED)

3:1	**MSI Multiple Message Capable** This field indicates the number of requested vectors. 000 – 1 001 – 2 010 – 4 011 – 8 100 – 16 101 – 32 110 – Reserved 111 – Reserved This device supports up to 8 vectors. Settings above this value may cause untoward operation and may yield unpredictable results.	RO (DBI – W)	011b (**Note 1**)
0	**MSI Enable** This field is used to enable MSI. If 1 and the MSI-X Enable bit in the Message Control for MSI-X register is 0, the function is permitted to use MSI to request service and is prohibited from using its INTx# pin. System configuration software sets this field to enable MSI. A device driver is prohibited from writing this field to mask a function's service request. If 0, the function is prohibited from using MSI to request service.	R/W	0b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2.3.4 MESSAGE LOWER ADDRESS FOR MSI

Offset: 054h
Size: 32 bits

This register provides the lower bits of the system memory address for the MSI memory write transaction. See Table 37.

TABLE 37: MESSAGE LOWER ADDRESS FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
31:2	**Message Address** This field specifies the lower bits of the DWORD-aligned address (AD[31:02]) for the MSI memory write transaction.	R/W	00000000h
1:0	**RESERVED**	RO	—

2.3.5 MESSAGE UPPER ADDRESS FOR MSI

Offset: 058h
Size: 32 bits

This register provides the lower bits of the system memory address for the MSI memory write transaction. See Table 38.

TABLE 38: MESSAGE UPPER ADDRESS FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Message Address** This field specifies the upper bits of the DWORD-aligned address (AD[63:32]) for the MSI memory write transaction. If this field is zero or if the MSI 64 Bit Address Capable is cleared, 32-bit format messages are used. Otherwise, 64-bit format messages are used.	R/W	00000000h

2.3.6 MESSAGE DATA FOR MSI

Offset: 05Ch
Size: 16 bits

This register provides the data bits for the MSI memory write transaction. See Table 39.

TABLE 39: MESSAGE DATA FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
15:0	**Message Data** This field specifies the data bits for the MSI memory write transaction. The MSI Multiple Message Enable field defines the number of low order message data bits the function may modify to generate its system software allocated vectors.	R/W	0000h

2.3.7 MASK BITS FOR MSI

Offset: 060Ch
Size: 32 bits

This register provides the vector mask bits. See Table 40.

TABLE 40: MASK BITS FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**Mask Bits** This field specifies the vector mask bits. (See **Note 1** and **Note 2**.)	R/W	00h

Note 1: All 8 bits remain R/W even if the The MSI Multiple Message Enable field is set to a value lower than 8.
2: This field is not affected by the state of the MSI Enable field in the Message Control for MSI register.

2.3.8 PENDING BITS FOR MSI

Offset: 064Ch
Size: 32 bits

This register provides the vector pending bits. See Table 41.

TABLE 41: PENDING BITS FOR MSI SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**Pending Bits** This field specifies the vector pending bits. (See **Note 1**.)	RO	00h

Note 1: This field is cleared if the MSI Enable field in the Message Control for MSI register is cleared.

2.4 PCI Express Capability

2.4.1 CAPABILITY ID FOR PCIE

Offset: 070h
Size: 8 bits

This register indicates that the data structure currently being pointed to is the PCIe data structure. See Table 42.

TABLE 42: CAPABILITY ID FOR PCIE SPECIFICATIONS

Bit	Description	Type	Default
7:0	**PCIe Capability ID** This field identifies the linked list item as being PCIe.	RO	10h

2.4.2 NEXT POINTER FOR PCIE

Offset: 071h
Size: 8 bits

This register describes the location of the next item in the function's capability list. See Table 43.

TABLE 43: NEXT POINTER FOR PCIE SPECIFICATIONS

Bit	Description	Type	Default
7:0	**PCIe Next Pointer** This field provides an offset into Configuration Space pointing to the location of next item in the function's capability list.	RO (DBI – W)	B0h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
0B0h (MSI-X Capability – default)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.

2.4.3 PCI EXPRESS CAPABILITIES

Offset: 072h
Size: 16 bits

See Table 44.

TABLE 44: PCI EXPRESS CAPABILITIES SPECIFICATIONS

Bit	Description	Type	Default
15	**RESERVED**	RO	—
14	**Undefined** In previous versions of the PCIe specification, this field was used to indicate support for TCS Routing. System software should ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b
13:9	**Interrupt Message Number** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base message data and the interrupt message that is generated. Hardware is required to update this field, so that it is correct if the number of MSI messages assigned to the function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X table entry is used to generate the interrupt message. For a given MSI-X implementation, the entry must remain constant. (See **Note 1**.)	RO (DBI – W)	00000b
8	**Slot Implemented** This field indicates that the link associated with this port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This device does not support slot options.	RO (DBI – W **Note 1**)	0b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its defaullt.

TABLE 44: PCI EXPRESS CAPABILITIES SPECIFICATIONS (CONTINUED)

7:4	**Device/Port Type** This field indicates the specific type of this PCI Express function. 0000b – PCI Express Endpoint 0001b – Legacy PCI Express Endpoint 1001b – Root Complex Integrated Endpoint 1010b – Root Complex Event Collector	RO	0h
3:0	**Capability Version** This field indicates PCI-SIG defined PCI Express Capability structure version number.	RO	2h

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its defaullt.

2.4.4 DEVICE CAPABILITIES

Offset: 074h
Size: 32 bits

See Table 45.

TABLE 45: DEVICE CAPABILITIES

Bit	Description	Type	Default
31:29	**RESERVED**	RO	—
28	**Function Level Reset Capability** A value of 1b indicates that this function supports the Function Level Reset mechanism	RO (DBI – W)	1b
27:26	**Captured Slot Power Limit Scale** This field specifies the scale used for the Slot Power Limit Value.	RO	00b
25:18	**Captured Slot Power Limit Value** In combination with the Captured Slot Power Limit Scale value, this specifies the upper limit on power available to the device.	RO	00h
17:16	**RESERVED**	RO	—
15	**Role-Based Error Reporting** This field indicates that the function implements the functionality.	RO (DBI – W)	1b
14	**Undefined** In previous versions of the PCIe specification, this field was used to indicate that a Power Indicator is implemented on the adapter and electrically controlled by the component on the adapter. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 45: DEVICE CAPABILITIES (CONTINUED)

Bit	Description	Type	Default
13	**Undefined** In previous versions of the PCIe specification, this field was used to indicate that an Attention Indicator is implemented on the adapter and electrically controlled by the component on the adapter. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b
12	**Undefined** In previous versions of the PCIe specification, this field was used to indicate that an Attention Button is implemented on the adapter and electrically controlled by the component on the adapter. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b
11:9	**Endpoint L1 Acceptable Latency** This field indicates the acceptable latency that the endpoint can withstand due to the transition from L1 state to the L0 state. 000 – Maximum of 1 µs 001 – Maximum of 2 µs 010 – Maximum of 4 µs 011 – Maximum of 8 µs 100 – Maximum of 16 µs 101 – Maximum of 32 µs 110 – Maximum of 64 µs 111 – No limit	RO (DBI – W)	101b (**Note 1**)
8:6	**Endpoint L0s Acceptable Latency** This field indicates the acceptable latency that the endpoint can withstand due to the transition from L0s state to the L0 state. 000 – Maximum of 64 ns 001 – Maximum of 128 ns 010 – Maximum of 256 ns 011 – Maximum of 512 ns 100 – Maximum of 1 µs 101 – Maximum of 2 µs 110 – Maximum of 4 µs 111 – No limit	RO (DBI – W)	011b (**Note 1**)
5	**Extended Tag Field Supported** This field indicates the maximum supported size of the Tag field as a Requester 0 – 5-bit Tag field supported 1 – 8-bit Tag field supported	RO (DBI - W **Note 2**)	0b
4:3	**Phantom Functions Supported** This field indicates the support for use of unclaimed Function Numbers. 00 – No Function Number bits are used for Phantom Functions. 01 – The most significant bit of the Function Number in Requester ID is used. 10 – The two most significant bits of Function Number are used. 11 – All 3 bits of Function Number are used.	RO (DBI - W **Note 2**)	00b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 45: DEVICE CAPABILITIES (CONTINUED)

Bit	Description	Type	Default
2:0	**Max_Payload_Size Supported** This field indicates the maximum payload size that the function can support for TLPs. 000 – 128 bytes max payload size 001 – 256 bytes max payload size 010 – 512 bytes max payload size 011 – 1024 bytes max payload size 100 – 2048 bytes max payload size 101 – 4096 bytes max payload size 110 – Reserved 111 – Reserved This device supports up to 512 bytes. Settings above this value may cause untoward operation and may yield unpredictable results.	RO (DBI - W)	010b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.4.5 DEVICE CONTROL

Offset: 07h
Size: 16 bits

See Table 46.

TABLE 46: DEVICE CONTROL SPECIFICATIONS

Bit	Description	Type	Default
15	**Initiate Function Level Reset** A write of 1b to this field initiates a Function Level Reset to the function. The value read by software from this field is always 0b.	WO	0b
14:12	**Max_Read_Request_Size** This field sets the maximum Read Request size for the function as a requester. 000 – 128 bytes maximum Read Request size 001 – 256 bytes maximum Read Request size 010 – 512 bytes maximum Read Request size 011 – 1024 bytes maximum Read Request size 100 – 2048 bytes maximum Read Request size 101 – 4096 bytes maximum Read Request size 110 – Reserved 111 – Reserved	R/W	010b
11	**Enable No Snoop** If this field is set, the function is permitted to set the No-Snoop bit in the Requester Attributes of transactions it initiates. This device does not use the No-Snoop bit.	RO	0b

TABLE 46: DEVICE CONTROL SPECIFICATIONS (CONTINUED)

10	**Aux Power PM Enable** When set, this field enables the device to draw Aux power independent of PME Aux power. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register independent of the PME_En bit in the Power Management Control/Status register. When this device is consuming auxiliary power (VAUX_DET pin is high), then this bit is sticky. When auxiliary power is not available (as indicated by the VAUX_DET pin) this bit is read only. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
9	**Phantom Functions Enable** When set, this field enables the function to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is clear, the function is not allowed to use Phantom Functions. This device does not use Phantom Functions.	RO	0b
8	**Extended Tag Field Enable** When set, this field enables the function to use an 8-bit Tag field as a Requester. If the bit is clear, the function is restricted to a 5-bit Tag field. This device does not use extended tags.	RO	0b
7:5	**Max_Payload_Size** This field sets maximum TLP payload size for the function. As a receiver, the function must handle TLPs as large as the set value. As a transmitter, the function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field in the Device Capabilities register. 000b – 128 bytes max payload size 001b – 256 bytes max payload size 010b – 512 bytes max payload size 011b – 1024 bytes max payload size 100b – 2048 bytes max payload size 101b – 4096 bytes max payload size 110b – Reserved 111b – Reserved This field is neither initialized nor modified by FLR.	R/W	000b
4	**Enable Relaxed Ordering** If this field is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering.	R/W	1b
3	**Unsupported Request Reporting Enable** This field, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error messages.	R/W	0b

TABLE 46: DEVICE CONTROL SPECIFICATIONS (CONTINUED)

2	**Fatal Error Reporting Enable** This field, in conjunction with other bits, controls sending ERR_FATAL Messages.	R/W	0b
1	**Non-Fatal Error Reporting Enable** This field, in conjunction with other bits, controls sending ERR_NONFATAL Messages.	R/W	0b
0	**Correctable Error Reporting Enable** This field, in conjunction with other bits, controls sending ERR_COR Messages.	R/W	0b

2.4.6 DEVICE STATUS

Offset: 07Ah
Size: 16 bits

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 47.

TABLE 47: DEVICE STATUS SPECIFICATIONS

Bit	Description	Type	Default
15:6	**RESERVED**	RO	—
5	**Transactions Pending** When set, this field indicates that the function has issued non-posted requests that have not been completed. The function reports this field cleared only when all outstanding non-posted requests have completed or have been terminated by the Completion Timeout mechanism. This field must is cleared upon the completion of an FLR.	RO	0b
4	**AUX Power Detected** This field indicates if Aux power is detected by the function. This bit is the live VAUX_DET pin value.	RO	0b
3	**Unsupported Request Detected** This field indicates that the function received an unsupported request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	R/W1C	0b
2	**Fatal Error Detected** This field indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.	R/W1C	0b

TABLE 47: DEVICE STATUS SPECIFICATIONS (CONTINUED)

1	**Non-Fatal Error Detected** This field indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.	R/W1C	0b
0	**Correctable Error Detected** This field indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Errors are logged in this register regardless of the settings of the Correctable Error Mask register.	R/W1C	0b

2.4.7 LINK CAPABILITIES

Offset: 07h
Size: 32 bits

See Table 48.

TABLE 48: LINK CAPABILITIES SPECIFICATIONS

Bit	Description	Type	Default
31:24	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.	RO (DBI – W **Note 3**)	00h
23	**RESERVED**	RO	—
22	**ASPM Optionality Compliance** This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this field set to 0b.	RO (DBI – W **Note 3**)	1b
21	**Link Bandwidth Notification Capability** A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This field is not applicable and is reserved for Endpoints.	RO	0b
20	**Data Link Layer Link Active Reporting Capable** For upstream ports, this field must be hardwired to 0b.	RO	0b
19	**Surprise Down Error Reporting Capable** For upstream ports, this field must be hardwired to 0b.	RO	0b

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

3: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 48: LINK CAPABILITIES SPECIFICATIONS (CONTINUED)

18	**Clock Power Management** A value of 1b in this field indicates that the device tolerates the removal of any reference clock(s) via the “clock request” (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the device does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	(**Note 1**, **Note 3**)
17:15	**L1 Exit Latency** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from ASPM L1 to L0. 000 – Less than 1 µs 001 – 1 µs to less than 2 µs 010 – 2 µs to less than 4 µs 011 – 4 µs to less than 8 µs 100 – 8 µs to less than 16 µs 101 – 16 µs to less than 32 µs 110 – 32 µs to 64 µs 111 – More than 64 µs	RO (DBI – W)	011b (**Note 2**)
14:12	**L0s Exit Latency** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from L0s to L0. 000 – Less than 64 ns 001 – 64 ns to less than 128 ns 010 – 128 ns to less than 256 ns 011 – 256 ns to less than 512 ns 100 – 512 ns to less than 1 µs 101 – 1 µs to less than 2 µs 110 – 2 µs to 4 µs 111 – More than 4 µs	RO (DBI – W)	100b (**Note 2**)
11:10	**Active State Power Management (ASPM) Support** This field indicates the level of ASPM supported on the given PCI Express Link.	RO (DBI – W)	11b

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

3: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 48: LINK CAPABILITIES SPECIFICATIONS (CONTINUED)

9:4	**Maximum Link Width** This field indicates the maximum Link width (xN – corresponding to N Lanes) implemented by the device. 000000 – Reserved 000001 – x1 000010 – x2 000100 – x4 001000 – x8 001100 – x12 010000 – x16 100000 – x32	RO (DBI – W Note 3)	000001b
3:0	**Max Link Speed** This field indicates the maximum Link speed of the device. The encoded value specifies a bit location in the Supported Link Speeds Vector in the Link Capabilities 2 register that corresponds to the maximum Link speed. 0001 – Supported Link Speeds Vector field bit 0 0010 – Supported Link Speeds Vector field bit 1 0011 – Supported Link Speeds Vector field bit 2 0100 – Supported Link Speeds Vector field bit 3 0101 – Supported Link Speeds Vector field bit 4 0110 – Supported Link Speeds Vector field bit 5 0111 – Supported Link Speeds Vector field bit 6	RO (DBI – W Note 3)	1h
31:24	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.	RO (DBI – W Note 3)	00h
23	**RESERVED**	RO	—
22	**ASPM Optionality Compliance** This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this field set to 0b.	RO (DBI – W Note 3)	1b
21	**Link Bandwidth Notification Capability** A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This field is not applicable and is reserved for endpoints.	RO	0b
20	**Data Link Layer Link Active Reporting Capable** For upstream ports, this field must be hardwired to 0b.	RO	0b
19	**Surprise Down Error Reporting Capable** For upstream ports, this field must be hardwired to 0b.	RO	0b

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

3: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 48: LINK CAPABILITIES SPECIFICATIONS (CONTINUED)

18	**Clock Power Management** A value of 1b in this field indicates that the device tolerates the removal of any reference clock(s) via the “clock request” (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the device does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	(**Note 1**, **Note 2**)
17:15	**L1 Exit Latency** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from ASPM L1 to L0. 000 – Less than 1 µs 001 – 1 µs to less than 2 µs 010 – 2 µs to less than 4 µs 011 – 4 µs to less than 8 µs 100 – 8 µs to less than 16 µs 101 – 16 µs to less than 32 µs 110 – 32 µs to 64 µs 111 – More than 64 µs	RO (DBI – W)	011b (**Note 2**)
14:12	**L0s Exit Latency** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from L0s to L0. 000 – Less than 64 ns 001 – 64 ns to less than 128 ns 010 – 128 ns to less than 256 ns 011 – 256 ns to less than 512 ns 100 – 512 ns to less than 1 µs 101 – 1 µs to less than 2 µs 110 – 2 µs to 4 µs 111 – More than 4 µs	RO (DBI – W)	100b (**Note 2**)
11:10	**Active State Power Management (ASPM) Support** This field indicates the level of ASPM supported on the given PCI Express Link.	RO (DBI – W)	11b

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

3: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

TABLE 48: LINK CAPABILITIES SPECIFICATIONS (CONTINUED)

9:4	**Maximum Link Width** This field indicates the maximum Link width (xN – corresponding to N Lanes) implemented by the device. 000000 – Reserved 000001 – x1 000010 – x2 000100 – x4 001000 – x8 001100 – x12 010000 – x16 100000 – x32	RO (DBI – W, **Note 3**)	000001b
3:0	**Max Link Speed** This field indicates the maximum Link speed of the device. The encoded value specifies a bit location in the Supported Link Speeds Vector in the Link Capabilities 2 register that corresponds to the maximum Link speed. 0001 – Supported Link Speeds Vector field bit 0 0010 – Supported Link Speeds Vector field bit 1 0011 – Supported Link Speeds Vector field bit 2 0100 – Supported Link Speeds Vector field bit 3 0101 – Supported Link Speeds Vector field bit 4 0110 – Supported Link Speeds Vector field bit 5 0111 – Supported Link Speeds Vector field bit 6	RO (DBI – W, **Note 3**)	1h

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

3: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.4.8 LINK STATUS

Offset: 07h
Size: 8 bits

See Table 49.

TABLE 49: LINK STATUS SPECIFICATIONS

Bit	Description	Type	Default
15	**Link Autonomous Bandwidth Status** This field is not applicable and is reserved for endpoints.	RO	0b
14	**Link Bandwidth Management Status** This field is not applicable and is reserved for endpoints.	RO	0b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

TABLE 49: LINK STATUS SPECIFICATIONS (CONTINUED)

13	**Data Link Layer Link Active** This field indicates the status of the data link control and management state machine. This device does not implement the data link layer link active reporting.	RO	0b
12	**Slot Clock Configuration** This field indicates that the device uses the same physical reference clock that the platform provides.	RO (DBI – W)	1b (Note 1)
11	**Link Training** This field is not applicable and is reserved for endpoints.	RO	0b
10	**Undefined** The value read from this field is undefined. In previous versions of this specification, this field was used to indicate a link training error. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b
9:4	**Negotiated Link Width** This field indicates the negotiated width of the given PCI Express Link. 000001 – x1 000010 – x2 000100 – x4 001000 – x8 001100 – x12 010000 – x16 100000 – x32	RO	000001b
3:0	**Current Link Speed** This field indicates the negotiated link speed of the given PCI Express link. The encoded value specifies a bit location in the Supported Link Speeds Vector in the Link Capabilities 2 that corresponds to the current Link speed. 0001 – Supported Link Speeds Vector field bit 0 0010 – Supported Link Speeds Vector field bit 1 0011 – Supported Link Speeds Vector field bit 2 0100 – Supported Link Speeds Vector field bit 3 0101 – Supported Link Speeds Vector field bit 4 0110 – Supported Link Speeds Vector field bit 5 0111 – Supported Link Speeds Vector field bit 6	RO	1h

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2.4.9 DEVICE CAPABILITIES 2

Offset: 094h
Size: 32 bits

See Table 50.

TABLE 50: DEVICE CAPABILITIES 2 SPECIFICATIONS

Bit	Description	Type	Default
31	**FRS Supported** When set, indicates support for the Function Readiness Status (FRS) capability. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	1b
30:24	**RESERVED**	RO	—
23:22	**Max End-End TLP Prefixes** Indicates the maximum number of End-End TLP Prefixes supported by this function. This device does not support End-End TLP Prefixes.	RO	00b
21	**End-End TLP Prefix Supported** Indicates whether End-End TLP Prefix support is offered by a function. 0 – No Support 1 – Support is provided to receive TLPs containing End-End TLP Prefixes.	RO	0b
20	**Extended Fmt Field Supported** If set, the function supports the 3-bit definition of the Fmt field. If clear, the function supports a 2-bit definition of the Fmt field.	RO	0b
19:18	**OBFF Supported** This field indicates if OBFF is supported and, if so, what signaling mechanism is used. 00 – OBFF Not Supported 01 – OBFF supported using Message signaling only 10 – OBFF supported using WAKE# signaling only 11 – OBFF supported using WAKE# and Message signaling This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	11b (**Note 1**)
17:16	**RESERVED**	RO	—
15:14	**LN System CLS** This field is not applicable and is reserved for endpoints.	RO	00b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

TABLE 50: DEVICE CAPABILITIES 2 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
13:12	**TPH Completer Supported** Value indicates Completer support for TPH or Extended TPH. 00 – TPH and Extended TPH Completer not supported 01 – TPH Completer supported; Extended TPH Completer not supported 10 – Reserved 11 – Both TPH and Extended TPH Completer supported	RO	00b
11	**LTR Mechanism Supported** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/STKY)	1b (Note 1)
10	**No RO-enabled PR-PR Passing** This field applies only for Switches and RCs that support peer-to-peer traffic between Root Ports.	RO	0b
9	**128-bit CAS Completer Supported** This device does not support this capability.	RO	0b
8	**64-bit AtomicOp Completer Supported** This device does not support this capability.	RO	0b
7	**32-bit AtomicOp Completer Supported** This device does not support this capability.	RO	0b
6	**AtomicOp Routing Supported** This device does not support this capability.	RO	0b
5	**ARI Forwarding Supported** This field is not applicable and reserved for endpoints.	RO	0b
4	**Completion Timeout Disable Supported** A value of 1b indicates support for the Completion Timeout Disable mechanism.	RO	1b

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

TABLE 50: DEVICE CAPABILITIES 2 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
3:0	**Completion Timeout Ranges Supported** This field indicates device function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. Four time value ranges are defined: Range A: 50 µs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000 – Completion Timeout programming not supported – the function must implement a timeout value in the range 50 µs to 50 ms. 0001 – Range A 0010 – Range B 0011 – Ranges A and B 0110 – Ranges B and C 0111 – Ranges A, B, and C 1110 – Ranges B, C, and D 1111 – Ranges A, B, C, and D All other values are reserved.	RO	Fh

Note 1: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2.4.10 DEVICE CONTROL 2

Offset: 098h
Size: 16 bits

See Table 51.

TABLE 51: DEVICE CONTROL 2 SPECIFICATIONS

Bit	Description	Type	Default
15	**End-End TLP Prefix Blocking** This field is not applicable and Reserved for Endpoints.	RO	0b
14:13	**OBFF Enable** This field enables the OBFF mechanism and selects the signaling method. 00 – Disabled 01 – Enabled using Message signaling [Variation A] 10 – Enabled using Message signaling [Variation B] 11 – Enabled using WAKE# signaling	R/W	00b
12:11	**RESERVED**	RO	—
10	**LTR Mechanism Enable** When set to 1b, this field enables Upstream Ports to send LTR messages and Downstream Ports to process LTR messages.	R/W (**Note 1**)	0b
9	**IDO Completion Enable** If this field is set, the function is permitted to set the ID-Based Ordering (IDO) bit (Attr[2]) of Completions it returns. This device does not set the IDO attribute in completions.	RO	0b
8	**IDO Request Enable** If this field is set, the function is permitted to set the ID-Based Ordering (IDO) bit (Attr[2]) of Requests it initiates. This device does not set the IDO attribute in requests.	RO	0b
7	**AtomicOp Egress Blocking** This field is not applicable and reserved for endpoints.	RO	0b
6	**AtomicOp Requester Enable** The function is allowed to initiate AtomicOp requests only if this field and the Bus Master field in the Command register are both set. This device does not initiate AtomicOp requests.	RO	0b
5	**ARI Forwarding Enable** This field is not applicable and is reserved for endpoints.	RO	0b

Note 1: This field is Read Only if the LTR Mechanism Supported field in Device Capabilities 2 is cleared.

TABLE 51: DEVICE CONTROL 2 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
4	**Completion Timeout Disable** When set, this field disables the Completion Timeout mechanism. Software is permitted to set or clear this field at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this field was cleared or the time each request was issued.	R/W	0b
3:0	**Completion Timeout Value** This field allows system software to modify the Completion Timeout value. 0000 – Default range: 50 µs to 50 ms Values available if Range A (50 µs to 10 ms) programmability range is supported: 0001 – 50 µs to 100 µs 0010 – 1 ms to 10 ms Values available if Range - (10 ms to 250 ms) programmability range is supported: 0101 – 16 ms to 55 ms 0110 – 65 ms to 210 ms Values available if Range C (250 ms to 4s) programmability range is supported: 1001 – 260 ms to 900 ms 1010 – 1 s to 3.5 s Values available if the Range D (4s to 64s) programmability range is supported: 1101 – 4 s to 13 s 1110 – 17 s to 64 s Values not defined above are reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.	R/W	0b

Note 1: This field is Read Only if the LTR Mechanism Supported field in Device Capabilities 2 is cleared.

2.4.11 DEVICE STATUS 2

Offset: 098h
Size: 16 bits

See Table 52.

TABLE 52: DEVICE STATUS 2 SPECIFICATIONS

Bit	Description	Type	Default
15:0	**RESERVED**	RO	—

2.4.12 LINK CAPABILITIES 2

Offset: 09Ch
Size: 32 bits

See Table 53.

TABLE 53: LINK CAPABILITIES 2 SPECIFICATIONS

Bit	Description	Type	Default
31	**DRS Supported** When set, indicates support for the optional Device Readiness Status (DRS) capability. This field is neither initialized nor modified by FLR.	RO (DBI – W)	1b
30:23	**RESERVED**	RO	—
22:16	**Lower SKP OS Reception Supported Speeds Vector** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP This device does not support the SRIS or receiving SKP OS.	RO	0b
15:9	**Lower SKP OS Generation Supported Speeds Vector** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and the software control of the SKP Ordered Set transmission scheduling rate. Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP This device does not support the SRIS or transmitting SKP OS.	RO	0b
8	**Crosslink Supported** When set to 1b, this field indicates that the associated Port supports crosslinks. When set to 0b, this field provides no information regarding the Port's level of crosslink support.	RO	0b

TABLE 53: LINK CAPABILITIES 2 SPECIFICATIONS (CONTINUED)

7:1	**Supported Link Speeds Vector** This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported. Otherwise, the Link speed is not supported. Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 Rsvd	RO	01h
0	**RESERVED**	RO	—

2.4.13 LINK CONTROL 2

Offset: 0A0h
Size: 16 bits

See Table 54.

TABLE 54: LINK CONTROL 2 SPECIFICATIONS

Bit	Description	Type	Default
15:12	**Compliance Preset/De-emphasis** When the Link is operating at 2.5 GT/s, the setting of this field has no effect. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0000b
11	**Compliance SOS** When set to 1b, the LTSSM is required to send SKP ordered sets between sequences when sending the compliance pattern or modified compliance pattern. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
10	**Enter Modified Compliance** When this field is set to 1b, the device transmits modified compliance pattern if the LTSSM enters Polling Compliance substate. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
9:7	**Transmit Margin** This field controls the value of the non-de-emphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling Configuration substate. 000 – Normal operating range 001 – 111b This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	000b

TABLE 54: LINK CONTROL 2 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
6	**Selectable De-emphasis** This field is not applicable and is reserved for Endpoints.	RO	0b
5	**Hardware Autonomous Speed Disable** When set, this field disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this field. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
4	**Enter Compliance** Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this field to 1b in both components on a Link and then initiating a hot reset on the Link. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
3:0	**Target Link Speed** This field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into Compliance mode. The encoded value specifies a bit location in the Supported Link Speeds Vector in the Link Capabilities 2 that corresponds to the current Link speed. 0001 – Supported Link Speeds Vector field bit 0 0010 – Supported Link Speeds Vector field bit 1 0011 – Supported Link Speeds Vector field bit 2 0100 – Supported Link Speeds Vector field bit 3 0101 – Supported Link Speeds Vector field bit 4 0110 – Supported Link Speeds Vector field bit 5 0111 – Supported Link Speeds Vector field bit 6 All other encodings are reserved. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1h

2.4.14 LINK STATUS 2

Offset: 0A2h
Size: 16 bits

See Table 55.

TABLE 55: LINK STATUS 2 SPECIFICATIONS

Bit	Description	Type	Default
15	**DRS Message Received** This field is not applicable and is reserved for endpoints.	RO	0b

TABLE 55: LINK STATUS 2 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
14:12	**Downstream Component Presence** This field is not applicable and is reserved for endpoints.	RO	000b
11:6	**RESERVED**	RO	—
5	**Link Equalization Request** This field is set by hardware to request the link equalization process to be performed on the link. This device does not support link equalization.	RO	0b
4	**Equalization Phase 3 Successful** When set to 1b, this field indicates that the Phase 3 of the transmitter equalization procedure has been successfully completed. This device does not support transmitter equalization.	RO	0b
3	**Equalization Phase 2 Successful** When set to 1b, this field indicates that the Phase 2 of the transmitter equalization procedure has been successfully completed. This device does not support transmitter equalization.	RO	0b
2	**Equalization Phase 1 Successful** When set to 1b, this field indicates that the Phase 1 of the transmitter equalization procedure has been successfully completed. This device does not support transmitter equalization.	RO	0b
1	**Equalization Complete** When set to 1b, this field indicates that the transmitter equalization procedure has been completed. This device does not support transmitter equalization.	RO	0b
0	**Current De-emphasis Level** The value in this field is undefined when the link is not operating at 5.0 GT/s speed.	RO	1b

2.5 MSI-X Capability

2.5.1 CAPABILITY ID FOR MSI-X

Offset: 0B0h
Size: 8 bits

This register indicates that the data structure currently being pointed to is the MSI-X data structure. See Table 56.

TABLE 56: CAPABILITY ID FOR MSI-X SPECIFICATIONS

Bit	Description	Type	Default
7:0	**MSI-X Capability ID** This field identifies the linked list item as being MSI-X.	RO	11h

2.5.2 NEXT POINTER FOR MSI-X

Offset: 0B1h
Size: 8 bits

This register describes the location of the next item in the function's capability list. See Table 57.

TABLE 57: NEXT POINTER FOR MSI-X SPECIFICATIONS

Bit	Description	Type	Default
7:0	**MSI-X Next Pointer** This field provides an offset into configuration space pointing to the location of next item in the function's capability list.	RO (DBI – W)	00h

2.5.3 MESSAGE CONTROL FOR MSI-X

Offset: 0B2h
Size: 16 bits

This register provides system software control over MSI-X. See Table 58.

TABLE 58: MESSAGE CONTROL FOR MSI-X SPECIFICATIONS

Bit	Description	Type	Default
15	**MSI-X Enable** This field is used to enable MSI-X. If 1 and the MSI Enable bit in the Message Control for MSI is 0, the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin. System configuration software sets this field to enable MSI-X. A device driver is prohibited from writing this field to mask a function's service request. If 0, the function is prohibited from using MSI-X to request service.	R/W	0b
14	**MSI-X Function Mask** If 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits.	R/W	0b
13:11	**RESERVED**	RO	—
10:0	**MSI-X Table Size** System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of "00000000011" indicates a table size of 4. The maximum table size supported (N) is 8.	RO (DBI – W)	007h (**Note 1**)

Note 1: The lower 3 bits of this field are loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2.5.4 TABLE OFFSET/BIR FOR MSI-X

Offset: 0B4h
Size: 32 bits

This register indicates the BAR used for the MSI-X Table. See Table 59.

TABLE 59: TABLE OFFSET/BIR FOR MSI-X SPECIFICATIONS

Bit	Description	Type	Default
31:3	**Table Offset** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.	RO (DBI – W **Note 1**)	00000000h
2:0	**Table BIR** Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, and is used to map the function's MSI-X Table into Memory Space. 0 – 10h 1 – 14h 2 – 18h 3 – 1Ch 4 – 20h 5 – 24h 6 – Reserved 7 – Reserved For a 64-bit Base Address register, the Table BIR indicates the lower DWORD.	RO (DBI –W **Note 1**)	010b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.5.5 MSI-X TABLE STRUCTURE

Memory Space Address: Bar 2 and 3
Size: 256 bytes

These registers contain the MSI-X Table structure. These registers total 256 bytes (128 bytes used, 128 bytes reserved) and adhere to the format of the MSI-X Table defined in the PCIe specification. See Table 60.

Note: When the MSI-X Table Size field is set to indicate less than 8 entries, the table entries corresponding to the removed vectors become reserved.

TABLE 60: MSI-X TABLE STRUCTURE SPECIFICATIONS

Table BYTE Offset	DWORD 3	DWORD 2	DWORD 1	DWORD 0
00h	Vector Control 0	Msg Data 0	Msg Uppr Addr 0	Msg Addr 0
10h	Vector Control 1	Msg Data 1	Msg Uppr Addr 1	Msg Addr 1
20h	Vector Control 2	Msg Data 2	Msg Uppr Addr 2	Msg Addr 2
30h	Vector Control 3	Msg Data 3	Msg Uppr Addr 3	Msg Addr 3

TABLE 60: MSI-X TABLE STRUCTURE SPECIFICATIONS (CONTINUED)

Table BYTE Offset	DWORD 3	DWORD 2	DWORD 1	DWORD 0
40h	Vector Control 4	Msg Data 4	Msg Uppr Addr 4	Msg Addr 4
50h	Vector Control 5	Msg Data 5	Msg Uppr Addr 5	Msg Addr 5
60h	Vector Control 6	Msg Data 6	Msg Uppr Addr 6	Msg Addr 6
70h	Vector Control 7	Msg Data 7	Msg Uppr Addr 7	Msg Addr 7
80h-FFh	Reserved			

2.5.6 MESSAGE ADDRESS FOR MSI-X TABLE ENTRIES

TABLE 61: MESSAGE ADDRESS FOR MSI-X TABLE ENTRIES SPECIFICATIONS

Bit	Description	Type	Default
31:2	**Message Address** System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the lower portion of the DWORD-aligned address for the memory write transaction	R/W	00000000h
2:0	**Message Address** For proper DWORD alignment, software must always write zeros to these two bits.	R/W	00b

2.5.7 MESSAGE UPPER ADDRESS FOR MSI-X TABLE ENTRIES

TABLE 62: MESSAGE UPPER ADDRESS FOR MSI-X TABLE ENTRIES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Message Upper Address** System-specified message upper address bits. If this field is zero, 32-bit format messages are used. If this field is non-zero, 64-bit format messages are used.	R/W	00000000h

2.5.8 **MESSAGE DATA FOR MSI-X TABLE ENTRIES**

TABLE 63: MESSAGE DATA FOR MSI-X TABLE ENTRIES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Message Data** System-specified message data. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the data during the memory write transaction. In contrast to message data used for MSI messages, the low-order message data bits in MSI-X messages are not modified by the function.	R/W	00000000h

2.5.9 VECTOR CONTROL FOR MSI-X TABLE ENTRIES

TABLE 64: VECTOR CONTROL FOR MSI-X TABLE ENTRIES SPECIFICATIONS

Bit	Description	Type	Default
31:1	**RESERVED** For potential future use, software must preserve the value of these reserved bits when modifying the value of other Vector Control bits.	RO	—
0	**Mask Bit** When this field is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. (See **Note 1**.)	R/W	1b

Note 1: This field is not affected by the state of the MSI-X Enable field in the Message Control for MSI-X register.

2.5.10 PBA OFFSET/BIR FOR MSI-X

Offset: 0B8h
Size: 32 bits

This register indicates the BAR used for the MSI-X PBA. See Table 65.

TABLE 65: PBA OFFSET/BIR FOR MSI-X SPECIFICATIONS

Bit	Description	Type	Default
31:3	**PBA Offset** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.	RO (DBI – W, **Note 1**)	00000000h
2:0	**PBA BIR** Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, and is used to map the function's MSI-X PBA into Memory Space. 0 – 10h 1 – 14h 2 – 18h 3 – 1Ch 4 – 20h 5 – 24h 6 – Reserved 7 – Reserved For a 64-bit Base Address register, the PBA BIR indicates the lower DWORD.	RO (DBI – W, **Note 1**)	100b

Note 1: Although this field is writable via the DBI, it is not recommended that this be changed from its default.

2.5.11 MSI-X PBA STRUCTURE

Memory Space Address: Bar 4 and 5
Size: 256 bytes

These registers contain the MSI-X PBA structure. These registers total 256 bytes (1 bytes used, 255 bytes reserved) and adhere to the format of the MSI-X PBA defined in the PCIe specification. (See Table 66.)

Note: The reserved locations may be read or written. Reads will return "unknown" data and writes are ignored.

TABLE 66: MSI-X PBA STRUCTURE SPECIFICATIONS

Table BYTE Offset	BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0
00h	Reserved							Pending Bits
10h – FFh	Reserved							

2.5.12 PENDING BITS FOR MSI-X PBA ENTRIES

TABLE 67: PENDING BITS FOR MSI-X PBA ENTRIES SPECIFICATIONS

Bit	Description	Type	Default
7:0	**Pending Bits** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Software should never write and should only read Pending Bits. (See **Note 1**.)	RO	00h

Note 1: This field is cleared if the MSI-X Enable field in the Message Control for MSI-X register is cleared.

2.6 Advanced Error Reporting Capability

2.6.1 ADVANCED ERROR REPORTING EXTENDED CAPABILITY HEADER

Offset: 100h
Size: 32 bits
This register contains the extended capability header for AER. See Table 68.

TABLE 68: ADVANCED ERROR REPORTING EXTENDED CAPABILITY HEADER SPECIFICATIONS

Bit	Description	Type	Default
31:20	**AER Next Capability Offset** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and is always either 000h (for terminating list of Capabilities) or greater than 0FFh. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	148h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow. Valid values are:

- 148h (Device Serial Number Capability – default)
- 158h (Latency Tolerance Reporting (LTR) Capability)
- 160h (L1 PM Substates Extended Capability)
- 170h (Reliability, Availability, and Serviceability (RAS) Debug, Error Injection, and Statistics (DES) Capability)
- 000h (End of list)
- The default is used in the absence of a programmed OTP or EEPROM.
- Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

TABLE 68: ADVANCED ERROR REPORTING EXTENDED CAPABILITY HEADER SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
19:16	**AER Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	2h
15:0	**AER PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the Extended Capability ID for the Advanced Error Reporting Capability. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	0001h

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow. Valid values are:

- 148h (Device Serial Number Capability – default)
- 158h (Latency Tolerance Reporting (LTR) Capability)
- 160h (L1 PM Substates Extended Capability)
- 170h (Reliability, Availability, and Serviceability (RAS) Debug, Error Injection, and Statistics (DES) Capability)
- 000h (End of list)
- The default is used in the absence of a programmed OTP or EEPROM.
- Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.6.2 UNCORRECTABLE ERROR STATUS

Offset: 104h
Size: 32 bits

This register indicates error detection status of individual errors on a PCI Express device function. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 69.

TABLE 69: UNCORRECTABLE ERROR STATUS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—
26	**Poisoned TLP Egress Blocked Status** This field is not applicable and Reserved for Endpoints.	RO	0b
25	**TLP Prefix Blocked Error Status** This field is not used.	RO	0b
24	**AtomicOp Egress Blocked Status** This field is not applicable and Reserved for Endpoints.	RO	0b
23	**MC Blocked TLP Status** This field is not used.	RO	0b

TABLE 69: UNCORRECTABLE ERROR STATUS (CONTINUED)

Bit	Description	Type	Default
22	**Uncorrectable Internal Error Status** This field is not used.	RO	0b
21	**ACS Violation Status** This field is not used.	RO	0b
20	**Unsupported Request Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
19	**ECRC Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
18	**Malformed TLP Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
17	**Receiver Overflow Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
16	**Unexpected Completion Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
15	**Completer Abort Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
14	**Completion Timeout Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
13	**Flow Control Protocol Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
12	**Poisoned TLP Received Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
11:6	**RESERVED**	RO	—
5	**Surprise Down Error Status** This field is not used for upstream ports.	RO	0b
4	**Data Link Protocol Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
3:1	**RESERVED**	RO	—

TABLE 69: UNCORRECTABLE ERROR STATUS (CONTINUED)

Bit	Description	Type	Default
0	**Undefined** The value read from this field is undefined. In previous versions of this specification, this field was used to indicate a Link Training Error. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b

2.6.3 UNCORRECTABLE ERROR MASK

Offset: 108h
Size: 32 bits

This register controls reporting of individual errors by the device function to the PCI Express Root Complex via a PCI Express error Message.

A masked error (respective bit set in the mask register) is not recorded or reported in the Header Log, TLP Prefix Log or First Error Pointer, and is not reported to the PCI Express Root Complex by this function.

There is a mask bit per error bit of the Uncorrectable Error Status register. See Table 70.

TABLE 70: UNCORRECTABLE ERROR MASK SPECIFICATIONS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—
26	**Poisoned TLP Egress Blocked Mask** This field is not applicable and Reserved for Endpoints.	RO	0b
25	**TLP Prefix Blocked Error Mask** This field is not used.	RO	0b
24	**AtomicOp Egress Blocked Mask** This field is not applicable and Reserved for Endpoints.	RO	0b
23	**MC Blocked TLP Mask** This field is not used.	RO	0b
22	**Uncorrectable Internal Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
21	**ACS Violation Mask** This field is not used.	RO	0b
20	**Unsupported Request Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
19	**ECRC Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
18	**Malformed TLP Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b

TABLE 70: UNCORRECTABLE ERROR MASK SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
17	**Receiver Overflow Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
16	**Unexpected Completion Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
15	**Completer Abort Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
14	**Completion Timeout Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
13	**Flow Control Protocol Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
12	**Poisoned TLP Received Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
11:6	**RESERVED**	RO	—
5	**Surprise Down Error Mask** This field is not used for upstream ports.	RO	0b
4	**Data Link Protocol Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
3:1	**RESERVED**	RO	—
0	**Undefined** The value read from this field is undefined. In previous versions of this specification, this field was used to mask a Link Training error. System software must ignore the value read from this field. System software must only write a value of 1b to this field.	RO	0b

2.6.4 UNCORRECTABLE ERROR SEVERITY

Offset: 10Ch
Size: 32 bits

This register controls whether an individual error is reported as a non-fatal or fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is clear, the corresponding error is considered non-fatal. See Table 71.

TABLE 71: UNCORRECTABLE ERROR SEVERITY SPECIFICATIONS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—

TABLE 71: UNCORRECTABLE ERROR SEVERITY SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
26	**Poisoned TLP Egress Blocked Severity** This field is not applicable and is reserved for endpoints.	RO	0b
25	**TLP Prefix Blocked Error Severity** This field is not used.	RO	0b
24	**AtomicOp Egress Blocked Severity** This field is not applicable and reserved for endpoints.	RO	0b
23	**MC Blocked TLP Severity** This field is not used.	RO	0b
22	**Uncorrectable Internal Error Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
21	**ACS Violation Severity** This field is not used.	RO	0b
20	**Unsupported Request Error Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
19	**ECRC Error Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
18	**Malformed TLP Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
17	**Receiver Overflow Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
16	**Unexpected Completion Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
15	**Completer Abort Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
14	**Completion Timeout Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
13	**Flow Control Protocol Error Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
12	**Poisoned TLP Received Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b

TABLE 71: UNCORRECTABLE ERROR SEVERITY SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
11:6	**RESERVED**	RO	—
5	**Surprise Down Error Severity** This field is not used for upstream ports.	RO	1b
4	**Data Link Protocol Error Severity** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
3:1	**RESERVED**	RO	—
0	**Undefined** The value read from this field is undefined. In previous versions of this specification, this field was used to set the severity of a Link Training error. System software must ignore the value read from this field. System software is permitted to write any value to this field.	RO	0b

2.6.5 CORRECTABLE ERROR STATUS

Offset: 110h
Size: 32 bits

This register reports error status of individual correctable error sources on a PCI Express device function. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 72.

TABLE 72: CORRECTABLE ERROR STATUS SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15	**Header Log Overflow Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
14	**Corrected Internal Error Status** This field is not used.	RO	0b
13	**Advisory Non-Fatal Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
12	**Replay Timer Timeout Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
11:9	**RESERVED**	RO	—
8	**REPLAY_NUM Rollover Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b

TABLE 72: CORRECTABLE ERROR STATUS SPECIFICATIONS **(CONTINUED)**

Bit	Description	Type	Default
7	**Bad DLLP Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
6	**Bad TLP Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b
5:1	**RESERVED**	RO	—
0	**Receiver Error Status** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W1C/ STKY	0b

2.6.6 CORRECTABLE ERROR MASK

Offset: 114h
Size: 32 bits

This register controls reporting of individual correctable errors by this function to the PCI Express Root Complex via a PCI Express error message. A masked error (respective bit set in the mask register) is not reported to the PCI Express Root Complex by this function. There is a mask bit per error bit in the Correctable Error Status register. See Table 73.

TABLE 73: CORRECTABLE ERROR MASK SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15	**Header Log Overflow Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
14	**Corrected Internal Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
13	**Advisory Non-Fatal Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	1b
12	**Replay Timer Timeout Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
11:9	**RESERVED**	RO	—
8	**REPLAY_NUM Rollover Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
7	**Bad DLLP Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b

TABLE 73: CORRECTABLE ERROR MASK SPECIFICATIONS **(CONTINUED)**

Bit	Description	Type	Default
6	**Bad TLP Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
5:1	**RESERVED**	RO	—
0	**Receiver Error Mask** This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b

2.6.7 ADVANCED ERROR CAPABILITIES AND CONTROL

Offset: 118h
Size: 32 bits

See Table 74.

TABLE 74: ADVANCED ERROR CAPABILITIES AND CONTROL SPECIFICATIONS

Bit	Description	Type	Default
31:13	**RESERVED**	RO	—
12	**Completion Timeout Prefix/Header Log Capable** If set, this bit indicates that the function records the prefix/header of Request TLPs that experience a Completion Timeout error.	RO	0b
11	**TLP Prefix Log Present** If set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.	RO	0b
10	**Multiple Header Recording Enable** When set, this bit enables the function to record more than one error header.	RO	0b
9	**Multiple Header Recording Capable** If set, this bit indicates that the function is capable of recording more than one error header.	RO	0b
8	**ECRC Check Enable** When set, ECRC checking is enabled. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
7	**ECRC Check Capable** If set, this bit indicates that the function is capable of checking ECRC.	RO	1b
6	**ECRC Generation Enable** When set, ECRC generation is enabled. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	R/W/STKY	0b
5	**ECRC Generation Capable** If set, this bit indicates that the function is capable of generating ECRC.	RO	1b
4:0	**First Error Pointer** The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO/STKY	00000b

2.6.8 HEADER LOG

Offset: 11Ch – 128h
Size: 16 bytes

These registers contain the header for the TLP corresponding to a detected error. These registers total 16 bytes and adhere to the format of the headers defined in the PCIe specification.

The header is captured such that, when read using DW access, the fields of the header are laid out in the same way the headers are presented in the PCIe specification. Therefore, byte 0 of the header is located in byte 3 of the Header Log register, byte 1 of the header is in byte 2 of the Header Log register and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log register are used and values in bytes 12 through 15 are undefined. See Table 75 and Table 76.

TABLE 75: HEADER LOG SPECIFICATIONS 1

Table DWORD Offset	31:24	23:16	15:8	7:0
0h	Header Byte 0	Header Byte 1	Header Byte 2	Header Byte 3
1h	Header Byte 4	Header Byte 5	Header Byte 6	Header Byte 7
2h	Header Byte 8	Header Byte 9	Header Byte 10	Header Byte 11
3h	Header Byte 12	Header Byte 13	Header Byte 14	Header Byte 15

TABLE 76: HEADER LOG SPECIFICATIONS 2

Bit	Description	Type	Default
127:0	**Header of TLP associated with error** This header log fields are “Sticky” in that they are neither initialized nor modified by hot reset or FLR.	RO/STKY	0

2.7 Device Serial Number Capability

2.7.1 DEVICE SERIAL NUMBER EXTENDED CAPABILITY HEADER

Offset: 148h
Size: 32 bits

This register contains the extended capability header for Device Serial Number. See Table 77.

TABLE 77: DEVICE SERIAL NUMBER EXTENDED CAPABILITY HEADER SPECIFICATIONS

Bit	Description	Type	Default
31:20	**SN Next Capability Offset** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and is always either 000h (for terminating list of Capabilities) or greater than 0FFh. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	158h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
158h (Latency Tolerance Reporting (LTR) Capability - default)
160h (L1 PM Substates Extended Capability)
170h (Miscellaneous Registers)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.
Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

TABLE 77: DEVICE SERIAL NUMBER EXTENDED CAPABILITY HEADER SPECIFICATIONS

Bit	Description	Type	Default
19:16	**SN Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	1h
15:0	**SN PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the Extended Capability ID for the Device Serial Number Capability. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	0003h

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
158h (Latency Tolerance Reporting (LTR) Capability - default)
160h (L1 PM Substates Extended Capability)
170h (Miscellaneous Registers)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.
Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.7.2 SERIAL NUMBER

Offset: 4Ch – 150h
Size: 2 bytes

The Serial Number register is a 64-bit field that contains the IEEE defined 64-bit extended unique identifier (EUI-64™). See Table 78.

TABLE 78: SERIAL NUMBER REGISTER

Table DWORD Offset	31:0
0h	Serial Number 1st DWORD
1h	Serial Number 2nd DWORD

TABLE 79: SERIAL NUMBER SPECIFICATIONS

Bit	Description	Type	Default
63:0	**PCI Express Device Serial Number** This field contains the IEEE defined 64-bit extended unique identifier (EUI-64™). This identifier includes a 24-bit company id value assigned by IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer.	RO (DBI – W)	00000000 00000000h (**Note 1**)

Note 1: The serial number is derived from the MAC address from OTP or EEPROM and may be overridden from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) The default is used in the absence of a programmed OTP or EEPROM.

The serial number is derived from the MAC address as shown in Table 80.

TABLE 80: SERIAL NUMBERS 1

	Company ID			Extension ID				
S/N	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
MAC address	7:0	15:8	23:16	FFh	FFh	31:24	39:32	47:40

For example if the MAC address is 00:80:0F (SMSC/Microchip) and the extension identifier is 12:34:56, the company IDs and the Extension IDs will be the ones in Table 81.

TABLE 81: SERIAL NUMBERS 2

	Company ID			Extension ID				
S/N	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
MAC address	00h	80h	0Fh	FFh	FFh	12h	34h	56h

Note 1: Although this register and the MAC Receive Address High register (RX_ADDRH) and MAC Receive Address Low register (RX_ADDRL) are derived from the same OTP / EEPROM fields, these registers are independently maintained. A change to one does not cause a change to the others.

2.8 Latency Tolerance Reporting (LTR) Capability

2.8.1 LTR EXTENDED CAPABILITY HEADER

Offset: 158h
Size: 32 bits

This register contains the extended capability header for LTR. See Table 82.

TABLE 82: LTR EXTENDED CAPABILITY HEADER SPECIFICATIONS

Bit	Description	Type	Default
31:20	**LTR Next Capability Offset** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and is always either 000h (for terminating list of Capabilities) or greater than 0FFh. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	160h (**Note 1**)

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
160h (L1 PM Substates Extended Capability – default)
170h (Reliability, Availability, and Serviceability (RAS) Debug, Error Injection, and Statistics (DES) Capability)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.
Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

TABLE 82: LTR EXTENDED CAPABILITY HEADER SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
19:16	**LTR Capability Version** This field is a PCI-SIG-defined version number that indicates the version of the Capability structure present. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	1h
15:0	**LTR PCI Express Extended Capability ID** This field is a PCI-SIG-defined ID number that indicates the Extended Capability ID for the LTR Capability. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	0018h

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
160h (L1 PM Substates Extended Capability – default)
170h (Reliability, Availability, and Serviceability (RAS) Debug, Error Injection, and Statistics (DES) Capability)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.
Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.8.2 MAX SNOOP LATENCY

Offset: 15Ch
Size: 16 bits

See Table 83.

TABLE 83: MAX SNOOP LATENCY SPECIFICATIONS

Bit	Description	Type	Default
15:13	**RESERVED**	RO	—
12:10	**Max Snoop Latency Scale** This field provides a scale for the value contained within the Max Snoop LatencyValue field. 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns	R/W	000b
9:0	**Max Snoop LatencyValue** Along with the Max Snoop Latency Scale field, this register specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform’s maximum supported latency or less.	R/W	000h

2.8.3 MAX NO-SNOOP LATENCY

Offset: 15Eh
Size: 16 bits

See Table 84.

TABLE 84: MAX NO-SNOOP LATENCY SPECIFICATIONS

Bit	Description	Type	Default
15:13	**RESERVED**	RO	—
12:10	**Max No-Snoop LatencyScale** This field provides a scale for the value contained within the Max No-Snoop LatencyValue field. 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns	R/W	000b
9:0	**Max No-Snoop LatencyValue** Along with the Max No-Snoop LatencyScale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less.	R/W	000h

2.9 L1 PM Substates Extended Capability

2.9.1 L1 PM SUBSTATES EXTENDED CAPABILITY HEADER

Offset: 160h
Size: 32 bits

This register contains the extended capability header for L1 PM Substates. See Table 85.

TABLE 85: L1 PM SUBSTATES EXTENDED CAPABILITY HEADER SPECIFICATIONS

Bit	Description	Type	Default
31:20	**L1 PM Next Capability Offset** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and is always either 000h (for terminating list of Capabilities) or greater than 0FFh. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	170h (**Note 1**)
19:16	**L1 PM Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	1h
15:0	**L1 PM PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the Extended Capability ID for the L1 PM Substates Capability. This field is “Sticky” in that it is neither initialized nor modified by hot reset or FLR.	RO (DBI – W/ STKY)	001Eh

Note 1: This field may be loaded from OTP or EEPROM using the method described in EEPROM User Initialization Table (See Table 112.) in order to bypass any of the Capability structures that follow.
Valid values are:
160h (L1 PM Substates Extended Capability – default)
170h (Reliability, Availability, and Serviceability (RAS) Debug, Error Injection, and Statistics (DES) Capability)
000h (End of list)
The default is used in the absence of a programmed OTP or EEPROM.
Although marked as STKY, this field will be reprogrammed from the OTP or EEPROM contents (if enabled within the OTP/EEPROM contents) upon a hot reset or FLR.

2.9.1.1 L1 PM Substates Capabilities

Offset: 164h
Size: 32 bits

See Table 86.

TABLE 86: L1 PM SUBSTATES CAPABILITIES SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RESERVED**	RO	—
23:19	**Port T_POWER_ON Value** Along with the Port T_POWER_ON Scale field sets the time (in µs) that this port requires the port on the opposite side of the link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This field is neither initialized nor modified by FLR.	RO (DBI – W)	00101b **Section 2.9.2, L1 PM Substates Control 1**
18	**RESERVED**	RO	—
17:16	**Port T_POWER_ON Scale** Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. 00 – 2 µs 01 – 10 µs 10 – 100 µs 11 – Reserved This field is neither initialized nor modified by FLR.	RO (DBI – W)	00b (**Note 2**)
15:8	**Port Common_Mode_Restore_Time** Time (in µs) required for this Port to re-establish common mode. This field is neither initialized nor modified by FLR.	RO (DBI – W)	0Ah (**Note 2**)
7:5	**RESERVED**	RO	—
4	**L1 PM Substates Supported** When set, this field indicates that this port supports L1 PM Substates. This field is neither initialized nor modified by FLR.	RO (DBI – W)	(**Note 1**) (**Note 2**)
3	**ASPM L1.1 Supported** When set, this field indicates that ASPM L1.1 is supported. This field is neither initialized nor modified by FLR.	RO (DBI – W)	(**Note 1**) (**Note 2**)
2	**ASPM L1.2 Supported** When set, this field indicates that ASPM L1.2 is supported. This field is neither initialized nor modified by FLR.	RO (DBI – W)	(**Note 1**) (**Note 2**)

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

TABLE 86: L1 PM SUBSTATES CAPABILITIES SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
1	**PCI-PM L1.1 Supported** When set, this field indicates that PCI-PM L1.1 is supported. This field is neither initialized nor modified by FLR.	RO (DBI – W)	(**Note 1**) (**Note 2**)
0	**PCI-PM L1.2 Supported** When set this field indicates that PCI-PM L1.2 is supported. This field is neither initialized nor modified by FLR.	RO (DBI – W)	(**Note 1**) (**Note 2**)

Note 1: This field is loaded from the inverse of the ADV_PM_DISABLE strap.

2: This field may be loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM.

2.9.2 L1 PM SUBSTATES CONTROL 1

Offset: 168h
Size: 32 bits

See Table 87.

TABLE 87: L1 PM SUBSTATES CONTROL 1 SPECIFICATIONS

Bit	Description	Type	Default
31:29	**LTR_L1.2_THRESHOLD_Scale** This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns Software must only modify this field when the ASPM L1.2 Enable field is clear. This field is neither initialized nor modified by FLR.	R/W	000b
28:26	**RESERVED**	RO	—
25:16	**LTR_L1.2_THRESHOLD_Value** Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). Software must only modify this field when the ASPM L1.2 Enable field is clear. This field is neither initialized nor modified by FLR.	R/W	000h
15:8	**Common_Mode_Restore_Time** Reserved for upstream ports.	RO	00h
7:4	**RESERVED**	RO	—

TABLE 87: L1 PM SUBSTATES CONTROL 1 SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
3	**ASPM L1.1 Enable** When set, this field enables ASPM L1.1. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is set. This field is neither initialized nor modified by FLR.	R/W	0b
2	**ASPM L1.2 Enable** When set, this field enables ASPM L1.2. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities register is set. This field is neither initialized nor modified by FLR.	R/W	0b
1	**PCI-PM L1.1 Enable** When set, this field enables PCI-PM L1.1. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities register is set. This field is neither initialized nor modified by FLR.	R/W	0b
0	**PCI-PM L1.2 Enable** When set, this field enables PCI-PM L1.2. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities register is set. This field is neither initialized nor modified by FLR.	R/W	0b

2.9.2.1 L1 PM Substates Control 2

Offset: 16Ch
Size: 32 bits
See Table 88.

TABLE 88: L1 PM SUBSTATES CONTROL 2 SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:3	**T_POWER_ON Value** Along with the T_POWER_ON Scale, this sets the minimum amount of time (in µs) that the port must wait in L1.2. Exit after sampling CLKREQ# asserted before actively driving the interface. Software must only modify this field when both the ASPM L1.2 Enable and PCI-PM L1.2 Enable fields are clear. This field is neither initialized nor modified by FLR.	R/W	00101b
2	**RESERVED**	RO	—
1:0	**T_POWER_ON Scale** This specifies the scale used for T_POWER_ON Value. 00 – 2 µs 01 – 10 µs 10 – 100 µs 11 – Reserved Software must only modify this field when both the ASPM L1.2 Enable and PCI-PM L1.2 Enable fields are clear. This field is neither initialized nor modified by FLR.	R/W	00b

3.0 MISCELLANEOUS REGISTERS

3.1 Miscellaneous System Configuration and Status Registers

This section details the remainder of the directly addressable System CSR's. Within the device, these registers start at offset 0008h and end at offset 009Fh (See Table 89.). This range is for exclusive use of the Miscellaneous registers. For an overview of the entire device register map, refer to Section 1.0, Register Map.

TABLE 89: MISCELLANEOUS REGISTER MAP

Byte Offset	Register Name (Symbol)
0008h	VLAN Type Register (VLAN_TYPE)
0018h	Ethernet PHY LED Mode Select Register
001Ch	Ethernet PHY LED Behavior Register
0050h	General Purpose IO Configuration 0 Register (GPIO_CFG0)
0054h	General Purpose IO Configuration 1 Register (GPIO_CFG1)
0058h	General Purpose IO Configuration 2 Register (GPIO_CFG2)
005Ch	General Purpose IO Configuration 3 Register (GPIO_CFG3)
0060h	General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
0064h	General Purpose IO Interrupt Status Register (GPIO_INT_STS)
0068h	General Purpose IO Interrupt Enable Set Register (GPIO_INT_EN_SET)
006Ch	General Purpose IO Interrupt Enable Clear Register (GPIO_INT_EN_CLR)
0070h	Software General Purpose Registers x (SW_GPx)
0074h	Software General Purpose Registers x (SW_GPx) (x=1)
0078h	Software General Purpose Registers x (SW_GPx) (x=2)
007Ch	Reserved
0080h	Latency Tolerance Reporting Control Register (LTR_CTRL)
0084h	Latency Tolerance Reporting High Value Register (LTR_HIGH_VALUE)
0088h	Latency Tolerance Reporting Low Value Register (LTR_LOW_VALUE)
008Ch	General Purpose Timer Configuration Register (GPT_CFG)
0090h	General Purpose Timer Count Register (GPT_CNT)
0094h-009Fh	Reserved

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

3.1.1 VLAN TYPE REGISTER (VLAN_TYPE)

Offset: 0008h
Size: 32 bits

This register extends the Ethernet type used to indicate the presence of a VLAN tag, in the RFE and 1588 modules, in addition to 8100h. In the FCT this is the value used for the Ethernet type when VLAN tag insertion is enabled.

The intention of this register is to allow for a proprietary VLAN type to be supported. If only the standard VLAN type of 8100h is desired to be supported, then this register should retain its default value of 8100h. See Table 90.

TABLE 90: VLAN TYPE REGISTER (VLAN_TYPE) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—

TABLE 90: VLAN TYPE REGISTER (VLAN_TYPE) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:0	**VLAN Ethernet Type**	R/W	8100h

3.1.2 ETHERNET PHY LED MODE SELECT REGISTER

Index in Decimal: 0018h
Size: 32 bits

This register selects the operating mode of the PHY LEDs. This register is only used in the LAN7430. See Table 91.

TABLE 91: ETHERNET PHY LED MODE SELECT REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:12	**LED3 Configuration** This field configures the LED3 pin function. (See **Note 1**.)	R/W	1000b (**Note 2**)
11:8	**LED2 Configuration** This field configures the LED2 pin function. (See **Note 1**.)	R/W	0000b (**Note 2**)
7:4	**LED1 Configuration** This field configures the LED1 pin function. (See **Note 1**.)	R/W	0010b (**Note 2**)
3:0	**LED0 Configuration** This field configures the LED0 pin function. (See **Note 1**.)	R/W	0001b (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.3 ETHERNET PHY LED BEHAVIOR REGISTER

Index in Decimal: 001Ch
Size: 32 bits

This register selects the operating parameters of the PHY LEDs. This register is only used in the LAN7430. See Table 92.

TABLE 92: ETHERNET PHY LED BEHAVIOR REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:15	**RESERVED**	RO	—
14	**LED Activity Output Select** (See **Note 1**.)	R/W	0b (**Note 2**)
13	**RESERVED**	RO	—
12	**LED Pulsing Enable** (See **Note 1**.)	R/W	0b (**Note 2**)

TABLE 92: ETHERNET PHY LED BEHAVIOR REGISTER SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
11:10	**LED Blink/Pulse-Stretch Rate** 00 = 2.5 Hz Blink Rate/400 ms pulse-stretch 01 = 5 Hz Blink Rate/200 ms pulse-stretch 10 = 10 Hz Blink Rate/100 ms pulse-stretch 11 = 20 Hz Blink Rate/50 ms pulse-stretch (See **Note 1**.)	R/W	01b (**Note 2**)
9	**RESERVED**	RO	—
8:5	**LED Pulse Stretch Enables** Configures LED3 (bit 8), LED2 (bit 7), LED1 (bit 6), LED0 (bit 5) to either pulse-stretch when 1, or blink when 0. (See **Note 1**.)	R/W	0000b (**Note 2**)
4	**RESERVED**	RO	—
3:0	**LED Combination Disables** Configures LED3 (bit 3), LED2 (bit 2), LED1 (bit 1), LED0 (bit 0) to either combine link/activity and duplex/collision when 0, or disable combination, providing link-only and duplex-only when 1. (See **Note 1**.)	R/W	0000b (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.4 GENERAL PURPOSE IO CONFIGURATION 0 REGISTER (GPIO_CFG0)

Offset: 0050h
Size: 32 bits

This register controls the GPIO direction and sets or reads the data value.

Note:	The number of available GPIOs varies by SKU but the register bits remain R/W.

In order for a GPIO to function as a wake event or interrupt source, it must be configured as an input. GPIO pins used to generate wake events must also be enabled by General Purpose IO Wake Enable and Polarity register (GPIO_WAKE). See Table 93.

TABLE 93: GENERAL PURPOSE IO CONFIGURATION 0 REGISTER (GPIO_CFG0) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:16	**GPIO Direction (GPIODIR)** (See **Note 2** and **Note 3**.)	R/W	000h (**Note 1**)

Note 1: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

2: When set, it enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.

3: This field is protected by Reset Protection (RST_PROTECT).

TABLE 93: GENERAL PURPOSE IO CONFIGURATION 0 REGISTER (GPIO_CFG0) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**GPIO Data (GPIOD)** (See **Note 2** and **Note 3**.)	R/W	000h (**Note 1**)

Note 1: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

2: When set, it enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.

3: This field is protected by Reset Protection (RST_PROTECT).

3.1.5 GENERAL PURPOSE IO CONFIGURATION 1 REGISTER (GPIO_CFG1)

Offset: 0054h
Size: 32 bits

This register enables the GPIO and sets the buffer type.

Note:	The number of available GPIOs varies by SKU but the register bits remain R/W.

In order for a GPIO to function as a wake event or interrupt source, it must be configured as an input. GPIO pins used to generate wake events must also be enabled by General Purpose IO Wake Enable and Polarity register (GPIO_WAKE). See Table 94.

TABLE 94: GENERAL PURPOSE IO CONFIGURATION 1 REGISTER (GPIO_CFG1) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:16	**GPIO Enable (GPIOEN)** When clear, the pin functions as a GPIO. (See **Note 1**.)	R/W	FFFh (**Note 2**)
15:12	**RESERVED**	RO	—
11:0	**GPIO Buffer Type (GPIOBUF)** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver. (See **Note 1**.)	R/W	000h (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.6 GENERAL PURPOSE IO CONFIGURATION 2 REGISTER (GPIO_CFG2)

Offset: 0058h
Size: 32 bits

This register sets the GPIO 1588 polarities. See Table 95.

Note:	The number of available GPIOs varies by SKU but the register bits remain R/W.

TABLE 95: GENERAL PURPOSE IO CONFIGURATION 2 REGISTER (GPIO_CFG2) SPECIFICATIONS

Bit	Description	Type	Default
31:12	**RESERVED**	RO	—
11:0	**GPIO 1588 Polarity 11-0 (GPIO_POL[11:0])** These bits set the 1588 clock event output polarity of the GPIO pins. 1588 clock events will be output active at the configured level (high/low). These bits also determine the polarity of the GPIO 1588 Timer Interrupt Clear inputs. 0 = Sets low logic level trigger on corresponding GPIO pin 1 = Sets high logic level trigger on corresponding GPIO pin (See **Note 1**.)	R/W	000h (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.7 GENERAL PURPOSE IO CONFIGURATION 3 REGISTER (GPIO_CFG3)

Offset: 005Ch
Size: 32 bits

This register enables the GPIOs as 1588 event outputs. See Table 96.

Note:	The number of available GPIOs varies by SKU but the register bits remain R/W.

TABLE 96: GENERAL PURPOSE IO CONFIGURATION 3 REGISTER (GPIO_CFG3) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

TABLE 96: GENERAL PURPOSE IO CONFIGURATION 3 REGISTER (GPIO_CFG3) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
27:16	**1588 GPIO Channel Select 11-0 (GPIO_CH_SEL[11:0])** These bits select the 1588 channel to be output on the corresponding GPIO[11:0]. 0 – Sets 1588 channel A as the output for the corresponding GPIO pin 1 – Sets 1588 channel B as the output for the corresponding GPIO pin (See **Note 1**.)	R/W	000h (**Note 2**)
15:12	**RESERVED**	RO	—
11:0	**1588 GPIO Output Enable 11-0 (1588_GPIO_OE[11:0])** These bits configure the GPIO pins to output 1588 clock compare events. 0 – Disables the output of 1588 clock compare events 1 – Enables the output of 1588 clock compare events The GPIO needs to be enabled and its direction set as an output via the General Purpose IO Configuration 1 register (GPIO_CFG1) and the General Purpose IO Configuration 0 register (GPIO_CFG0). The GPIO Buffer Type (GPIOBUF) field in the General Purpose IO Configuration 1 register (GPIO_CFG1) also applies. (See **Note 1**.)	R/W	000h (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.8 GENERAL PURPOSE IO WAKE ENABLE AND POLARITY REGISTER (GPIO_WAKE)

Offset: 0060h
Size: 32 bits

This register enables the GPIOs to function as wake events for the device when asserted. It also allows the polarity used for a wake event/interrupt to be configured. See Table 97.

Note: The number of available GPIOs varies by SKU but the register bits remain R/W.

TABLE 97: GENERAL PURPOSE IO WAKE ENABLE AND POLARITY REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

TABLE 97: GENERAL PURPOSE IO WAKE ENABLE AND POLARITY REGISTER SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
27:16	**GPIO Polarity 0-11 (GPIOPOL[11:0])** When clear, the pin functions as a GPIO. 0 = Wakeup/interrupt is triggered when GPIO is driven low. 1 = Wakeup/interrupt is triggered when GPIO is driven high. GPIOPOL0 – bit 16 GPIOPOL1 – bit 17 GPIOPOL2 – bit 18 GPIOPOL3 – bit 19 GPIOPOL4 – bit 20 GPIOPOL5 – bit 21 GPIOPOL6 – bit 22 GPIOPOL7 – bit 23 GPIOPOL8 – bit 24 GPIOPOL9 – bit 25 GPIOPOL10 – bit 26 GPIOPOL11 – bit 27 (See **Note 1**.)	R/W	00h (**Note 2**)
15:12	**RESERVED**	RO	—
11:0	**GPIO Wake 0-11 (GPIOWK[11:0])** These bits enable the GPIO interrupts (GPIO Interrupt (GPIO_INT) as wakeup events. These bits are automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. 0 = The GPIO can not wake up the device. 1 = The GPIO can trigger a wake up event. GPIOWK0 – bit 0 GPIOWK1 – bit 1 GPIOWK2 – bit 2 GPIOWK3 – bit 3 GPIOWK4 – bit 4 GPIOWK5 – bit 5 GPIOWK6 – bit 6 GPIOWK7 – bit 7 GPIOWK8 – bit 8 GPIOWK9 – bit 9 GPIOWK10 – bit 10 GPIOWK11 – bit 11 (See **Note 1**.)	R/W	00h (**Note 2**)

Note 1: This field is protected by Reset Protection (RST_PROTECT).

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3.1.9 GENERAL PURPOSE IO INTERRUPT STATUS REGISTER (GPIO_INT_STS)

Offset: 0064h
Size: 32 bits

This read/write register contains the GPIO interrupt status bits.

Writing a '1' to the corresponding bits acknowledges and clears the interrupt. Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

If the host attempts to clear a R/W1C bit within the GPIO_INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding GPIO_INT_STS bit will remain set. See Table 98.

Note 1: The number of available GPIOs varies by SKU.
2: GPIOs must not cause an interrupt status to be set when not configured as a GPIO.

TABLE 98: GENERAL PURPOSE IO INTERRUPT STATUS REGISTER (GPIO_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:12	**RESERVED**	RO	—
11:0	**GPIO Interrupt (GPIO_INT)** Interrupts are generated from the GPIOs.	R/W1C (**Note 1**)	**Note 2**

Note 1: The sources for these interrupts are level sensitive.
2: The GPIO inputs must be stable for 160 ns (4 crystal clocks) to be recognized.

3.1.10 GENERAL PURPOSE IO INTERRUPT ENABLE SET REGISTER (GPIO_INT_EN_SET)

Offset: 0068h
Size: 32 bits

This register is used to set the interrupt enables for the corresponding bits in the General Purpose IO Interrupt Status register (GPIO_INT_STS). Writing a '1' to a bit sets the corresponding enable and configures the corresponding interrupt as a source for the assertion of the GPIO interrupt. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables. See Table 99.

Note: The number of available GPIOs varies by SKU. The register bits remain R/W regardless.

TABLE 99: GENERAL PURPOSE IO INTERRUPT ENABLE SET REGISTER (GPIO_INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:12	**RESERVED**	RO	—
11:0	**GPIO Interrupt Enable Set (GPIO_INT_EN_SET)**	R/W1S	000h

3.1.11 GENERAL PURPOSE IO INTERRUPT ENABLE CLEAR REGISTER (GPIO_INT_EN_CLR)

Offset: 006Ch
Size: 32 bits

This register is used to clear the interrupt enables for the corresponding bits in the General Purpose IO Interrupt Status register (GPIO_INT_STS). Writing a '1' to a bit clears the corresponding enable. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables. See Table 100.

Note:	The number of available GPIOs varies by SKU. The register bits remain R/W regardless.

TABLE 100: GENERAL PURPOSE IO INTERRUPT ENABLE CLEAR REGISTER (GPIO_INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:12	**RESERVED**	RO	—
11:0	**GPIO Interrupt Enable Clear (GPIO_INT_EN_CLR)**	R/W1C	000h

3.1.12 SOFTWARE GENERAL PURPOSE REGISTERS X (SW_GPX)

Offset 0: 0070h
Offset 1: 0074h
Offset 2: 0078h
Offset: 32 bits

The device implements three general purpose registers for use by host software. See Table 101.

Note:	These registers are intended to be used as a message passing mechanism between the pre-boot environment and the device driver.

TABLE 101: SOFTWARE GENERAL PURPOSE REGISTERS X (SW_GPX) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Software General Purpose Register (SW_GPx)** (See **Note 1**.)	R/W	00000000h

Note 1: This field is protected by Reset Protection (RST_PROTECT).

3.1.13 LATENCY TOLERANCE REPORTING CONTROL REGISTER (LTR_CTRL)

Offset: 0080h
Size: 32 bits
See Table 102.

TABLE 102: LATENCY TOLERANCE REPORTING CONTROL REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:5	**RESERVED**	RO	—

Note 1: The values in the LTR_LOW_VALUE and LTR_HIGH_VALUE registers may need to be adjusted and a "Send LTR Low" command issued by S/W based on a new link speed.

TABLE 102: LATENCY TOLERANCE REPORTING CONTROL REGISTER SPECIFICATIONS

Bit	Description	Type	Default
4	**Send LTR on RX LPI** When set: An LTR message with the values in the LTR_HIGH_VALUE register is sent when the Ethernet MAC detects RX LPI. An LTR message with the values in the LTR_LOW_VALUE register is sent when the Ethernet MAC no longer detects RX LPI.	R/W	0b
3	**Send LTR on MAC Disable** When set: An LTR message with the Snoop and No-Snoop requirement bits cleared is sent when the Ethernet MAC is disabled. An LTR message with the values in the LTR_LOW_VALUE register is sent when the Ethernet MAC detect is enabled. (See **Note 1**.)	R/W	0b
2	**Send LTR on Link Drop** When set: An LTR message with the Snoop and No-Snoop requirement bits cleared is sent on Ethernet Link drop. An LTR message with the values in the LTR_LOW_VALUE register is sent when the on Ethernet Link establishment.	R/W	0b
1	**Send LTR High** Setting this bit will cause an LTR message to be sent with the values from the Latency Tolerance Reporting High Value Register (LTR_HIGH_VALUE).	R/W1S/SC	0b
0	**Send LTR Low** Setting this bit will cause an LTR message to be sent with the values from the Latency Tolerance Reporting Low Value register (LTR_LOW_VALUE).	R/W1S/SC	0b

Note 1: The values in the LTR_LOW_VALUE and LTR_HIGH_VALUE registers may need to be adjusted and a "Send LTR Low" command issued by S/W based on a new link speed.

3.1.14 LATENCY TOLERANCE REPORTING HIGH VALUE REGISTER (LTR_HIGH_VALUE)

Offset: 0084h
Size: 32 bits

This register sets the reported LTR value for when the device state can tolerate a higher latency. See Table 103.

TABLE 103: LATENCY TOLERANCE REPORTING HIGH VALUE REGISTER (LTR_HIGH_VALUE) SPECIFICATIONS

Bit	Description	Type	Default
31	**No-Snoop Requirement** When set, indicates that the No-Snoop LatencyValue and No-Snoop Latency-Scale fields describe the latency requirement. When cleared, there is no latency requirement and the No-Snoop Latency-Value and No-Snoop LatencyScale fields are ignored.	R/W	0b
30:29	**RESERVED**	RO	—

TABLE 103: LATENCY TOLERANCE REPORTING HIGH VALUE REGISTER (LTR_HIGH_VALUE) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
28:26	**No-Snoop LatencyScale** Scale of the No-Snoop LatencyValue field: 000 – value times 1 ns 001 – value times 32 ns 010 – value times 1024 ns 011 – value times 32768 ns 100 – value times 1048576 ns 101 – value times 33554432 ns 110 – value times not permitted 111 – value times not permitted	R/W	000b
25:16	**No-Snoop LatencyValue**	R/W	000h
15	**Snoop Requirement** When set, indicates that the Snoop LatencyValue and Snoop LatencyScale fields describe the latency requirement. When cleared, there is no latency requirement and the Snoop LatencyValue and Snoop LatencyScale fields are ignored.	R/W	0b
14:13	**RESERVED**	RO	—
12:10	**Snoop LatencyScale** Scale of the Snoop LatencyValue field: 000 – value times 1 ns 001 – value times 32 ns 010 – value times 1024 ns 011 – value times 32768 ns 100 – value times 1048576 ns 101 – value times 33554432 ns 110 – value times not permitted 111 – value times not permitted	R/W	000b
9:0	**Snoop LatencyValue**	R/W	000h

3.1.15 LATENCY TOLERANCE REPORTING LOW VALUE REGISTER (LTR_LOW_VALUE)

Offset: 0088h
Size: 32 bits

This register sets the reported LTR value for when the device state requires a lower latency. See Table 104.

TABLE 104: LATENCY TOLERANCE REPORTING LOW VALUE REGISTER (LTR_LOW_VALUE) SPECIFICATIONS

Bit	Description	Type	Default
31	**No-Snoop Requirement** When set, indicates that the No-Snoop LatencyValue and No-Snoop Latency-Scale fields describe the latency requirement. When cleared, there is no latency requirement and the No-Snoop Latency-Value and No-Snoop LatencyScale fields are ignored.	R/W	0b
30:29	**RESERVED**	RO	—

TABLE 104: LATENCY TOLERANCE REPORTING LOW VALUE REGISTER (LTR_LOW_VALUE) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
28:26	**No-Snoop LatencyScale** Scale of the No-Snoop LatencyValue field: 000 – value times 1 ns 001 – value times 32 ns 010 – value times 1024 ns 011 – value times 32768 ns 100 – value times 1048576 ns 101 – value times 33554432 ns 110 – value times not permitted 111 – value times not permitted	R/W	000b
25:16	**No-Snoop LatencyValue**	R/W	000h
15	**Snoop Requirement** When set, indicates that the Snoop LatencyValue and Snoop Latency Scale fields describe the latency requirement. When cleared, there is no latency requirement and the Snoop LatencyValue and Snoop Latency Scale fields are ignored.	R/W	0b
14:13	**RESERVED**	RO	—
12:10	**Snoop Latency Scale** Scale of the Snoop LatencyValue field: 000 – value times 1 ns 001 – value times 32 ns 010 – value times 1024 ns 011 – value times 32768 ns 100 – value times 1048576 ns 101 – value times 33554432 ns 110 – value times not permitted 111 – value times not permitted	R/W	000b
9:0	**Snoop LatencyValue**	R/W	000h

3.1.16 GENERAL PURPOSE TIMER CONFIGURATION REGISTER (GPT_CFG)

Offset: 008Ch
Size: 32 bits

This read/write register configures the device's General Purpose Timer (GPT). The GPT can be configured to generate host interrupts at the interval defined in this register. The current value of the GPT can be monitored via the General Purpose Timer Configuration register. See Table 105.

TABLE 105: GENERAL PURPOSE TIMER CONFIGURATION REGISTER (GPT_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31	**General Purpose Timer 100us Bypass (GPT_100US_BYPASS)** When set the GPT counts at a rate of 62.5 MHz (16 ns).	R/W	0b
30	**General Purpose Timer Stop on Zero (TIMER_STOP_ZERO)** If this bit is set when the counter reaches 0000h, the General Purpose Timer Enable (TIMER_EN) is cleared and the GPT stops counting.	R/W	0b

TABLE 105: GENERAL PURPOSE TIMER CONFIGURATION REGISTER (GPT_CFG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
29	**General Purpose Timer Enable (TIMER_EN)** This bit enables the GPT. When set, the GPT enters the run state. When cleared, the GPT is halted. On the 1 to 0 transition of this bit, the GPT_LOAD field of this register will be preset to FFh. 0 – GPT Disabled 1 – GPT Enabled	R/W	0b
28:16	**RESERVED**	RO	—
15:0	**General Purpose Timer Pre-Load (GPT_LOAD)** This value is per-loaded into the GPT. This is the starting value of the GPT. The timer will begin decrementing from this value when enabled.	R/W	FFFFh

3.1.17 GENERAL PURPOSE TIMER COUNT REGISTER (GPT_CNT)

Offset: 0090h
Size: 32 bits

This read-only register reflects the current general purpose timer (GPT) value. The register should be used in conjunction with the General Purpose Timer Configuration register (GPT_CFG) to configure and monitor the GPT. See Table 106.

TABLE 106: GENERAL PURPOSE TIMER COUNT REGISTER (GPT_CNT) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**General Purpose Timer Current Count (GPT_CNT)** This 16-bit field represents the current value of the GPT.	RO	FFFFh

4.0 EEPROM CONTROLLER (EEP)

4.1 EEPROM Format

Table 107 illustrates the format in which data is stored inside of the EEPROM. All reserved EEPROM bits must be set to 0.

TABLE 107: EEPROM FORMAT SPECIFICATIONS

EEPROM Byte Offset	EEPROM Contents
000h	A5h or AAh (EEPROM Programmed Indicator) F3h or F7h (OTP Programmed Indicator)
001h	MAC Address [7:0]
002h	MAC Address [15:8]
003h	MAC Address [23:16]
004h	MAC Address [31:24]
005h	MAC Address [39:32]
006h	MAC Address [47:40]
007h-00Ah	PCIe Configuration Enables
00Bh-01Ah	PCIe Configuration Values
01Bh-01Ch	MAC Configuration Values
01Dh-021h	LED Configuration Values
starting at 026h	EEPROM User Initialization Table

4.1.1 PCIE CONFIGURATION ENABLES

Offset: 007h – 00Ah
Size: 32 bits

These bytes enable the usage of the PCIe Configuration values. If a bit is set, the appropriate PCIe Configuration Space register is written with the associated data value. Otherwise, the PCIe Configuration Space register is left with its default value. See Table 108.

TABLE 108: PCIE CONFIGURATION ENABLES SPECIFICATIONS

Bit	Description
31:29	RESERVED
28	ASPM L1 Entry Control
27	L1 Entrance Latency
26	L0s Entrance Latency
25	Port T_POWER_ON Scale
24	Port T_POWER_ON Value
23	Port Common_Mode_Restore_Time
22	L1 PM Substates Supported
21	ASPM L1.1 Supported
20	ASPM L1.2 Supported
19	PCI-PM L1.1 Supported
18	PCI-PM L1.2 Supported
17	MSI-X Table Size
16	OBFF Supported
15	LTR Mechanism Supported
14	Slot Clock Configuration

TABLE 108: PCIE CONFIGURATION ENABLES SPECIFICATIONS (CONTINUED)

Bit	Description
13	RESERVED
12	RESERVED
11	Clock Power Management
10	L1 Exit Latency
9	L0s Exit Latency
8	Endpoint L1 Acceptable Latency
7	Endpoint L0s Acceptable Latency
6	MSI Multiple Message Capable
5	No_Soft_Reset
4	Immediate Readiness on Return to D0
3	PME_Support
2	Aux_Current
1	Subsystem ID
0	Subsystem Vendor ID

4.1.2 PCIE CONFIGURATION VALUES

These bytes specify the data values for the indicated PCIe Configuration Space register fields. See Table 109.

TABLE 109: PCIE CONFIGURATION VALUES SPECIFICATIONS

Byte Offset	Bit							
	7	6	5	4	3	2	1	0
00Bh	Subsystem Vendor ID							
00Ch								
00Dh	Subsystem ID							
00Eh								
00Fh	PME_Support					Aux_Current		
010h	No_Soft_Reset	MSI Multiple Message Capable			Immediate Readiness on Return to D0	reserved		
011h	rsvd	Endpoint L1 Acceptable Latency			rsvd	Endpoint L0s Acceptable Latency		
012h	Clock Power Management	L1 Exit Latency			rsvd	L0s Exit Latency		
013h	reserved							
014h	rsvd	MSI-X Table Size			OBFF Supported		LTR Mechanism Supported	Slot Clock Configuration
015h	rsvd			L1 PM Substates Supported	ASPM L1.1 Supported	ASPM L1.2 Supported	PCI-PM L1.1 Supported	PCI-PM L1.2 Supported

TABLE 109: PCIE CONFIGURATION VALUES SPECIFICATIONS (CONTINUED)

Byte Offset	Bit							
	7	6	5	4	3	2	1	0
016h	Port Common_Mode_Restore_Time							
017h	Port T_POWER_ON Scale		rsvd	Port T_POWER_ON Value				
018h	ASPM L1 Entry Control	L1 Entrance Latency			rsvd	L0s Entrance Latency		
019h	reserved							
01Ah	reserved							

4.1.3 MAC CONFIGURATION VALUES

Offset: 01Bh-01Ch
Size: 2 bytes

The following bytes specify the data values for the indicated MAC related CSR fields. These fields are always loaded with the values from EEPROM. There are no individual enable bits. See Table 110.

TABLE 110: MAC CONFIGURATION VALUES SPECIFICATIONS

Byte Offset	Bit							
	7	6	5	4	3	2	1	0
01Bh	Energy Efficient Ethernet Enable (EEEEN)	Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN)	Automatic Duplex Polarity (ADP)	Automatic Duplex Detection (ADD)	Automatic Speed Detection (ASD)	Duplex Mode (DPX)	MAC Configuration (CFG)	
01Ch	rsvd		Generate CLK125 MHz Enable (CLK125_EN)	Reference CLK 25 MHZ Out Enable (REFCLK25_EN)	EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_SPEED_UP)	RGMII TXC Delay Enable	RGMII RXC Delay Enable	Energy Efficient Ethernet TX Clock Stop Enable (EEE_TX_CLK_STOP_EN)

4.1.4 LED CONFIGURATION VALUES

Offset: 01Dh – 021h
Size: 5 bytes

The following bytes in Table 111 specify the data values for the indicated LED-related CSR fields. These fields are always loaded with the values from EEPROM. There are no individual enable bits.

TABLE 111: LED CONFIGURATION SPECIFICATIONS

Byte Offset	Bit							
	7	6	5	4	3	2	1	0
01Dh	Invert LED Polarity				LED3 Enable (LED3_EN)	LED2 Enable (LED2_EN)	LED1 Enable (LED1_EN)	LED0 Enable (LED0_EN)
01Eh	Ethernet PHY LED Mode Select Register[15:8]							
01Fh	Ethernet PHY LED Mode Select Register[7:0]							
020h	Ethernet PHY LED Behavior Register[15:8]							
021h	Ethernet PHY LED Behavior Register[7:0]							

4.1.5 EEPROM USER INITIALIZATION TABLE

Immediately following the fixed fields in the EEPROM is a structured User Initialization Table. Each entry in this table specifies a CSR or PCIe configuration register address, byte enables and 1 to 4 bytes of data. A zero in the upper NIBBLE (Byte Enable) of an entry terminates the table. See Table 112.

TABLE 112: EEPROM USER INITIALIZATION TABLE

EEPROM Byte Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
M-1	Last fixed field from above							
M	Byte Enable [3:0]				PCIe_nCSR 1 - PCIe Configuration space 0 - CSR	Address [12:10] (**Note 1**)		
M+1	Address[9:2]							
M+2	Data Byte 0 (if Byte Enable [0] = 1 else skipped)							
M+3	Data Byte 1(if Byte Enable [1] = 1 else skipped)							
M+4	Data Byte 2 (if Byte Enable [2] = 1 else skipped)							
M+5	Data Byte 3 (if Byte Enable [3] = 1 else skipped)							

Note 1: Address 12 selects the PCIe shadow registers if appropriate.

TABLE 112: EEPROM USER INITIALIZATION TABLE (CONTINUED)

EEPROM Byte Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	Byte Enable [3:0]				PCIe_ nCSR 1 - PCIe config space 0 - CSR	Address [12:10] (**Note 1**)		
N+1	Address[9:2]							
.....								
	0h (END of TABLE marker)				Reserved			

Note 1: Address 12 selects the PCIe shadow registers if appropriate.

4.2 EEPROM Controller Registers

This section details the EEPROM registers. The EEPROM registers are at offsets 0040h and 0044h within the device. See Table 113 for an overview of the entire device register map.

TABLE 113: EEPROM REGISTER MAP

Byte Offset	Register Name (Symbol)
0040h	EEPROM Command Register (E2P_CMD)
0044h	EEPROM Data Register (E2P_DATA)

4.2.1 EEPROM COMMAND REGISTER (E2P_CMD)

Offset: 0040h
Size: 32 bits

This register is used to control the read and write operations on the Serial EEPROM. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 114.

TABLE 114: EEPROM COMMAND REGISTER (E2P_CMD) SPECIFICATIONS

Bit	Description	Type	Default
31	**EPC Busy (EPC_BSY)** When a “1” is written into this bit, the operation specified in the EEPROM OTP Reload (EE_OTP_RELOAD) is performed at the specified EEPROM address. This bit will remain set until the operation is at which time it will clear. In the case of a read, this means that the Host can read valid data from the EEPROM Data Register (E2P_DATA). Software should not be modified the E2P_CMD and E2P_DATA registers until this bit is cleared. In the case where a write is attempted and an EEPROM is not present, the EPC Busy remains busy until an EPC Time-out (EPC_TO) occurs. At that time, the busy bit is cleared.	SC	0b

Note 1: The EEPROM device will power up in the erase/Write-Disabled state. Any erase or write operations will fail until an Erase/Write Enable command is issued.

2: **ERAL (Erase All):** If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.

3: If the EEDI pin is pulled-high, EPC commands will not time out if the EEPROM device is missing. In this case, the EPC Busy bit will be cleared as soon as the command sequence is complete. It should also be noted that the ERASE, ERAL, WRITE and WRAL commands are the only EPC commands that will time-out if an EEPROM device is not present and the EEDI signal is pulled low.

TABLE 114: EEPROM COMMAND REGISTER (E2P_CMD) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
30:28	**EPC Command (EPC_CMD)** This field is used to issue commands to the EEPROM Controller. The EPC will execute commands when the EPC Busy (EPC_BSY) bit is set. A new command must not be issued until the previous command completes. This field is encoded as follows: 000 – READ 001 – EWDS 010 – EWEN 011 – WRITE 100 – WRAL 101 – ERASE 110 – ERAL 111 – reserved **READ (Read Location):** This command will cause a read of the EEPROM location pointed to by EPC Address (EPC_ADDR). The result of the read is available in the EEPROM Data register (E2P_DATA). **EWDS (Erase/Write Disable):** After issued, the EEPROM will ignore erase and write commands. To re-enable erase/write operations, issue the EWEN command. **EWEN (Erase/Write Enable):** Enables the EEPROM for erase and write operations. The EEPROM will allow erase and write operations until the Erase/Write Disable command is sent, or until power is cycled. (See **Note 1**.) **WRITE (Write Location):** If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data register (E2P_DATA) to be written to the EEPROM location selected by the EPC Address (EPC_ADDR) field. **WRAL (Write All):** If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data register (E2P_DATA) to be written to every EEPROM memory location. **ERASE (Erase Location):** If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC Address (EPC_ADDR) field. (See **Note 2**.)	R/W	000b
27:11	**RESERVED**	RO	—
10	**EPC Time-out (EPC_TO)** If an EEPROM operation is performed, and there is no response from the EEPROM within 30 mS, the EEPROM Controller will time-out and return to its idle state. This bit is set when a time-out occurs, indicating that the last operation was unsuccessful. (See **Note 3**.)	R/W1C	0b

Note 1: The EEPROM device will power up in the erase/Write-Disabled state. Any erase or write operations will fail until an Erase/Write Enable command is issued.

2: **ERAL (Erase All):** If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.

3: If the EEDI pin is pulled-high, EPC commands will not time out if the EEPROM device is missing. In this case, the EPC Busy bit will be cleared as soon as the command sequence is complete. It should also be noted that the ERASE, ERAL, WRITE and WRAL commands are the only EPC commands that will time-out if an EEPROM device is not present and the EEDI signal is pulled low.

TABLE 114: EEPROM COMMAND REGISTER (E2P_CMD) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
9	**RESERVED**	RO	—
8:0	**EPC Address (EPC_ADDR)** The 9-bit value in this field is used by the EEPROM Controller to address a specific memory location in the Serial EEPROM. This is a BYTE aligned address.	R/W	000h

Note 1: The EEPROM device will power up in the erase/Write-Disabled state. Any erase or write operations will fail until an Erase/Write Enable command is issued.

2: **ERAL (Erase All):** If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.

3: If the EEDI pin is pulled-high, EPC commands will not time out if the EEPROM device is missing. In this case, the EPC Busy bit will be cleared as soon as the command sequence is complete. It should also be noted that the ERASE, ERAL, WRITE and WRAL commands are the only EPC commands that will time-out if an EEPROM device is not present and the EEDI signal is pulled low.

4.2.2 EEPROM DATA REGISTER (E2P_DATA)

Offset: 0044h
Size: 32 bits

This register is used in conjunction with the EEPROM Command register (E2P_CMD) to perform read and write operations to the Serial EEPROM. See Table 115.

TABLE 115: EEPROM DATA REGISTER (E2P_DATA) SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**EEPROM Data (EPC_DATA)** Value read from or written to the EEPROM.	R/W	—

5.0 FIFO CONTROLLER (FCT)

5.1 Overview

The FIFO controller uses internal RAMs to buffer RX and TX traffic. Host transmit data, via the DMAC, is directly stored into the FCT TX FIFO(s). The FCT is responsible for extracting Ethernet frames from the host data and passing the frames to the MAC.

Received Ethernet Frames are stored into the FCT RX FIFOs and become the basis for DMAC to host memory transfers.

5.2 FCT Controller Registers

This section details the FCT registers. The FCT registers are at offsets 00A0h through 00FFh within the device. This range is for exclusive use of the FCT registers. For an overview of the entire device register map, refer to Section 1.0, Register Map. For some RX FIFO related registers, each channel has a set of registers. These sets of registers are identical in functionality for each FIFO, and thus their register descriptions have been consolidated. In these cases, the register names will be amended with a lowercase “x” in place of the channel designation. The wildcard “x” should be replaced with “0” through “3”. See Table 116.

TABLE 116: FCT REGISTER MAP

Byte Offset	Register Name (Symbol)
00A0h	FIFO Controller Configuration Register (FCT_CFG)
00A4h	FIFO Controller Interrupt Enable Set Register (FCT_INT_EN_SET)
00A8h	FIFO Controller Interrupt Enable Clear Register (FCT_INT_EN_CLR)
00ACh	FIFO Controller RX FIFO Control Register (FCT_RX_CTL)
00B0h	FCT RX FIFO End Register (FCT_RX_FIFO_END)
00B4h	FCT RX FIFO x USED Register (FCT_RX_USED_x) (x=0)
00B8h	FCT RX FIFO x USED Register (FCT_RX_USED_x) (x=1)
00BCh	FCT RX FIFO x USED Register (FCT_RX_USED_x) (x=2)
00C0h	FCT RX FIFO x USED Register (FCT_RX_USED_x) (x=3)
00C4h	FIFO Controller TX FIFO Control Register (FCT_TX_CTL)
00C8h	FCT TX FIFO End Register (FCT_TX_FIFO_END)
00CCh	FCT TX FIFO USED Register (FCT_TX_USED)
00D0h-00DBh	Reserved for future FCT TX FIFO USED Register (FCT_TX_USED) 1,2,3
00DCh	FIFO Controller Configuration Register (FCT_CFG)
00E0h	FCT Flow Control X Threshold Register (FCT_FLOW_X) (x=0)
00E4h	FCT Flow Control X Threshold Register (FCT_FLOW_X) (x=1)
00E8h	FCT Flow Control X Threshold Register (FCT_FLOW_X) (x=2)
00ECh	FCT Flow Control X Threshold Register (FCT_FLOW_X) (x=3)
00F0h-00FFh	Reserved for future expansion

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

5.2.1 FIFO CONTROLLER INTERRUPT STATUS REGISTER (FCT_INT_STS)

Offset: 00A0h
Size: 32 bits

If the host attempts to clear a R/W1C bit within the FCT_INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding FCT_INT_STS bit will remain set. See Table 117.

TABLE 117: FIFO CONTROLLER INTERRUPT STATUS REGISTER (FCT_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RX Data FIFO Packet Available x Interrupt (RDFPAx_INT)** This interrupt is set when there is at least one frame available to be read from the RX Data FIFO. This bit will persist until there is no longer a frame available. It can only be cleared once all available frames have been read. There is one bit per channel. The source of this interrupt is a level and will persist until the source is cleared.	R/W1C/ NASR (**Note 2**)	0000b
27:24	**RX Data FIFO Overflow x Interrupt (RDFOx_INT)** This interrupt is set when if either a) at the start of the frame, there is insufficient space for a minimum size frame or b) the receive logic attempts to place data into the RX Data FIFO after it has been completely filled. There is one bit per channel. This bit will be set for all frames (good/bad, filtered, etc.) (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0000b
23:20	**RX Dropped Frame x Interrupt (RXDFx_INT)** This interrupt is set when a frame is dropped due to insufficient room in the RX FIFO due to either a) insufficient space for a minimum size frame at the start of the frame or b) the receive logic attempts to place data into the RX Data FIFO after it has been completely filled. There is one bit per channel. If a frame would have been dropped due to other reasons (such as RFE filtering, RFE channel determination, wake up frame filtering or NS/ARP offloading), this bit will not be set. If a frame to be dropped has an Ethernet receive error, it will be not be indicated by this bit unless the Store Bad Frames bit is set.The source of this interrupt is a pulse.	R/W1C/ NASR (**Note 2**)	0000b
19:17	**RESERVED**	RO	—
16	**Transmitter Error Interrupt (TXE_INT)** This interrupt indicates that the transmitter has encountered an error. (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0b
15:13	**RESERVED**	RO	—
12	**TX Data FIFO Overrun Interrupt (TDFO_INT)** Generated when the TX Data FIFO is full, and another write is attempted. This interrupt should never occur and indicates a catastrophic hardware error. (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0b
11:9	**RESERVED**	RO	—

Note 1: The source of this interrupt is a pulse.

2: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 117: FIFO CONTROLLER INTERRUPT STATUS REGISTER (FCT_INT_STS) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
8	**TX Data FIFO Under-run Interrupt (TDFU_INT)** Generated when the TX Data FIFO under runs. This interrupt should never occur and indicates a catastrophic hardware error. (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0b
7:4	**FCT RX Disabled x Interrupt (FCT_RX_DISx_INT)** This interrupt is issued after the RX FIFO has been successfully disabled via writing a 1 to the FCT RX Disable x bit. It is set when the hardware disabling process, invoked by writing a 1 to the appropriate FCT RX Disable x bit, completes. There is one bit per channel. (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0000b
3:1	**RESERVED**	RO	—
0	**FCT TX Disabled Interrupt (FCT_TX_DIS_INT)** This interrupt is issued after the TX FIFO has been successfully disabled via writing a 1 to the FCT TX Disable bit. It is set when the hardware disabling process, invoked by writing a 1 to the FCT TX Disable bit, completes. (See **Note 1**.)	R/W1C/ NASR (**Note 2**)	0b

Note 1: The source of this interrupt is a pulse.

2: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.2 FIFO CONTROLLER INTERRUPT ENABLE SET REGISTER (FCT_INT_EN_SET)

Offset: 00A4h
Size: 32 bits

This register is used to set the interrupt enables for the corresponding bits in the FIFO Controller Interrupt Status register (FCT_INT_STS). Writing a '1' to a bit sets the corresponding enable and configures the corresponding interrupt as a source for the assertion of the FCT interrupt. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables. See Table 118.

TABLE 118: FIFO CONTROLLER INTERRUPT ENABLE SET REGISTER (FCT_INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RX Data FIFO Packet Available x Interrupt Enable Set (RDFPAx_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0000b
27:24	**RX Data FIFO Overflow x Interrupt Enable Set (RDFOx_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0000b
23:20	**RX Dropped Frame x Interrupt Enable Set (RXDFx_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0000b

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 118: FIFO CONTROLLER INTERRUPT ENABLE SET REGISTER (FCT_INT_EN_SET) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
19:17	**RESERVED**	RO	—
16	**Transmitter Error Interrupt Enable Set (TXE_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0b
15:13	**RESERVED**	RO	—
12	**TX Data FIFO Overrun Interrupt Enable Set (TDFO_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0b
11:9	**RESERVED**	RO	—
8	**TX Data FIFO Under-run Interrupt Enable Set (TDFU_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0b
7:4	**FCT RX Disabled x Interrupt Enable Set (FCT_RX_DISx_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0000b
3:1	**RESERVED**	RO	—
0	**FCT TX Disabled Interrupt Enable Set (FCT_TX_DIS_INT_EN_SET)**	R/W1S/ NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.3 FIFO CONTROLLER INTERRUPT ENABLE CLEAR REGISTER (FCT_INT_EN_CLR)

Offset: 00A8h
Size: 32 bits

This register is used to clear the interrupt enables for the corresponding bits in the FIFO Controller Interrupt Status register (FCT_INT_STS). Writing a ‘1’ to a bit clears the corresponding enable. Writing a ‘0’ has no effect. A read of this register returns the state of the interrupt enables. See Table 119.

TABLE 119: FIFO CONTROLLER INTERRUPT ENABLE CLEAR REGISTER (FCT_INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RX Data FIFO Packet Available x Interrupt Enable Clear (RDFPAx_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0000b
27:24	**RX Data FIFO Overflow x Interrupt Enable Clear (RDFOx_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0000b
23:20	**RX Dropped Frame x Interrupt Enable Clear (RXDFx_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0000b
19:17	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 119: FIFO CONTROLLER INTERRUPT ENABLE CLEAR REGISTER (FCT_INT_EN_CLR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
16	**Transmitter Error Interrupt Enable Clear (TXE_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0b
15:13	**RESERVED**	RO	—
12	**TX Data FIFO Overrun Interrupt Enable Clear (TDFO_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0b
11:9	**RESERVED**	RO	—
8	**TX Data FIFO Under-run Interrupt Enable Clear (TDFU_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0b
7:4	**FCT RX Disabled x Interrupt Enable Clear (FCT_RX_DISx_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0000b
3:1	**RESERVED**	RO	—
0	**FCT TX Disabled Interrupt Enable Clear (FCT_TX_DIS_INT_EN_CLR)**	R/W1C/ NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.4 FIFO CONTROLLER RX FIFO CONTROL REGISTER (FCT_RX_CTL)

Offset: 00ACh
Size: 32 bits

See Table 120.

Note: Some bits in this register are new for LAN743x.

TABLE 120: FIFO CONTROLLER RX FIFO CONTROL REGISTER (FCT_RX_CTL) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**FCT RX Enable x** Writing a one to an appropriate bit enables the corresponding FIFO. Writing a zero has no affect. When set, the FIFO is capable of accepting traffic from the RFE. If this bit is de-asserted, all received frames from the RFE are aborted and not written into the FIFO. After this bit is asserted, the FIFO will accept the next full frame it receives. After the FIFO is enabled, the FIFO begins accepting data after it receives the first complete frame. There is one bit per channel. This bit, being low, does not cause frame dropped counter to increment.	R/W1S	0000b

TABLE 120: FIFO CONTROLLER RX FIFO CONTROL REGISTER (FCT_RX_CTL) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
27:24	**FCT RX Disable x** Writing a one to an appropriate bit will request the h/w to disable the corresponding FIFO. Writing a zero has no affect. If the FIFO is disabled while receiving a frame, the FIFO will allow the current frame to be received before disabling the FIFO. After the FIFO is successfully disabled the corresponding FCT RX Enable x bit will clear and the corresponding FCT RX Disabled x Interrupt (FCT_RX_DISx_INT) bit is asserted. There is one bit per channel.	WO	0000b
23:20	**FCT RX Reset x** When set, the FCT RX is reset. Register bits for the channel marked as NASR are not reset. The corresponding FIFO must be disabled before a reset is issued. There is one bit per channel.	R/W1S/SC	0000b
19:0	**RESERVED**	RO	—

5.2.5 FCT RX FIFO END REGISTER (FCT_RX_FIFO_END)

Offset: 00B0h
Size: 32 bits

This register specifies the end address of the RX FIFO in DWORD units. The contents of this register times 128 plus 127 is the end address of the FIFO. See Table 121. This register contains separate fields for each channel.

Note:	This register's contents may not be modified at run time. The RX datapath for a channel must be halted before changing the channel's FIFO size. After modifying the FIFO's size, the channel's FIFO must be flushed.

TABLE 121: FCT RX FIFO END REGISTER (FCT_RX_FIFO_END) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:24	**FCT_RX_FIFO_END_3**	R/W/ NASR (**Note 2**)	3Fh
23:22	**RESERVED**	RO	—
21:16	**FCT_RX_FIFO_END_2**	R/W/ NASR (**Note 2**)	3Fh
15:14	**RESERVED**	RO	—
13:8	**FCT_RX_FIFO_END_1**	R/W/ NASR (**Note 2**)	3Fh
7:6	**RESERVED**	RO	—

TABLE 121: FCT RX FIFO END REGISTER (FCT_RX_FIFO_END) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
5:0	**FCT_RX_FIFO_END_0**	R/W/ NASR (**Note 2**)	3Fh

Note 1: The maximum RX FIFO size is 32 kB which is the default value. Values exceeding this size will cause operation and unexpected results.

2: The NASR designerstiev is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.6 FCT RX FIFO X USED REGISTER (FCT_RX_USED_X)

Offset:
Channel 0: 00B4h
Channel 1: 00B8h
Channel 2: 00BCh
Channel 3: 00C0h
Size: 32 bit

This register indicates the amount of space in bytes, used by the FIFO. For each frame, this field is incremented by the length of the frame rounded up to the nearest DWORD (if the payload does not end on a DWORD boundary). Additionally any Command Words or checksums associated with the frame are also added in. See Table 122.

Note: This is a live value reflecting the amount of space used at the time of the register read. It could include bytes from a frame in progress as well as bytes from a complete frame that have been temporarily placed in the FIFO which could be removed due to RFE filtering.

TABLE 122: FCT RX FIFO X USED REGISTER (FCT_RX_USED_X) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**RX Data FIFO Used Space (RXUSED)**	RO	0000h

5.2.7 FIFO CONTROLLER TX FIFO CONTROL REGISTER (FCT_TX_CTL)

Offset: 00C4h
Size: 32 bits

See Table 123.

TABLE 123: FIFO CONTROLLER TX FIFO CONTROL REGISTER (FCT_TX_CTL) SPECIFICATIONS

Bit	Description	Type	Default
31:29	**RESERVED**	RO	—
28	FCT TX Enable Writing a one to this bit enables the FIFO. Writing a zero has no affect. When set, the FIFO is capable of transmitting frames to the MAC.	R/W1S	0b
27:25	RESERVED	RO	—

TABLE 123: FIFO CONTROLLER TX FIFO CONTROL REGISTER (FCT_TX_CTL) SPECIFICATIONS

Bit	Description	Type	Default
24	FCT TX Disable Writing a one to this bit will request the h/w to disable the FIFO. Writing a zero has no affect. If the FIFO is disabled while transmitting a frame, the frame transmission is allowed to complete. An exception to the above can happen in half duplex mode in which the FIFO may discard the frame in transmit. This case happens when the frame in transmit is retried by the MAC, due to a collision, after the FIFO has been disabled. Upon completion of the last frame, the FCT TX Enable bit will clear and the FCT TX Disabled Interrupt (FCT_TX_DIS_INT) bit is asserted.	WO	0b
23:21	**RESERVED**	RO	—
20	**FCT TX Reset** When set, this bit resets the FCT TX. Register bits marked as NASR are not reset. The FIFO must be disabled before a reset is issued.	R/W1S/SC	0b
19:0	**RESERVED**	RO	—

5.2.8 FCT TX FIFO END REGISTER (FCT_TX_FIFO_END)

Offset: 00C8h
Size: 32 bits

This register specifies the end address of the TX FIFO in DWORD units. The contents of this register times 128 plus 127 is the end address of the FIFO. See Table 124.

Note:	This register's contents may not be modified at run time. The TX datapath must be halted before changing the FIFO size. After modifying the FIFO's size, the FIFO must be flushed.

TABLE 124: FCT TX FIFO END REGISTER (FCT_TX_FIFO_END)

Bit	Description	Type	Default
31:6	**RESERVED**	RO	—
5:0	**FCT_TX_FIFO_END**	R/W/ NASR (**Note 2**)	27h

Note 1: The maximum TX FIFO size is 20 kB which is the default value.

2: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.9 FCT TX FIFO USED REGISTER (FCT_TX_USED)

Offset: 00CCh
Size: 32 bits

This register indicates the amount of space in bytes, used by the FIFO. For each frame, this field is incremented by the length of the frame rounded up to the nearest DWORD (if the payload does not end on a DWORD boundary). Additionally any Command Words or checksums associated with the frame are also added in. See Table 125.

TABLE 125: FCT TX FIFO USED REGISTER (FCT_TX_USED) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**TX Data FIFO Used Space (TXUSED)**	RO	0000h

5.2.10 FIFO CONTROLLER CONFIGURATION REGISTER (FCT_CFG)

Offset: 00DCh
Size: 32 bits

See Table 126.

TABLE 126: FIFO CONTROLLER CONFIGURATION REGISTER (FCT_CFG)SPECIFICATIONS

Bit	Description	Type	Default
31:5	**RESERVED**	RO	—
4	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when calculating the UDP, TCP or ICMPv6 checksum for TX checksum offloading or TX large send offloading. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not calculated or inserted. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not calculated or inserted.	R/W/ NASR (**Note 1**)	0b
3:1	**RESERVED**	RO	—
0	**Store Bad Frames** When set, the RX FCT will store errored frames that were detected by the Ethernet MAC. The following conditions cause the MAC to consider a frame bad: RX error, FCS error, runt frame, alignment error, jabber error, undersized frame error, and oversized frame error. One bit controls all RX channels.	R/W/ NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

5.2.11 FCT FLOW CONTROL X THRESHOLD REGISTER (FCT_FLOW_X)

Offset:

Channel 0: 00E0h
Channel 1: 00E4h
Channel 2: 00E8h
Channel 3: 00ECh
Size: 32 bits

This register specifies the thresholds for controlling pause frame generation. The units of the thresholds are 512 bytes and correspond to high and low watermarks in the RX FIFO. See Table 127.

Note:	The values in this register must be programmed before the TX Flow Control Enable (TX_FCEN) bit is set. Conversely, the TX Flow Control Enable (TX_FCEN) bit must be cleared before the threshold values are programmed to 0.

TABLE 127: FCT FLOW CONTROL X THRESHOLD REGISTER (FCT_FLOW_X) SPECIFICATIONS

Bit	Description	Type	Default
31:15	**RESERVED**	RO	—
14:8	**Flow Control Off Threshold** The threshold to de-assert the flow control request for this channel. If RX Data FIFO Used Space (RXUSED) / 512 is less than or equal to this value, then the flow control request is de-asserted.	R/W/ NASR (**Note 1**)	0000000b
7	**Flow Control Request Enable** A setting of one enables flow control requests for this channel. Both threshold based and overflow “panic” flow control are enabled / disabled with this bit.	R/W/ NASR (**Note 1**)	0b
6:0	**Flow Control On Threshold** The threshold to assert the flow control request for this channel. If RX Data FIFO Used Space (RXUSED) / 512 is greater than or equal to this value, then the flow control request is asserted.	R/W/ NASR (**Note 1**)	0000000b

Note 1: The NASR designation is only applicable when the FCT RX Reset x bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the FCT TX Reset bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.0 MEDIA ACCESS CONTROLLER (MAC)

The Ethernet Media Access controller (MAC) incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface to the Ethernet PHY. The MAC can operate in full-duplex 1000 Mbps or half/full-duplex 10/100 Mbps mode.

When operating in Half-Duplex mode, the MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in Full-Duplex mode, the MAC complies with IEEE 802.3x full-duplex operation standard.

The MAC provides programmable enhanced features designed to minimize Host supervision, bus utilization, and pre- or post-message processing. These features include the ability to disable retries after a collision, dynamic FCS (Frame Check Sequence) generation on a frame-by-frame basis, automatic pad field insertion and deletion to enforce minimum frame size attributes, and automatic retransmission and detection of collision frames.

The primary attributes of the MAC Function are:

- Interfaces to PHY
- Transmit and receive message data encapsulation
- Framing (frame boundary delimitation, frame synchronization)
- Error detection (physical medium transmission errors)
  - Including Length Field testing
- FCS checking/stripping/generation
- Preamble stripping/generation
- Media access management
- Medium allocation (collision detection, except in full-duplex operation)
- Contention resolution (collision handling, except in full-duplex operation)
- Flow control during Full-Duplex mode
- Decoding of control frames (PAUSE command) and disabling the transmitter
- Generation of control frames (PAUSE command)
- Maintains minimum inter-packet gap (IPG)
- Magic packet/Wake-On-LAN (WOL) detection
- Remote wakeup frame detection
- Neighbor solicitation offload
- ARP offload
- Implements Simple Network Management Protocol (SNMP) and Remote Monitoring (RMON) management counter sets

The transmit and receive datapaths are separate within the device from the MAC to the USB interface, allowing the highest performance, especially in Full-Duplex mode.

On the backend, the MAC interfaces with the PHY using internal GMII and MII ports. The GMII port is used for 1000 Mbps operation, while the MII port is used for 10/100 Mbps operation. The device's registers also provide a mechanism for accessing the PHY's registers through the internal Management Data Input/Output (MDIO) Interface bus.

The FCT RX and TX FIFO allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the Host interface and the MAC through which all transmitted and received data and various command/status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks, reducing and minimizing overrun conditions.

6.1 MAC Registers

This section details the MAC registers. The MAC registers start at offset 0100h and end at offset 06FFh within the device. MAC statistics start at offset 1200h and end at offset 12FFh. These ranges are for exclusive use of the MAC registers. See Table 127 and Table 128.

TABLE 128: MAC REGISTER MAP

Byte Offset	Register Name (Symbol)
0100h	MAC Control Register (MAC_CR)

TABLE 128: MAC REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
0104h	MAC Receive Register (MAC_RX)
0108h	MAC Transmit Register (MAC_TX)
010Ch	Flow Control Register (FLOW)
0110h	Random Number Seed Value Register (RAND_SEED)
0114h	Error Status Register (ERR_STS)
0118h	MAC Receive Address High Register (RX_ADDRH)
011Ch	MAC Receive Address Low Register (RX_ADDRL)
012Ch-012Fh	Reserved for future expansion
0130h	EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT)
0134h	EEE Time Wait TX System Register (EEE_TW_TX_SYS)
0138h	EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY)
013Ch-013Fh	Reserved for future expansion
0140h	Wakeup Control and Status Register 1 (WUCSR1)
0144h	Wakeup Source Register (WK_SRC)
0148h-014Fh	Reserved for future expansion
0150h through 01CCh	Wakeup Filter x Configuration Register (WUF_CFGx)
01D0h-01FFh	Reserved for future expansion
0200h through 03FCh	Wakeup Filter x Byte Mask Registers (WUF_MASKx)
0600h	Wakeup Filter x Byte Mask Registers (WUF_MASKx)
0604h	FIFO Controller Interrupt Status Register (FCT_INT_STS)
0608h	FIFO Controller Interrupt Enable Set Register (FCT_INT_EN_SET)
060Ch	FIFO Controller Interrupt Enable Clear Register (FCT_INT_EN_CLR)
0610h through 061Ch	NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) (x=0)
0620h through 062Ch	NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC) (x=0)
0630h through 063Ch	NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0)(x=0)
0640h through 064Ch	NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1) (x=0)
0650h through 065Ch	SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST) (x=1)
0660h through 066Ch	SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) (x=1)
0670h through 067Ch	NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0)(x=1)

TABLE 128: MAC REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
0680h through 068Ch	NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1) (x=1)
0690h	SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC)
0694h	SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST)
0698h	SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS)
069Ch through 06A8h	SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC)
06ACh through 06B8h	SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST)
06BCh	SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS)
06C0h	ARP Sender Protocol Address Register (ARP_SPA)
06C4h	ARP Target Protocol Address Register (ARP_TPA)
06C8h-06FFh	Reserved for future expansion

TABLE 129: MAC STATISTICS REGISTER MAP

Byte Offset	Register Name (Symbol)
1200h	RX FCS Errors
1204h	RX Alignment Errors
1208h	RX Fragment Errors
120Ch	RX Jabber Errors
1210h	RX Undersized Frame Errors
1214h	RX Oversized Frame Errors
1218h	RX Dropped Frames
121Ch	RX Unicast Byte Count
1220h	RX Broadcast Byte Count
1224h	RX Multicast Byte Count
1228h	RX Unicast Frames
122Ch	RX Broadcast Frames
1230h	RX Multicast Frames
1234h	RX Pause Frames
1238h	RX 64 Byte Frames
123Ch	RX 65 – 127 Byte Frames
1240h	RX 128 – 255 Byte Frames
1244h	RX 256 – 511 Byte Frames
1248h	RX 512 – 1023 Byte Frames
124Ch	RX 1024 – 1518 Byte Frames
1250h	RX Greater 1518 Byte Frames
1254h	RX Total Frames
1258h	EEE RX LPI Transitions
125Ch	EEE RX LPI Time
1260h-127Bh	Reserved for future expansion
127Ch	RX Counter Rollover Status

TABLE 129: MAC STATISTICS REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
1280h	TX FCS Errors
1284h	TX Excess Deferral Errors
1288h	TX Carrier Errors
128Ch	TX Bad Byte Count
1290h	TX Single Collisions
1294h	TX Multiple Collisions
1298h	TX Excessive Collisions
129Ch	TX Late Collisions
12A0h	TX Unicast Byte Count
12A4h	TX Broadcast Byte Count
12A8h	TX Multicast Byte Count
12ACh	TX Unicast Frames
12B0h	TX Broadcast Frames
12B4h	TX Multicast Frames
12B8h	TX Pause Frames
12BCh	TX 64 Byte Frames
12C0h	TX 65 – 127 Byte Frames
12C4h	TX 128 – 255 Byte Frames
12C8h	TX 256 – 511 Byte Frames
12CCh	TX 512 – 1023 Byte Frames
12D0h	TX 1024 – 1518 Byte Frames
12D4h	TX Greater 1518 Byte Frames
12D8h	TX Total Frames
12DCh	TX TX LPI Transitions
12E0h	TX TX LPI Time
12E4h-12FBh	Reserved for future expansion
12FCh	TX Counter Rollover Status

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

6.1.1 MAC CONTROL REGISTER (MAC_CR)

Offset: 0100h
Size: 32 bits

This register establishes the RX and TX operating modes. See Table 130.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**RESERVED**	RO	—
19	**MII/RGMII Selection (MII_EN)** When set, the MAC will operate in MII mode at 10 Mbps and 100 Mbps, or GMII mode at 1000Mbps. When reset, the MAC will operate in RGMII mode. (See **Note 9** and **Note 10**.)	R/W NASR (**Note 1**)	**Note 2**
18	**Energy Efficient Ethernet TX Clock Stop Enable (EEE_TX_CLK_STOP_EN)** When set, the MAC will halt the GMII GTX_CLK to the PHY during TX LPI. This bit is unused in 100 Mbs mode. Software or OTP/EEPROM contents should only set this bit if the Clock stop capable bit in PHY MMD register 3.1 indicates that the PHY is capable of allowing a stopped TX clock. (See **Note 7**.)	R/W NASR (**Note 1**)	0b (**Note 3**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
17	**Energy Efficient Ethernet Enable (EEEEN)** When set, this enables Energy Efficient Ethernet operation in the MAC. When cleared, the Energy Efficient Ethernet operation is disabled. (See **Note 4**.) The MAC will generate LPI requests even if Transmitter Enable (TXEN) is cleared and will decode the LPI indication even if Receiver Enable (RXEN) is cleared. (See **Note 11** and **Note 7**.)	R/W NASR (**Note 1**)	0b (**Note 3**)
16	**Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN)** When set, this enables the automatic de-assertion of LPI in anticipation of a periodic transmission event. The time to wait is specified in the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY). The interval is timed from the point where the MAC initiates LPI signaling. Software should only change this field when Energy Efficient Ethernet Enable (EEEEN) field is cleared. (See **Note 7**.)	R/W NASR (**Note 1**)	0b (**Note 3**)
15:14	**RESERVED**	RO	—
13	**Automatic Duplex Polarity (ADP)** This bit indicates the polarity of the FDUPLEX PHY LED. 0 – DUPLEX asserted low indicates the PHY is in Full-Duplex mode. 1 – DUPLEX asserted high indicates the PHY is in Full-Duplex mode. (See **Note 8** and **Note 7**.)	R/W NASR (**Note 1**)	1b (**Note 3**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
12	**Automatic Duplex Detection (ADD)** When set, the MAC ignores the setting of the Duplex Mode (DPX) bit and automatically determines the Duplex Operational mode. The MAC uses a PHY LED/signal, or DUPLEX pin for the LAN7431 and LAN743F, to accomplish mode detection and reports the last determined status via the Duplex Mode (DPX) bit. When reset, the setting of the Duplex Mode (DPX) bit determines Duplex operation. (See **Note 8** and **Note 7**.)	R/W NASR (**Note 1**)	1b (**Note 3**)
11	**Automatic Speed Detection (ASD)** When set, the MAC ignores the setting of the MAC Configuration (CFG) field and automatically determines the speed of operation. The MAC samples the RX_CLK input to accomplish speed detection and reports the last determined speed via the MAC Configuration (CFG) field. When reset, the setting of the MAC Configuration (CFG) field determines operational speed. (See **Note 8** and **Note 7**.)	R/W NASR (**Note 1**)	0b (**Note 3**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
10	**Internal Loopback Operation Mode (INT_LOOP)** Loops back data between the TX datapath and RX datapath interfaces. This is only for Full-Duplex mode. In internal Loopback mode, the TX frame is received by the Internal GMII interface, and sent back to the MAC without being sent to the PHY. 0 – Normal mode 1 – Internal loopback enabled (See **Note 8**.)	R/W NASR (**Note 1**)	0b
9:8	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
7:6	**Back Off Limit (BOLMT)** The BOLMT bits allow the user to set its back-off limit in a relaxed or aggressive mode. According to IEEE 802.3, the MAC has to wait for a random number [r] of slot-times after it detects a collision, where: *(eq.1)0 < r < 2^K* The exponent K is dependent on how many times the current frame to be transmitted has been retried, as follows: *(eq.2) K = min (n, 10) where n is the current number of retries.* If a frame has been retried three times, then K = 3 and r = 8 slot-times maximum. If it has been retried 12 times, then K = 10, and r = 1024 slot-times maximum. An LFSR (linear feedback shift register) counter emulates a random number generator, from which r is obtained. Once a collision is detected, the number of the current retry of the current frame is used to obtain K (eq.2). This value of K translates into the number of bits to use from the LFSR counter. If the value of K is 3, the MAC takes the value in the first three bits of the LFSR counter and uses it to count down to zero on every slot-time. This effectively causes the MAC to wait eight slot-times. To give the user more flexibility, the BOLMT value forces the number of bits to be used from the LFSR counter to a predetermined value as in the table below. Thus, if the value of K = 10, the MAC will look at the BOLMT if it is 00, then use the lower ten bits of the LFSR counter for the wait countdown. If the BOLMT is 10, then it will only use the value in the first four bits for the wait countdown, etc. Slot-time = 512 bit times. (See IEEE 802.3 Spec., Sections 4.2.3.2.5 and 4.4.2.1). (See **Note 8**.)	R/W NASR (**Note 1**)	00b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
5	**Counter Reset (CNTR_RST)** When this bit is set, all of the statistics counters and rollover statuses are reset. This bit self-clears.	R/W1S/SC	0b
4	**Counter Write En (CNTR_WEN)** When this bit is set, all of the statistics counters are writable for test purposes. When clear, the statistics counters are read-only.	R/W NASR (**Note 1**)	0b
3	**Duplex Mode (DPX)** This bit determines the Duplex Operational mode of the MAC when the Automatic Duplex Detection (ADD) bit is reset. When the Automatic Duplex Detection (ADD) bit is set, this bit is read-only and reports the last determined Duplex Operational mode. 0 – MAC is in Half-Duplex mode 1 – MAC is in Full-Duplex mode (See **Note 8**, **Note 11**, and **Note 7**.)	NASR (**Note 1**) (**Note 5**)	0b (**Note 3**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

TABLE 130: MAC CONTROL REGISTER (MAC_CR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
2:1	**MAC Configuration (CFG)** This field determines the operational speed of the MAC when the Automatic Speed Detection (ASD) bit is reset. When the Automatic Speed Detection (ASD) bit is set, this field is read-only and reports the last determined operational speed. 0 – MII Mode – 10 Mbps 1 – MII Mode – 100 Mbps 2,3 – RGMII/GMII Mode – 1000 Mbps (See **Note 8** and **Note 7**.)	NASR (**Note 1**) (**Note 6**)	00b (**Note 3**)
0	**MAC Reset (MRST)** 0 – MAC is enabled 1 – MAC is reset Register bits marked as NASR are not reset.	R/W1S/SC	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from the MII_EN strap.

3: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

4: If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

5: When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last Duplex Operational mode determined by the MAC.

6: When Automatic Speed Detection (ASD) is reset, this bit is R/W and determines duplex operation. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

7: This field is protected by Reset Protection (RST_PROTECT).

8: Software should not modify this field while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).

9: This bit only has meaning for the LAN7431.

10: For the LAN7431, only 10 and 100 MII mode is supported. External GMII mode is not supported.

11: For the LAN7431 and LAN743F the assertion of this bit does not immediately initiate LPI transmission. LPI is delayed by the amount specified in EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_-SPEED_UP)

12: Half-Duplex mode is disabled if the detected or manually set speed is 1000 Mbs, regardless of the setting of this bit.

6.1.2 MAC RECEIVE REGISTER (MAC_RX)

Offset: 0104h
Size: 32 bits

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 131.

TABLE 131: MAC RECEIVE REGISTER (MAC_RX) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:16	**Maximum Frame Size (MAX_SIZE)** Defines the maximum size for a received frame. Frames exceeding this size are aborted. (See **Note 4**, **Note 5**, and **Note 2**.)	R/W NASR (**Note 1**)	1518
15:7	**RESERVED**	RO	—
6	**Length Field Less Than Check (LEN_FLD_LT_CHK)** 0 = Allow frames larger than 64 bytes to have a length/type field value less than the received frame length (minus 18 bytes). 1 = Abort frames larger than 64 bytes whose length/type field value is less than the received frame length (minus 18 bytes). (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	1b
5	**Watchdog Truncation Length (WTL)** 0 = The MAC truncates the Rx FRAME at MAC_RX.MAX_SIZE+1 or 15361, whichever is smaller. The RxCmdA of the truncated received frame passed to the FCT will have a length value of MAC_RX. MAX_SIZE+1 or 15361, whichever is smaller. The RWT bit will be set if the MAC_RX. MAX_SIZE is set to 15360 or larger. The LONG bit will be set if MAC_RX. MAX_SIZE is set to 15360 or less. The truncation will most likely result in an FCS error (FCS bit set). 1 = The MAC truncates the Rx FRAME at 15361. The RxCmdA of the truncated received frame passed to the FCT will have the RWT bit set and a length value of 15361. The LONG bit will be set if MAC_RX. MAX_SIZE is set to 15360 or less. The truncation will most likely result in an FCS error (FCS bit set). (See **Note 2**.)	R/W NASR (**Note 1**)	1b
4	**FCS Stripping** When set, the MAC will strip the FC (last 4 bytes) off of all received frames. (See **Note 2**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Hardware prevents this field from being modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX).

3: This field is protected by Reset Protection (RST_PROTECT).

4: The maximum guaranteed supported frame size is 9,220 bytes.

5: Values for this field larger than 15360 are ineffective since the watchdog timer would take effect and truncate the frame at 15361.

TABLE 131: MAC RECEIVE REGISTER (MAC_RX) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
3	**Length Field Checking Disable (LFCD)** 0 = Abort all frames whose frame length is inconsistent with the length value specified in the length/type field. 1 = Ignore length field. When cleared, frames whose frame length is inconsistent with the length value specified in the length/type field are considered to be errored and are dropped at the RX FIFO (unless the RX FIFO is configured to store bad frames). Wakeup frames do not cause a wake event and ARP/NS offload requests do not cause a response. When set, frame length errors are still reported but the frame is not dropped. Wakeup frames may cause a wake event and ARP/NS offload requests may cause a response. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	1b
2	**VLAN Frame Size Enforcement (FSE)** 0 = Abort all frames larger than the maximum frame size. 1 = Abort all non-VLAN frames larger than maximum frame size. Abort all frames with a single VLAN tag that are larger the maximum frame size +4. Abort all frames with two VLAN tags that are larger than the maximum frame size +8. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
1	**Receiver Disabled (RXD)** This bit indicates that the MAC's receiver has been successfully disabled via clearing the Receiver Enable (RXEN) bit. It is set when the hardware disabling process, invoked by a transition of the Receiver Enable (RXEN) bit from 1 to 0 (enabled to disabled), completes.	R/W1C NASR (**Note 1**)	0b
0	**Receiver Enable (RXEN)** When set, the MAC's receiver is enabled and will receive frames from the PHY. When reset, the MAC's receiver is disabled and will not receive any frames from the PHY. If this bit is deasserted while a frame is being received, the received frames are allowed to complete. Upon completion, the MAC's receiver is disabled and the Receiver Disabled (RXD) bit is asserted.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Hardware prevents this field from being modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX).

3: This field is protected by Reset Protection (RST_PROTECT).

4: The maximum guaranteed supported frame size is 9,220 bytes.

5: Values for this field larger than 15360 are ineffective since the watchdog timer would take effect and truncate the frame at 15361.

6.1.3 MAC TRANSMIT REGISTER (MAC_TX)

Offset: 0108h
Size: 32 bits

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 132.

TABLE 132: MAC TRANSMIT REGISTER (MAC_TX) SPECIFICATIONS

Bit	Description	Type	Default
31:3	**RESERVED**	RO	—
2	**Bad FCS (BFCS)** When set, the MAC's transmitter will append a bad FCS on all transmitted frames. This feature is useful for diagnostic purposes. This function may only be used in conjunction with Insert FCS and Pad of TX Command A.	R/W NASR (**Note 1**)	0b
1	**Transmitter Disabled (TXD)** This bit indicates the MAC's transmitter has been successfully disabled via clearing the Transmitter Enable (TXEN) bit. It is set when the hardware disabling process, invoked by a transition of the Transmitter Enable (TXEN) bit from 1 to 0 (enabled to disabled), completes.	R/W1C NASR (**Note 1**)	0b
0	**Transmitter Enable (TXEN)** When set, the MAC's transmitter is enabled and it will transmit frames from the transmit buffer onto the cable. When reset, the MAC's transmitter is disabled and will not transmit any frames. If this bit is cleared while a frame is being transmitted, the frame is allowed to complete when in Full-Duplex mode. Upon completion, the MAC's transmitter is disabled and the Transmitter Disabled (TXD) bit is asserted. In Half-Duplex mode the frame shall be aborted if a collision is encountered while transmitting.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.4 FLOW CONTROL REGISTER (FLOW)

Offset: 010Ch
Size: 32 bits

This register is used to control the handling of the RX and TX flow control frames by the MAC.

RX flow control frames are received by the MAC. When RX flow control is enabled, the MAC will pause transmissions from the transmit datapath for the amount of time specified in the flow control frame.

TX flow control frames may be generated manually or automatically using RX FIFO thresholds. By setting the FORCE_FC bit, a flow control frame will be manually transmitted with the value specified by Pause Time (FCPT). After the frame is transmitted, the FORCE_FC bit clears.

Whenever TX_FCEN is set, transmit flow control frames are generated automatically, based on the thresholds set in the FCT Flow Control X Threshold Register (FCT_FLOW_X). Whenever the high watermark is crossed (RX Data FIFO Used Space (RXUSED)/512 greater than or equal to Flow Control On Threshold), the MAC transmits a flow control frame with the pause value specified by the Pause Time (FCPT) field. When the low watermark is subsequently crossed (RX Data FIFO Used Space (RXUSED)/512 less than or equal to Flow Control Off Threshold), the MAC transmits a flow control frame with a pause value of zero. See Table 133.

Note: Flow Control is only applicable when the MAC is set in Full-Duplex mode.

TABLE 133: FLOW CONTROL REGISTER (FLOW) SPECIFICATIONS

Bit	Description	Type	Default
31	**Force Transmission of TX Flow Control Frame (FORCE_FC)** This bit forces the transmission of a TX flow control frames. Writing a “1” initiates the frame transmission. The frame will be generated with the Pause Time value. After the frame is transmitted, the MAC will clear this bit.	R/W1S/SC	0b
30	**TX Flow Control Enable (TX_FCEN)** When set, this enables the transmit MAC flow control function based on high and low watermarks in the RX FIFO, as discussed in this section. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
29	**RX Flow Control Enable (RX_FCEN)** When set, enables the receive MAC flow control function. The MAC decodes all incoming frames for control frames. If it receives a valid control frame (PAUSE command), it disables the transmitter for a specified time (Decoded pause time x slot time). When not set, the MAC flow control function is disabled. The MAC does not decode frames for control frames.	R/W NASR (**Note 1**)	0b
28	**Forward Pause Frames (FPF)** Enables passing received pause frames to RX datapath interface. 0 = Sink received pause frames. 1 = Pass received pause frames to the RX datapath interface. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
27:16	**RESERVED**	RO	—
15:0	**Pause Time (FCPT)** This field indicates the value to be used in the PAUSE TIME field in the control frame.	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The threshold values in the FCT Flow Control X Threshold Register (FCT_FLOW_X) must be programmed before this bit is set. Conversely, this bit must be cleared before the threshold values in the FCT Flow Control X Threshold Register (FCT_FLOW_X) are programmed to 0.

3: Flow Control is applicable when the MAC is set in Full-Duplex mode.

6.1.5 RANDOM NUMBER SEED VALUE REGISTER (RAND_SEED)

Offset: 0110h
Size: 32 bits

See Table 134.

TABLE 134: RANDOM NUMBER SEED VALUE REGISTER (RAND_SEED) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**Random Number Seed (RAND_SEED)** This is the MAC random number generator seed value. The content of this register is the seed value for the LFSR (linear feedback shift register) counter used to emulate the random number generator in the MAC TX back-off timer logic.	R/W NASR (**Note 1**)	9876h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.6 ERROR STATUS REGISTER (ERR_STS)

Offset: 0114h
Size: 32 bits

Note:	Some bits in this register are new for LAN743x

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 135.

TABLE 135: ERROR STATUS REGISTER (ERR_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:11	**RESERVED**	RO	—
10	**Length Field Error (LEN_ERR)** Indicates that the frame length was inconsistent with the length value specified in the length/type field.	R/W1C NASR (**Note 1**)	0b
9	**RX Error (RXERR)** Indicates that a receive error (PHY RX error signal asserted) has been detected during frame reception. (See **Note 2**.)	R/W1C NASR (**Note 1**)	0b
8	**FCS Error (FERR)** An FCS errored frame has been received. This bit is set regardless of the frame length. (See **Note 3** and **Note 4**.)	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.
2: This bit will be set regardless of other error conditions (alignment, FCS, lengths, etc.).
3: This bit will not be set if the ALERR bit is set.
4: Only frames with an integer multiple of 8 bits are considered.

TABLE 135: ERROR STATUS REGISTER (ERR_STS) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
7	**Large Frame Error (LFERR)** A frame larger than the allowed maximum frame size has been received.	R/W1C NASR (**Note 1**)	0b
6	**Runt/Short Frame Error (RFERR)** A runt frame or a short frame has been received. This bit is set regardless of the FCS status.	R/W1C NASR (**Note 1**)	0b
5	**Receive Watchdog Timer Expired (RWTERR)** When set, this bit indicates the received frame was longer than 15,360 bytes and was truncated by the MAC.	R/W1C NASR (**Note 1**)	0b
4	**Excessive Collision Error (ECERR)** A transmit frame was aborted due to sixteen collisions occurring.	R/W1C NASR (**Note 1**)	0b
3	**Alignment Error (ALERR)** An alignment error (non-integer multiple of 8 bits and a bad FCS or an RX symbol error) has been detected on a received frame.	R/W1C NASR (**Note 1**)	0b
2	**Under Run Error (URERR)** The MAC has been under run by the transmit data-path.	R/W1C NASR (**Note 1**)	0b
1:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This bit will be set regardless of other error conditions (alignment, FCS, lengths, etc.).

3: This bit will not be set if the ALERR bit is set.

4: Only frames with an integer multiple of 8 bits are considered.

6.1.7 MAC RECEIVE ADDRESS HIGH REGISTER (RX_ADDRH)

Offset: 0118h
Size: 32 bits

This register contains the upper 16 bits of the physical address of the MAC, where RX_ADDRH[15:8] is the 6th octet of the received frame.

This register used to specify the address used for Perfect DA, Magic Packet and Wakeup frames, the unicast destination address for received pause frames, and the source address for transmitted pause frames. This register is not used for packet filtering. See Table 136.

TABLE 136: MAC RECEIVE ADDRESS HIGH REGISTER (RX_ADDRH)

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**Physical Address [47:32]** This field contains the upper 16 bits [47:32] of the physical address of the device. (See **Note 2**.)	R/W NALR NASR (**Note 1**)	FFFFh

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set.

2: This field is protected by Reset Protection (RST_PROTECT).

6.1.8 MAC RECEIVE ADDRESS LOW REGISTER (RX_ADDRL)

Offset: 011Ch
Size: 32 bits

Note:	This register contains the lower 32 bits of the physical address of the MAC, where RX_ADDRL[7:0] is the first octet of the Ethernet frame.

This register used to specify the address used for Perfect DA, Magic Packet, and Wakeup frames, the unicast destination address for received pause frames, and the source address for transmitted pause frames. This register is not used for packet filtering. See Table 137.

TABLE 137: MAC RECEIVE ADDRESS LOW REGISTER (RX_ADDRL) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Physical Address [31:0]** This field contains the lower 32 bits [31:0] of the physical address of the device. (See **Note 3**.)	R/W NALR NASR (**Note 1**)	FFFF_FFFFh (**Note 2**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set.

2: The default value of this field is determined by the value of the MAC Address filed contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then FFFF_FFFFh is the default. PCIe Resets will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3: This field is protected by Reset Protection (RST_PROTECT).

Table 138 illustrates the byte ordering of the RX_ADDRL and RX_ADDRH registers with respect to the reception of the Ethernet physical address.

TABLE 138: RX_ADDRL, RX_ADDRH BYTE ORDERING

RX_ADDRL, RX_ADDRH	Order of Reception on Ethernet
RX_ADDRL[7:0]	1st
RX_ADDRL[15:8]	2nd
RX_ADDRL[23:16]	3rd
RX_ADDRL[31:24]	4th
RX_ADDRH[7:0]	5th
RX_ADDRH[15:8]	6th

6.1.9 MII ACCESS REGISTER (MII_ACCESS)

Offset: 0120h
Size: 32 bits

This register is used to control the management cycles to the PHY. See Table 139.

TABLE 139: MII ACCESS REGISTER (MII_ACCESS) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:11	**PHY Address** This field specifies the PHY address. For the LAN7430, this field must be set to 00001b. For the LAN7431 and LAN743F, this field must be set to the address of the external PHY.	R/W NASR (**Note 1**)	00001b
10:6	**MII Register Index (MIIRINDA)** These bits select the desired MII register in the PHY.	R/W NASR (**Note 1**)	00000b
5:2	**RESERVED**	RO	—
1	**MII Write (MIIWnR)** Setting this bit tells the PHY that this will be a write operation using the MII data register. If this bit is not set, this will be a read operation, packing the data in the MII data register.	R/W NASR (**Note 1**)	0b
0	**MII Busy (MIIBZY)** This bit must be polled to determine when the MII register access is complete. This bit must read a logical 0 before writing to this register or to the MII data register. The LAN driver software must set (1) this bit in order for the Host to read or write any of the MII PHY registers. During a MII register access, this bit will be set, signifying a read or write access is in progress. The MII data register must be kept valid until the MAC clears this bit during a PHY write operation. The MII data register is invalid until the MAC has cleared this bit during a PHY read operation.	R/W1S/SC	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.10 MII DATA REGISTER (MII_DATA)

Offset: 0124h
Size: 32 bits

This register contains either the data to be written to the PHY register specified in the MII Access Register, or the read data from the PHY register whose index is specified in the PCIe PHY Access Register (PCIE_PHY_ACCESS). See Table 140.

Note: The PCIe PHY Busy (PCIE_PHY_BZY) bit in the PCIe PHY Access Register (PCIE_PHY_ACCESS) must be cleared when writing to this register.

TABLE 140: MII DATA REGISTER (MII_DATA) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**MII Data** This contains the 16-bit value read from the PHY read operation or the 16-bit data value to be written to the PHY before an MII write operation.	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.11 MAC RGMII INTERNAL DELAY REGISTER (MAC_RGMII_ID)

Offset: 0128h
Size: 32 bits

This CSR is used for enabling RGMII ID, internal delay mode when the device is operating with an external PHY. This CSR controls the MAC side delays. See Table 141.

TABLE 141: MAC RGMII INTERNAL DELAY REGISTER (MAC_RGMII_ID) SPECIFICATIONS

Bit	Description	Type	Default
31:2	**RESERVED**	RO	—
1	**RGMII TXC Delay Enable** Configures the RGMII TXC delay mode: 0 = RGMII TXC delay mode disabled 1 = RGMII TXC delay mode enabled (See **Note 3** and **Note 4**.)	R/W NASR (**Note 1**)	1b (**Note 2**)
0	**RGMII RXC Delay Enable** Configures the RGMII RXC delay mode: 0 = RGMII RXC delay mode disabled 1 = RGMII RXC delay mode enabled (See **Note 3** and **Note 4**.)	R/W NASR (**Note 1**)	0b (**Note 2**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is loaded from OTP or EEPROM. The default is used in the absence of a programmed OTP or EEPROM. PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

3: This bit only has meaning for the LAN7431.

4: This field is protected by Reset Protection (RST_PROTECT).

6.1.12 EEE TX LPI REQUEST DELAY COUNT REGISTER (EEE_TX_LPI_REQUEST_DELAY_CNT)

Offset: 0130h
Size: 32 bits

Contains the count corresponding to the amount of time, in µs, the MAC must wait after the TX FIFO is empty or after a Pause frame or ARP/NS response is transmitted before invoking the LPI protocol.

Whenever the TX FIFO is empty, the device checks the Energy Efficient Ethernet Enable (EEEEN) bit of the MAC Control Register (MAC_CR) to determine whether or not the Energy Efficient Ethernet mode of operation is in effect. If the bit is clear, no action is taken. Otherwise, the device waits the amount of time indicated in this register. After the wait period has expired, the LPI protocol is initiated and the Energy Efficient Ethernet Start TX Low Power Interrupt (EEE_START_TX_LPI_INT) bit of the FIFO Controller Interrupt Status Register (FCT_INT_STS) will be set.

Due to a 1 µs pre-scaler, the actual time can be up to 1 µs longer than specified.

Note:	A value of zero is valid and will not cause any delays.

If the TX FIFO becomes non-empty or the MAC autonomously sends a Pause frame or ARP/NS response, the timer is restarted. See Table 142.

TABLE 142: EEE TX LPI REQUEST DELAY COUNT REGISTER (EEE_TX_LPI_REQUEST_DELAY_CNT) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**EEE TX LPI Request Delay Count (EEE_TX_LPI_REQUEST_DELAY_CNT)** Count representing time to wait before invoking LPI protocol. Units are in µs. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. (See **Note 2**.)	R/W NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The time is in MAC TX Clock period increments when EEE Timer Speed Up (EEE_TIMER_SPEED_UP) is set.

6.1.13 EEE TIME WAIT TX SYSTEM REGISTER (EEE_TW_TX_SYS)

Offset: 0134h
Size: 32 bits

Contains the count corresponding to the amount of time, in µs, the MAC must wait after LPI is exited before it can transmit packets. Time is specified in separate fields for 100 Mbs and 1000 Mbs operation.

This wait time is in addition to the IPG time. See Table 143.

TABLE 143: EEE TIME WAIT TX SYSTEM REGISTER (EEE_TW_TX_SYS) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**EEE TIME Wait TX System Count 1000 (EEE_TW_TX_SYS_CNT_1000)** Count representing time to wait before commencing transmission after LPI is exited when operating at 1000 Mbs. Units are in 0.5 µs. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	000021h
15:0	**EEE TIME Wait TX System Count 100 (EEE_TW_TX_SYS_CNT_100)** Count representing time to wait before commencing transmission after LPI is exited when operating at 100 Mbs. Units are in µs. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. (See **Note 4** and **Note 5**.)	R/W NASR (**Note 1**)	00001Eh

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The time is in MAC TX clock period increments (8 ns) when EEE Timer Speed Up (EEE_TIMER_-SPEED_UP) is set.

3: In order to meet the IEEE 802.3 specified requirement, the minimum value of this field should be 000021h.

4: The time is in MAC TX clock period increments (40 ns) when EEE Timer Speed Up (EEE_TIMER_-SPEED_UP) is set.

5: In order to meet the IEEE 802.3 specified requirement, the minimum value of this field should be 00001Eh.

6.1.14 EEE TX LPI AUTOMATIC REMOVAL DELAY REGISTER (EEE_TX_LPI_AUTO_REMOVAL_DELAY)

Offset: 0138h
Size: 32 bits

Contains the count corresponding to the amount of time, in µs, the MAC will wait after the TX LPI protocol is initiated until it automatically de-asserts LPI in anticipation of a periodic transmission. TX LPI automatic removal functionality is enabled via the Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN) bit of the MAC Control Register (MAC_CR).

When this time period expires, the Energy Efficient Ethernet Stop TX Low Power Interrupt (EEE_STOP_TX_LPI_INT) bit of the FIFO Controller Interrupt Status Register (FCT_INT_STS) and the Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) bit of the Wakeup Control and Status Register 1 (WUCSR1) will be set.

Upon automatic TX LPI de-assertion, the MAC will return to waiting for the TX FIFO to be empty with no Pause or ARP/NS offload packets to be sent, for the time specified in EEE TX LPI Request Delay Count (EEE_TX_LPI_REQUEST_DELAY_CNT) before requesting LPI once again.

Note:	Due to a 1 µs pre-scaler, the actually time can be up to 1 µs longer than specified.

The MAC will generate LPI requests only when the Energy Efficient Ethernet Enable (EEEEN) bit of the MAC Control Register (MAC_CR) is set, the current speed is 100 Mbps or 1000 Mbps, the current duplex is full and the auto-negotiation result indicates that both the local and partner device support EEE at the current operating speed. See Table 144.

TABLE 144: EEE TX LPI AUTOMATIC REMOVAL DELAY REGISTER (EEE_TX_LPI_AUTO_REMOVAL_DELAY)

Bit	Description	Type	Default
31:24	**RESERVED**	RO	—
23:0	**EEE TX LPI Automatic Removal Delay Count (EEE_TX_LPI_AUTO_REMOVAL_DELAY_CNT)** Count representing time to wait after the TX LPI protocol is initiated until it is automatically de-asserted in anticipation of a periodic transmission. Units are in µs. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. (See **Note 2**.)	R/W NASR (**Note 1**)	000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The time is in MAC TX Clock period increments when EEE Timer Speed Up (EEE_TIMER_SPEED_UP) is set.

6.1.15 WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1)

Offset: 0140h
Size: 32 bits

This register contains data pertaining to the MAC's remote wakeup status and capabilities. All enables within this register must be clear during normal operation. Failure to do so will result in improper MAC receive operation. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 145.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1)

Bit	Description	Type	Default
31	**WUCSR Testmode** This tests bit enables the WUCSR logic to be tested while the device is in a state that does not support PME. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
30:21	**RESERVED**	RO	—
20	**Ignore Wake-up (IGNORE_WU)** When set, the wake up logic will be disabled. When the device changes from the D0a state to the D3 state, this bit automatically clears after the time specified by the Ignore Wake-up Auto Clear Time (IGNORE_WU_TIME) field. This bit also automatically clears when the device state changes and the new state is any non-D3 state.	R/W NASR (**Note 1**)	0b
19:16	**Ignore Wake-up Auto Clear Time (IGNORE_WU_TIME)** This field specifies the amount of time, upon the device entering the D3 state, after which the Ignore Wake-up (IGNORE_WU) bit automatically clears. 0: 0 ms (immediate) 1: 1 ms 2: 2 ms 3: 4 ms 4: 8 ms 5: 16 ms 6: 32 ms 7: 64 ms 8: 128 ms 9: 256 ms 10: 512 ms 11: 1024 ms 12: 2048 ms 13: 4096 ms 14: 8192 ms 15: 16384 ms **Note:** For all but the 0 setting, the actual time can be low by up to 1 µs.	R/W NASR (**Note 1**)	0h
15	**Discard Frames During D0a (DISCARD_FRAMES_D0A)** When set, the receive FCTs will discard frames while in the D0a state. As with the D3 state, the Store Wakeup Frame (STORE_WAKE) will allow wakeup and subsequent frames to be stored while in D0a. This bit automatically clears when the device state is not D0a.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1) (CONTINUED)

Bit	Description	Type	Default
14	**RFE Wake Enable (RFE_WAKE_EN)** When set, Remote Wakeup mode is enabled and the device is capable of generating a wakeup from a non-errored receive frame that passes the RFE's filters. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
13	**Energy Efficient Ethernet TX Wake (EEE_TX_WAKE)** The MAC sets this bit upon the transmitter exiting the Low Power Idle state due to the expiration of the time specified in EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY). This bit will not set if Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) is cleared. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/W1C NASR (**Note 1**)	0b
12	**Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN)** When set, remote wakeup is enabled upon the transmitter exiting the Low Power Idle state. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
11	**Energy Efficient Ethernet RX Wake (EEE_RX_WAKE)** The MAC sets this bit upon the receiver exiting Low Power Idle state due to the reception of wake signaling. This bit will not set if Energy Efficient Ethernet RX Wake (EEE_RX_WAKE) is cleared. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1) (CONTINUED)

Bit	Description	Type	Default
10	**Energy Efficient Ethernet RX Wake Enable (EEE_RX_WAKE_EN)** When set, remote wakeup is enabled upon reception of wake signaling. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
9	**RFE Wakeup Frame Received (RFE_WAKE_FR)** This bit is set upon reception of a non-errored frame that passes the RFE filters. This bit will not set if RFE Wake Enable (RFE_WAKE_EN) is cleared. This bit will not set if either: Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) are already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b
8	**Store Wakeup Frame (STORE_WAKE)** When set, the frame associated with a wake event is stored in the FCT RX FIFO. All subsequents frames received after the wake event which are not corrupted and pass any applicable frame filters in the MAC and RFE are stored in the FIFO. When cleared, only frames received after the wake event are stored in the RX FIFO. The frames must not be corrupted and pass any applicable frame filters in the MAC and RFE. (See **Note 3**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1) (CONTINUED)

Bit	Description	Type	Default
7	**Perfect DA Frame Received (PFDA_FR)** The MAC sets this bit upon receiving a valid frame with a destination address that matches the physical address. This bit will not set if Perfect DA Wakeup Enable (PFDA_EN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) are already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b
6	**Remote Wakeup Frame Received (WUFR)** The MAC sets this bit upon receiving a valid remote Wakeup Frame. This bit will not set if Wakeup Frame Enable (WUEN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) are already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1) (CONTINUED)

Bit	Description	Type	Default
5	**Magic Packet Received (MPR)** The MAC sets this bit upon receiving a valid Magic Packet. This bit will not set if Magic Packet Enable (MPEN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Broadcast Frame Received (BCAST_FR) IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) are already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b
4	**Broadcast Frame Received (BCAST_FR)** The MAC Sets this bit upon receiving a valid broadcast frame. This bit will not set if Broadcast Wakeup Enable (BCAST_EN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) are already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b
3	**Perfect DA Wakeup Enable (PFDA_EN)** When set, remote wakeup mode is enabled and the MAC is capable of waking up on receipt of a frame with a destination address that matches the physical address of the device. The physical address is stored in the MAC Receive Address High Register (RX_ADDRH) and MAC Receive Address Low Register (RX_ADDRL). This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

TABLE 145: WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1) (CONTINUED)

Bit	Description	Type	Default
2	**Wakeup Frame Enable (WUEN)** When set, remote wakeup mode is enabled and the MAC is capable of detecting Wakeup Frames as programmed in the Wakeup Frame Filter. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
1	**Magic Packet Enable (MPEN)** When set, Magic Packet wakeup mode is enabled. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
0	**Broadcast Wakeup Enable (BCAST_EN)** When set, remote wakeup mode is enabled and the MAC is capable of waking up from a broadcast frame. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

3: It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO.

6.1.16 WAKEUP SOURCE REGISTER (WK_SRC)

Offset: 0144h
Size: 32 bits

This register indicates the source of the wakeup event that resulted in the device issuing PME/wakeup signaling. Any wake events that occur before the device is enabled for PME generation are ignored. Additionally, any wake events that occur after the device has commenced the process of waking up are likewise ignored.

It is possible for a received wakeup packet to match several of the conditions listed in this CSR. In that case, all matching bits for that packet shall be set. The status fields in this CSR are not cleared until explicitly done so by SW.

During reset handling of this register, if the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 146.

TABLE 146: WAKEUP SOURCE REGISTER (WK_SRC) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**GPIO [11:0] (GPIOx_INT_WK)** These bits assert from a GPIO wake event that results in the device issuing wakeup signaling. These bits are set when a corresponding GPIO Interrupt (GPIO_INT) bit is set. These bits will not set if the corresponding GPIO Wake 0-11 (GPIOWK[11:0]) is cleared. (See **Note 2**.)	R/W1C NASR (**Note 1**)	000h
19:18	**RESERVED**	RO	—
17	**Ethernet PHY Wakeup (ETH_PHY_WK)** This bit is set upon a Ethernet PHY interrupt, typically configured to indicate link change or energy detection, that results in the device issuing wakeup signaling. This bit is set if WUPS[0] is set. This bit will not set if the Ethernet PHY Interrupt and EDPD Enable (ETH_PHY_WAKE_EN) bit is cleared.	R/W1C NASR (**Note 1**)	0b
16	**IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD_WK)** The MAC sets this bit upon receiving a valid IPv6 TCP SYN packet that results in the device issuing wakeup signaling. This bit is set if IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) is set.	R/W1C NASR (**Note 1**)	0b
15	**IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD_WK)** The MAC sets this bit upon receiving a valid IPv4 TCP SYN packet that results in the device issuing wakeup signaling. This bit is set if IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) is set.	R/W1C NASR (**Note 1**)	0b
14	**Energy Efficient Ethernet TX Wake (EEE_TX_WK)** The MAC sets this bit upon the transmitter exiting the Low Power Idle state due to the expiration of the time specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT). This bit will not set if Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) is cleared. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The number of available GPIOs varies by SKU and although the register bits remain R/W1C, the non-existent GPIOs should never set their corresponding bits.

TABLE 146: WAKEUP SOURCE REGISTER (WK_SRC) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
13	**Energy Efficient Ethernet RX Wake (EEE_RX_WK)** The MAC sets this bit upon the receiver exiting Low Power Idle state due to the reception of wake signaling. This bit will not set if Energy Efficient Ethernet RX Wake Enable (EEE_RX-_WAKE_EN) is cleared. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/W1C NASR (**Note 1**)	0b
12	**RFE Wakeup Frame Received (RFE_FR_WK)** This bit is set bit upon reception of a non-errored frame that passes the RFE's filters and results in the device issuing wakeup signaling. This bit is set if RFE Wakeup Frame Received (RFE_WAKE_FR) is set.	R/W1C NASR (**Note 1**)	0b
11	**Perfect DA Frame Received (PFDA_FR_WK)** The MAC sets this bit upon receiving a valid frame with a destination address that matches the physical address that results in the device issuing wakeup signaling. This bit is set if Perfect DA Frame Received (PFDA_FR) is set.	R/W1C NASR (**Note 1**)	0b
10	**Magic Packet Received (MP_FR_WK)** The MAC sets this bit upon receiving a valid Magic Packet that results in the device issuing wakeup signaling. This bit is set if Magic Packet Received (MPR) is set.	R/W1C NASR (**Note 1**)	0b
9	**Broadcast Frame Received (BCAST_FR_WK)** The MAC Sets this bit upon receiving a valid broadcast frame that results in the device issuing wakeup signaling. This bit is set if Broadcast Frame Received (BCAST_FR) is set.	R/W1C NASR (**Note 1**)	0b
8	**Remote Wakeup Frame Received (WU_FR_WK)** The MAC sets this bit upon receiving a valid remote Wakeup Frame that results in the device issuing wakeup signaling. This bit is set if Remote Wakeup Frame Received (WUFR) is set.	R/W1C NASR (**Note 1**)	0b
7	**Wakeup Frame Saved (WK_FR_SAVED)** This bit indicates that the Wakeup Frame was saved in a RX FIFO.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The number of available GPIOs varies by SKU and although the register bits remain R/W1C, the non-existent GPIOs should never set their corresponding bits.

TABLE 146: WAKEUP SOURCE REGISTER (WK_SRC) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
6:5	**Wakeup Frame Save Channel (WK_FR_SAVE_RX_CH)** This field indicates which RX FIFO contains the Wakeup Frame. The contents of this field are only valid when Wakeup Frame Saved (WK_FR_SAVED) is set. This field is not overwritten if Wakeup Frame Saved (WK_FR_SAVED) was already set.	RO NASR (**Note 1**)	00b
4:0	**Remote Wakeup Frame Match (WUFF_MATCH)** This field indicates which wakeup frame filter caused the wakeup event. The contents of this field are only valid when Remote Wakeup Frame Received (WU_FR_WK) is set.	RO NASR (**Note 1**)	00000b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The number of available GPIOs varies by SKU and although the register bits remain R/W1C, the non-existent GPIOs should never set their corresponding bits.

6.1.17 WAKEUP FILTER X CONFIGURATION REGISTER (WUF_CFGX)

Offset: 0150h – 01CCh
Size: 32 bits

These CSRs enable the respective wakeup filter to be enabled. A total of 32 programmable filters are available in this device where each filter can match a pattern up to 128 bytes in length. See Table 147.

Note:	WUF_CFG0 supports Reset Protection (RST_PROTECT).

TABLE 147: WAKEUP FILTER X CONFIGURATION REGISTER (WUF_CFGX) SPECIFICATIONS

Bit	Description	Type	Default
31	**Filter Enable** 0b: Filter disabled 1b: Filter enabled	R/W NASR (**Note 1**	0b (**Note 2**)
30:26	**RESERVED**	RO	—
25:24	**Filter Address Type** Defines the destination address type of the pattern (as specified for filter *x* in the Wakeup Filter x Byte Mask Registers (WUF_MASKx) block). 00b: Pattern applies only to unicast frames. 10b: Pattern applies only to multicast frames. X1b: Pattern applies to all frames.	R/W NASR (**Note 1**)	00b (**Note 2**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. For WUF_CFG0, *PCIe Resets* or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

TABLE 147: WAKEUP FILTER X CONFIGURATION REGISTER (WUF_CFGX) SPECIFICATIONS

Bit	Description	Type	Default
23:16	**Filter Pattern Offset** Specifies the offset of the first byte in the frame on which CRC checking begins for Wakeup Frame recognition. Offset 0 is the first byte of the incoming frame's destination address.	R/W NASR (**Note 1**)	00h (**Note 2**)
15:0	**Filter CRC-16** Specifies the expected 16-bit CRC value for the filter that should be obtained by using the pattern offset and the byte mask programmed for the filter. This value is compared against the CRC calculated on the incoming frame, and a match indicates the reception of a Wakeup Frame.	R/W NASR (**Note 1**)	0000h (**Note 2**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. For WUF_CFG0, *PCIe Resets* or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

6.1.18 WAKEUP FILTER *X* BYTE MASK REGISTERS (WUF_MASK*X*)

Offset: 0200h – 03FCh
Size: 32 bits

Each of the 32 wakeup filters has a 128-bit byte mask. The 128-bit mask is accessed via 4 consecutive byte mask (DWORD) registers. The DWORD offset required to access a particular portion of the mask is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit filter block is the first element in the range indicated in the preceding table and in the register map (See Table 128.)

If bit j of the byte mask is set, the CRC machine processes byte *pattern offset + j* of the incoming frame. Otherwise, byte *pattern offset + j* is ignored. See Table 148.

Note: WUF_MASK0 supports Reset Protection (RST_PROTECT).

TABLE 148: WAKEUP FILTER *X* BYTE MASK REGISTERS (WUF_MASK*X*) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
00h	31:0	**Filter *x* Byte Mask [31:0]**	R/W NASR (**Note 2**)	0h (**Note 1**)
01h	31:0	**Filter *x* Byte Mask [63:32]**	R/W NASR (**Note 2**)	0h (**Note 1**)
02h	31:0	**Filter *x* Byte Mask [95:64]**	R/W NASR (**Note 2**)	0h (**Note 1**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. For WUF_MASK0, PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

TABLE 148: WAKEUP FILTER *X* BYTE MASK REGISTERS (WUF_MASK*X*) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
03h	31:0	**Filter *x* Byte Mask [127:96]**	R/W NASR (**Note 2**)	0h (**Note 1**)

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The EEPROM format does not assign fixed location to set the default values. However, these registers may optionally be initialized by EEPROM or OTP by using the EEPROM User Initialization Table. For WUF_MASK0, PCIe Resets or a Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to the default if neither was available.

6.1.19 WAKEUP CONTROL AND STATUS REGISTER 2 (WUCSR2)

Offset: 0600h
Size: 32 bits

Note: Some bits in this register are new for LAN743x.

All enables within this register must be clear during normal operation. Failure to do so will result in improper MAC receive and/or transmit operation. See Table 149.

TABLE 149: WAKEUP CONTROL AND STATUS REGISTER 2 (WUCSR2) SPECIFICATIONS

Bit	Description	Type	Default
31	**Checksum Disable (CSUM_DISABLE)** When clear, the IP header checksum, TCP checksum, ICMP payload checksum, and FCS are calculated and all must agree with the frame contents, in order for the frame (TCP_SYN, or NS) to be considered for detection analysis. When set, only the FCS is calculated and checked for TCP_SYN, and NS frames. The IP header checksum, ICMP payload checksum, and TCP checksum are not calculated. Hence, any mismatches are ignored. (See **Note 2.**)	R/W NASR (**Note 1**)	0b
30	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the TCP checksum for TCP SYN frames. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not verified. When set, IPv6 Routing headers other than type 0 and 2 are skipped if the Segments Left field in the header is zero. Otherwise, the checksum is not verified. (See **Note 2**.)	R/W NASR (**Note 1**)	*0b*
29:11	**RESERVED**	RO	—
10	**Forward ARP Frames (FARP_FR)** Enables passing received ARP frames that target this device and were processed by the ARP offload logic to the RX datapath interface. 0 = Sink received ARP frames. 1 = Pass received ARP frames to the RX datapath interface.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

TABLE 149: WAKEUP CONTROL AND STATUS REGISTER 2 (WUCSR2) SPECIFICATIONS

Bit	Description	Type	Default
9	**Forward NS Frames (FNS_FR)** Enables passing received NS frames that target this device and were processed by the NS offload logic to the RX datapath interface. 0 = Sink received NS frames. 1 = Pass received NS frames to the RX datapath interface.	R/W NASR (**Note 1**)	0b
8	**NA SA Select (NA_SA_SEL)** Used to select source for IPv6 SA in NA message. When set, NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) value is used as the source. When cleared, the Target Address in NS packet is used.	R/W NASR (**Note 1**)	0b
7	**NS Packet Received (NS_RCD)** The MAC sets this bit upon receiving a valid NS packet.	R/W1C NASR (**Note 1**)	0b
6	**ARP Packet Received (ARP_RCD)** The MAC sets this bit upon receiving a valid ARP packet.	R/W1C NASR (**Note 1**)	0b
5	**IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD)** The MAC sets this bit upon receiving a valid IPv6 TCP SYN packet. This bit will not set if IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) or IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) is already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

TABLE 149: WAKEUP CONTROL AND STATUS REGISTER 2 (WUCSR2) SPECIFICATIONS

Bit	Description	Type	Default
4	**IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD)** The MAC sets this bit upon receiving a valid IPv4 TCP SYN packet. This bit will not set if IPv4 TCP SYN Wake Enable (IPV4_TCPSYN-_WAKE_EN) is cleared. This bit will not set if either: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) or IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) is already set. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/W1C NASR (**Note 1**)	0b
3	**NS Offload Enable (NS_OFFLOAD_EN)** When set, this enables the response to Neighbor Solicitation packets.	R/W NASR (**Note 1**)	0b
2	**ARP Offload Enable (ARP_OFFLOAD_EN)** When set, this enables the response to ARP packets.	R/W NASR (**Note 1**)	0b
1	**IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN)** When set, this enables the wakeup on receiving an IPv6 TCP SYN packet. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2.**)	R/W NASR (**Note 1**)	0b
0	**IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN)** When set, this enables the wakeup on receiving an IPv4 TCP SYN packet. This bit is automatically cleared when the device sends the PM_PME message due to a wakeup event if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. (See **Note 2**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

6.1.20 MAC INTERRUPT STATUS REGISTER (MAC_INT_STS)

Offset: 0604h
Size: 32 bits

If the host attempts to clear a R/W1C bit within the MAC_INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding MAC_INT_STS bit will remain set. See Table 150.

TABLE 150: MAC INTERRUPT STATUS REGISTER (MAC_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—
26	**Energy Efficient Ethernet Start TX Low-Power Interrupt (EEE_START_TX_LPI_INT)** This interrupt is asserted when the transmitter enters Low-Power Idle mode due to the expiration of the time specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT). This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. (See **Note 2**.)	R/W1C NASR (**Note 1**	0b
25	**Energy Efficient Ethernet Stop TX Low-Power Interrupt (EEE_STOP_TX_LPI_INT)** This interrupt is asserted when the transmitter exits Low-Power Idle mode, due to the expiration of the time specified in the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY). This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. (See **Note 2**.)	R/W1C NASR (**Note 1**)	0b
24	**Energy Efficient Ethernet RX Low-Power Interrupt (EEE_RX_LPI_INT)** This interrupt is asserted when the receiver enters Low-Power Idle mode. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. (See **Note 2**.)	R/W1C NASR (**Note 1**)	0b
23	**MAC Reset Time Out (MACRTO_INT)** This interrupt signifies that the 8 ms reset watchdog timer has timed out. This means that the Ethernet PHY is not supplying RX and TX clocking to the MAC. After the timer times out, the MAC reset is deasserted asynchronously. (See **Note 2**.)	R/W1C NASR (**Note 1**)	0b
22:20	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The source of this interrupt is a pulse.

3: The source of this interrupt is a level and will persist until the source is cleared.

4: This is a level-triggered interrupt event that remains asserted until all the error event bits in the Error Status Register (ERR_STS) are cleared.

5: This is a level-triggered interrupt event that remains asserted until all the bits in the RX Counter Rollover Status are cleared.

6: This is a level-triggered interrupt event that remains asserted until all the bits in the TX Counter Rollover Status are cleared.

TABLE 150: MAC INTERRUPT STATUS REGISTER (MAC_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
19	**MAC TX Disabled Interrupt (MAC_TX_DIS_INT)** This interrupt is issued after the MAC transmitter has been successfully disabled. This interrupt persists while the Transmitter Disabled (TXD) bit of the MAC Transmit Register (MAC_TX) is set. (See **Note 3**.)	RO	0b
18	**MAC RX Disabled Interrupt (MAC_RX_DIS_INT)** This interrupt is issued after the MAC receiver has been successfully disabled. This interrupt persists while the Receiver Disabled (RXD) bit of the MAC Receive Register (MAC_RX) is set. (See **Note 3**.)	RO	0b
17:16	**RESERVED**	RO	—
15	**MAC Error Interrupt (MAC_ERR_INT)** This interrupt is set whenever any error condition tracked in the MAC's Error Status Register (ERR_STS) occurs. The application program can determine the specific error(s) that occurred by examining the Error Status Register (ERR_STS). (See **Note 4**.) This is a level-triggered interrupt event that remains asserted until all the error event bits in the Error Status Register (ERR_STS) are cleared.	RO	0b
14	**MAC RX Counter Rollover Interrupt (MAC_RX_CNT_ROLL_INT)** This interrupt is set whenever any RX counter rollover is indicated in the MAC's RX Counter Rollover status. (See **Note 5**.)	RO	0b
13	**MAC TX Counter Rollover Interrupt (MAC_TX_CNT_ROLL_INT)** This interrupt is set whenever any TX counter rollover is indicated in the MAC's TX Counter Rollover status. (See **Note 6**.)	RO	0b
12:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The source of this interrupt is a pulse.

3: The source of this interrupt is a level and will persist until the source is cleared.

4: This is a level-triggered interrupt event that remains asserted until all the error event bits in the Error Status Register (ERR_STS) are cleared.

5: This is a level-triggered interrupt event that remains asserted until all the bits in the RX Counter Rollover Status are cleared.

6: This is a level-triggered interrupt event that remains asserted until all the bits in the TX Counter Rollover Status are cleared.

6.1.21 MAC INTERRUPT ENABLE SET REGISTER (MAC_INT_EN_SET)

Offset: 0608h
Size: 32 bits

This register is used to set the interrupt enables for the corresponding bits in the FIFO Controller Interrupt Status Register (FCT_INT_STS). Writing a '1' to a bit sets the corresponding enable and configures the corresponding interrupt as a source for the assertion of the MAC interrupt. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables. See Table 151.

TABLE 151: MAC INTERRUPT ENABLE SET REGISTER (MAC_INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—
26	**Energy Efficient Ethernet Start TX Low Power Interrupt Enable Set (EEE_START_TX_LPI_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
25	**Energy Efficient Ethernet Stop TX Low Power Interrupt Enable Set (EEE_STOP_TX_LPI_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
24	**Energy Efficient Ethernet RX Low Power Interrupt Enable Set (EEE_RX_LPI_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
23	**MAC Reset Time Out Interrupt Enable Set (MACRTO_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
22:20	**RESERVED**	RO	—
19	**MAC TX Disabled Interrupt Enable Set (MAC_TX_DIS_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
18	**MAC RX Disabled Interrupt Enable Set (MAC_RX_DIS_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
17:16	**RESERVED**	RO	—
15	**MAC Error Interrupt Enable Set (MAC_ERR_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
14	**MAC RX Counter Rollover Interrupt Enable Set (MAC_RX_CNT_ROLL_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
13	**MAC TX Counter Rollover Interrupt Enable Set (MAC_TX_CNT_ROLL_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
12:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.22 MAC INTERRUPT ENABLE CLEAR REGISTER (MAC_INT_EN_CLR)

Offset: 060Ch
Size: 32 bits

This register is used to clear the interrupt enables for the corresponding bits in the FIFO Controller Interrupt Status Register (FCT_INT_STS). Writing a ‘1’ to a bit clears the corresponding enable. Writing a ‘0’ has no effect. A read of this register returns the state of the interrupt enables. See Table 152.

TABLE 152: MAC INTERRUPT ENABLE CLEAR REGISTER (MAC_INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:27	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 152: MAC INTERRUPT ENABLE CLEAR REGISTER (MAC_INT_EN_CLR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
26	**Energy Efficient Ethernet Start TX Low Power Interrupt Enable Clear (EEE_START_TX_LPI_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
25	**Energy Efficient Ethernet Stop TX Low Power Interrupt Enable Clear (EEE_STOP_TX_LPI_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
24	**Energy Efficient Ethernet RX Low Power Interrupt Enable Clear (EEE_RX_LPI_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
23	**MAC Reset Time Out Interrupt Enable Clear (MACRTO_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
22:20	**RESERVED**	RO	—
19	**MAC TX Disabled Interrupt Enable Clear (MAC_TX_DIS_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
18	**MAC RX Disabled Interrupt Enable Clear (MAC_RX_DIS_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
17:16	**RESERVED**	RO	—
15	**MAC Error Interrupt Enable Clear (MAC_ERR_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
14	**MAC RX Counter Rollover Interrupt Enable Clear (MAC_RX_CNT_ROLL_INT_EN_SET)**	R/W1C NASR (**Note 1**)	0b
13	**MAC TX Counter Rollover Interrupt Enable Clear (MAC_TX_CNT_ROLL_INT_EN_SET)**	R/W1C NASR (**Note 1**)	0b
12:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.23 NS*X* IPV6 DESTINATION ADDRESS REGISTER (NS*X*_IPV6_ADDR_DEST)

Offset: x = 0: 0610h – 061Ch
x = 1: 0650h – 065Ch
Size: 128 bits

Used in IPv6 NS header matching, each IPv6 destination address is 128-bits. The 128-bit address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map (See Table 128.).

These registers are used when NS Offload Enable (NS_OFFLOAD_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). Received packets whose Ethernet destination address is the device's MAC address, a multicast address, or the broadcast address are processed as follows:

1. The headers of all IPv6 packets are checked to determine whether NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) matches the destination address specified in the IPv6 header.
2. In the event that the IPv6 header destination address is a solicited node multicast address (i.e. it has a prefix that matches FF02::1:FF00:0/104), only the upper three bytes (NSx_IPv6_ADDR_DEST_3 [127:104]) are compared against the last 24 bits of the IPv6 header destination address.

There are two sets of NSx IPv6 Destination Address Registers, x = 0 and x = 1. Each set is compared and combined with the results of other comparisons within that set. See Table 153.

TABLE 153: NS*X* IPV6 DESTINATION ADDRESS REGISTER (NS*X*_IPV6_ADDR_DEST) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
00h	31:0	**NS*x*_IPv6_ADDR_DEST_0 [31:0]**	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**NS*x*_IPv6_ADDR_DEST_1 [63:32]**	R/W NASR (**Note 1**)	0000_0000h
02h	31:0	**NS*x*_IPv6_ADDR_DEST_2 [95:64]**	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**NS*x*_IPv6_ADDR_DEST_3 [127:96]**	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

TABLE 154: IPV6 ADDRESS TRANSMISSION BYTE ORDERING

NS*x*_IPV6_ADDR_DEST_X	IPv6 Address	Order of Reception on Ethernet
NSx_IPv6_ADDR_DEST_3[31:24]	[127:120]	1st
NSx_IPv6_ADDR_DEST_3[23:16]	[119:112]	2nd
NSx_IPv6_ADDR_DEST_3[15:8]	[111:104]	3rd
NSx_IPv6_ADDR_DEST_3[7:0]	[103:96]	4th
NSx_IPv6_ADDR_DEST_2[31:24]	[95:88]	5th
NSx_IPv6_ADDR_DEST_2[23:16]	[87:80]	6th
NSx_IPv6_ADDR_DEST_2[15:8]	[79:72]	7th
NSx_IPv6_ADDR_DEST_2[7:0]	[71:64]	8th

TABLE 154: IPV6 ADDRESS TRANSMISSION BYTE ORDERING (CONTINUED)

NS*x*_IPV6_ADDR_DEST_X	IPv6 Address	Order of Reception on Ethernet
NSx_IPv6_ADDR_DEST_1[31:24]	[63:56]	9th
NSx_IPv6_ADDR_DEST_1[23:16]	[55:48]	10th
NSx_IPv6_ADDR_DEST_1[15:8]	[47:40]	11th
NSx_IPv6_ADDR_DEST_1[7:0]	[39:32]	12th
NSx_IPv6_ADDR_DEST_0[31:24]	[31:24]	13th
NSx_IPv6_ADDR_DEST_0[23:16]	[23:16]	14th
NSx_IPv6_ADDR_DEST_0[15:8]	[15:8]	15th
NSx_IPv6_ADDR_DEST_0[7:0]	[7:0]	16th

This example applies to all other IPv6 address CSRs.

6.1.24 NS*X* IPV6 SOURCE ADDRESS REGISTER (NS*X*_IPV6_ADDR_SRC)

Offset: x = 0:0620h – 062Ch
x = 1:0660h – 066Ch
Size: 128 bits

Used in IPv6 NS header matching, each IPv6 source address is 128-bits. The 128-bit address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map. (See Table 128.)

These registers are used when NS Offload Enable (NS_OFFLOAD_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). Received packets whose destination address is the device's MAC address, a multicast address, or the broadcast address are processed as follows:

1. The headers of all IPv6 packets are checked to determine whether NSx IPv6 Source Address Register (NSx-_IPV6_ADDR_SRC) matches the source address specified in the IPv6 header.
2. There are two sets of NSx IPv6 Source Address Registers, x = 0 and x = 1. Each set is compared and combined with the results of other comparisons within that set. See Table 155.

Note:	A value of all 0's in all 4 DWORD registers = wild-card, causes checking to be ignored, and yields a match.

TABLE 155: NSX IPV6 SOURCE ADDRESS REGISTER (NSX_IPV6_ADDR_SRC) SPECIFICATIONS

DWORD Offset	Bits	Description	Type	Default
00h	31:0	**NS*x*_IPv6_ADDR_SRC_0 [31:0]**	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**NS*x*_IPv6_ADDR_SRC_1 [63:32]**	R/W NASR (**Note 1**)	0000_0000h
02h	31:0	**NS*x*_IPv6_ADDR_SRC_2 [95:64]**	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**NS*x*_IPv6_ADDR_SRC_3 [127:96]**	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

6.1.25 NS*X* ICMPV6 ADDRESS 0 REGISTER (NS*X*_ICMPV6_ADDR0)

Offset: x = 0:0630h – 063Ch
x = 1:0670h – 067Ch

Size: 128 bits

Used in ICMPv6 NS target address matching. Each address is 128-bits and is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map. (See Table 128.)

NS offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2).

The target address specified in the NS request is compared to the values contained in the NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) (these registers) and the corresponding NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1).

There are two sets of NSx ICMPv6 Address 0 Registers and two sets of NSx ICMPv6 Address 1 Registers, x = 0 and x = 1. Each set is compared and combined with the results of other comparisons within that set. See Table 156.

Note:	A value of all 0's in all 4 DWORD registers disables the comparison with this field. No match is yielded.

TABLE 156: NSX ICMPV6 ADDRESS 0 REGISTER (NSX_ICMPV6_ADDR0) SPECIFICATIONS

DWORD Offset	Bits	Description	Type	Default
00h	31:0	**NS*x*_ICMPV6_ADDR0_0[31:0]**	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**NS*x*_ICMPV6_ADDR0_1[63:32]**	R/W NASR (**Note 1**)	0000_0000h
02h	31:0	**NS*x*_ICMPV6_ADDR0_2[95:64]**	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**NS*x*_ICMPV6_ADDR0_3[127:96]**	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

6.1.26 NS*X* ICMPV6 ADDRESS 1 REGISTER (NS*X*_ICMPV6_ADDR1)

Offset: x = 0: 0640h – 064Ch
x = 1: 0680h – 068Ch

Size: 128 bits

Refer to the NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) for a description of the usage of this register. See Table 157.

Note:	A value of all 0's in all 4 DWORD registers disables the comparison with this field. No match is yielded.

TABLE 157: NSX ICMPV6 ADDRESS 1 REGISTER (NSX_ICMPV6_ADDR1) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
00h	31:0	**NS*x*_ICMPV6_ADDR1_0[31:0]**	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**NS*x*_ICMPV6_ADDR1_1[63:32]**	R/W NASR (**Note 1**)	0000_0000h
02h	31:0	**NS*x*_ICMPV6_ADDR1_2[95:64]**	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**NS*x*_ICMPV6_ADDR1_3[127:96]**	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

6.1.27 SYN IPV4 SOURCE ADDRESS REGISTER (SYN_IPV4_ADDR_SRC)

Offset: 0690h
Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the source address to be compared to that of received IPv4 headers prefixing TCP packets whose SYN bit is asserted.

IPv4 frames whose destination address is the device's MAC address, a multicast address, or the broadcast address are processed by having a check made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN-_IPV4_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS), will cause a wakeup. See Table 158.

TABLE 158: SYN IPV4 SOURCE ADDRESS REGISTER (SYN_IPV4_ADDR_SRC) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**SYN IPv4 Source Address [31:0]** Used in IPv4 header matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.

3: This field is protected by Reset Protection (RST_PROTECT).

The ordering for transmission of an IPv4 address over Ethernet is illustrated in Table 159.

TABLE 159: IPV4 ADDRESS TRANSMISSION BYTE ORDERING

SYN_IPV4_ADDR_SRC	IPv4 Address	Order of Reception on Ethernet
SYN_IPV4_ADDR_SRC[31:24]	[31:24]	1st
SYN_IPV4_ADDR_SRC[23:16]	[23:16]	2nd
SYN_IPV4_ADDR_SRC[15:8]	[15:8]	3rd
SYN_IPV4_ADDR_SRC[7:0]	[7:0]	4th

This example applies to all other IPv4 address CSRs.

6.1.28 SYN IPV4 DESTINATION ADDRESS REGISTER (SYN_IPV4_ADDR_DEST)

Offset: 0694h
Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the destination address to be compared to that of received IPv4 headers prefixing TCP packets whose SYN bit is asserted.

IPv4 frames whose destination address is the device's MAC address, a multicast address, or the broadcast address are processed by having a check made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN-_IPV4_ADDR_DEST), and whose source port and destination port match those specified by SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS), will cause a wakeup.

See Table 160.

TABLE 160: SYN IPV4 DESTINATION ADDRESS REGISTER (SYN_IPV4_ADDR_DEST) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**SYN IPv4 Destination Address[31:0]** Used in IPv4 heading matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.

3: This field is protected by Reset Protection (RST_PROTECT).

The ordering for transmission of an IPv4 address over Ethernet is illustrated in Table 159.

6.1.29 SYN IPV4 TCP PORTS REGISTER (SYN_IPV4_TCP_PORTS)

Offset: 0698h
Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the source and destination ports to be compared to that of received TCP packets whose SYN bit is asserted that are prefixed by a IPv4 header.

IPv4 frames whose destination address is the device's MAC address, a multicast address, or the broadcast address are processed by having a check made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN

IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN-_IPV4_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS), will cause a wakeup.

See Table 161.

TABLE 161: SYN IPV4 TCP PORTS REGISTER (SYN_IPV4_TCP_PORTS) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**Destination Port (IPV4_DEST_PORT)** Used in IPv4 TCP port matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000h
15:0	**Source Port (IPV4_SRC_PORT)** Used in IPv4 TCP port matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.

3: This field is protected by Reset Protection (RST_PROTECT).

6.1.30 SYN IPV6 SOURCE ADDRESS REGISTER (SYN_IPV6_ADDR_SRC)

Offset: 069Ch – 06A8h
Size: 128 bits

This register is used in IPv6 header matching for TCP SYN packets and is 128-bit. The address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for the 128-bit address block is the first element in the range indicated in the preceding table and in the register map. (See Table 128.)

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the source address to be compared to that of the IPv6 header (or an extension header) prefixing a TCP packet whose SYN bit is asserted. The IPv6 frame must have previously passed a check to ensure that its destination address is the device's MAC address, a multicast address, or the broadcast address.

Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified by the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup.

See Table 162.

Note: A value of all 0's in all 4 DWORD registers = wild-card, causes checking to be ignored, and yields a match.

TABLE 162: SYN IPV6 SOURCE ADDRESS REGISTER (SYN_IPV6_ADDR_SRC) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
00h	31:0	**SYN_IPV6_ADDR_SRC_0[31:0]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**SYN_IPV6_ADDR_SRC_1[63:32]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

TABLE 162: SYN IPV6 SOURCE ADDRESS REGISTER (SYN_IPV6_ADDR_SRC) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
02h	31:0	**SYN_IPV6_ADDR_SRC_2[95:64]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**SYN_IPV6_ADDR_SRC_3 [127:96]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

6.1.31 SYN IPV6 DESTINATION ADDRESS REGISTER (SYN_IPV6_ADDR_DEST)

Offset: 06ACh-06B8h
Size: 128 bits

This register is used in IPv6 header matching for TCP SYN packets and is 128-bits. The address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for the 128-bit address block is the first element in the range indicated in the preceding table and in the register map. (See Table 128.)

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the destination address to be compared to that of the IPv6 header (or an extension header) prefixing a TCP packet whose SYN bit is asserted. The IPv6 frame must have previously passed a check to ensure that its destination address is the device's MAC address, a multicast address, or the broadcast address.

Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified by the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup.

See Table 163.

Note: A value of all 0's in all 4 DWORD registers = wild-card, causes checking to be ignored, and yields a match.

TABLE 163: SYN IPV6 DESTINATION ADDRESS REGISTER (SYN_IPV6_ADDR_DEST) SPECIFICATIONS

DWORD Offset	Bit	Description	Type	Default
00h	31:0	**SYN_IPV6_ADDR_DEST_0 [31:0]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h
01h	31:0	**SYN_IPV6_ADDR_DEST_1 [63:32]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h
02h	31:0	**SYN_IPV6_ADDR_DEST_2 [95:64]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h
03h	31:0	**SYN_IPV6_ADDR_DEST_3 [127:96]** (See **Note 2**.)	R/W NASR (**Note 1**)	0000_0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This field is protected by Reset Protection (RST_PROTECT).

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 154.

6.1.32 SYN IPV6 TCP PORTS REGISTER (SYN_IPV6_TCP_PORTS)

Offset: 06BCh
Size: 32 bits

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). It holds the source and destination ports to be compared to that of received TCP packets whose SYN bit is asserted that are prefixed by a IPv6 header or extension header.

IPv6 frames whose destination address is the device's MAC address, a multicast address, or the broadcast address are processed by having a check made for a TCP protocol match within the IPv6 header. Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified in the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN-_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup. See Table 164.

TABLE 164: SYN IPV6 TCP PORTS REGISTER (SYN_IPV6_TCP_PORTS) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**Destination Port (IPV6_DEST_PORT)** Used in IPv6 TCP port matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000h
15:0	**Source Port (IPV6_SRC_PORT)** Used in IPv6 TCP port matching for TCP SYN packets. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.
2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.
3: This field is protected by Reset Protection (RST_PROTECT).

6.1.33 ARP SENDER PROTOCOL ADDRESS REGISTER (ARP_SPA)

Offset: 06C0h
Size: 32 bits

This register is utilized when ARP offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2). The frame type for all received Ethernet frames is examined and those of type 0806h (ARP frames) are checked to ensure that the MAC destination address matches the device's MAC address or is the broadcast address. If the packet passes these tests, the contents of this register are compared to the SPA field of the ARP message and the contents of the ARP Target Protocol Address Register (ARP_TPA) are compared to the TPA field of the ARP message. If the contents of both registers match the contents of the message and no errors occurred on the frame, then the MAC TX is signaled to transmit an ARP response frame to the sender. See Table 165.

TABLE 165: ARP SENDER PROTOCOL ADDRESS REGISTER (ARP_SPA) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**ARP_SPA[31:0]** Used in ARP matching. (See **Note 2**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.
2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.

The ordering for transmission of an IPv4 address over Ethernet is illustrated in Table 159.

6.1.34 ARP TARGET PROTOCOL ADDRESS REGISTER (ARP_TPA)

Offset: 06C4h
Size: 32 bits

This register is utilized when ARP offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2). The frame type for all received Ethernet frames is examined and those of type 0806h (ARP frames) are checked to ensure that the MAC destination address matches the device's MAC address or is the broadcast address. If the packet passes these tests, the contents of the ARP Sender Protocol Address Register (ARP_SPA) is compared to the SPA field of the ARP message and the contents of the this register is compared to the TPA field of the ARP message. If the contents of both registers match the contents of the message and no errors occurred on the frame, then the MAC TX is signaled to transmit an ARP response frame to the sender. See Table 166.

TABLE 166: ARP TARGET PROTOCOL ADDRESS REGISTER (ARP_TPA) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**ARP_TPA[31:0]** Used in ARP matching. (See **Note 2**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A value of all 0's = wild-card, causes checking to be ignored, and yields a match.

The ordering for transmission of an IPv4 address over Ethernet is illustrated in Table 159.

6.1.35 RX FCS ERRORS

Offset: 1200h
Size: 32 bits

See Table 167.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.

This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 167: RX FCS ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX FCS Errors** Number of frames received with CRC-32 errors or RX symbol errors. (See **Note 2**, **Note 3**, and **Note 4**.)	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Only frames with an integer multiple of 8 bits are considered for FCS errors.

3: If a frame has a Jabber Error and FCS error, only the RX Jabber Errors counter will be incremented.

4: If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.

6.1.36 RX ALIGNMENT ERRORS

Offset: 1204h
Size: 32 bits

See Table 168.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 168: RX ALIGNMENT ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Alignment Errors** Number of RX frames received with a non-integer multiple of 8 bits and a bad FCS or an RX symbol error.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.37 RX FRAGMENT ERRORS

Offset: 1208h
Size: 32 bits

See Table 169.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 169: RX FRAGMENT ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Fragment Errors** Number of frames received that are < 64 bytes in size and have an FCS error or RX symbol error. If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.38 RX JABBER ERRORS

Offset: 120Ch
Size: 32 bits

See Table 170.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 170: RX JABBER ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Jabber Errors** Number of frames received with a length greater than Maximum Frame Size (MAX_SIZE) and have FCS errors or RX errors. (See **Note 2** and **Note 3**.)	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The existence of extra bits does not trigger a jabber error. A jabber error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received

3: If a frame has a Jabber Error and an FCS error, only the RX Jabber Errors counter will be incremented.

6.1.39 RX UNDERSIZED FRAME ERRORS

Offset: 1210h
Size: 32 bits

See Table 171.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 171: RX UNDERSIZED FRAME ERRORS

Bit	Description	Type	Default
31:0	**RX Undersized Frame Errors** Number of frames received with a length less than 64 bytes. No other errors have been detected in the frame.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.40 RX OVERSIZED FRAME ERRORS

Offset: 1214h
Size: 32 bits

See Table 172.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 172: RX OVERSIZED FRAME ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Oversized Frame Errors** Number of frames received with a length greater than the programmed maximum Ethernet frame size (Maximum Frame Size (MAX_SIZE) field of the MAC Receive Register (MAC_RX). No other errors have been detected in the frame. (See **Note 2** and **Note 3**.) The existence of extra bits does not trigger an oversize error. An oversize error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The VLAN Frame Size Enforcement (FSE) bit allows for the maximum legal size to be increased by 4-bytes to account for a single VLAN tag or 8-bytes to account for stacked VLAN tags.

3: The MAC determines a VLAN tag is present if the type field is equal to 8100h or the value programmed in the VLAN Type Register (VLAN_TYPE).

6.1.41 RX DROPPED FRAMES

Offset: 1218h
Size: 32 bits

See Table 173.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 173: RX DROPPED FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Dropped Frames** Number of RX frames dropped by the FCT due to insufficient room in the RX FIFO. (See **Note 2** and **Note 3**.) As the packet is written into all four FIFOs until rejected from all but the final destination, a frame is only counted as dropped if the full FIFO was that of destined RX channel.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: If a frame to be dropped has an Ethernet error, it will be counted in the relevant bad frame counter. The RX Dropped Frames counter will be incremented for the errored frame only if Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL).

3: A frame is counted as dropped only if it was not to be otherwise filtered.

6.1.42 RX UNICAST BYTE COUNT

Offset: 121Ch
Size: 32 bits

See Table 174.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 174: RX UNICAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Unicast Byte Count** Total number of bytes received from unicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL)). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.43 RX BROADCAST BYTE COUNT

Offset: 1220h
Size: 32 bits

See Table 175.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 175: RX BROADCAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Broadcast Byte Count** Total number of bytes received from broadcast frames without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is de-asserted. Frames that are discarded from FIFO overflow are not counted. The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL)). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.44 RX MULTICAST BYTE COUNT

Offset: 1224h
Size: 32 bits

See Table 176.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 176: RX MULTICAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Multicast Byte Count** Total number of bytes received from multicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL)). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.45 RX UNICAST FRAMES

Offset: 1228h
Size: 32 bits

See Table 177.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 177: RX UNICAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Unicast Frames** Number of unicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.46 RX BROADCAST FRAMES

Offset: 122Ch
Size: 32 bits

See Table 178.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 178: RX BROADCAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Broadcast Frames** Number of broadcast frames received without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is de-asserted. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.47 RX MULTICAST FRAMES

Offset: 1230h
Size: 32 bits

See Table 179.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 179: RX MULTICAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Multicast Frames** Number of multicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.48 RX PAUSE FRAMES

Offset: 1234h
Size: 32 bits

See Table 180.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 180: RX PAUSE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Pause Frames** Number of pause frames received without errors. Address filtering results do not prevent this counter from incrementing.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.49 RX 64 BYTE FRAMES

Offset: 1238h
Size: 32 bits

See Table 181.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 181: RX 64 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 64 Byte Frames** Number of frames received with a length of 64 bytes without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.50 RX 65 – 127 BYTE FRAMES

Offset: 123Ch
Size: 32 bits

See Table 182.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 182: RX 65 – 127 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 65 – 127 Byte Frames** Number of frames received with a length between 65 bytes and 127 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.51 RX 128 – 255 BYTE FRAMES

Offset: 1240h
Size: 32 bits

See Table 183.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 183: RX 128 – 255 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 128 – 255 Byte Frames** Number of frames received with a length between 128 bytes and 255 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.52 RX 256 – 511 BYTE FRAMES

Offset: 1244h
Size: 32 bits

See Table 184.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 184: RX 256 – 511 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 256 – 511 Byte Frames** Number of frames received with a length between 256 bytes and 511 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.53 RX 512 – 1023 BYTE FRAMES

Offset: 1248h
Size: 32 bits

See Table 185.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 185: RX 512 – 1023 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 512 – 1023 Byte Frames** Number of frames received with a length between 512 bytes and 1023 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.54 RX 1024 – 1518 BYTE FRAMES

Offset: 124Ch
Size: 32 bits

See Table 186.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 186: RX 1024 – 1518 BYTE FRAME SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX 1024 – 1518 Byte Frames** Number of frames received with a length between 1024 bytes and 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.55 RX GREATER 1518 BYTE FRAMES

Offset: 1250h
Size: 32 bits

See Table 187.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 187: RX GREATER 1518 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Greater 1518 Byte Frames** Number of frames received with a length greater than 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.56 RX TOTAL FRAMES

Offset: 1254h
Size: 32 bits

See Table 188.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 188: RX TOTAL FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Total Frames** Number of frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.57 EEE RX LPI TRANSITIONS

Offset: 1258h
Size: 32 bits

See Table 189.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 189: EEE RX LPI TRANSITIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**EEE RX LPI Transitions** Number of times that the LPI indication from the PHY changes from de-asserted to asserted. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during all Power states while the PHY is in normal operation.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.58 EEE RX LPI TIME

Offset: 125Ch
Size: 32 bits

See Table 190.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 190: EEE RX LPI TIME SPECIFICATIONS

Bit	Description	Type	Default
31:0	**EEE RX LPI Time** The amount of time, in micro-seconds, that the PHY indicates LPI. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. When EEE Timer Speed Up (EEE_TIMER_SPEED_UP) is set, the time is changed to increments of the crystal clock period. This counters is required to operate during all Power states while the PHY is in normal operation.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.59 RX COUNTER ROLLOVER STATUS

Offset: 127Ch
Size: 32 bits

See Table 191.

This register indicates when each RX counter rolls over. This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set.

TABLE 191: RX COUNTER ROLLOVER STATUS SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RESERVED**	RO	—
23	EEE RX LPI Time	R/W1C NASR (**Note 1**)	0b
22	EEE RX LPI Transitions	R/W1C NASR (**Note 1**)	0b
21	RX Total Frames	R/W1C NASR (**Note 1**)	0b
20	RX Greater 1518 Byte Frames	R/W1C NASR (**Note 1**)	0b
19	RX 1024 – 1518 Byte Frames	R/W1C NASR (**Note 1**)	0b
18	RX 512 – 1023 Byte Frames	R/W1C NASR (**Note 1**)	0b
17	RX 256 – 511 Byte Frames	R/W1C NASR (**Note 1**)	0b
16	RX 128 – 255 Byte Frames	R/W1C NASR (**Note 1**)	0b
15	RX 65 – 127 Byte Frames	R/W1C NASR (**Note 1**)	0b
14	RX 64 Byte Frames	R/W1C NASR (**Note 1**)	0b
13	RX Pause Frames	R/W1C NASR (**Note 1**)	0b
12	RX Multicast Frames	R/W1C NASR (**Note 1**)	0b
11	RX Broadcast Frames	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 191: RX COUNTER ROLLOVER STATUS SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
10	RX Unicast Frames	R/W1C NASR (**Note 1**)	0b
9	RX Multicast Byte Count	R/W1C NASR (**Note 1**)	0b
8	RX Broadcast Byte Count	R/W1C NASR (**Note 1**)	0b
7	RX Unicast Byte Count	R/W1C NASR (**Note 1**)	0b
6	RX Dropped Frames	R/W1C NASR (**Note 1**)	0b
5	RX Oversized Frame Errors	R/W1C NASR (**Note 1**)	0b
4	RX Undersized Frame Errors	R/W1C NASR (**Note 1**)	0b
3	RX Jabber Errors	R/W1C NASR (**Note 1**)	0b
2	RX Fragment Errors	R/W1C NASR (**Note 1**)	0b
1	RX Alignment Errors	R/W1C NASR (**Note 1**)	*0b*
0	RX FCS Errors	R/W1C NASR (**Note 1**)	*0b*

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.60 TX FCS ERRORS

Offset: 1280h
Size: 32 bits

See Table 192.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 192: TX FCS ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX FCS Errors** Number of frames transmitted with an FCS error. The MAC can be forced to transmit frames with FCS errors by setting the Bad FCS (BFCS) bit.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.61 TX EXCESS DEFERRAL ERRORS

Offset: 1284h
Size: 32 bits

See Table 193.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 193: TX EXCESS DEFERRAL ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Excess Deferral Errors** Number of frames that were excessively deferred. The frame has been deferred for more than two max-sized frame times + 16 bytes. The maximum frame length is defined by Maximum Frame Size (MAX_SIZE) in MAC Receive Register (MAC_RX). (See **Note 2** and **Note 3**.)	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts.

3: The 16 bytes of margin is to account for the possibility of double VLAN tags.

6.1.62 TX CARRIER ERRORS

Offset: 1288h
Size: 32 bits

See Table 194.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 194: TX CARRIER ERRORS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Carrier Errors** Number of frames that had a carrier sense error occur during transmission. This error is caused by no carrier or loss of carrier.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.63 TX BAD BYTE COUNT

Offset: 128Ch
Size: 32 bits

See Table 195.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 195: TX BAD BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Bad Byte Count** Total number of bytes sent from errored transmissions.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.64 TX SINGLE COLLISIONS

Offset: 1290h
Size: 32 bits

See Table 196.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 196: TX SINGLE COLLISIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Single Collisions** Number of frames successfully transmitted after a single collision occurs.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.65 TX MULTIPLE COLLISIONS

Offset: 1294h
Size: 32 bits

See Table 197.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 197: TX MULTIPLE COLLISIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Multiple Collisions** Number of frames successfully transmitted after multiple collision occur.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.66 TX EXCESSIVE COLLISIONS

Offset: 1298h
Size: 32 bits

See Table 198.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 198: TX EXCESSIVE COLLISIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Excessive Collisions** Number of transmitted frames aborted due to excessive collisions. (See **Note 2**.)	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Sixteen collisions result in an excessive collision.

6.1.67 TX LATE COLLISIONS

Offset: 129Ch
Size: 32 bits

See Table 199.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 199: TX LATE COLLISIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Late Collisions** Number of transmitted frames aborted because of a late collision.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.68 TX UNICAST BYTE COUNT

Offset: 12A0h
Size: 32 bits

See Table 200.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 200: TX UNICAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Unicast Byte Count** Total number of bytes transmitted by unicast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.69 TX BROADCAST BYTE COUNT

Offset: 12A4h
Size: 32 bits

See Table 201.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 201: TX BROADCAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Broadcast Byte Count** Total number of bytes transmitted by broadcast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.70 TX MULTICAST BYTE COUNT

Offset: 12A8h
Size: 32 bits

See Table 202.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 202: TX MULTICAST BYTE COUNT SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Multicast Byte Count** Total number of bytes transmitted by multicast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.71 TX UNICAST FRAMES

Offset: 12ACh
Size: 32 bits

See Table 203.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 203: TX UNICAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Unicast Frames** Number of unicast TX frames transmitted without errors. This counter does not count flow control frames.	RO NASR (Note 1)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.72 TX BROADCAST FRAMES

Offset: 12B0h
Size: 32 bits

See Table 204.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 204: TX BROADCAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Broadcast Frames** Number of broadcast TX frames transmitted without errors. This counter does not count flow control frames.	RO NASR (Note 1)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.73 TX MULTICAST FRAMES

Offset: 12B4h
Size: 32 bits

See Table 205.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set.This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 205: TX MULTICAST FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Multicast Frames** Number of multicast TX frames transmitted without errors. This counter does not count flow control frames.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.74 TX PAUSE FRAMES

Offset: 12B8h
Size: 32 bits

See Table 206.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 206: TX PAUSE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Pause Frames** Number of successfully transmitted pause frames.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.75 TX 64 BYTE FRAMES

Offset: 12BCh
Size: 32 bits

See Table 207.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 207: TX 64 BYTE FRAMSPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 64 Byte Frames** Number of frames transmitted with a length of 64 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.76 TX 65 – 127 BYTE FRAMES

Offset: 12C0h
Size: 32 bits

See Table 208.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 208: TX 65 – 127 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 65 – 127 Byte Frames** Number of frames transmitted with a length between 65 bytes and 127 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.77 TX 128 – 255 BYTE FRAMES

Offset: 12C4h
Size: 32 bits

See Table 209.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note:	If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 209: TX 128 – 255 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 128 – 255 Byte Frames** Number of frames transmitted with a length between 128 bytes and 255 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.78 TX 256 – 511 BYTE FRAMES

Offset: 12C8h
Size: 32 bits

See Table 210.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 210: TX 256 – 511 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 256 – 511 Byte Frames** Number of frames transmitted with a length between 256 bytes and 511 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.79 TX 512 – 1023 BYTE FRAMES

Offset: 12CCh
Size: 32 bits

See Table 211.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 211: TX 512 – 1023 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 512 – 1023 Byte Frames** Number of frames transmitted with a length between 512 bytes and 1023 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.80 TX 1024 – 1518 BYTE FRAMES

Offset: 12D0h
Size: 32 bits

See Table 212.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 212: TX 1024 – 1518 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX 1024 – 1518 Byte Frames** Number of frames transmitted with a length between 1024 bytes and 1518 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.81 TX GREATER 1518 BYTE FRAMES

Offset: 12D4h
Size: 32 bits

See Table 213.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 213: TX GREATER 1518 BYTE FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Greater 1518 Byte Frames** Number of frames transmitted with a length greater than 1518 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.82 TX TOTAL FRAMES

Offset: 12D8h
Size: 32 bits

See Table 214.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 214: TX TOTAL FRAMES SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Total Frames** Number of TX frames transmitted without errors. This counter does not count flow control frames.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.83 TX TX LPI TRANSITIONS

Offset: 12DCh
Size: 32 bits

See Table 215.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 215: TX TX LPI TRANSITIONS SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX TX LPI Transitions** Number of times that the LPI request to the PHY changes from de-asserted to asserted. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during all Power states while the PHY is in normal operation.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.84 TX TX LPI TIME

Offset: 12E0h
Size: 32 bits

See Table 216.

This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. This register becomes R/W if the Counter Write En (CNTR_WEN) bit in the MAC Control Register (MAC_CR) is set.

Note: If byte-wide reads are used to access this register, there is the potential for the counter to update before all four bytes have been read, resulting in an incorrect intermediate value. DWORD-wide reads are suggested.

TABLE 216: TX TX LPI TIME SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX TX LPI Time** The amount of time, in microseconds, that the PHY is requested to send LPI. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. When EEE Timer Speed Up (EEE_TIMER_SPEED_UP) is set, the time is changed to increments of the crystal clock period. This counters is required to operate during all Power states while the PHY is in normal operation.	RO NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

6.1.85 TX COUNTER ROLLOVER STATUS

Offset: 12FCh
Size: 32 bits

See Table 217.

This register indicates when each TX counter rolls over. This register is reset when the Counter Reset (CNTR_RST) bit in the MAC Control Register (MAC_CR) is set. If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set.

TABLE 217: TX COUNTER ROLLOVER STATUS SPECIFICATIONS

Bit	Description	Type	Default
31:25	**RESERVED**	RO	—
24	TX TX LPI Time	R/W1C NASR (**Note 1**)	0b
23	TX TX LPI Transitions	R/W1C NASR (**Note 1**)	0b
22	TX Total Frames	R/W1C NASR (**Note 1**)	0b
21	TX Greater 1518 Byte Frames	R/W1C NASR (**Note 1**)	0b
20	TX 1024 – 1518 Byte Frames	R/W1C NASR (**Note 1**)	0b
19	TX 512 – 1023 Byte Frames	R/W1C NASR (**Note 1**)	0b
18	TX 256 – 511 Byte Frames	R/W1C NASR (**Note 1**)	0b
17	TX 128 – 255 Byte Frames	R/W1C NASR (**Note 1**)	0b
16	TX 128 – 255 Byte Frames	R/W1C NASR (**Note 1**)	0b
15	TX 65 – 127 Byte Frames	R/W1C NASR (**Note 1**)	0b
14	TX 64 Byte Frames	R/W1C NASR (**Note 1**)	0b
13	TX Multicast Frames	R/W1C NASR (**Note 1**)	0b
12	TX Broadcast Frames	R/W1C NASR (**Note 1**)	0b
11	TX Unicast Frames	R/W1C NASR (**Note 1**)	0b
10	TX Multicast Byte Count	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 217: TX COUNTER ROLLOVER STATUS SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
9	TX Broadcast Byte Count	R/W1C NASR (**Note 1**)	0b
8	TX Unicast Byte Count	R/W1C NASR (**Note 1**)	0b
7	TX Late Collisions	R/W1C NASR (**Note 1**)	0b
6	TX Excessive Collisions	R/W1C NASR (**Note 1**)	0b
5	TX Multiple Collisions	R/W1C NASR (**Note 1**)	0b
4	TX Single Collisions	R/W1C NASR (**Note 1**)	0b
3	TX Bad Byte Count	R/W1C NASR (**Note 1**)	0b
2	TX Carrier Errors	R/W1C NASR (**Note 1**)	0b
1	TX Excess Deferral Errors	R/W1C NASR (**Note 1**)	0b
0	TX FCS Errors	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the MAC Reset (MRST) bit of the MAC Control Register (MAC_CR) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

7.0 INTERRUPT CONTROLLER REGISTERS

This section details the Interrupt Controller registers that are not part of the PCIe configuration space. The Interrupt Controller registers start at offset 0780h and end at offset 07FFh within the device. This range is for exclusive use of the Interrupt Controller registers. See Table 218.

TABLE 218: INTERRUPT CONTROLLER REGISTER MAP

Byte Offset	Register Name (Symbol)
0780h	Interrupt Status Register (INT_STS)
0784h	Interrupt Set Register (INT_SET)
0788h	Interrupt Enable Set Register (INT_EN_SET)
078Ch	Interrupt Enable Clear Register (INT_EN_CLR)
0790h	Interrupt Status Read to Clear Register (INT_STS_R2C)
0794h	Interrupt Vector Enable Set Register (INT_VEC_EN_SET)
0798h	Interrupt Vector Enable Clear Register (INT_VEC_EN_CLR)
079Ch	Interrupt Vector Enable Auto Clear Register (INT_VEC_EN_AUTO_CLR)
07A0h 07A4h 07A8h	Interrupt Vector Mapping Table Registers (INT_VEC_MAPX)
07ACh	Interrupt Vector Status Register (INT_VEC_STS)
07E0h-07FFh	Reserved for future expansion

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

7.1 Interrupt Status Register (INT_STS)

Offset: 0780h
Size: 32 bits

This register indicates the major interrupt request status. Any of the non-reserved bits may be set by software when the corresponding bit in Interrupt Set Register (INT_SET) is written high.

This register contains the same information as the INT_STS_R2C Register.

The value in this register and the INT_STS_R2C Register will always match. Bits that are cleared by writing this register will also be cleared in the INT_STS_R2C Register. Bits that are cleared by reading the INT_STS_R2C Register will also be cleared in this register.

If the host attempts to clear a R/W1C bit within the INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding INT_STS bit will remain set. See Table 219.

TABLE 219: INTERRUPT STATUS REGISTER (INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**DMA RX Channel 3:0 Interrupt (DMA_RXx_INT)** Indicates a DMA controller interrupt event from an RX channel. This bit is set whenever the following bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS) are set: • RXFRMx_INT In addition to other clearing methods, the RXFRMx_INT and RXPRIx bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS) are cleared when this bit is written with a 1. (See **Note 2**.)	R/W1C	0000b
23:17	**RESERVED**	RO	—
16	**DMA TX Channel 0 Interrupt (DMA_TX0_INT)** Indicates a DMA controller Interrupt event from TX channel 0. This bit is set whenever the following bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS) are set: • TX0_INT In addition to other clearing methods, the TX0_INT bit in the DMA Controller Interrupt Status Register (DMAC_INT_STS) is cleared when this register is written with a 1. (See **Note 2**.)	R/W1C	0b
15:12	**RESERVED**	RO	—
11	**GPIO Interrupt (GPIO_INT)** Indicates an interrupt generated from the GPIOs. This bit is set whenever any enabled bits in the General Purpose IO Interrupt Status Register (GPIO_INT_STS) are set. (See **Note 2**.)	RO	(**Note 1**)

Note 1: The default depends on the state of the GPIO pins.

2: The source of this interrupt is a level. The interrupt persists until the bits in the DMA controller are cleared or disabled.

3: The source of this interrupt is a pulse.

4: The source of this interrupt is a level. The interrupt persists until the bits in the PCIe Interrupt Status Register (PCIe_INT_STS) are cleared or disabled.

5: The source of this interrupt is a level. The interrupt persists until the bits in the 1588 block are cleared or disabled.

6: The source of this interrupt is a level. The interrupt persists until the bits in the OTP block are cleared or disabled.

7: The source of this interrupt is a level. The interrupt persists until the bits in the PHY are cleared or disabled or the PHY_INT_N pin is inactive.

8: The source of this interrupt is a level. The interrupt persists until the bits in the MAC block are cleared or disabled.

9: The source of this interrupt is a level. The interrupt persists until the bits in the FCT block are cleared or disabled.

TABLE 219: INTERRUPT STATUS REGISTER (INT_STS) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
10	**DMA General Interrupt (DMA_GEN_INT)** Indicates a general DMA controller Interrupt event. This bit is set whenever the following bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS) are set: • DMA_ERR_INT • RXx_STOP_INT (Note: This bit cascaded into the DMA_RXx_INT bits in silicon revision A0.) • TX0_STOP_INT (Note: This bit cascaded into the DMA_TX0_INT bit in silicon revision A0.) (See **Note 2**.)	RO	0b
9	**Software General Purpose (SW_GP_INT)** This interrupt is issued when the Software General Purpose Interrupt Set (SW_GP_INT_SET) bit in the Interrupt Set Register (INT_SET) is written high. There is no associated hardware event to set this field. (See **Note 3**.)	R/W1C	0b
8	**PCIe Interrupt (PCIe_INT)** Indicates a PCIe Interrupt event. This bit is set whenever any enabled bits in the PCIe Interrupt Status Register (PCIe_INT_STS) are set. (See **Note 4**.)	RO	0b
7	**1588 Interrupt (1588_INT)** Indicates a 1588 PTP Interrupt event. This bit is set whenever any enabled bits in the PTP Interrupt Status Register (PTP_INT_STS) are set. (See **Note 5**.)	RO	0b
6	**OTP Ready Interrupt (OTP_RDY_INT)** This will be set whenever a OTP ready interrupt occurs. This bit is set whenever any enabled bits in the OTP Interrupt Status Register are set. (See **Note 6**.)	RO	0b
5	**Ethernet PHY Interrupt (ETH_PHY_INT)** Indicates an Ethernet PHY Interrupt event. For the LAN7430, this bit is set whenever any enabled status bits in the Ethernet PHY Interrupt Control/Status Register are set. For the LAN7431, this bit is set when the PHY_INT_N pin is active. (See **Note 7**.)	RO	0b

Note 1: The default depends on the state of the GPIO pins.

2: The source of this interrupt is a level. The interrupt persists until the bits in the DMA controller are cleared or disabled.

3: The source of this interrupt is a pulse.

4: The source of this interrupt is a level. The interrupt persists until the bits in the PCIe Interrupt Status Register (PCIe_INT_STS) are cleared or disabled.

5: The source of this interrupt is a level. The interrupt persists until the bits in the 1588 block are cleared or disabled.

6: The source of this interrupt is a level. The interrupt persists until the bits in the OTP block are cleared or disabled.

7: The source of this interrupt is a level. The interrupt persists until the bits in the PHY are cleared or disabled or the PHY_INT_N pin is inactive.

8: The source of this interrupt is a level. The interrupt persists until the bits in the MAC block are cleared or disabled.

9: The source of this interrupt is a level. The interrupt persists until the bits in the FCT block are cleared or disabled.

TABLE 219: INTERRUPT STATUS REGISTER (INT_STS) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
4	**Data Port Interrupt (DP_INT)** Indicates that a pending data port operation has been completed. (See **Note 3**.)	R/W1C	0b
3	**MAC Interrupt (MAC_INT)** Indicates a Ethernet MAC interrupt event. This bit is set whenever any enabled status bits in the MAC Interrupt Status Register (MAC_INT_STS) are set. (See **Note 8**.)	RO	0b
2	**FCT Interrupt (FCT_INT)** Indicates a FIFO controller interrupt event. This bit is set whenever any enabled status bits in the FIFO Controller Interrupt Status Register (FCT_INT_STS) are set. (See **Note 9**.)	RO	0b
1	**GP Timer Interrupt (GPT_INT)** This interrupt is issued when the General Purpose Timer reaches zero. (See **Note 3**.)	R/W1C	0b
0	**Master Interrupt (MAS_INT)** This bit reflects the “ORing” of all the enabled bits in this register. Disabled interrupts (via the individual enables) do not contribute to this bit.	RO	0b

Note 1: The default depends on the state of the GPIO pins.

2: The source of this interrupt is a level. The interrupt persists until the bits in the DMA controller are cleared or disabled.

3: The source of this interrupt is a pulse.

4: The source of this interrupt is a level. The interrupt persists until the bits in the PCIe Interrupt Status Register (PCIe_INT_STS) are cleared or disabled.

5: The source of this interrupt is a level. The interrupt persists until the bits in the 1588 block are cleared or disabled.

6: The source of this interrupt is a level. The interrupt persists until the bits in the OTP block are cleared or disabled.

7: The source of this interrupt is a level. The interrupt persists until the bits in the PHY are cleared or disabled or the PHY_INT_N pin is inactive.

8: The source of this interrupt is a level. The interrupt persists until the bits in the MAC block are cleared or disabled.

9: The source of this interrupt is a level. The interrupt persists until the bits in the FCT block are cleared or disabled.

7.2 Interrupt Set Register (INT_SET)

Offset: 0784h
Size: 32 bits

This register may be used by software to set any of the non-reserved bits in the Interrupt Status Register (INT_STS). See Table 220.

TABLE 220: INTERRUPT SET REGISTER (INT_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**DMA RX Channel 3:0 Interrupt Set (DMA_RXx_INT_SET)**	R/W	0000b
23:17	**RESERVED**	RO	—

TABLE 220: INTERRUPT SET REGISTER (INT_SET) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
16	**DMA TX Channel 0 Interrupt Set (DMA_TX0_INT_SET)**	R/W	0b
15:12	**RESERVED**	RO	—
11	**GPIO Interrupt Set (GPIO_INT_SET)**	R/W	0b
10	**DMA General Interrupt Set (DMA_GEN_INT_SET)**	R/W	0b
9	**Software General Purpose Interrupt Set (SW_GP_INT_SET)**	R/W	0b
8	**PCIe Interrupt Set (PCIe_INT_SET)**	R/W	0b
7	**1588 Interrupt Set (1588_INT_SET)**	R/W	0b
6	**OTP Ready Interrupt Set (OTP_RDY_INT_SET)**	R/W	0b
5	**Ethernet PHY Interrupt Set (ETH_PHY_INT_SET)**	R/W	0b
4	**Data Port Interrupt Set (DP_INT_SET)**	R/W	0b
3	**MAC Interrupt Set (MAC_INT_SET)**	R/W	0b
2	**FCT Interrupt Set (FCT_INT_SET)**	R/W	0b
1	**GP Timer Interrupt Set (GPT_INT_SET)**	R/W	0b
0	**RESERVED**	RO	0b

7.3 Interrupt Enable Set Register (INT_EN_SET)

Offset: 0788
Size: 32 Bits

This register is used to set the interrupt enables for the corresponding bits in the Interrupt Status Register (INT_STS). Writing a ‘1’ to a bit sets the corresponding enable and configures the corresponding interrupt as a source for a system interrupt. Writing a ‘0’ has no effect. A read of this register returns the state of the interrupt enables. See Table 221.

TABLE 221: INTERRUPT ENABLE SET REGISTER (INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**DMA RX Channel 3:0 Interrupt Enable Set (DMA_RXx_INT_EN_SET)**	R/W1S	0b
23:17	**RESERVED**	RO	—
16	**DMA TX Channel 0 Interrupt Enable Set (DMA_TX0_INT_EN_SET)**	R/W1S	0b
15:12	**RESERVED**	RO	—
11	**GPIO Interrupt Enable Set (GPIOx_INT_EN_SET)**	R/W1S	0b
10	**DMA General Interrupt Enable Set (DMA_GEN_INT_EN_SET)**	R/W1S	0b

TABLE 221: INTERRUPT ENABLE SET REGISTER (INT_EN_SET) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
9	**Software General Purpose Interrupt Enable Set (SW_GP_INT_EN_SET)**	R/W1S	0b
8	**PCIe Interrupt Enable Set (PCIe_INT_EN_SET)**	R/W1S	0b
7	**1588 Interrupt Enable Set (1588_INT_EN_SET)**	R/W1S	0b
6	**OTP Ready Interrupt Enable Set (OTP_RDY_INT_EN_SET)**	R/W1S	0b
5	**Ethernet PHY Interrupt Enable Set (ETH_PHY_INT_EN_SET)**	R/W1S	0b
4	**Data Port Interrupt Enable Set (DP_INT_EN_SET)**	R/W1S	0b
3	**MAC Interrupt Enable Set (MAC_INT_EN_SET)**	R/W1S	0b
2	**FCT Interrupt Enable Set (FCT_INT_EN_SET)**	R/W1S	0b
1	**GP Timer Interrupt Enable Set (GPT_INT_EN_SET)**	R/W1S	0b
0	**Master Interrupt Enable Set (MAS_INT_EN_SET)** This bit is an additional enable that affects all the main interrupts sources.	R/W1S	0b

7.4 Interrupt Enable Clear Register (INT_EN_CLR)

Offset: 078Ch
Size: 32 bits

This register is used to clear the interrupt enables for the corresponding bits in the Interrupt Status Register (INT_STS). Writing a ‘1’ to a bit clears the corresponding enable. Writing a ‘0’ has no effect. A read of this register returns the state of the interrupt enables. See Table 222.

TABLE 222: INTERRUPT ENABLE CLEAR REGISTER (INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**DMA RX Channel 3:0 Interrupt Enable Clear (DMA_RXx_INT_EN_CLR)**	R/W1C	0b
23:17	**RESERVED**	RO	—
16	**DMA TX Channel 0 Interrupt Enable Clear (DMA_TX0_INT_EN_CLR)**	R/W1C	0b
15:12	**RESERVED**	RO	—
11	**GPIO Interrupt Enable Clear (GPIOx_INT_EN_CLR)**	R/W1C	0b
10	**DMA General Interrupt Enable Clear (DMA_GEN_INT_EN_CLR)**	R/W1C	0b
9	**Software General Purpose Interrupt Enable Clear (SW_GP_INT_EN_CLR)**	R/W1C	0b
8	**PCIe Interrupt Enable Clear (PCIe_INT_EN_CLR)**	R/W1C	0b
7	**1588 Interrupt Enable Clear (1588_INT_EN_CLR)**	R/W1C	0b

TABLE 222: INTERRUPT ENABLE CLEAR REGISTER (INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
6	**OTP Ready Interrupt Enable Clear (OTP_RDY_INT_EN_CLR)**	R/W1C	0b
5	**Ethernet PHY Interrupt Enable Clear (ETH_PHY_INT_EN_CLR)**	R/W1C	0b
4	**Data Port Interrupt Enable Clear (DP_INT_EN_CLR)**	R/W1C	0b
3	**MAC Interrupt Enable Clear (MAC_INT_EN_CLR)**	R/W1C	0b
2	**FCT Interrupt Enable Clear (FCT_INT_EN_CLR)**	R/W1C	0b
1	**GP Timer Interrupt Enable Clear (GPT_INT_EN_CLR)**	R/W1C	0b
0	**Master Interrupt Enable Clear (MAS_INT_EN_CLR)** This bit is an additional enable that affects all the main interrupts sources.	R/W1C	0b

7.5 Interrupt Status Read to Clear Register (INT_STS_R2C)

Offset: 0790h
Size: 32 bits

This register contains the same information as the INT_STS Register.

The value in this register and the INT_STS Register will always match. Bits that are cleared by reading this register will also be cleared in the INT_STS Register. Bits that are cleared by writing the INT_STS Register will also be cleared in this register.

As with the INT_STS Register:

- These bits are set regardless of the interrupt moderation timers or the PCIe function and vector masking.
- Bits, other than the master interrupt, are set regardless of the state of their interrupt enables and regardless of the state of the master enable.
- The master interrupt is set regardless of the state of the master enable but the other individual enables affect their contribution to the master interrupt.

Reading the interrupt status through this register may cause the indicated bits to be cleared.

For each DMA channel, based on the RX/TX_INT_STS_R2C_MODE bits in the RX Channel x Error Status Register (RX_ERR_STSx) or TX Channel x Configuration C Register (TX_CFG_Cx), the Read to Clear may be enabled, disabled or gated by the interrupt enables in the DMAC_INT_EN_SET and INT_EN_SET registers.

If the host reads this register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding bit will remain set. See Table 223.

TABLE 223: INTERRUPT STATUS READ TO CLEAR REGISTER (INT_STS_R2C) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**DMA RX Channel 3:0 Interrupt (DMA_RXx_INT)** In addition to other clearing methods, the RXFRMx_INT and RXPRIx bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS) are optionally cleared when this register is read.	RC	0000b
23:17	**RESERVED**	RO	—

Note 1: The default depends on the state of the GPIO pins.

TABLE 223: INTERRUPT STATUS READ TO CLEAR REGISTER (INT_STS_R2C) SPECIFICATIONS

Bit	Description	Type	Default
16	**DMA TX Channel 0 Interrupt (DMA_TX0_INT)** In addition to other clearing methods, the TX0_INT bit in the DMA Controller Interrupt Status Register (DMAC_INT_STS) is optionally cleared when this register is read.	RC	0b
15:12	**RESERVED**	RO	—
11	**GPIO Interrupt (GPIO_INT)** This bit is not cleared when this register is read.	RO	(Note 1)
10	**DMA General Interrupt (DMA_GEN_INT)** This bit is not cleared when this register is read.	RO	0b
9	**Software General Purpose (SW_GP_INT)** This bit is not cleared when this register is read.	RO	0b
8	**PCIe Interrupt (PCIe_INT)** This bit is not cleared when this register is read.	RO	0b
7	**1588 Interrupt (1588_INT)** This bit is not cleared when this register is read.	RO	0b
6	**OTP Ready Interrupt (OTP_RDY_INT)** This bit is not cleared when this register is read.	RO	0b
5	**Ethernet PHY Interrupt (ETH_PHY_INT)** This bit is not cleared when this register is read.	RO	0b
4	**Data Port Interrupt (DP_INT)** This bit is not cleared when this register is read.	RO	0b
3	**MAC Interrupt (MAC_INT)** This bit is not cleared when this register is read.	RO	0b
2	**FCT Interrupt (FCT_INT)** This bit is not cleared when this register is read.	RO	0b
1	**GP Timer Interrupt (GPT_INT)** This bit is not cleared when this register is read.	RO	0b
0	**Master Interrupt (MAS_INT)** This bit is not cleared when this register is read unless the clearing the DMA bits results in this bit naturally clearing.	RO	0b

Note 1: The default depends on the state of the GPIO pins.

7.6 Interrupt Vector Enable Set Register (INT_VEC_EN_SET)

Offset: 0794h
Size 32 bits

This register is used to set interrupt enables for the MSI and MSI-X interrupt vectors. Writing a '1' to a bit sets the corresponding enable and enables the corresponding vector message. Writing a '0' has no effect. A read of this register returns the state of the interrupt vector enables. The same enable bits are used for MSI and MSI-X since those mechanisms are used alternately. See Table 224.

TABLE 224: INTERRUPT VECTOR ENABLE SET REGISTER (INT_VEC_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7	**Interrupt Vector 7 Enable Set (INT_VEC7_EN_SET)**	R/W1S	0b
6	**Interrupt Vector 6 Enable Set (INT_VEC6_EN_SET)**	R/W1S	0b
5	**Interrupt Vector 5 Enable Set (INT_VEC5_EN_SET)**	R/W1S	0b
4	**Interrupt Vector 4 Enable Set (INT_VEC4_EN_SET)**	R/W1S	0b
3	**Interrupt Vector 3 Enable Set (INT_VEC3_EN_SET)**	R/W1S	0b
2	**Interrupt Vector 2 Enable Set (INT_VEC2_EN_SET)**	R/W1S	0b
1	**Interrupt Vector 1 Enable Set (INT_VEC1_EN_SET)**	R/W1S	0b
0	**Interrupt Vector 0 Enable Set (INT_VEC0_EN_SET)**	R/W1S	0b

7.7 Interrupt Vector Enable Clear Register (INT_VEC_EN_CLR)

Offset: 0798h
Size: 32 bits

This register is used to clear interrupt enables for the MSI and MSI-X interrupt vectors. Writing a '1' to a bit clears the corresponding enable. Writing a '0' has no effect. A read of this register returns the state of the interrupt vector enables.

The same enable bits are used for MSI and MSI-X since those mechanisms are used alternately. See Table 225.

TABLE 225: INTERRUPT VECTOR ENABLE CLEAR REGISTER (INT_VEC_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7	**Interrupt Vector 7 Enable Clear (INT_VEC7_EN_CLR)**	R/W1C	0b
6	**Interrupt Vector 6 Enable Clear (INT_VEC6_EN_CLR)**	R/W1C	0b
5	**Interrupt Vector 5 Enable Clear (INT_VEC5_EN_CLR)**	R/W1C	0b
4	**Interrupt Vector 4 Enable Clear (INT_VEC4_EN_CLR)**	R/W1C	0b
3	**Interrupt Vector 3 Enable Clear (INT_VEC3_EN_CLR)**	R/W1C	0b

TABLE 225: INTERRUPT VECTOR ENABLE CLEAR REGISTER (INT_VEC_EN_CLR) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
2	**Interrupt Vector 2 Enable Clear (INT_VEC2_EN_CLR)**	R/W1C	0b
1	**Interrupt Vector 1 Enable Clear (INT_VEC1_EN_CLR)**	R/W1C	0b
0	**Interrupt Vector 0 Enable Clear (INT_VEC0_EN_CLR)**	R/W1C	0b

7.8 Interrupt Vector Enable Auto Clear Register (INT_VEC_EN_AUTO_CLR)

Offset: 079Ch
Size: 32 bits

This register is used to enable the automatic clearing of the interrupt enables for the MSI and MSI-X interrupt vectors. When set to a '1' the corresponding bit in the Interrupt Vector Enable Set Register (INT_VEC_EN_SET) is cleared when an MSI/MSI-X message is sent for the vector.

The same enable bits are used for MSI and MSI-X since those mechanisms are used alternately. See Table 226.

TABLE 226: INTERRUPT VECTOR ENABLE AUTO CLEAR REGISTER (INT_VEC_EN_AUTO_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7	**Interrupt Vector 7 Enable Auto Clear (INT_VEC7_EN_AUTO_CLR)**	R/W	0b
6	**Interrupt Vector 6 Enable Auto Clear (INT_VEC6_EN_AUTO_CLR)**	R/W	0b
5	**Interrupt Vector 5 Enable Auto Clear (INT_VEC5_EN_AUTO_CLR)**	R/W	0b
4	**Interrupt Vector 4 Enable Auto Clear (INT_VEC4_EN_AUTO_CLR)**	R/W	0b
3	**Interrupt Vector 3 Enable Auto Clear (INT_VEC3_EN_AUTO_CLR)**	R/W	0b
2	**Interrupt Vector 2 Enable Auto Clear (INT_VEC2_EN_AUTO_CLR)**	R/W	0b
1	**Interrupt Vector 1 Enable Auto Clear (INT_VEC1_EN_AUTO_CLR)**	R/W	0b
0	**Interrupt Vector 0 Enable Auto Clear (INT_VEC0_EN_AUTO_CLR)**	R/W	0b

7.9 Interrupt Vector Mapping Table Registers (INT_VEC_MAPX)

Offset:

07A0h
07A4h
07A8h

Size: 32 bits

These registers assign the major interrupt sources onto MSI/MSI-X vectors. There are 3 registers in the table. For all entires, valid values are 0 though 7. Values of 8 through 15 are reserved. See Table 227.

TABLE 227: INTERRUPT VECTOR MAPPING TABLE REGISTERS (INT_VEC_MAPX) SPECIFICATIONS

Offset	Bit	Description	Type	Default
07A0h	15:12	**DMA RX Channel 3 Vector (DMA_RX3_VEC)** Maps a vector to RX channel 3 interrupt.	R/W	0h
07A0h	11:8	**DMA RX Channel 2 Vector (DMA_RX2_VEC)** Maps a vector to RX channel 2 interrupt.	R/W	0h
07A0h	7:4	**DMA RX Channel 1 Vector (DMA_RX1_VEC)** Maps a vector to RX channel 1 interrupt.	R/W	0h
07A0h	3:0	**DMA RX Channel 0 Vector (DMA_RX0_VEC)** Maps a vector to RX channel 0 interrupt.	R/W	0h
07A4h	31:4	**RESERVED**	RO	—
07A4h	3:0	**DMA TX Channel 0 Vector (DMA_TX0_VEC)** Maps a vector to TX channel 0 interrupt.	R/W	0h
07A8h	31:24	**RESERVED**	RO	—
07A8h	23:20	**FCT Vector (FCT_VEC)** Maps a vector to the FCT Controller interrupt event.	R/W	0h
07A8h	19:16	**DMA General Vector (DMA_GEN_VEC)** Maps a vector to a general DMA Controller interrupt event.	R/W	0h
07A8h	15:12	**Software General Purpose Vector (SW_GP_VEC)** Maps a vector to the Software General Purpose interrupt.	R/W	0h
07A8h	11:8	**1588 Vector (1588_VEC)** Maps a vector to a 1588 PTP interrupt event.	R/W	0h
07A8h	7:4	**GP Timer Vector (GPT_VEC)** Maps a vector to the General Purpose Timer interrupt.	R/W	0h
07A8h	3:0	**Other Vector (OTHER_VEC)** Maps a vector to the other interrupt sources (GPIO, MAC, PHY, OTP, PCIe, and Data Port).	R/W	0h

7.10 Interrupt Vector Status Register (INT_VEC_STS)

Offset:
Size: 32 bits
This register indicates the interrupt request status for each MSI/MSI-X vector following the vector mapping. See Table 228.

Note:	These bits will be active regardless of the state of the interrupt vector enables and regardless of the PCIe function and vector masking. However, interrupts that are masked due to the low-level interrupt enables, the main interrupt enable register, the master interrupt enable or interrupt moderation will not be indicated in this register.

TABLE 228: INTERRUPT VECTOR STATUS REGISTER (INT_VEC_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7	**Interrupt Vector 7 Status (INT_VEC7_STS)**	RO	0b
6	**Interrupt Vector 6 Status (INT_VEC6_STS)**	RO	0b
5	**Interrupt Vector 5 Status (INT_VEC5_STS)**	RO	0b
4	**Interrupt Vector 4 Status (INT_VEC4_STS)**	RO	0b
3	**Interrupt Vector 3 Status (INT_VEC3_STS)**	RO	0b
2	**Interrupt Vector 2 Status (INT_VEC2_STS)**	RO	0b
1	**Interrupt Vector 1 Status (INT_VEC1_STS)**	RO	0b
0	**Interrupt Vector 0 Status (INT_VEC0_STS)**	RO	0b

8.0 RFE CONTROLLER REGISTERS

This section details the RFE registers (See Table 229.). The RFE registers are at offsets 0400h through 05FFh within the device. This range is for exclusive use of the RFE registers. For an overview of the entire device register map, refer to Section 1.0, Register Map.

TABLE 229: RFE REGISTER MAP

Byte Offset	Register Name (Symbol)
0400h-0504h	MAC Address Perfect Filter Registers (ADDR_FILTx)
0508h	FIFO Controller RX FIFO Control Register (FCT_RX_CTL)
050Ch	Receive Filtering Engine Priority Selection Register (RFE_PRI_SEL)
0510h-052Ch	RFE DIFFSERV Table Registers (RFE_DIFFSERVx)
0530h-0553h	Reserved for future expansion
0554h	Receive Filtering Engine RSS Configuration Register (RFE_RSS_CFG)
0558h-057Ch	Receive Filtering Engine RSS Hash Key Registers (RFE_HASH_KEYx)
0580h-05FCh	Receive Filtering Engine RSS Indirection Table Registers (RFE_INDx)

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

8.1 Receive Filtering Engine Control Register (RFE_CTL)

Offset: 0024h
Size: 32 bits

This register configures the Receive Filtering Engine.

If neither Enable IGMP Checksum Validation, Enable ICMP Checksum Validation or Enable TCP/UDP Checksum Validation bits are set then the RFE inserts 0000h for the L3 raw checksum field. See Table 230.

TABLE 230: RECEIVE FILTERING ENGINE CONTROL REGISTER (RFE_CTL) SPECIFICATIONS

Bit	Description	Type	Default
31:19	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The raw checksum is still calculated regardless of this bit.

3: If the frame is not IGMP, the raw checksum is still calculated.

4: If destination address filtering is enabled (perfect or hash), the frame must pass both source address filtering and destination address filtering to not be discarded.

5: The broadcast address is never hashed.

TABLE 230: RECEIVE FILTERING ENGINE CONTROL REGISTER (RFE_CTL) SPECIFICATIONS

Bit	Description	Type	Default
18	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP, TCP or ICMPv6 checksum for RX checksum offloading. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not verified. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not verified. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
17:16	**Default Receive Channel** This field specifies the default receive channel.	R/W NASR (**Note 1**)	00b
15	**Always Pass Wakeup Frame (PASS_WKP)** When set, the RFE shall never discard a received wakeup frame which awakened the device while in D3 and Store Wakeup Frame (STORE_WAKE) is set.	R/W NASR (**Note 1**)	0b
14	**Enable IGMP Checksum Validation** When set, the RFE will check the IGMP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Command B. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
13	**Enable ICMP Checksum Validation** When set, the RFE will check the ICMP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Command B. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
12	**Enable TCP/UDP Checksum Validation** When set, the RFE will check the TCP or UDP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Command B. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
11	**Enable IP Checksum Validation** When set, the RFE will check the IP checksum. This bit has no effect if the frame is not IPv4 or IPv6.	R/W NASR (**Note 1**)	0b
10	**Accept Broadcast Frames (AB)** When set, all broadcast frames are accepted. Otherwise broadcast frames are dropped.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The raw checksum is still calculated regardless of this bit.

3: If the frame is not IGMP, the raw checksum is still calculated.

4: If destination address filtering is enabled (perfect or hash), the frame must pass both source address filtering and destination address filtering to not be discarded.

5: The broadcast address is never hashed.

TABLE 230: RECEIVE FILTERING ENGINE CONTROL REGISTER (RFE_CTL) SPECIFICATIONS

Bit	Description	Type	Default
9	**Accept Multicast Frames (AM)** When set, all multicast frames are accepted. Otherwise multicast frames must pass the perfect filtering or hash filtering. This bit, however, does not apply to broadcast frames.	R/W NASR (**Note 1**)	0b
8	**Accept Unicast Frames (AU)** When set, all unicast frames are accepted.	R/W NASR (**Note 1**)	0b
7	**Enable VLAN Tag Stripping** When set, this bit enables stripping of a received frame's VLAN ID.	R/W NASR (**Note 1**)	0b
6	**Untagged Frame Filtering (UF)** When set, all untagged receive frames are discarded.	R/W NASR (**Note 1**)	0b
5	**Enable VLAN Filtering (VF)** When set, this bit enables filtering of a received frame's VLAN ID.	R/W NASR (**Note 1**)	0b
4	**Enable Source Address Perfect Filtering (SPF)** When set, this bit enables perfect filtering of a received frame's Ethernet source address. (See **Note 4**.)	R/W NASR (**Note 1**)	0b
3	**Enable Multicast Address Hash Filtering (MHF)** When set, multicast destination addresses will be hashed. (See **Note 5**.)	R/W NASR (**Note 1**)	0b
2	**Enable Destination Address Hash Filtering (DHF)** When set, unicast destination addresses will be hashed.	R/W NASR (**Note 1**)	0b
1	**Enable Destination Address Perfect Filtering (DPF)** When set, this bit enables perfect filtering of a received frame's Ethernet destination address.	R/W NASR (**Note 1**)	0b
0	**Reset Receive Filtering Engine** When set, this bit resets the RFE. Register bits marked as NASR are not reset.	SC	0b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The raw checksum is still calculated regardless of this bit.

3: If the frame is not IGMP, the raw checksum is still calculated.

4: If destination address filtering is enabled (perfect or hash), the frame must pass both source address filtering and destination address filtering to not be discarded.

5: The broadcast address is never hashed.

8.2 Receive Filtering Engine Priority Selection Register (RFE_PRI_SEL)

Offset: 0028h
Size: 32 bits

This register configures the FCT selection via priority. See Table 231.

TABLE 231: RECEIVE FILTERING ENGINE PRIORITY SELECTION REGISTER (RFE_PRI_SEL) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**Channel Number Priority 7** Indicates the destination FCT for priority 7 if RSS is not used.	R/W NASR (**Note 1**)	00b
29:28	**Channel Number Priority 6** Indicates the destination FCT for priority 6 if RSS is not used.	R/W NASR (**Note 1**)	00b
27:26	**Channel Number Priority 5** Indicates the destination FCT for priority 5 if RSS is not used.	R/W NASR (**Note 1**)	00b
25:24	**Channel Number Priority 4** Indicates the destination FCT for priority 4 if RSS is not used.	R/W NASR (**Note 1**)	00b
23:22	**Channel Number Priority 3** Indicates the destination FCT for priority 3 if RSS is not used.	R/W NASR (**Note 1**)	00b
21:20	**Channel Number Priority 2** Indicates the destination FCT for priority 2 if RSS is not used.	R/W NASR (**Note 1**)	00b
19:18	**Channel Number Priority 1** Indicates the destination FCT for priority 1 if RSS is not used.	R/W NASR (**Note 1**)	00b
17:16	**Channel Number Priority 0** Indicates the destination FCT for priority 0 if RSS is not used.	R/W NASR (**Note 1**)	00b
15:8	**Priority RSS Enable** Each bit in this field represents one priority level and indicates for that priority that the RSS result is used as the destination FCT.	R/W NASR (**Note 1**)	00h
7	**Frame Priority Enable** When set, this bit enables the use of the Frame Priority Threshold field to determine if the frame is considered a priority frame.	R/W NASR (**Note 1**)	0b
6:4	**Frame Priority Threshold** When the frame's calculated priority is equal to or larger than this field, the frame is considered a priority frame. (See **Note 2**.)	R/W NASR (**Note 1**)	000b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This bit only has an effect if the Frame Priority Enable bit is set.

TABLE 231: RECEIVE FILTERING ENGINE PRIORITY SELECTION REGISTER (RFE_PRI_SEL) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
3	**Use Precedence** When the priority is taken from an IPV4 packet (enabled via the Use IP bit), this bit selects between precedence bits in the TOS octet or the DIFFSERV table. When set, IPv4 packets will use the precedence bits in the TOS octet to select the destination FIFO. When cleared, IPv4 packets will use the DIFFSERV table to select the destination FIFO.	R/W NASR (**Note 1**)	0b
2	**Use IP** When set, the IPv4 TOS or IPv6 TC field is enabled as a destination FIFO choice.	R/W NASR (**Note 1**)	0b
1	**Use Tag** When set, the priority from the VLAN tag is enabled as a destination FIFO choice.	R/W NASR (**Note 1**)	0b
0	**VL Higher Priority** When this bit is set and VLAN priority is enabled (via the Use Tag bit), the priority from the VLAN tag has higher priority than the IP TOS/TC field.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This bit only has an effect if the Frame Priority Enable bit is set.

8.3 RFE DIFFSERV Table Registers (RFE_DIFFSERVx)

Offset: 0510h – 052Ch
Size: 32 bytes

These registers contain the 64 entry DIFFSERV mapping table. There are 8 registers each containing 8 code points. Each code point entry is 4 bits wide with the 3 least significant bits mapping the code point to a priority. See Table 232 and Table 233.

TABLE 232: RFE DIFFSERV TABLE REGISTERS (RFE_DIFFSERVX)

Table DWORD Offset	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0h	CP 7	CP 6	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0
1h	CP 15	CP 14	CP 13	CP 12	CP 11	CP10	CP9	CP 8
...	...	...	...	...	...	...	...	...
6h	CP 55	CP 54	CP 53	CP 52	CP 51	CP 50	CP 49	CP 48
7h	CP 63	CP 62	CP 61	CP 60	CP 59	CP 58	CP 57	CP 56

TABLE 233: RFE DIFFSERV TABLE REGISTERS (RFE_DIFFSERVX) SPECIFICATIONS

Bit	Description	Type	Default
31	**RESERVED**	RO	—
30:28	**Code Point [7, 15, 23,...63]** Receive channel for entry 8*n+7 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
27	**RESERVED**	RO	—
26:24	**Code Point [6, 14, 22,...62]** Receive channel for entry 8*n+6 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
23	**RESERVED**	RO	—
22:20	**Code Point [5, 13, 21,...61]** Receive channel for entry 8*n+5 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
19	**RESERVED**	RO	—
18:16	**Code Point [4, 12, 20,...60]** Receive channel for entry 8*n+4 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
15	**RESERVED**	RO	—
14:12	**Code Point [3, 11, 19,...59]** Receive channel for entry 8*n+3 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
11	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 233: RFE DIFFSERV TABLE REGISTERS (RFE_DIFFSERVX) SPECIFICATIONS

Bit	Description	Type	Default
10:8	**Code Point [2, 10, 18,...58]** Receive channel for entry 8*n+2 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
7	**RESERVED**	RO	—
6:4	**Code Point [1, 9, 17,...57]** Receive channel for entry 8*n+1 (n=0,1,...7)	R/W NASR (**Note 1**)	000b
3	**RESERVED**	RO	—
2:0	**Code Point [0, 8, 16,...56]** Receive channel for entry 8*n (n=0,1,...7)	R/W NASR (**Note 1**)	000b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

8.4 MAC Address Perfect Filter Registers (ADDR_FILTx)

Offset: 0400h – 0504h
Size: 32 bytes

These registers specify the MAC addresses used for perfect filtering. There are 33 entries each using 8 bytes (2 DWORDS).

It is permissible to change the value of an entry at run time. However, the address valid bit must be cleared before doing so. Otherwise an invalid value will temporarily be in the MAC address filter. See Table 234 and Table 235.

TABLE 234: MAC ADDRESS PERFECT FILTER REGISTERS (ADDR_FILTX)

Table DWORD Offset	31:24	23:16	15:8	7:0
0h	Entry 0 Address Valid / Type	Entry 0 RSS / Ch En / Ch #	Entry 0 Address [47:32]	
1h	Entry 0 Address [31:0]			
2h	Entry 1 Address Valid / Type	Entry 1 RSS / Ch En / Ch #	Entry 1 Address [47:32]	
3h	Entry 1 Address [31:0]			
...	...	...	...	...
100h	Entry 32 Address Valid / Type	Entry 32 RSS / Ch En / Ch #	Entry 32 Address [47:32]	
104h	Entry 32 Address [31:0]			

TABLE 235: MAC ADDRESS PERFECT FILTER REGISTERS (ADDR_FILTX) SPECIFICATIONS

DWORD Offset	Bits	Description	Type	Default
0h, 2h, etc.	31	**Address Valid** When set, this bit indicates that the entry has valid data and is used in the perfect filtering.	R/W	0b

TABLE 235: MAC ADDRESS PERFECT FILTER REGISTERS (ADDR_FILTX) SPECIFICATIONS

DWORD Offset	Bits	Description	Type	Default
0h, 2h, etc.	30	**Address Type** When set, this bit indicates the address represents the MAC source address. Otherwise this entry applies to the MAC destination address.	R/W	0b
0h, 2h, etc.	29:21	**RESERVED**	RO	—
0h, 2h, etc.	20	**MAC Priority Frame** When the MAC address matches that of this entry, this bit indicates that the received frame is considered a priority frame.	R/W	0b
0h, 2h, etc.	19	**MAC RSS Enable** When the MAC address matches that of this entry, this bit indicates that the RSS result is used as the destination FIFO.	R/W	0b
0h, 2h, etc.	18	**Channel Number Enable** When the MAC address matches that of this entry, this bit indicates that the Channel Number field is used as the destination FCT.	R/W	0b
0h, 2h, etc.	17:16	**Channel Number** Indicates the destination FCT for this entry.	R/W	00b
0h, 2h, etc.	15:0	**Physical Address [47:32]** This field contains the upper 16 bits [47:32] of the physical address of the device.	R/W	0000h
1h, 3h, etc.	31:0	**Physical Address [31:0]** This field contains the lower 32 bits [31:0] of the physical address of the device.	R/W	00000000h

Table 236 illustrates the byte ordering of the Physical Address fields with respect to the reception of the Ethernet physical address.

TABLE 236: PHYSICAL ADDRESS BYTE ORDERING

RX_ADDRL, RX_ADDRH	ORDER OF RECEPTION ON ETHERNET
Physical Address[7:0]	1st
Physical Address[15:8]	2nd
Physical Address[23:16]	3rd
Physical Address[31:24]	4th
Physical Address[39:32]	5th
Physical Address[47:40]	6th

8.5 Receive Filtering Engine RSS Configuration Register (RFE_RSS_CFG)

Offset: 0554h
Size: 32 bits

Note:	This register is new for LAN743x.

This register configures the RSS logic. See Table 237.

TABLE 237: RECEIVE FILTERING ENGINE RSS CONFIGURATION REGISTER (RFE_RSS_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:17	**RESERVED**	RO	—
16:8	**RSS Hash Type Enable** These bits enable the various hash types. Bit 16 = Enable UdpIPv6Ex hash function Bit 15 = Enable TcpIPv6Ex hash function Bit 14 = Enable IPv6Ex hash function Bit 13 = Enable UdpIPv6 hash function Bit 12 = Enable TcpIPv6 hash function Bit 11 = Enable IPv6 hash function Bit 10 = Enable UdpIPv4 hash function Bit 9 = Enable TcpIPv4 hash function Bit 8 = Enable IPv4 hash function	R/W NASR (**Note 1**)	000000000b
7:5	**Valid Hash Bits** This field selects the number of the least significant bits of the hash value that is used to index into the indirection table. The number can range inclusively from 1 to 7. The number effectively defines the size of the indirection table. A value of 1 results in 2 byte deep indirection table, while value of 7 results in 128 byte deep table.	R/W NASR (**Note 1**)	000b
4:3	**RESERVED**	RO	—
2	**RSS Queue Enable** When set, the RSS hash is enabled as part of the RX channel selection process.	R/W NASR (**Note 1**)	0b
1	**RSS Hash Store** When set, the RSS hash value and type are passed to the FIFOs.	R/W NASR (**Note 1**)	0b
0	**RSS Enable** When set, the RSS hashing function is enabled, allowing the RSS hash to be calculated and used in the determination of the RX channel.	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

8.6 Receive Filtering Engine RSS Hash Key Registers (RFE_HASH_KEYx)

Offset: 0558h – 057Ch
Size: 40 bytes

Note:	This register is new for LAN743x.

These registers specify the 40-byte RSS hash key. There are 10 registers each containing 4 of the bytes. See Table 238 and Table 239.

TABLE 238: RECEIVE FILTERING ENGINE RSS HASH KEY REGISTERS (RFE_HASH_KEYX)

Table DWORD Offset	31:24	23:16	15:8	7:0
0h	Key Byte 3	Key Byte 2	Key Byte 1	Key Byte 0
1h	Key Byte 7	Key Byte 6	Key Byte 5	Key Byte 4
...	...	...	...	...
08h	Key Byte 35	Key Byte 35	Key Byte 33	Key Byte 32
09h	Key Byte 39	Key Byte 38	Key Byte 37	Key Byte 36

TABLE 239: RECEIVE FILTERING ENGINE RSS HASH KEY REGISTERS (RFE_HASH_KEYX) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RSS Key [3, 7, 11,...39]** RSS key byte 4*n+3 (n=0,1,...9)	R/W NASR (**Note 1**)	00h
23:16	**RSS Key [2, 6, 10,...38]** RSS key byte 4*n+2 (n=0,1,...9)	R/W NASR (**Note 1**)	00h
15:8	**RSS Key [1, 5, 9,...37]** RSS key byte 4*n+1 (n=0,1,...9)	R/W NASR (**Note 1**)	00h
7:0	**RSS Key [0, 4, 8,...36]** RSS key byte 4*n (n=0,1,...9)	R/W NASR (**Note 1**)	00h

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

8.7 Receive Filtering Engine RSS Indirection Table Registers (RFE_INDx)

Offset: 0580h – 05FCh
Size: 128 bytes

Note:	This register is new for LAN743x.

These registers specify the 128 byte RSS indirection table. There are 32 registers each containing 4 entries. Each entry is one byte-wide with the 2 least significant bits specifying the receive channel. See Table 240 and Table 241.

TABLE 240: RECEIVE FILTERING ENGINE RSS INDIRECTION TABLE REGISTERS (RFE_INDX)

Table DWORD Offset	31:24	23:16	15:8	7:0
0h	Entry 3	Entry 2	Entry 1	Entry 0
1h	Entry 7	Entry 6	Entry 5	Entry 4

TABLE 240: RECEIVE FILTERING ENGINE RSS INDIRECTION TABLE REGISTERS (RFE_INDX)

Table DWORD Offset	31:24	23:16	15:8	7:0
...	...	...	...	...
1Eh	Entry 123	Entry 122	Entry 121	Entry 120
1Fh	Entry 127	Entry 126	Entry 125	Entry 124

TABLE 241: RECEIVE FILTERING ENGINE RSS INDIRECTION TABLE REGISTERS (RFE_INDX) SPECIFICATIONS

Bit	Description	Type	Default
31:26	**RESERVED**	RO	—
25:24	**Entry [3, 7, 11,...127]** Receive channel for entry 4*n+3 (n=0,1,...31)	R/W NASR (**Note 1**)	00b
23:18	**RESERVED**	RO	—
17:16	**Entry [2, 6, 10,...126]** Receive channel for entry 4*n+2 (n=0,1,...31)	R/W NASR (**Note 1**)	00b
15:10	**RESERVED**	RO	—
9:8	**Entry [1, 5, 9,...125]** Receive channel for entry 4*n+1 (n=0,1,...31)	R/W NASR (**Note 1**)	00b
7:2	**RESERVED**	RO	—
1:0	**Entry [0, 4, 8,...124]** Receive channel for entry 4*n (n=0,1,...31)	R/W NASR (**Note 1**)	00b

Note 1: The NASR designation is only applicable when the Reset Receive Filtering Engine bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is set. Register bits designated as NASR are reset via other chip level software initiated resets.

9.0 1588 REGISTERS

This section details the 1588 registers. The 1588 registers are at offsets 0A00h to 0AFFh within the device. This range is for exclusive use of the 1588 registers. For an overview of the entire device register map, refer to Section 1.0, Register Map.

For GPIO related registers, each GPIO has a set of registers. These sets of registers are identical in functionality for each GPIO, and thus their register descriptions have been consolidated. In these cases, the register names will be amended with a lowercase “x” in place of the GPIO designation. The wildcard “x” should be replaced with “0” to “7.”

Similarly, for Clock Compare events, the wildcard “x” should be replaced with “A” or “B”.

GPIO register sets share a common address space. GPIO register sets are selected by using the PTP GPIO Select Register (PTP_GPIO_SEL) in the PTP GPIO Select Register (PTP_GPIO_SEL). See Table 242.

Note: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available.

TABLE 242: 1588 REGISTER MAP

Byte Offset	Register Name (Symbol)
0A00h	PTP Command and Control Register (PTP_CMD_CTL)
0A04h	PTP General Configuration Register (PTP_GENERAL_CONFIG)
0A08h	PTP Interrupt Status Register (PTP_INT_STS)
0A0Ch	PTP Interrupt Enable Set Register (PTP_INT_EN_SET)
0A10h	PTP Interrupt Enable Clear Register (PTP_INT_EN_CLR)
0A14h	PTP Clock Seconds Register (PTP_CLOCK_SEC)
0A18h	PTP Clock NanoSeconds Register (PTP_CLOCK_NS)
0A1Ch	PTP Clock Sub-NanoSeconds Register (PTP_CLOCK_SUBNS)
0A20h	PTP Clock Rate Adjustment Register (PTP_CLOCK_RATE_ADJ)
0A24h	PTP Clock Temporary Rate Adjustment Register (PTP_CLOCK_TEMP_RATE_ADJ)
0A28h	PTP Clock Temporary Rate Duration Register (PTP_CLOCK_TEMP_RATE_DURATION)
0A2Ch	PTP Clock Step Adjustment Register (PTP_CLOCK_STEP_ADJ)
0A30h	PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) (x = A)
0A34h	PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) (x = A)
0A38h	PTP Clock Target x Reload/Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) (x = A)
0A3Ch	PTP Clock Target x Reload / Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x) (x = A)
0A40h	PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) (x = B)
0A44h	PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) (x = B)
0A48h	PTP Clock Target x Reload/Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) (x = B)
0A4Ch	PTP Clock Target x Reload / Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x) (x = B)
0A50h	PTP User MAC Address High-WORD Register (PTP_USER_MAC_HI)
0A54h	PTP User MAC Address Low-DWORD Register (PTP_USER_MAC_LO)
0A58h	PTP GPIO Select Register (PTP_GPIO_SEL)
0A5Ch	PTP Latency Register (PTP_LATENCY)
0A60h	PTP Capture Information Register (PTP_CAP_INFO)
0A64h	PTP RX Parsing Configuration Register (PTP_RX_PARSE_CONFIG)
0A68h	PTP RX Timestamp Configuration Register (PTP_RX_TIMESTAMP_CONFIG)

TABLE 242: 1588 REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
0A78h	PTP RX Ingress Time Seconds Register (PTP_RX_INGRESS_SEC)
0A7Ch	PTP RX Ingress Time NanoSeconds Register (PTP_RX_INGRESS_NS)
0A80h	PTP RX Message Header Register (PTP_RX_MSG_HEADER)
0A9Ch	PTP TX Parsing Configuration Register (PTP_TX_PARSE_CONFIG)
0AA0h	PTP TX Timestamp Configuration Register (PTP_TX_TIMESTAMP_CONFIG)
0AA4h	PTP TX Modification Register (PTP_TX_MOD)
0AA8h	PTP TX Modification Register 2 (PTP_TX_MOD2)
0AACh	PTP TX Egress Time Seconds Register (PTP_TX_EGRESS_SEC)
0AB0h	PTP TX Egress Time NanoSeconds Register (PTP_TX_EGRESS_NS)
0AB4h	PTP TX Message Header Register (PTP_TX_MSG_HEADER)
0AC0h	PTP TX One-Step Sync Upper Seconds Register (PTP_TX_ONE_STEP_SYNC_SEC)
0AC4h	PTP GPIO Capture Configuration Register (PTP_GPIO_CAP_CONFIG)
0AC8h	PTP GPIO x Rising Edge Clock Seconds Capture Register (PTP_GPIO_RE_CLOCK_SEC_-CAP_x)
0ACCh	PTP GPIO x Rising Edge Clock NanoSeconds Capture Register (PTP_GPIO_RE_-CLOCK_NS_CAP_x)
0AD0h	PTP GPIO x Falling Edge Clock Seconds Capture Register (PTP_GPIO_FE_CLOCK_SEC_-CAP_x)
0AD4h	PTP GPIO x Falling Edge Clock NanoSeconds Capture Register (PTP_GPIO_FE_-CLOCK_NS_CAP_x)

9.1 PTP Command and Control Register (PTP_CMD_CTL)

Offset: 0A00h
Size: 32 bits

See Table 243.

TABLE 243: PTP COMMAND AND CONTROL REGISTER (PTP_CMD_CTL) SPECIFICATIONS

Bit	Description	Type	Default
31:14	**RESERVED**	RO	—
13	**Clock Target Read (PTP_CLOCK_TARGET_READ)** Writing a one to this bit causes the current values of both of the 1588 clock targets (A and B) to be saved into the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) and the PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) so they can be read. Writing a zero to this bit has no effect.	W1S/SC	0b
12:9	**PTP Manual Capture Select 3-0 (PTP_MANUAL_CAPTURE_SEL[3:0])** These bits specify which GPIO PTP Clock Capture Registers are used during a manual capture. Bit 3 selects the rising edge (0) or falling edge (1) registers. Bits 2-0 select the GPIO number. All 8 GPIO register sets are available.	R/W	0000b

TABLE 243: PTP COMMAND AND CONTROL REGISTER (PTP_CMD_CTL) SPECIFICATIONS

Bit	Description	Type	Default
8	**PTP Manual Capture (PTP_MANUAL_CAPTURE)** Writing a one to this bit causes the current value of the 1588 clock to be saved into the GPIO PTP Clock Capture Registers specified above. The corresponding bit in the PTP Interrupt Status Register (PTP_INT_STS) is also set. Writing a zero to this bit has no effect.	W1S/SC	0b
7	**Clock Temporary Rate (PTP_CLOCK_TEMP_RATE)** Writing a one to this bit enables the use of the temporary clock rate adjustment specified in the PTP Clock Temporary Rate Adjustment Register (PTP_CLOCK_TEMP_RATE_ADJ) for the duration specified in the PTP Clock Temporary Rate Duration Register (PTP_CLOCK_TEMP_RATE_DURATION). Writing a zero to this bit has no effect.	W1S/SC	0b
6	**Clock Step NanoSeconds (PTP_CLOCK_STEP_NANOSECONDS)** Writing a one to this bit adds the value of the Clock Step Adjustment Value (PTP_CLOCK_STEP_ADJ_VALUE) field in the PTP Clock Step Adjustment Register (PTP_CLOCK_STEP_ADJ) to the nanoseconds portion of the 1588 Clock. Writing a zero to this bit has no effect.	W1S/SC	0b
5	**Clock Step Seconds (PTP_CLOCK_STEP_SECONDS)** Writing a one to this bit adds or subtracts the value of the Clock Step Adjustment Value (PTP_CLOCK_STEP_ADJ_VALUE) field in the PTP Clock Step Adjustment Register (PTP_CLOCK_STEP_ADJ) to or from the seconds portion of the 1588 Clock. The choice of adding or subtracting is set using the Clock Step Adjustment Direction (PTP_CLOCK_STEP_ADJ_DIR) bit. Writing a zero to this bit has no effect.	W1S/SC	0b
4	**Clock Load (PTP_CLOCK_LOAD)** Writing a one to this bit writes the value of the PTP Clock Seconds Register (PTP_CLOCK_SEC), the PTP Clock NanoSeconds Register (PTP_CLOCK_NS) and the PTP Clock Sub-NanoSeconds Register (PTP_CLOCK_SUBNS) into the 1588 Clock. Writing a zero to this bit has no effect.	W1S/SC	0b
3	**Clock Read (PTP_CLOCK_READ)** Writing a one to this bit causes the current value of the 1588 clock to be saved into the PTP Clock Seconds Register (PTP_CLOCK_SEC), the PTP Clock NanoSeconds Register (PTP_CLOCK_NS) and the PTP Clock Sub-NanoSeconds Register (PTP_CLOCK_SUBNS) so it can be read. Writing a zero to this bit has no effect.	W1S/SC	0b

TABLE 243: PTP COMMAND AND CONTROL REGISTER (PTP_CMD_CTL) SPECIFICATIONS

Bit	Description	Type	Default
2	**PTP Enable (PTP_ENABLE)** Writing a one to this bit will enable the 1588 unit. Reading this bit will return the current enabled value. Writing a zero to this bit has no effect.	R/W1S	0b
1	**PTP Disable (PTP_DISABLE)** Writing a one to this bit will cause the PTP Enable (PTP_ENABLE) to clear once all current frame processing is completed. No new frame processing will be started if this bit is set. Writing a zero to this bit has no effect.	W1S/SC	0b
0	**PTP Reset (PTP_RESET)** Writing a one to this bit resets the 1588 H/W, state machines and registers and disables the 1588 unit. Any frame modifications in progress are halted at the risk of causing frame data or FCS errors. PTP_Reset should only be used once the 1588 unit is disabled as indicated by the PTP Enable (PTP_ENABLE) bit. Writing a zero to this bit has no effect.	W1S/SC	0b

9.2 PTP General Configuration Register (PTP_GENERAL_CONFIG)

Offset: 0A04h
Size: 32 bits

See Table 244.

Note:	Some bits in this register are new, moved or updated for LAN743x.

TABLE 244: PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31	**Time-Stamp Unit Enable (TSU_ENABLE)** This bit enables the receive and transmit functions of the time-stamp unit. The PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) bit must also be set. (See **Note 1**.)	R/W	1b
30:26	**RESERVED**	RO	—
25	**GPIO Falling Edge Capture Remap** This bit selects GPIOs 8-11 for falling edge capture in place of GPIOs 0-3.	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

2: The GPIO must be configured as an input for this function to operate. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 ns to be recognized.

3: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIO pins may be available.

4: The General Purpose IO Configuration 3 Register (GPIO_CFG3) is used to enable the clock event onto the GPIO pins. General Purpose IO Configuration 2 Register (GPIO_CFG2) sets the polarity, General Purpose IO Configuration 1 Register (GPIO_CFG1) sets the output buffer type.

TABLE 244: PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
24	**GPIO Rising Edge Capture Remap** This bit selects GPIOs 8-11 for rising edge capture in place of GPIOs 0-3.	R/W	0b
23:21	**RESERVED**	RO	—
20	**GPIO PTP Timer Interrupt B Clear Enable (GPIO_PTP_TIMER_INT_B_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP_TIMER_INT_B bit of the PTP Interrupt Status Register (PTP_INT_STS). The GPIO input is selected using the GPIO PTP Timer Interrupt B Clear Select (GPIO_PTP_TIMER_INT_B_CLEAR_SEL[3:0]) bits in this register. The polarity of the GPIO input is determined by GPIO Polarity 0-11 (GPIOPOL[11:0]) in the General Purpose IO Configuration 2 Register (GPIO_CFG2). (See **Note 2**.)	R/W	0b
19:16	**GPIO PTP Timer Interrupt B Clear Select (GPIO_PTP_TIMER_INT_B_CLEAR_SEL[3:0])** These bits determine which GPIO is used to clear the PTP Timer Interrupt B (PTP_TIMER_INT_B) bit of the PTP Interrupt Status Register (PTP_INT_STS). (See **Note 3**.)	R/W	000b
15:13	**RESERVED**	RO	—
12	**GPIO PTP Timer Interrupt A Clear Enable (GPIO_PTP_TIMER_INT_A_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP Timer Interrupt A (PTP_TIMER_INT_A) bit of the PTP Interrupt Status Register (PTP_INT_STS). The GPIO input is selected using the GPIO PTP Timer Interrupt A Clear Select (GPIO_PTP_TIMER_INT_A_CLEAR_SEL[3:0]) bits in this register. The polarity of the GPIO input is determined by GPIO Polarity 0-11 (GPIOPOL[11:0]) in the General Purpose IO Configuration 2 Register (GPIO_CFG2). (See **Note 2**.)	R/W	0b
11:8	**GPIO PTP Timer Interrupt A Clear Select (GPIO_PTP_TIMER_INT_A_CLEAR_SEL[3:0])** These bits determine which GPIO is used to clear the PTP_TIMER_INT_A bit of the PTP Interrupt Status Register (PTP_INT_STS). (See **Note 3**.)	R/W	000b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

2: The GPIO must be configured as an input for this function to operate. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 ns to be recognized.

3: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIO pins may be available.

4: The General Purpose IO Configuration 3 Register (GPIO_CFG3) is used to enable the clock event onto the GPIO pins. General Purpose IO Configuration 2 Register (GPIO_CFG2) sets the polarity, General Purpose IO Configuration 1 Register (GPIO_CFG1) sets the output buffer type.

TABLE 244: PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
7:5	**Clock Event Channel B Mode (CLOCK_EVENT_B)** These bits determine the output on Clock Event Channel B when a Clock Target compare event occurs. 000: 100 ns 001: 10 µs 010: 100 µs 011: 1 ms 100: 10 ms 101: 200 ms 110: Toggle 111: PTP_TIMER_INT_B bit value in the PTP_INT_STS register (See **Note 4**.)	R/W	000b
4	**Reload/Add B (RELOAD_ADD_B)** This bit determines the course of action when a Clock Target compare event for Clock Event Channel B occurs. When set, the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) and PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) are loaded from the PTP Clock Target x Reload / Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) and PTP Clock Target x Reload / Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x) x = B. When low, the Clock Target Registers are incremented by the Clock Target Reload Registers. 0: Increment upon a clock target compare event 1: Reload upon a clock target compare event	R/W	0b
3:1	**Clock Event Channel A Mode (CLOCK_EVENT_A)** These bits determine the output on Clock Event Channel A when a Clock Target compare event occurs. 000: 100 ns 001: 10 µs 010: 100 µs 011: 1 ms 100: 10 ms 101: 200 ms 110: Toggle 111: PTP_TIMER_INT_A bit value in the PTP_INT_STS register (See **Note 4**.)	R/W	000b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

2: The GPIO must be configured as an input for this function to operate. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 ns to be recognized.

3: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIO pins may be available.

4: The General Purpose IO Configuration 3 Register (GPIO_CFG3) is used to enable the clock event onto the GPIO pins. General Purpose IO Configuration 2 Register (GPIO_CFG2) sets the polarity, General Purpose IO Configuration 1 Register (GPIO_CFG1) sets the output buffer type.

TABLE 244: PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
0	**Reload/Add A (RELOAD_ADD_A)** This bit determines the course of action when a Clock Target compare event for Clock Event Channel A occurs. When set, the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) and PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) are loaded from the PTP Clock Target x Reload / Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) and PTP Clock Target x Reload / Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x) x = A. When low, the Clock Target Registers are incremented by the Clock Target Reload Registers. 0: Increment upon a clock target compare event 1: Reload upon a clock target compare event	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

2: The GPIO must be configured as an input for this function to operate. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 ns to be recognized.

3: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIO pins may be available.

4: The General Purpose IO Configuration 3 Register (GPIO_CFG3) is used to enable the clock event onto the GPIO pins. General Purpose IO Configuration 2 Register (GPIO_CFG2) sets the polarity, General Purpose IO Configuration 1 Register (GPIO_CFG1) sets the output buffer type.

9.3 PTP Interrupt Status Register (PTP_INT_STS)

Offset: 0A08h
Size: 32 bits

This read/write register contains the 1588 interrupt status bits. (See Table 245.)

Writing a 1 to a interrupt status bits acknowledges and clears the individual interrupt. If enabled in the PTP Interrupt Enable Set Register (PTP_INT_EN_SET), these interrupt bits are cascaded into the 1588 Interrupt (1588_INT) bit of the Interrupt Status Register (INT_STS). Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt. The 1588 Interrupt Enable Set (1588_INT_EN_SET) bit of the Interrupt Enable Set Register (INT_EN_SET) must also be set in order for an actual system level interrupt to occur. Refer to Section 7.0, Interrupt Controller Registers for additional information.

If the host attempts to clear a R/W1C bit within the PTP_INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding PTP_INT_STS bit will remain set.

TABLE 245: PTP INTERRUPT STATUS REGISTER (PTP_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**PTP GPIO Falling Edge Interrupt (PTP_GPIO_FE_INT[7:0])** This interrupt indicates that a falling event occurred and the 1588 Clock was captured. (See **Note 1**.)	R/W1C	00h
23:16	**PTP GPIO Rising Edge Interrupt (PTP_GPIO_RE_INT[7:0])** This interrupt indicates that a rising event occurred and the 1588 Clock was captured. (See **Note 2**.)	R/W1C	00h
15:14	**RESERVED**	RO	—
13	**PTP TX Software Timestamp Error Interrupt (PTP_TX_SWTS_ERR_INT)** This interrupt indicates that a software triggered TX timestamp request was unsuccessful due to a full capture buffer.	R/W1C	0b
12	**PTP TX Timestamp Interrupt (PTP_TX_TS_INT)** This interrupt indicates that a packet was transmitted and its egress time stored. Up to four events, as indicated by the PTP TX Timestamp Count (PTP_TX_TS_CNT[2:0]) field in the PTP Capture Information Register (PTP_CAP_INFO), are buffered.	R/W1C	0b
11:9	**RESERVED**	RO	—
8	**PTP RX Timestamp Interrupt (PTP_RX_TS_INT)** This interrupt indicates that a packet was received and its ingress time and associated data stored. Only one capture is saved at a time. Further captures are suppressed until this bit is cleared.	R/W1C	
7:2	**RESERVED**	RO	—
1	**PTP Timer Interrupt B (PTP_TIMER_INT_B)** This interrupt indicates that the 1588 clock equaled or passed the Clock Event Channel B Clock Target value in the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) and PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) x = B. (See **Note 3**.)	R/W1C	0b
0	**PTP Timer Interrupt A (PTP_TIMER_INT_A)** This interrupt indicates that the 1588 clock equaled or passed the Clock Event Channel A Clock Target value in the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) and PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) x = A. (See **Note 2**.)	R/W1C	0b

Note 1: As 1588 capture inputs, GPIO inputs are edge sensitive and must be low for greater than 40 ns to be recognized as interrupt inputs. These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).

2: As 1588 capture inputs, GPIO inputs are edge sensitive and must be high for greater than 40 ns to be recognized as interrupt inputs.These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).

3: This bit is also cleared by an active edge on a GPIO if enabled. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 ns to be recognized as a clear input.

9.4 PTP Interrupt Enable Set Register (PTP_INT_EN_SET)

Offset: 0A0Ch
Size: 32 bits

See Table 246.

This register is used to set the interrupt enables for the corresponding bits in the PTP Interrupt Status Register (PTP_INT_STS). Writing a '1' to a bit sets the corresponding enable and configures the corresponding interrupt as a source for the assertion of the 1588 interrupt. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables.

TABLE 246: PTP INTERRUPT ENABLE SET REGISTER (PTP_INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**PTP GPIO Falling Edge Interrupt Enable Set (PTP_GPIO_FE_EN_SET[7:0])**	R/W1S	00h
23:16	**PTP GPIO Rising Edge Interrupt Enable Set (PTP_GPIO_RE_EN_SET[7:0])**	R/W1S	00h
15:14	**RESERVED**	RO	—
13	**PTP TX Software Timestamp Error Enable Set (PTP_TX_SWTS_ERR_EN_SET)**	R/W1S	0b
12	**PTP TX Timestamp Enable Set (PTP_TX_TS_EN_SET)**	R/W1S	0b
11:9	**RESERVED**	RO	—
8	**PTP RX Timestamp Enable Set (PTP_RX_TS_EN_SET)**	R/W1S	0b
7:2	**RESERVED**	RO	—
1	**PTP Timer B Interrupt Enable Set (PTP_TIMER_EN_SET_B)**	R/W1S	0b
0	**PTP Timer A Interrupt Enable Set (PTP_TIMER_EN_SET_A)**	R/W1S	0b

9.5 PTP Interrupt Enable Clear Register (PTP_INT_EN_CLR)

Offset: 0A10h
Size: 32 bits
See Table 247.

This register is used to clear the interrupt enables for the corresponding bits in the PTP Interrupt Status Register (PTP_INT_STS). Writing a '1' to a bit clears the corresponding enable. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables.

TABLE 247: PTP INTERRUPT ENABLE CLEAR REGISTER (PTP_INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**PTP GPIO Falling Edge Interrupt Enable Clear (PTP_GPIO_FE_EN_CLR[7:0])**	R/W1C	00h
23:16	**PTP GPIO Rising Edge Interrupt Enable Clear (PTP_GPIO_RE_EN_CLR[7:0])**	R/W1C	00h
15:14	**RESERVED**	RO	—
13	**PTP TX Software Timestamp Error Enable Clear (PTP_TX_SWTS_ERR_EN_CLR)**	R/W1C	0b
12	**PTP TX Timestamp Enable Clear (PTP_TX_TS_EN_CLR)**	R/W1C	0b
11:9	**RESERVED**	RO	—
8	**PTP RX Timestamp Enable Clear (PTP_RX_TS_EN_CLR)**	R/W1C	0b
7:2	**RESERVED**	RO	—
1	**PTP Timer B Interrupt Enable Clear (PTP_TIMER_EN_CLR_B)**	R/W1C	0b
0	**PTP Timer A Interrupt Enable Clear (PTP_TIMER_EN_CLR_A)**	R/W1C	0b

9.6 PTP Clock Seconds Register (PTP_CLOCK_SEC)

Offset: 0A14h
Size: 32 bits
See Table 248.

This register contains the seconds portion of the 1588 Clock. It is used to read the 1588 Clock following the setting of the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) and to directly change the 1588 Clock when the Clock Load (PTP_CLOCK_LOAD) bit is set.

TABLE 248: PTP CLOCK SECONDS REGISTER (PTP_CLOCK_SEC) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Clock Seconds (PTP_CLOCK_SEC)** This field contains the seconds portion of the 1588 Clock.	R/W	00000000h

Note 1: The value read is the saved value of the 1588 Clock when the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

9.7 PTP Clock NanoSeconds Register (PTP_CLOCK_NS)

Offset: 0A18h
Size: 32 bits

This register contains the nanoseconds portion of the 1588 Clock. It is used to read the 1588 Clock following the setting of the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) and to directly change the 1588 Clock when the Clock Load (PTP_CLOCK_LOAD) bit is set. See Table 249.

TABLE 249: PTP CLOCK NANOSECONDS REGISTER (PTP_CLOCK_NS) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Clock NanoSeconds (PTP_CLOCK_NS)** This field contains the nanoseconds portion of the 1588 Clock.	R/W	00000000h

Note 1: The value read is the saved value of the 1588 Clock when the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

9.8 PTP Clock Sub-NanoSeconds Register (PTP_CLOCK_SUBNS)

Offset: 0A1Ch
Size: 32 bits

This register contains the sub-nanoseconds portion of the 1588 Clock. It is used to read the 1588 Clock following the setting of the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) and to directly change the 1588 Clock when the Clock Load (PTP_CLOCK_LOAD) bit is set. See Table 250.

TABLE 250: PTP CLOCK SUB-NANOSECONDS REGISTER (PTP_CLOCK_SUBNS) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Clock Sub-NanoSeconds (PTP_CLOCK_SUBNS)** This field contains the sub-nanoseconds portion of the 1588 Clock.	R/W	00000000h

Note 1: The value read is the saved value of the 1588 Clock when the Clock Read (PTP_CLOCK_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

9.9 PTP Clock Rate Adjustment Register (PTP_CLOCK_RATE_ADJ)

Offset: 0A20h
Size: 32 bits

This register is used to adjust the rate of the 1588 Clock. Every 8 ns, 1588 Clock is normally incremented by 8 ns. This register is used to occasionally change that increment to 7 ns or 9 ns. See Table 251.

TABLE 251: PTP CLOCK RATE ADJUSTMENT REGISTER (PTP_CLOCK_RATE_ADJ) SPECIFICATIONS

Bit	Description	Type	Default
31	**Clock Rate Adjustment Direction (PTP_CLOCK_RATE_ADJ_DIR)** This field specifies if the 1588 Rate Adjustment causes the 1588 Clock to be faster or slower than the reference clock. 0 = slower (1588 Clock increments by 7 ns) 1 = faster (1588 Clock increments by 9 ns)	R/W	0b
30	**RESERVED**	RO	—
29:0	**Clock Rate Adjustment Value (PTP_CLOCK_RATE_ADJ_VALUE)** This field indicates an adjustment to the reference clock period of the 1588 Clock in units of 2^{-32} ns. On each 8 ns reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Clock. When the sub-nanoseconds portion wraps around to zero, the 1588 Clock will be adjusted by 1 ns.	R/W	00000000h

9.10 PTP Clock Temporary Rate Adjustment Register (PTP_CLOCK_TEMP_RATE_ADJ)

Offset: 0A24h
Size: 32 bits

This register is used to temporarily adjust the rate of the 1588 Clock. Every 8 ns, 1588 Clock is normally incremented by 8 ns. This register is used to occasionally change that increment to 7 ns or 9 ns. See Table 252.

TABLE 252: PTP CLOCK TEMPORARY RATE ADJUSTMENT REGISTER (PTP_CLOCK_TEMP_RATE_ADJ) SPECIFICATIONS

Bit	Description	Type	Default
31	**Clock Temporary Rate Adjustment Direction (PTP_CLOCK_TEMP_RATE_ADJ_DIR)** This field specifies if the 1588 Temporary Rate Adjustment causes the 1588 Clock to be faster or slower than the reference clock. 0 = slower (1588 Clock increments by 7 ns) 1 = faster (1588 Clock increments by 9 ns)	R/W	0b
30	**RESERVED**	RO	—
29:0	**Clock Temporary Rate Adjustment Value (PTP_CLOCK_TEMP_RATE_ADJ_VALUE)** This field indicates a temporary adjustment to the reference clock period of the 1588 Clock in units of 2^{-32} ns. On each 8 ns reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Clock. When the sub-nanoseconds portion wraps around to zero, the 1588 Clock will be adjusted by 1 ns (a 7 ns or 9 ns increment instead of the normal 8 ns).	R/W	00000000h

9.11 PTP Clock Temporary Rate Duration Register (PTP_CLOCK_TEMP_RATE_DURATION)

Offset: 0A28h
Size: 32 bits

This register specifies the active duration of the temporary clock rate adjustment. See Table 253.

TABLE 253: PTP CLOCK TEMPORARY RATE DURATION REGISTER (PTP_CLOCK_TEMP_RATE_DURATION) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Clock Temporary Rate Duration (PTP_CLOCK_TEMP_RATE_DURATION)** This field specifies the duration of the temporary rate adjustment in reference clock cycles.	R/W	00000000h

9.12 PTP Clock Step Adjustment Register (PTP_CLOCK_STEP_ADJ)

Offset: 0A2Ch
Size: 32 bits

This register is used to perform a one-time adjustment to either the seconds portion or the nanoseconds portion of the 1588 Clock. The amount and direction can be specified. See Table 254.

TABLE 254: PTP CLOCK STEP ADJUSTMENT REGISTER (PTP_CLOCK_STEP_ADJ) SPECIFICATIONS

Bit	Description	Type	Default
31	**Clock Step Adjustment Direction (PTP_CLOCK_STEP_ADJ_DIR)** This field specifies if the Clock Step Adjustment Value (PTP_CLOCK_STEP_-ADJ_VALUE) is added to or subtracted from the 1588 Clock. 0 = subtracted 1 = added (See **Note 1**.)	R/W	0b
30	**RESERVED**	RO	—
29:0	**Clock Step Adjustment Value (PTP_CLOCK_STEP_ADJ_VALUE)** When the nanoseconds portion of the 1588 Clock is being adjusted, this field specifies the amount to add. This is in lieu of the normal 7 ns, 8 ns or 9 ns increment. When the seconds portion of the 1588 Clock is being adjusted, the lower 4 bits of this field specify the amount to add to or subtract.	R/W	00000000h

Note 1: Only addition is supported for the nanoseconds portion of the 1588 Clock.

9.13 PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x)

Offset: Channel A: 0A30h
Channel B: 0A40h
Size: 32 bits

This read/write register combined with PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) form the 1588 Clock Target value. The 1588 Clock Target value is compared to the current 1588 Clock value and can be used to trigger an interrupt upon at match. See Table 255.

TABLE 255: PTP CLOCK TARGET X SECONDS REGISTER (PTP_CLOCK_TARGET_SEC_X) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Clock Target Seconds (CLOCK_TARGET_SEC)** This field contains the seconds portion of the 1588 Clock Compare value.	R/W	00000000h

Note 1: Both this register and the PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x) must be written for either to be affected.

2: The value read is the saved value of the 1588 Clock Target when the Clock Target Read (PTP_-CLOCK_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

3: When the Clock Target Read (PTP_CLOCK_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command should not be requested in between writing this register and the PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x).

9.14 PTP Clock Target x NanoSeconds Register (PTP_CLOCK_TARGET_NS_x)

Offset: Channel A: 0A34h
Channel B: 0A34h
Size: 32 bits

This read/write register combined with PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) form the 1588 Clock Target value. The 1588 Clock Target value is compared to the current 1588 Clock value and can be used to trigger an interrupt upon at match. See Table 256.

TABLE 256: PTP CLOCK TARGET X NANOSECONDS REGISTER (PTP_CLOCK_TARGET_NS_X) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Clock Target NanoSeconds (CLOCK_TARGET_NS)** This field contains the nanoseconds portion of the 1588 Clock Compare value.	R/W	00000000h

Note 1: Both this register and the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x) must be written for either to be affected.

2: The value read is the saved value of the 1588 Clock Target when the Clock Target Read (PTP_-CLOCK_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

3: When the Clock Target Read (PTP_CLOCK_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command should not be requested in between writing this register and the PTP Clock Target x Seconds Register (PTP_CLOCK_TARGET_SEC_x).

9.15 PTP Clock Target x Reload/Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x)

Offset: Channel A: 0A38h
Channel B: 0A48h
Size: 32 bits

This read/write register combined with PTP Clock Target x Reload/Add NanoSeconds Register (PTP_CLOCK_TAR-GET_RELOAD_NS_x) form the 1588 Clock Target Reload value. The 1588 Clock Target Reload is the value that is reloaded or added to the 1588 Clock Compare value when a clock compare event occurs. See Table 257.

TABLE 257: PTP CLOCK TARGET X RELOAD / ADD SECONDS REGISTER (PTP_CLOCK_TARGET_RELOAD_SEC_X) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Clock Target Reload Seconds (CLOCK_TARGET_RELOAD_SEC)** This field contains the seconds portion of the 1588 Clock Target Reload value that is reloaded to the 1588 Clock Compare value.	R/W	00000000h

Note 1: Both this register and the PTP Clock Target x Reload/Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x) must be written for either to be affected.

9.16 PTP Clock Target x Reload / Add NanoSeconds Register (PTP_CLOCK_TARGET_RELOAD_NS_x)

Offset: Channel A: 0A3Ch
Channel B: 0A4Ch
Size: 32 bits

This read/write register combined with PTP Clock Target x Reload / Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) form the 1588 Clock Target Reload value. The 1588 Clock Target Reload is the value that is reloaded or added to the 1588 Clock Compare value when a clock compare event occurs. See Table 258.

TABLE 258: PTP CLOCK TARGET X RELOAD / ADD NANOSECONDS REGISTER (PTP_CLOCK_TARGET_RELOAD_NS_X) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Clock Target Reload NanoSeconds (CLOCK_TARGET_RELOAD_NS)** This field contains the nanoseconds portion of the 1588 Clock Target Reload value that is reloaded to the 1588 Clock Compare value.	R/W	00000000h

Note 1: Both this register and the PTP Clock Target x Reload/Add Seconds Register (PTP_CLOCK_TARGET_RELOAD_SEC_x) must be written for either to be affected.

9.17 PTP User MAC Address High-WORD Register (PTP_USER_MAC_HI)

Offset: 0A50h
Size: 32 bits

This read/write register combined with the PTP User MAC Address Low-DWORD Register (PTP_USER_MAC_LO) forms the 48-bit user defined MAC address. The Auxiliary MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bit in the PTP RX Parsing Configuration Register (PTP_RX_PARSE_CONFIG). See Table 259.

TABLE 259: PTP USER MAC ADDRESS HIGH-WORD REGISTER (PTP_USER_MAC_HI) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**User MAC Address High (USER_MAC_HI)** This field contains the high 16 bits of the user defined MAC address used for PTP packet detection. The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

9.18 PTP User MAC Address Low-DWORD Register (PTP_USER_MAC_LO)

Offset: 0A54h
Size: 32 bits

This read/write register combined with the PTP User MAC Address High-WORD Register (PTP_USER_MAC_HI) forms the 48-bit user defined MAC address. The Auxiliary MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bit in the PTP RX Parsing Configuration Register (PTP_RX_PARSE_CONFIG). See Table 260.

TABLE 260: PTP USER MAC ADDRESS LOW-DWORD REGISTER (PTP_USER_MAC_LO) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**User MAC Address Low (USER_MAC_LO)** This field contains the low 32 bits of the user defined MAC address used for PTP packet detection. (See **Note 1**.)	R/W	00000000h

Note 1: The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.19 PTP GPIO Select Register (PTP_GPIO_SEL)

Offset: 0A58h
Size: 32 bits
See Table 261.

TABLE 261: PTP GPIO SELECT REGISTER (PTP_GPIO_SEL) SPECIFICATIONS

Bit	Description	Type	Default
31:11	**RESERVED**	RO	—
10:8	**GPIO Select (GPIO_SEL[2:0])** This field specifies which GPIO the various GPIO x registers will access. Although there could be more GPIO inputs, there are eight sets of capture registers (x = 0 to 7).	R/W	000b
7:0	**RESERVED**	RO	—

9.20 PTP Latency Register (PTP_LATENCY)

Offset: 0A5Ch
Size: 32 bits
See Table 262.

TABLE 262: PTP LATENCY REGISTER (PTP_LATENCY) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**TX Latency (TX_LATENCY[15:0])** This field specifies the egress delay in nanoseconds between the PTP timestamp point and the network medium. The setting is used to adjust the internally captured 1588 clock value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The value depends on the port mode. Typical values are: • 1000BASE-T: 117 ns • 100BASE-TX: 181 ns • 1000Mbps GMII: 8 ns plus any external transmit latency • 100Mbps MII: 63 ns plus any external transmit latency • 10Mbps MII: 783 ns plus any external transmit latency • 1000Mbps RGMII: 19 ns plus any external transmit latency • 100Mbps RGMII: 115 ns plus any external transmit latency • 10Mbps RGMII: 1195 ns plus any external transmit latency (See **Note 1**.)	R/W	0000h
15:0	**RX Latency (RX_LATENCY[15:0])** This field specifies the ingress delay in nanoseconds between the network medium and the PTP timestamp point. The setting is used to adjust the internally captured 1588 clock value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The value depends on the port mode. Typical values are: • 1000BASE-T: 444 ns • 100BASE-TX: 594 ns • 1000Mbps GMII: 18 ns plus any external receive latency • 100Mbps MII: 18 ns plus any external receive latency • 10Mbps MII: 18 ns plus any external receive latency • 1000Mbps RGMII: 50 ns plus any external receive latency • 100Mbps RGMII: 179 ns plus any external receive latency • 10Mbps RGMII: 1618 ns plus any external receive latency (See **Note 1**.)	R/W	0000h

Note 1: The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.21 PTP Asymmetry and Peer Delay Register (PTP_ASYM_PEERDLY)

Port Delay Asymmetry (DELAY_ASYM[15:0]) and RX Peer Delay (RX_PEER_DELAY[15:0]) are handled by S/W in ordinary clocks, therefore the register is removed.

9.22 PTP Capture Information Register (PTP_CAP_INFO)

Offset: 0A60h
Size: 32 bits
See Table 263.

This read only register provides information about transmit capture buffers.

TABLE 263: PTP CAPTURE INFORMATION REGISTER (PTP_CAP_INFO) SPECIFICATIONS

Bit	Description	Type	Default
31:7	**RESERVED**	RO	—
6:4	**PTP TX Timestamp Count (PTP_TX_TS_CNT[2:0])** This field indicates how many transmit timestamps are available to be read. It is incremented when a PTP packet is transmitted and decremented when the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) bit is written with a '1.'	RO	000b
3:0	**RESERVED**	RO	—

9.22.1 PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG)

Offset:
Size: 32 bits
See Table 264.

This register is used to configure the PTP receive message detection.

TABLE 264: PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31:18	**RESERVED**	RO	—
17	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP checksum for PTP frame parsing. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not validated and the frame is not timestamped. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not validated and the frame is not timestamped. (See **Note 1**.)	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 264: PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
16	**RX MAC/IP Consistency Checking** When cleared, the destination MAC and IP addresses are independently tested. When set, the destination MAC must be consistent with the corresponding IP address. (See **Note 1**.)	R/W	0b
15	**RX Peer/Non-peer Mixing** When cleared, the destination MAC and IP addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages respectively. When set, either address may be used for either peer delay messages or non-peer delay messages. (See **Note 1**.)	R/W	0b
14	**RX Layer 2 Address 1 Enable (RX_LAYER2_ADD1_EN)** This bit enables the Layer 2 MAC address of 01:80:C2:00:00:0E for PTP packets. (See **Note 1**.)	R/W	1b
13	**RX Layer 2 Address 2 Enable (RX_LAYER2_ADD2_EN)** This bit enables the Layer 2 MAC address of 01:1B:19:00:00:00 for PTP packets. (See **Note 1**.)	R/W	1b
12	**RX Address 1 Enable (RX_ADD1_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:81 and IPv4 destination address of 224.0.1.129 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:81 and IPv6 destination address of FF0X:0:0:0:0:0:0:181 for PTP packets. (See **Note 1**.)	R/W	1b
11	**RX Address 2 Enable (RX_ADD2_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:82 and IPv4 destination address of 224.0.1.130 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:82 and IPv6 destination address of FF0X:0:0:0:0:0:0:182 for PTP packets. (See **Note 1**.)	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 264: PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
10	**RX Address 3 Enable (RX_ADD3_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:83 and IPv4 destination address of 224.0.1.131 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:83 and IPv6 destination address of FF0X:0:0:0:0:0:0:183 for PTP packets. (See **Note 1**.)	R/W	0b
9	**RX Address 4 Enable (RX_ADD4_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:84 and IPv4 destination address of 224.0.1.132 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:84 and IPv6 destination address of FF0X:0:0:0:0:0:0:184 for PTP packets. (See **Note 1**.)	R/W	0b
8	**RX Address 5 Enable (RX_ADD5_EN)** This bit enables the IPv4 MAC address of 01:00:5e:00:00:6B and IPv4 destination address of 224.0.0.107 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:00:6B and IPv6 destination address of FF02:0:0:0:0:0:0:6B for PTP packets. (See **Note 1.**)	R/W	1b
7	**RX User Defined Layer 2 MAC Address Enable (RX_LAYER2_USER_MAC_EN)** This bit enables a user defined Layer 2 MAC address in PTP messages. (See **Note 1.**)	R/W	0b
6	**RX User Defined IPv6 MAC Address Enable (RX_IPV6_USER_MAC_EN)** This bit enables a user defined IPv6 MAC address in PTP messages. (See **Note 1.**)	R/W	0b
5	**RX User Defined IPv4 MAC Address Enable (RX_IPV4_USER_MAC_EN)** This bit enables the user defined IPv4 MAC address in PTP messages. The address is defined via the PTP User MAC Address High-WORD Register (PTP_USER_MAC_HI) and the PTP User MAC Address Low-DWORD Register (PTP_USER_MAC_LO). (See **Note 1.**)	R/W	0b
4	**RX IP Address Enable (RX_IP_ADDR_EN)** This bit enables the checking of the IP destination address in PTP messages for both IPv4 and IPv6 formats. (See **Note 1.**)	R/W	1b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 264: PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
3	**RX MAC Address Enable (RX_MAC_ADDR_EN)** This bit enables the checking of the MAC destination address in PTP messages. (See **Note 1.**)	R/W	1b
2	**RX Layer 2 Enable (RX_LAYER2_EN)** This bit enables the detection of the layer 2 formatted PTP messages. (See **Note 1.**)	R/W	1b
1	**RX IPv6 Enable (RX_IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. (See **Note 1.**)	R/W	1b
0	**RX IPv4 Enable (RX_IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. (See **Note 1.**)	R/W	1b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.23 PTP RX Timestamp Configuration Register (PTP_RX_TIMESTAMP_CONFIG)

Offset: 0A68h
Size: 32 bits
See Table 265.

This register is used to configure PTP receive message timestamping.

TABLE 265: PTP RX TIMESTAMP CONFIGURATION REGISTER (PTP_RX_TIMESTAMP_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RX PTP Domain (RX_PTP_DOMAIN[7:0])** This field specifies the PTP domain in use. If RX PTP Domain Match Enable (RX_PTP_DOMAIN_EN) is set, the domainNumber in the PTP message must match the value in this field in order to recorded the ingress time. (See **Note 1**.)	R/W	00h
23	**RX PTP Domain Match Enable (RX_PTP_DOMAIN_EN)** When this bit is set, the domainNumber in the PTP message is checked against the value in RX PTP Domain (RX_PTP_DOMAIN[7:0]). (See **Note 1**.)	R/W	0b
22	**RX PTP Alternate Master Enable (RX_PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. (See **Note 1**.)	R/W	0b
21	**RX PTP UDP Checksum Check Disable (RX_PTP_UDP_CHKSUM_DIS)** When this bit is cleared, ingress times are not saved and ingress messages are not filtered if the frame has an invalid UDP checksum. When this bit is set, the UDP checksum check is bypassed and the ingress time is saved and ingress messages are filtered regardless. (See **Note 1**.)	R/W	0b
20	**RX PTP FCS Check Disable (RX_PTP_FCS_DIS)** When this bit is cleared, ingress times are not saved and ingress messages are not filtered if the frame has an invalid FCS. When this bit is set, the FCS check is bypassed. (See **Note 1**.)	R/W	0b
19:16	**RX PTP Version (RX_PTP_VERSION[3:0])** This field specifies the PTP version in use. A setting of 0 allows any PTP version. (See **Note 1**.)	R/W	2h

Note 1: The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 265: PTP RX TIMESTAMP CONFIGURATION REGISTER (PTP_RX_TIMESTAMP_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:0	**RX PTP Message Type Enable (RX_PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, PDelay_Req and PDelay_Resp messages are enabled.	R/W	0000h

Note 1: The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.24 PTP RX Timestamp Insertion Configuration Register (PTP_RX_TS_INSERT_CONFIG)

RX timestamp insertion is removed, therefore this register is removed.

9.25 PTP RX Correction Field Modification Register (PTP_RX_CF_MOD)

RX correction field modification is removed, therefore this register is removed.

9.26 PTP RX Filter Configuration Register (PTP_RX_FILTER_CONFIG)

RX message filtering is removed, therefore this register is removed.

9.27 PTP RX Ingress Time Seconds Register (PTP_RX_INGRESS_SEC)

Offset: 0A78h
Size: 32 bits
See Table 266.

This read only register combined with the PTP RX Ingress Time NanoSeconds Register (PTP_RX_INGRESS_NS) contains the RX timestamp captures.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field is set.

TABLE 266: PTP RX INGRESS TIME SECONDS REGISTER (PTP_RX_INGRESS_SEC) SPECIFICATIONS

Bits	Description	Type	Default
31:0	**Timestamp Seconds (TS_SEC)** This field contains the seconds portion of the receive ingress time.	RO	00000000h

9.28 PTP RX Ingress Time NanoSeconds Register (PTP_RX_INGRESS_NS)

Offset: 0A7Ch
Size: 32 bits
See Table 267.

This read only register combined with the PTP RX Ingress Time Seconds Register (PTP_RX_INGRESS_SEC) contains the RX timestamp capture.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field is set.

TABLE 267: PTP RX INGRESS TIME NANOSECONDS REGISTER (PTP_RX_INGRESS_NS) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Timestamp NanoSeconds (TS_NS)** This field contains the nanoseconds portion of the receive ingress time.	RO	00000000h

9.29 PTP RX Message Header Register (PTP_RX_MSG_HEADER)

Offset: 0A80h
Size: 32 bits

This read only register contains the RX message header. See Table 268.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field is set.

TABLE 268: PTP RX MESSAGE HEADER REGISTER (PTP_RX_MSG_HEADER) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**Source Port Identity CRC (SRC_PRT_CRC)** This field contains the 12-bit CRC of the source port identity field of the received PTP packet.	RO	000h
19:16	**Message Type (MSG_TYPE)** This field contains the message type field of the received PTP packet.	RO	0h
15:0	**Sequence ID (SEQ_ID)** This field contains the sequenced field of the received PTP packet.	RO	0000h

9.30 PTP RX Pdelay_Req Ingress Time Seconds Register (PTP_RX_PDREQ_SEC)

One-step Pdelay_Resp TX messages correctionField modification is removed, therefore this register is removed.

9.31 PTP RX Pdelay_Req Ingress Time NanoSeconds Register (PTP_RX_PDREQ_NS)

One-step Pdelay_Resp TX messages correctionField modification is removed, therefore this register is removed.

9.32 PTP RX Pdelay_Req Ingress Correction Field High Register (PTP_RX_PDREQ_CF_HI)

One-step Pdelay_Resp TX messages correctionField modification is removed, therefore this register is removed.

9.33 PTP RX Pdelay_Req Ingress Correction Field Low Register (PTP_RX_PDREQ_CF_LOW)

One-step Pdelay_Resp TX messages correctionField modification is removed, therefore this register is removed.

9.34 PTP RX Checksum Dropped Count Register (PTP_RX_CHKSUM_DROPPED_CNT)

Dropping ingress checksum errors is removed, therefore this register is removed.

9.35 PTP RX Filtered Count Register (PTP_RX_FILTERED_CNT)

Ingress filtering is removed, therefore this register is removed.

9.36 PTP TX Parsing Configuration Register (PTP_TX_PARSE_CONFIG)

Offset: 0A9Ch
Size: 32 bits

This register is used to configure the PTP transmit message detection. See Table 269.

TABLE 269: PTP TX PARSING CONFIGURATION REGISTER (PTP_TX_PARSE_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31:17	**RESERVED**	RO	—
16	**TX MAC/IP Consistency Checking** When cleared, the destination MAC and IP addresses are independently tested. When set, the destination MAC must be consistent with the corresponding IP address. (See **Note 1**.)	R/W	0b
15	**TX Peer/Non-peer Mixing** When cleared, the destination MAC and IP addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages respectively. When set, either address may be used for either peer delay messages or non-peer delay messages. (See **Note 1**.)	R/W	0b
14	**TX Layer 2 Address 1 Enable (TX_LAYER2_ADD1_EN)** This bit enables the Layer 2 MAC address of 01:80:C2:00:00:0E for PTP packets. (See **Note 1**.)	R/W	1b
13	**TX Layer 2 Address 2 Enable (TX_LAYER2_ADD2_EN)** This bit enables the Layer 2 MAC address of 01:1B:19:00:00:00 for PTP packets. (See **Note 1**.)	R/W	1b
12	**TX Address 1 Enable (TX_ADD1_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:81 and IPv4 destination address of 224.0.1.129 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:81 and IPv6 destination address of FF0X:0:0:0:0:0:0:181 for PTP packets. (See **Note 1**.)	R/W	1b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 269: PTP TX PARSING CONFIGURATION REGISTER (PTP_TX_PARSE_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
11	**TX Address 2 Enable (TX_ADD2_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:82 and IPv4 destination address of 224.0.1.130 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:82 and IPv6 destination address of FF0X:0:0:0:0:0:0:182 for PTP packets. (See **Note 1**.)	R/W	0b
10	**TX Address 3 Enable (TX_ADD3_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:83 and IPv4 destination address of 224.0.1.131 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:83 and IPv6 destination address of FF0X:0:0:0:0:0:0:183 for PTP packets. (See **Note 1**.)	R/W	0b
9	**TX Address 4 Enable (TX_ADD4_EN)** This bit enables the IPv4 MAC address of 01:00:5E:00:01:84 and IPv4 destination address of 224.0.1.132 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:01:84 and IPv6 destination address of FF0X:0:0:0:0:0:0:184 for PTP packets. (See **Note 1**.)	R/W	0b
8	**TX Address 5 Enable (TX_ADD5_EN)** This bit enables the IPv4 MAC address of 01:00:5e:00:00:6B and IPv4 destination address of 224.0.0.107 for PTP packets. This bit enables the IPv6 MAC address of 33:33:00:00:00:6B and IPv6 destination address of FF02:0:0:0:0:0:0:6B for PTP packets. (See **Note 1**.)	R/W	1b
7	**TX User Defined Layer 2 MAC Address Enable (TX_LAYER2_USER_MAC_EN)** This bit enables a user defined Layer 2 MAC address in PTP messages. (See **Note 1**.)	R/W	0b
6	**TX User Defined IPv6 MAC Address Enable (TX_IPV6_USER_MAC_EN)** This bit enables a user defined IPv6 MAC address in PTP messages. (See **Note 1**.)	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

TABLE 269: PTP TX PARSING CONFIGURATION REGISTER (PTP_TX_PARSE_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
5	**TX User Defined IPv4 MAC Address Enable (TX_IPV4_USER_MAC_EN)** This bit enables the user defined IPv4 MAC address in PTP messages. The address is defined via the PTP User MAC Address High-WORD Register (PTP_USER_MAC_HI) and the PTP User MAC Address Low-DWORD Register (PTP_USER_MAC_LO). (See **Note 1**.)	R/W	0b
4	**TX IP Address Enable (TX_IP_ADDR_EN)** This bit enables the checking of the IP destination address in PTP messages for both IPv4 and IPv6 formats. (See **Note 1**.)	R/W	1b
3	**TX MAC Address Enable (TX_MAC_ADDR_EN)** This bit enables the checking of the MAC destination address in PTP messages. (See **Note 1**.)	R/W	1b
2	**TX Layer 2 Enable (TX_LAYER2_EN)** This bit enables the detection of the layer 2 formatted PTP messages. (See **Note 1**.)	R/W	1b
1	**TX IPv6 Enable (TX_IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. (See **Note 1**.)	R/W	1b
0	**TX IPv4 Enable (TX_IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. (See **Note 1**.)	R/W	1b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.37 PTP TX Timestamp Configuration Register (PTP_TX_TIMESTAMP_CONFIG)

Offset: 0AA0h
Size: 32 bits

This register is used to configure PTP transmit message timestamping. See Table 270.

TABLE 270: PTP TX TIMESTAMP CONFIGURATION REGISTER (PTP_TX_TIMESTAMP_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**TX PTP Domain (TX_PTP_DOMAIN[7:0])** This field specifies the PTP domain in use. If TX PTP Domain Match Enable (TX_PTP_DOMAIN_EN) is set, the domainNumber in the PTP message must match the value in this field in order to recorded the egress time. (See **Note 1**.)	R/W	00h
23	**TX PTP Domain Match Enable (TX_PTP_DOMAIN_EN)** When this bit is set, the domainNumber in the PTP message is checked against the value in TX PTP Domain (TX_PTP_DOMAIN[7:0]). (See **Note 1**.)	R/W	0b
22	**TX PTP Alternate Master Enable (TX_PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. (See **Note 1**.)	R/W	0b
21:20	**RESERVED**	RO	—
19:16	**TX PTP Version (TX_PTP_VERSION[3:0])** This field specifies the PTP version in use. A setting of 0 allows any PTP version. (See **Note 1**.)	R/W	2h
15:0	**TX PTP Message Type Enable (TX_PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, PDelay_Req and PDelay_Resp messages are enabled.	R/W	0000h

Note 1: The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.38 PTP TX Modification Register (PTP_TX_MOD)

Offset: 0AA4h
Size: 32 bits

This register is used to configure TX PTP message modifications. See Table 271.

TABLE 271: PTP TX MODIFICATION REGISTER (PTP_TX_MOD) SPECIFICATIONS

Bit	Description	Type	Default
31:29	**RESERVED**	RO	—

TABLE 271: PTP TX MODIFICATION REGISTER (PTP_TX_MOD) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
28	**TX PTP Sync Message Egress Time Insertion (TX_PTP_SYNC_TS_INSERT)** This bit enables the egress time to be inserted into the originTimestamp field of Sync messages sent by the Host.	R/W	0b
27:13	**RESERVED**	RO	—
12:0	**TX Software Timestamp Insertion Offset (TX_SW_TS_INS_OFFSET)** This field specifies the offset into the frame where the 10 byte timestamp is placed. The offset is from the start of the actual transmitted frame including any optionally inserted VLAN tag.	R/W	0000h

9.39 PTP TX Modification Register 2 (PTP_TX_MOD2)

Offset: 0AA8h
Size: 32 bits

This register is used to configure TX PTP message modifications. See Table 272.

TABLE 272: PTP TX MODIFICATION REGISTER 2 (PTP_TX_MOD2) SPECIFICATIONS

Bit	Description	Type	Default
31:1	**RESERVED**	RO	—
0	**TX PTP Clear UDP/IPv4 Checksum Enable (TX_PTP_CLR_UDPV4_CHKSUM)** This bit enables the clearing of the UDP/IPv4 checksum when Pdelay_Resp Message Turnaround Time Insertion or Sync Message Egress Time Insertion is enabled. (See **Note 1**.)	R/W	0b

Note 1: The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.

9.40 PTP TX Egress Time Seconds Register (PTP_TX_EGRESS_SEC)

Offset: 0AACh
Size: 32 bits

This read only register combined with the PTP TX Egress Time NanoSeconds Register (PTP_TX_EGRESS_NS) contains the TX timestamp captures. Up to four captures are buffered. See Table 273.

Note: Values are only valid if the PTP TX Timestamp Count (PTP_TX_TS_CNT[2:0]) field indicates that at least one timestamp is available.

TABLE 273: PTP TX EGRESS TIME SECONDS REGISTER (PTP_TX_EGRESS_SEC) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Timestamp Seconds (TS_SEC)** This field contains the seconds portion of the transmit egress time.	RO	00000000h

9.41 PTP TX Egress Time NanoSeconds Register (PTP_TX_EGRESS_NS)

Offset: 0AB0h
Size: 32 bits

This read only register combined with the PTP TX Egress Time Seconds Register (PTP_TX_EGRESS_SEC) contains the TX timestamp capture. Up to four captures are buffered. See Table 274.

Note:	Values are only valid if the PTP TX Timestamp Count (PTP_TX_TS_CNT[2:0]) field indicates that at least one timestamp is available.

TABLE 274: PTP TX EGRESS TIME NANOSECONDS REGISTER (PTP_TX_EGRESS_NS) SPECIFICATIONS

Bits	Description	Type	Default
31:30	**Capture Cause (CAPTURE_CAUSE)** This field indicates the cause of the timestamp capture. 00 = Autonomous 01 = Software Requested 10 = reserved 11 = reserved	RO	00b
29:0	**Timestamp NanoSeconds (TS_NS)** This field contains the nanoseconds portion of the transmit egress time.	RO	00000000h

9.42 PTP TX Message Header Register (PTP_TX_MSG_HEADER)

Offset: 0AB4h
Size: 32 bits

This read only register contains the TX message header. Up to four captures are buffered. See Table 275.

Note:	Values are only valid if the PTP TX Timestamp Count (PTP_TX_TS_CNT[2:0]) field indicates that at least one timestamp is available.

TABLE 275: PTP TX MESSAGE HEADER REGISTER (PTP_TX_MSG_HEADER) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**Source Port Identity CRC (SRC_PRT_CRC)** This field contains the 12-bit CRC of the sourcePortIdentity field of the transmitted PTP packet.	RO	000h
19:16	**Message Type (MSG_TYPE)** This field contains the messageType field of the transmitted PTP packet.	RO	0h
15:0	**Sequence ID (SEQ_ID)** This field contains the sequenceId field of the transmitted PTP packet.	RO	0000h

9.43 PTP TX Delay_Req Egress Time Seconds Register (PTP_TX_DREQ_SEC)

Delay request egress time insertion into delay response packet is removed. Therefore, this register is removed.

9.44 PTP TX Delay_Req Egress Time NanoSeconds Register (PTP_TX_DREQ_NS)

Delay request egress time insertion into delay response packet is removed. Therefore, this register is removed.

9.45 PTP TX One-Step Sync Upper Seconds Register (PTP_TX_ONE_STEP_SYNC_SEC)

Offset: 0AC0h
Size: 32 bits

This register contains the highest 16 bits of the originTimestamp which is inserted into Sync messages when one-step timestamp insertion is enabled. See Table 276.

Note 1: This is a static field that is maintained by the Host. It is not incremented when the lower 32 bits of the 1588 Clock rollover.

2: This register applies to all ports.

TABLE 276: PTP TX ONE-STEP SYNC UPPER SECONDS REGISTER (PTP_TX_ONE_STEP_SYNC_SEC) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**Clock Seconds High (PTP_CLOCK_SEC_HI)** This field contains the highest 16 bits of seconds of the 1588 Clock.	R/W	0000h

9.46 PTP GPIO Capture Configuration Register (PTP_GPIO_CAP_CONFIG)

Offset: 0AC4h
Size: 32 bits
See Table 277.

Note 1: There are eight sets of capture registers (x = 0 to 7). Normally, GPIOs 0-7 are used as the capture sources. GPIOs 8-11 can selected in place of GPIOs 0-3 for rising edge or falling edge capture independently by setting the GPIO Rising Edge Capture Remap bit or GPIO Falling Edge Capture Remap bit, respectively, within the PTP General Configuration Register (PTP_GENERAL_CONFIG).

2: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available.

TABLE 277: PTP GPIO CAPTURE CONFIGURATION REGISTER (PTP_GPIO_CAP_CONFIG) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**Lock Enable GPIO Falling Edge (LOCK_GPIO_FE)** These bits enable/disable the GPIO falling edge lock. This lock prevents a 1588 capture from overwriting the Clock value if the GPIO interrupt in the PTP Interrupt Status Register (PTP_INT_STS) is already set due to a previous capture. 0: Disables GPIO falling edge lock 1: Enables GPIO falling edge lock	R/W	FFh
23:16	**Lock Enable GPIO Rising Edge (LOCK_GPIO_RE)** These bits enable/disable the GPIO rising edge lock. This lock prevents a 1588 capture from overwriting the Clock value if the GPIO interrupt in the PTP Interrupt Status Register (PTP_INT_STS) is already set due to a previous capture. 0: Disables GPIO rising edge lock 1: Enables GPIO rising edge lock	R/W	FFh

TABLE 277: PTP GPIO CAPTURE CONFIGURATION REGISTER (PTP_GPIO_CAP_CONFIG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:8	**GPIO Falling Edge Capture Enable 7-0 (GPIO_FE_CAPTURE_ENABLE[7:0])** These bits enable the falling edge of the respective GPIO input to capture the 1588 clock value and to set the respective PTP_GPIO interrupt in the PTP Interrupt Status Register (PTP_INT_STS). 0: Disables GPIO Capture 1: Enables GPIO Capture (See **Note 1**.)	R/W	00h
7:0	**GPIO Rising Edge Capture Enable 7-0 (GPIO_RE_CAPTURE_ENABLE[7:0])** These bits enable the rising edge of the respective GPIO input to capture the 1588 clock value and to set the respective PTP_GPIO interrupt in the PTP Interrupt Status Register (PTP_INT_STS). 0: Disables GPIO Capture 1: Enables GPIO Capture (See **Note 1**.)	R/W	00h

Note 1: The GPIO must be configured as an input for this function to operate. GPIO inputs are edge sensitive and must be low for greater than 40 ns to be recognized.

9.47 PTP GPIO x Rising Edge Clock Seconds Capture Register (PTP_GPIO_RE_CLOCK_SEC_CAP_x)

Offset: 0AC8h
Size: 32 bits
See Table 278.

This read only register combined with the PTP GPIO x Rising Edge Clock NanoSeconds Capture Register (PTP_GPIO_RE_CLOCK_NS_CAP_x) forms the GPIO rising edge timestamp capture.

Note 1: Values are only valid if the appropriate PTP GPIO Rising Edge Interrupt (PTP_GPIO_RE_INT[7:0]) in the PTP Interrupt Status Register (PTP_INT_STS) indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this register and the PTP GPIO x Rising Edge Clock NanoSeconds Capture Register (PTP_GPIO_RE_CLOCK_NS_CAP_x). Software techniques are required to avoid reading intermediate values.

3: The GPIO accessed (“x”) is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

4: There are eight sets of capture registers (x = 0 to 7). Normally, GPIOs 0-7 are used as the capture sources. GPIOs 8-11 can selected in place of GPIOs 0-3 for rising edge or falling edge capture independently by setting the GPIO Rising Edge Capture Remap bit or GPIO Falling Edge Capture Remap bit, respectively, within the PTP General Configuration Register (PTP_GENERAL_CONFIG).

5: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available. However, all 8 GPIO register sets are still available for software triggered captures.

TABLE 278: PTP GPIO X RISING EDGE CLOCK SECONDS CAPTURE REGISTER (PTP_GPIO_RE_CLOCK_SEC_CAP_X) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Timestamp Seconds (TS_SEC)** This field contains the seconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	00000000h

9.48 PTP GPIO x Rising Edge Clock NanoSeconds Capture Register (PTP_GPIO_RE_CLOCK_NS_CAP_x)

Offset: 0ACCh
Size: 32 bits
See Table 279.

This read only register combined with the PTP GPIO x Rising Edge Clock Seconds Capture Register (PTP_GPIO_RE_-CLOCK_SEC_CAP_x) forms the GPIO rising edge timestamp capture.

Note 1: Values are only valid if the appropriate PTP GPIO Rising Edge Interrupt (PTP_GPIO_RE_INT[7:0]) in the PTP Interrupt Status Register (PTP_INT_STS) indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this register and the PTP GPIO x Rising Edge Clock Seconds Capture Register (PTP_GPIO_RE_CLOCK_SEC_CAP_x). Software techniques are required to avoid reading intermediate values.

3: The GPIO accessed (“x”) is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

4: There are eight sets of capture registers (x = 0 through 7). Normally, GPIOs 0-7 are used as the capture sources. GPIOs 8-11 can selected in place of GPIOs 0-3 for rising edge or falling edge capture independently by setting the GPIO Rising Edge Capture Remap bit or GPIO Falling Edge Capture Remap bit, respectively, within the PTP General Configuration Register (PTP_GENERAL_CONFIG).

5: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available. However, all 8 GPIO register sets are still available for software triggered captures.

TABLE 279: PTP GPIO X RISING EDGE CLOCK NANOSECONDS CAPTURE REGISTER (PTP_GPIO_RE_CLOCK_NS_CAP_X) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Timestamp NanoSeconds (TS_NS)** This field contains the nanoseconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	00000000h

9.49 PTP GPIO x Falling Edge Clock Seconds Capture Register (PTP_GPIO_FE_CLOCK_SEC_CAP_x)

Offset: 0AD0h
Size: 32 bits
See Table 280.

This read only register combined with the PTP GPIO x Falling Edge Clock NanoSeconds Capture Register (PTP_GPI-O_FE_CLOCK_NS_CAP_x) forms the GPIO falling edge timestamp capture.

Note 1: Values are only valid if the appropriate PTP GPIO Falling Edge Interrupt (PTP_GPIO_FE_INT[7:0]) in the PTP Interrupt Status Register (PTP_INT_STS) indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this register and the PTP GPIO x Falling Edge Clock NanoSeconds Capture Register (PTP_GPIO_FE_CLOCK_NS_CAP_x). Software techniques are required to avoid reading intermediate values.

3: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

4: There are eight sets of capture registers (x = 0 to 7). Normally, GPIOs 0-7 are used as the capture sources. GPIOs 8-11 can selected in place of GPIOs 0-3 for rising edge or falling edge capture independently by setting the GPIO Rising Edge Capture Remap bit or GPIO Falling Edge Capture Remap bit, respectively, within the PTP General Configuration Register (PTP_GENERAL_CONFIG).

5: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available. However, all 8 GPIO register sets are still available for software triggered captures.

TABLE 280: PTP GPIO X FALLING EDGE CLOCK SECONDS CAPTURE REGISTER (PTP_GPIO_FE_CLOCK_SEC_CAP_X) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Timestamp Seconds (TS_SEC)** This field contains the seconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	00000000h

9.50 PTP GPIO x Falling Edge Clock NanoSeconds Capture Register (PTP_GPIO_FE_CLOCK_NS_CAP_x)

Offset: 0AD4h
Size: 32 bits
See Table 281.

This read only register combined with the PTP GPIO x Falling Edge Clock Seconds Capture Register (PTP_GPIO_FE_-CLOCK_SEC_CAP_x) forms the GPIO falling edge timestamp capture.

Note 1: Values are only valid if the appropriate PTP GPIO Falling Edge Interrupt (PTP_GPIO_FE_INT[7:0]) in the PTP Interrupt Status Register (PTP_INT_STS) indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this register and the PTP GPIO x Falling Edge Clock Seconds Capture Register (PTP_GPIO_FE_CLOCK_SEC_CAP_x). Software techniques are required to avoid reading intermediate values.

3: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

4: There are eight sets of capture registers (x = 0 through 7). Normally, GPIOs 0-7 are used as the capture sources. GPIOs 8-11 can selected in place of GPIOs 0-3 for rising edge or falling edge capture independently by setting the GPIO Rising Edge Capture Remap bit or GPIO Falling Edge Capture Remap bit, respectively, within the PTP General Configuration Register (PTP_GENERAL_CONFIG).

5: The IEEE 1588 Unit supports up to 12 GPIO signals. Depending upon the device, fewer GPIOs pins may be available. However, all 8 GPIO register sets are still available for software triggered captures.

TABLE 281: PTP GPIO X FALLING EDGE CLOCK NANOSECONDS CAPTURE REGISTER (PTP_GPIO_FE_CLOCK_NS_CAP_X) SPECIFICATIONS

Bit	Description	Type	Default
31:30	**RESERVED**	RO	—
29:0	**Timestamp NanoSeconds (TS_NS)** This field contains the nanoseconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	00000000h

10.0 DMA CONTROLLER REGISTERS

This section details the DMAC registers. The DMAC registers start at offset 0C00h and end at offset 0FFFh within the device. This range is for exclusive use of the DMA registers. See Table 282.

TABLE 282: DMAC REGISTER MAP

Byte Offset	Register Name (Symbol)
Common	
0C00h	DMA Controller Configuration Register (DMAC_CFG)
0C04h	DMA Controller Coalescing Configuration Register (DMAC_COAL_CFG)
0C08h	DMA Controller OBFF Configuration Register (DMAC_OBFF_CFG)
0C0Ch	DMA Controller Command Register (DMAC_CMD)
0C10h	DMA Controller Interrupt Status Register (DMAC_INT_STS)
0C14h	DMA Controller Interrupt Enable Set Register (DMAC_INT_EN_SET)
0C18h	DMA Controller Interrupt Enable Clear Register (DMAC_INT_EN_CLR)
0C1Ch	RX Absolute Timer Configuration Register (RX_ABSTMR_CFG)
0C20h	RX Relative Timer Configuration Register (RXRELTMR_CFG)
0C24h	TX Delay Timer Configuration Register (TXTMR_CFG)
0C28h	TX Absolute Timer Configuration Register (TX_ABSTMR_CFG)
0C2Ch	DMA Controller Interrupt Status Read to Clear Register (DMAC_INT_STS_R2C)
RX Channel	
0C40h	RX Channel *x* Configuration A Register (RX_CFG_A*x*) (x = 0)
0C44h	RX Channel *x* Configuration B Register (RX_CFG_B*x*) (x = 0)
0C48h	RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*) (x = 0)
0C4Ch	RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) (x = 0)
0C50h	RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*) (x=0)
0C54h	RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*) (x=0)
0C58h	RX Channel *x* Descriptor Head Register (RX_HEAD*x*) (x = 0)
0C5Ch	RX Channel *x* Descriptor Tail Register (RX_*TAIL*x) (x = 0)
0C60h	RX Channel *x* Error Status Register (RX_ERR_STSx) (x = 0)
0C64h	RX Channel *x* Configuration C Register (RX_CFG_C*x*) (x = 0)
RX Channel 1	
0C80h	RX Channel *x* Configuration A Register (RX_CFG_A*x*) (x = 1)
0C84h	RX Channel *x* Configuration B Register (RX_CFG_B*x*) (x = 1)
0C88h	RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*) (x = 1)
0C8Ch	RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) (x = 1)
0C90h	RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*) (x = 1)
0C94h	RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*) (x = 1)
0C98h	RX Channel *x* Descriptor Head Register (RX_HEAD*x*) (x = 1)
0C9Ch	RX Channel *x* Descriptor Tail Register (RX_*TAIL*x) (x = 1)
0CA0h	RX Channel *x* Error Status Register (RX_ERR_STSx) (x = 1)
0CA4h	RX Channel *x* Configuration C Register (RX_CFG_C*x*) (x = 1)
RX Channel 2	
0CC0h	RX Channel *x* Configuration A Register (RX_CFG_A*x*) (x = 2)

TABLE 282: DMAC REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
0CC4h	RX Channel *x* Configuration B Register (RX_CFG_B*x*) (x = 2)
0CC8h	RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*) (x = 2)
0CCCh	RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) (x = 2)
0CD0h	RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*) (x=2)
0CD4h	RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*) (x=2)
0CD8h	RX Channel *x* Descriptor Head Register (RX_HEAD*x*) (x = 2)
0CDCh	RX Channel *x* Descriptor Tail Register (RX_*TAIL*x*) (x = 2)
0CE0h	RX Channel *x* Error Status Register (RX_ERR_STSx) (x = 2)
0CE4h	RX Channel *x* Configuration C Register (RX_CFG_C*x*) (x = 2)
RX Channel 3	
0D00h	RX Channel *x* Configuration A Register (RX_CFG_A*x*) (x = 3)
0D04h	RX Channel *x* Configuration B Register (RX_CFG_B*x*) (x = 3)
0D08h	RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*) (x = 3)
0D0Ch	RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) (x = 3)
0D10h	RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*) (x = 3)
0D14h	RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*) (x = 3)
0D18h	RX Channel *x* Descriptor Head Register (RX_HEAD*x*) (x = 3)
0D1Ch	RX Channel *x* Descriptor Tail Register (RX_*TAIL*x*) (x = 3)
0D20h	RX Channel *x* Error Status Register (RX_ERR_STSx) (x = 3)
0D24h	RX Channel *x* Configuration C Register (RX_CFG_C*x*) (x = 3)
TX Channel 0	
0D40h	TX Channel *x* Configuration A Register (TX_CFG_Ax) (x = 0)
0D44h	TX Channel *x* Configuration B Register (TX_CFG_Bx) (x = 0)
0D48h	TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*) (x = 0)
0D4Ch	TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*) (x= 0)
0D50h	TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*) (x = 0)
0D54h	TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*) (x=0)
0D58h	TX Channel *x* Descriptor Head Register (TX_HEAD*x*) (x = 0)
0D5Ch	TX Channel *x* Descriptor Tail Register (TX_TAILx) (x = 0)
0D60h	TX Channel *x* Error Status Register (TX_ERR_STSx) (x = 0)
0D64h	TX Channel *x* Configuration C Register (TX_CFG_C*x*) (x = 0)
TX Channel 1	
0D80h	TX Channel *x* Configuration A Register (TX_CFG_Ax) (x = 1)
0D84h	TX Channel *x* Configuration B Register (TX_CFG_Bx) (x = 1)
0D88h	TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*) (x = 1)
0D8Ch	TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*) (x = 1)
0D90h	TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*) (x = 1)
0D94h	TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*) (x = 1)

TABLE 282: DMAC REGISTER MAP (CONTINUED)

Byte Offset	Register Name (Symbol)
0D98h	TX Channel *x* Descriptor Head Register (TX_HEAD*x*) (x = 1)
0D9Ch	TX Channel *x* Descriptor Tail Register (TX_TAIL*x*) (x=1)
0DA0h	TX Channel *x* Error Status Register (TX_ERR_STSx) (x = 1)
0DA4h	TX Channel *x* Configuration C Register (TX_CFG_C*x*) (x = 1)
0DA8h-0DBFh	Reserved for future expansion
TX Channel 2	
0DC0h	TX Channel *x* Configuration A Register (TX_CFG_A*x*) (x = 2)
0DC4h	TX Channel *x* Configuration B Register (TX_CFG_B*x*) (x = 2)
0DC8h	TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*) (x = 2)
0DCCh	TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*) (x = 2)
0DD0h	TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*) (x = 2)
0DD4h	TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*) (x = 2)
0DD8h	TX Channel *x* Descriptor Head Register (TX_HEAD*x*) (x = 2)
0DDCh	TX Channel *x* Descriptor Tail Register (TX_TAIL*x*) (x = 2)
0DE0h	TX Channel *x* Error Status Register (TX_ERR_STSx) (x = 2)
0DE4h	TX Channel *x* Configuration C Register (TX_CFG_C*x*) (x = 2)
0DEh8-0DFFh	Reserved for future expansion
TX Channel 3	
0E00h	TX Channel *x* Configuration A Register (TX_CFG_A*x*) (x = 3)
0E04h	TX Channel *x* Configuration B Register (TX_CFG_B*x*) (x = 3)
0E08h	TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*) (x = 3)
0E0Ch	TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*) (x = 3)
0E10h	TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*) (x = 3)
0E14h	TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*) (x = 3)
0E18h	TX Channel *x* Descriptor Head Register (TX_HEAD*x*) (x = 3)
0E1Ch	TX Channel *x* Descriptor Tail Register (TX_TAIL*x*) (x = 3)
0E20h	TX Channel *x* Error Status Register (TX_ERR_STSx) (x = 3)
0E24h	TX Channel *x* Configuration C Register (TX_CFG_C*x*) (x = 3)
0E28h-0E3Fh	Reserved for future expansion
0E40h – 0FEFh	Reserved for future expansion
0FF0h	DMAC Debug Register 0 (DMAC_DEBUG_0)
0FF4h	DMAC Debug Register 1 (DMAC_DEBUG_1)
0FF8h	DMAC Debug Register 2 (DMAC_DEBUG_2)
0FFCh-0FFFh	

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

10.0.1 DMA CONTROLLER CONFIGURATION REGISTER (DMAC_CFG)

Offset: 0024h
Size: 32 bits

This register establishes the operating parameters for the DMA Controller. See Table 283.

TABLE 283: DMA CONTROLLER CONFIGURATION REGISTER (DMAC_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:19	**RESERVED**	RO	—
18	**DMA Inter Descriptor Space Read Enable (DMA_INTR_DSCR_RD_EN)** When set, the DMAC will read the reserved space between descriptors. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0b
17	**DMA Inter Descriptor Space Write Enable (DMA_INTR_DSCR_WR_EN)** When set, the DMAC will overwrite the reserved space between descriptors. (See **Note 4** and **Note 5**.)	R/W NASR (**Note 1**)	0b
16	**DMA Coalescing Enable (DMA_COAL_EN)** When set, DMA coalescing is enabled. (Software should not modify this field unless all TX DMA channels are in the Initial state as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits. (See **Note 6**.)	R/W NASR (**Note 1**)	0b
15	**RESERVED**	RO	—
14:13	**DMA Completion Retry Count (DMA_CMPL_RETRY_CNT)** This field specifies the number of retries the DMA will use if a read request resulted in a timeout or had a poisoned indication. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00b
12	**DMA Completion Retry Enable (DMA_CMPL_RETRY_EN)** When set, the DMA will retry read requests that resulted in a timeout or had a poisoned indication. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	0b
11:10	**DMA Channel Arbitration Select (DMA_CH_ARB_SEL)** This field controls the DMA channel arbitration scheme. 00 = Fixed priority – RX higher than TX 01 = Fixed priority – Channel number order (RX higher than TX when channel number is equal) 10 = Fixed priority – RX higher than TX. Round robin priority within channels 11 = Round robin (See **Note 4** and **Note 5**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless all DMA channels are in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) and Start Transmit x (STRT_T_x) /Stop Transmit x (STP_T_x) bits.

3: One bit controls all RX and TX channels.

4: Software should not modify this field unless all RX DMA channels are in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

5: One bit controls all RX channels.

6: Software should not modify this field unless all TX DMA channels are in the Initial State as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

7: One field controls all TX channels.

TABLE 283: DMA CONTROLLER CONFIGURATION REGISTER (DMAC_CFG) SPECIFICATIONS

Bit	Description	Type	Default
9:7	**RESERVED**	RO	—
6:4	**Maximum Outstanding Data Read Requests (MAX_READ_REQ)** This field limits the number of maximum outstanding DMA read requests for TX data. Valid values are 1 to 6. (See **Note 6** and **Note 7**.)	R/W NASR (**Note 1**)	110b
3:2	**RESERVED**	RO	—
1:0	**Descriptor Spacing (DSPACE)** The size, in bytes, of the block reserved for each descriptor in memory is specified by this field. The descriptor itself will reside in the first 16 bytes of the reserved block. This field is programmed by the host to match the cache line size of the host CPU. 00 = 16 01 = 32 10 = 64 11 = 128 (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless all DMA channels are in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) and Start Transmit x (STRT_T_x) /Stop Transmit x (STP_T_x) bits.

3: One bit controls all RX and TX channels.

4: Software should not modify this field unless all RX DMA channels are in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

5: One bit controls all RX channels.

6: Software should not modify this field unless all TX DMA channels are in the Initial State as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

7: One field controls all TX channels.

10.0.2 DMA CONTROLLER COALESCING CONFIGURATION REGISTER (DMAC_COAL_CFG)

Offset: 0C04h
Size: 32 bits

This register establishes the coalescing operating parameters for the DMA Controller. See Table 284.

TABLE 284: DMA CONTROLLER COALESCING CONFIGURATION REGISTER (DMAC_COAL_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**DMA Coalescing Timer Limit (DMA_COAL_TIMER_LIMIT)** This field specifies the timeout when the DMAC will exit the coalescing state. This is specified in 100 µs increments. A value of 0 will disable exiting the coalescing state based on the timer. (See **Note 2**.)	R/W NASR (**Note 1**)	000h
19	**Start DMA Coalescing Timer on Available TX Buffer Transfer (DMA_COAL_TIMER_TX_START)** When this bit is set, the DMA Coalescing Timer is started when a new TX buffer transfer can be requested (there is a buffer available, the maximum number of outstanding requests is not reached and there is sufficient room in the device).	R/W NASR (**Note 1**)	0b
18	**Flush Interrupts upon DMA Coalescing Entrance (DMA_COAL_FLUSH_INTS)** When this bit is set, all pending moderated interrupts are flushed (sent) when the DMA enters the coalescing state.	R/W NASR (**Note 1**)	0b
17	**DMA Exit Coalescing on Interrupt (DMA_INT_EXIT_COAL)** When this bit is set, DMA coalescing is exited immediately on an interrupt.	R/W NASR (**Note 1**)	0b
16	**DMA Exit Coalescing on CSR (DMA_CSR_EXIT_COAL)** When this bit is set, DMA coalescing is exited on any device register access.	R/W NASR (**Note 1**)	0b
15:8	**DMA Coalescing TX Threshold (DMA_COAL_TX_THRES)** This field specifies the threshold of the total TX FCT free space when the DMAC will exit the coalescing state. This is specified in 1 kB increments. A value of 0 will disable exiting the coalescing state based on the TX space used. (See **Note 3**.)	R/W NASR (**Note 1**)	00h
7:0	**DMA Coalescing RX Threshold (DMA_COAL_RX_THRES)** This field specifies the threshold of the total RX FCT used space when the DMAC will exit the coalescing state. This is specified in 1 kB increments. A value of 0 will disable exiting the coalescing state based on the RX space used. (See **Note 4** and **Note 5**.)	R/W NASR (**Note 1**)	00h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The actual time can be low by up to 1 µs.

3: One field controls all TX channels.

4: This value should set be lower than the Flow Control On Threshold otherwise the network partner would be needlessly paused.

5: One field controls all RX channels.

10.0.3 DMA CONTROLLER OBFF CONFIGURATION REGISTER (DMAC_OBFF_CFG)

Offset: 0C08h
Size: 32 bits

This register establishes the Optimized Buffer Flush/Fill operating parameters for the DMA Controller. See Table 285.

TABLE 285: DMA CONTROLLER OBFF CONFIGURATION REGISTER (DMAC_OBFF_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:8	**DMA OBFF TX Threshold (DMA_OBFF_TX_THRES)** This field specifies the threshold of the total TX FCT free space when the DMAC will exit the coalescing state while in the OBFF or Active state. This is specified in 1 kB increments. A value of 0 will disable exiting the coalescing state based on the TX space used. (**Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00h
7:0	**DMA OBFF RX Threshold (DMA_OBFF_RX_THRES)** This field specifies the threshold of the total RX FCT used space when the DMAC will exit the coalescing state while in the OBFF or Active state. This is specified in 1 kB increments. A value of 0 will disable exiting the coalescing state based on the RX space used. (**Note 3**, **Note 4**, and **Note 5**.)	R/W NASR (**Note 1**)	00h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: This value should be lower than DMA Coalescing TX Threshold (DMA_COAL_TX_THRES) otherwise this value would be ineffective (since DMA_COAL_TX_THRES would trigger first).

3: One field controls all TX channels.

4: This value should set be lower than the Flow Control On Threshold otherwise the network partner would be needlessly paused.

5: This value should be lower than DMA Coalescing RX Threshold (DMA_COAL_RX_THRES) otherwise this value would be ineffective (since DMA_COAL_RX_THRES would trigger first).

6: One field controls all RX channels.

10.0.4 DMA CONTROLLER COMMAND REGISTER (DMAC_CMD)

Offset: 0C0Ch
Size: 32 bits

This register establishes the operating parameters for the DMA Controller. See Table 286.

TABLE 286: DMA CONTROLLER COMMAND REGISTER (DMAC_CMD) SPECIFICATIONS

Bit	Description	Type	Default
31	**DMA Software Reset (DMAC_SWR)** When this bit is set, the entire DMA Engine is reset. Register bits for the channel marked as NASR are not reset. Writing a 0 has no effect. This is a self-clearing bit. (**Note 1**)	R/W1S/SC	0b
30:29	**RESERVED**	RO	—
28	**DMA Coalescing Exit (DMA_COAL_EXIT)** Writing a one to this bit will force the DMA Controller to exit the coalescing state. (See **Note 2**.)	R/W1S/SC	0b
27:25	**RESERVED**	RO	—

Note 1: This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.

2: One bit controls all RX and TX channels.

3: Before the Start Transmit Command is initially issued a valid base address for the ring must be programmed into
TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*)
TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
TX Channel *x* Configuration A Register (TX_CFG_Ax) and
TX Channel *x* Configuration B Register (TX_CFG_Bx);
and if head pointer write-back is used,
TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*)
TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*)

4: Unless otherwise noted, software should not modify any DMA parameters that affect the Stopped channel, The channel should be set to the Initial State via a reset command before changing parameters.

5: Before the Start Receive Command is initially issued a valid base address for the ring must be programmed into
RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*)
RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
RX Channel *x* Configuration A Register (RX_CFG_A*x*) and
RX Channel *x* Configuration B Register (RX_CFG_B*x*);
and if head pointer write-back is used,
RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*)
RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*)
otherwise the RX DMAC's behavior will be undefined.

TABLE 286: DMA CONTROLLER COMMAND REGISTER (DMAC_CMD) SPECIFICATIONS

Bit	Description	Type	Default
24	**TX DMA Software Reset x (TX_SWR_x)** When this bit is set, the Transmit DMA Engine for channel x is reset, including pending and completed requests for the channel within the reorder buffer. Register bits for the channel marked as NASR are not reset. Writing a 0 has no effect. This is a self-clearing bit. This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.	R/W1S/SC	0b
23:21	**RESERVED**	RO	—
20	**Start Transmit x (STRT_T_x)** When this bit is written as a 1, the TX DMAC is either started (if in the Initial State) or resumes operation (if in the Stopped State). The Start Transmit command is effective only when the TX DMAC is not running (Initial or Stopped States). Writing this bit while in the Started or Stop Pending States has no effect. (See **Note 3**.) This bit will clear once Stop Transmit request is completed. The reading of this field along with the Stop Transmit x (STP_T_x) field indicates the current state of the TX DMAC channel. STRT_T_x / STP_T_x 00 – Initial 10 – Started 11 – Stop Pending 01 – Stopped	R/W1S	0b

Note 1: This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.

2: One bit controls all RX and TX channels.

3: Before the Start Transmit Command is initially issued a valid base address for the ring must be programmed into
TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*)
TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
TX Channel *x* Configuration A Register (TX_CFG_Ax) and
TX Channel *x* Configuration B Register (TX_CFG_Bx);
and if head pointer write-back is used,
TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*)
TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*)

4: Unless otherwise noted, software should not modify any DMA parameters that affect the Stopped channel, The channel should be set to the Initial State via a reset command before changing parameters.

5: Before the Start Receive Command is initially issued a valid base address for the ring must be programmed into
RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*)
RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
RX Channel *x* Configuration A Register (RX_CFG_A*x*) and
RX Channel *x* Configuration B Register (RX_CFG_B*x*);
and if head pointer write-back is used,
RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*)
RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*)
otherwise the RX DMAC's behavior will be undefined.

TABLE 286: DMA CONTROLLER COMMAND REGISTER (DMAC_CMD) SPECIFICATIONS

Bit	Description	Type	Default
19:17	**RESERVED**	RO	—
16	**Stop Transmit x (STP_T_x)** When this bit is written as a 1, the TX DMAC enters the Stopped state. The Stop Transmit command is effective only when the TX DMAC is in the Started State. Writing this bit while in the Initial, Stop Pending or Stopped States has no effect. (See **Note 4**.) This bit will clear once Start Transmit request is issued. The reading of this field along with the Start Transmit x (STRT_T_x) indicates the current state of the TX DMAC channel. STRT_T_x / STP_T_x 00 – Initial 10 – Started 11 – Stop Pending 01 – Stopped	R/W1S	0b
15:12	**RESERVED**	RO	—
11:8	**RX DMA Software Reset x (RX_SWR_x)** When this bit is set, the Receive DMA Engine for channel x is reset. Register bits for the channel marked as NASR are not reset. Writing a 0 has no effect. This is a self-clearing bit. This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.	R/W1S/SC	0000b

Note 1: This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.

2: One bit controls all RX and TX channels.

3: Before the Start Transmit Command is initially issued a valid base address for the ring must be programmed into
TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*)
TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
TX Channel *x* Configuration A Register (TX_CFG_Ax) and
TX Channel *x* Configuration B Register (TX_CFG_Bx);
and if head pointer write-back is used,
TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*)
TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*)

4: Unless otherwise noted, software should not modify any DMA parameters that affect the Stopped channel, The channel should be set to the Initial State via a reset command before changing parameters.

5: Before the Start Receive Command is initially issued a valid base address for the ring must be programmed into
RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*)
RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
RX Channel *x* Configuration A Register (RX_CFG_A*x*) and
RX Channel *x* Configuration B Register (RX_CFG_B*x*);
and if head pointer write-back is used,
RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*)
RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*)
otherwise the RX DMAC's behavior will be undefined.

TABLE 286: DMA CONTROLLER COMMAND REGISTER (DMAC_CMD) SPECIFICATIONS

Bit	Description	Type	Default
7:4	**Start Receive x (STRT_R_x)** When this bit is written as a 1, the RX DMAC is either started (if in the Initial state) or resumes operation (if in the Stopped State). The Start Receive command is effective only when the RX DMAC is not running (Initial or Stopped States). Writing this bit while in the Started or Stop Pending States has no effect. (See **Note 5**.) The reading of this field along with the Stop Receive x (STP_R_x) field indicates the current state of the RX DMAC channel. STRT_R_x/STP_R_x 00 – Initial 10 – Started 11 – Stop Pending 01 – Stopped	R/W1S	0000b

Note 1: This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.

2: One bit controls all RX and TX channels.

3: Before the Start Transmit Command is initially issued a valid base address for the ring must be programmed into
TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*)
TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
TX Channel *x* Configuration A Register (TX_CFG_Ax) and
TX Channel *x* Configuration B Register (TX_CFG_Bx);
and if head pointer write-back is used,
TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*)
TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*)

4: Unless otherwise noted, software should not modify any DMA parameters that affect the Stopped channel, The channel should be set to the Initial State via a reset command before changing parameters.

5: Before the Start Receive Command is initially issued a valid base address for the ring must be programmed into
RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*)
RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
RX Channel *x* Configuration A Register (RX_CFG_A*x*) and
RX Channel *x* Configuration B Register (RX_CFG_B*x*);
and if head pointer write-back is used,
RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*)
RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*)
otherwise the RX DMAC's behavior will be undefined.

TABLE 286: DMA CONTROLLER COMMAND REGISTER (DMAC_CMD) SPECIFICATIONS

Bit	Description	Type	Default
3:0	**Stop Receive x (STP_R_x)** When this bit is written as a 1, the RX DMAC enters the Stopped State. The Stop Receive command is effective only when the RX DMAC is in the Started State. Writing this bit while in the Initial, Stop Pending or Stopped States has no effect. (See **Note 4**.) This bit will clear once Start Receive request is issued. The reading of this field along with the Start Receive x (STRT_R_x) indicates the current state of the RX DMAC channel. STRT_R_x/STP_R_x 00 – Initial 10 – Started 11 – Stop Pending 01 – Stopped	R/W1S	0000b

Note 1: This is an immediate reset and will cause any, in process, PCIe request to aborted. This may likely result in a corrupt PCIe packet.

2: One bit controls all RX and TX channels.

3: Before the Start Transmit Command is initially issued a valid base address for the ring must be programmed into
TX Channel *x* Ring Base Address High Register (TX_BASE_ADDRH*x*)
TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
TX Channel *x* Configuration A Register (TX_CFG_Ax) and
TX Channel *x* Configuration B Register (TX_CFG_Bx);
and if head pointer write-back is used,
TX Channel *x* Head Write-back Address High Register (TX_HEAD_WRITEBACK_ADDRH*x*)
TX Channel *x* Head Write-back Address LOW Register (TX_HEAD_WRITEBACK_ADDRL*x*)

4: Unless otherwise noted, software should not modify any DMA parameters that affect the Stopped channel, The channel should be set to the Initial State via a reset command before changing parameters.

5: Before the Start Receive Command is initially issued a valid base address for the ring must be programmed into
RX Channel *x* Ring Base Address High Register (RX_BASE_ADDRH*x*)
RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*);
and the Ring Length and other parameters programmed into
RX Channel *x* Configuration A Register (RX_CFG_A*x*) and
RX Channel *x* Configuration B Register (RX_CFG_B*x*);
and if head pointer write-back is used,
RX Channel *x* Head Write-back Address High Register (RX_HEAD_WRITEBACK_ADDRH*x*)
RX Channel *x* Head Write-back Address LOW Register (RX_HEAD_WRITEBACK_ADDRL*x*)
otherwise the RX DMAC's behavior will be undefined.

10.0.5 DMA CONTROLLER INTERRUPT STATUS REGISTER (DMAC_INT_STS)

Offset: 0C10h
Size: 32 bits

This register contains the current status of the DMA interrupt sources. Unless otherwise noted, writing a '1' to the corresponding bits acknowledges and clears the interrupt. Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

This register contains the same information as the INT_STS_R2C Register.

The value in this register and the DMAC_INT_STS_R2C Register will always match. Bits that are cleared by writing this register will also be cleared in the DMAC_INT_STS_R2C Register. Bits that are cleared by reading the DMAC_INT_STS_R2C Register will also be cleared in this register.

If the host attempts to clear a R/W1C bit within the DMAC_INT_STS register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding DMAC_INT_STS bit will remain set. See Table 287.

TABLE 287: DMA CONTROLLER INTERRUPT STATUS REGISTER (DMAC_INT_STS) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**RX Priority Frame x Status (RXPRIx)** These separate status bits indicate that the current corresponding interrupts are due to a frame classified as a priority frame. Each bit is (possibly) set when the corresponding interrupt bit is set. A bit could remain unset upon an initial setting of the corresponding interrupt bit and be set if a subsequent priority frame occurs. The bits stay set even if a subsequent non-priority frame occurs. The bit is cleared when the corresponding interrupt bit is cleared. (See **Note 2**.)	RO NASR (**Note 1**)	0000b
23:22	**RESERVED**	RO	—
21	**DMA Error Interrupt (DMA_ERR_INT)** This interrupt is set when any status bit in the RX Channel *x* Error Status Register (RX_ERR_STSx) or TX Channel *x* Error Status Register (TX_ERR_STSx) is set. RX and TX Tail Pointer errors and TX Sequence errors are reported here only if they enabled. This bit cascades to the DMA_GEN_INT bit in the INT_STS register. (See **Note 3**.)	RO NASR (**Note 1**)	0b
20	**RESERVED**	RO	—
19:16	**RX Frame x Interrupt (RXFRMx_INT)** These separate interrupts are set when a frame is transferred to host memory. These bits cascade to the DMA_RXx_INT bits in the INT_STS register. (See **Note 4**.)	R/W1C NASR (**Note 1**)	0000b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A simultaneous setting, due to a new priority frame, and clearing will result in the bit (and corresponding interrupt bit) staying set.

3: This is a level-triggered interrupt event that remains asserted until all the error event bits in the RX Channel *x* Error Status Register (RX_ERR_STSx) and TX Channel *x* Error Status Register (TX_ERR_STSx) are cleared.

4: This is an edge-triggered interrupt event.

5: In silicon revision A0, this bit cascaded to DMA_RXx_INT.

TABLE 287: DMA CONTROLLER INTERRUPT STATUS REGISTER (DMAC_INT_STS) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:12	**RX DMA x Stopped Interrupt (RXx_STOP_INT)** This interrupt is set whenever RX DMA channel x enters into the Stopped state as a result of processing a Stop command. This bit cascades to the DMA_GEN_INT bit in the INT_STS register. (See **Note 4** and **Note 5**.)	R/W1C NASR (**Note 1**)	1111b
11:9	**RESERVED**	RO	—
8	**TX DMA x Stopped Interrupt (TXx_STOP_INT)** This interrupt is set whenever TX DMA channel x enters into the Stopped state as a result of processing a stop command. This bit cascades to the DMA_GEN_INT bit in the INT_STS register. (See **Note 4** and **Note 5**.)	R/W1C NASR (**Note 1**)	1b
7:1	**RESERVED**	RO	—
0	**TX x Interrupt (TXx_INT)** This interrupt is set whenever the TX DMA engine closes a transmit descriptor whose IOC or LS (or either) bit is set (as determined by the TX Timer and Head Pointer Write-back Select (TX_TMR_HPWB_SEL) field). The interrupt may be immediate or delayed. If the transmit descriptor also has the DTI bit set, this interrupt is set after a delay. This bit cascades to the DMA_TXx_INT bit in the INT_STS register. (See **Note 4**.)	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: A simultaneous setting, due to a new priority frame, and clearing will result in the bit (and corresponding interrupt bit) staying set.

3: This is a level-triggered interrupt event that remains asserted until all the error event bits in the RX Channel *x* Error Status Register (RX_ERR_STSx) and TX Channel *x* Error Status Register (TX_ERR_STSx) are cleared.

4: This is an edge-triggered interrupt event.

5: In silicon revision A0, this bit cascaded to DMA_RXx_INT.

10.0.6 DMA CONTROLLER INTERRUPT ENABLE SET REGISTER (DMAC_INT_EN_SET)

Offset: 0C14h
Size: 32 bit

This register is used to set the interrupt enables for the corresponding bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS). Writing a ‘1’ to a bit sets the corresponding enable and configures the corresponding interrupt as a source for the assertion of the DMA interrupt. Writing a ‘0’ has no effect. A read of this register returns the state of the interrupt enables. See Table 288.

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TABLE 288: DMA CONTROLLER INTERRUPT ENABLE SET REGISTER (DMAC_INT_EN_SET) SPECIFICATIONS

Bit	Description	Type	Default
31:22	**RESERVED**	RO	—
21	**DMA Error Interrupt Enable Set (DMA_ERR_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
20	**RESERVED**	RO	—
19:16	**RX Frame x Interrupt Enable Set (RXFRMx_INT_EN_SET)** (See **Note 2**.)	R/W1S NASR (**Note 1**)	0000b
15:12	**RX DMA x Stopped Interrupt Enable Set (RXx_STOP_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0000b
11:9	**RESERVED**	RO	—
8	**TX DMA 0 Stopped Interrupt Enable Set (TX0_STOP_INT_EN_SET)**	R/W1S NASR (**Note 1**)	0b
7:1	**RESERVED**	RO	—
0	**TX 0 Interrupt Enable Set (TX0_INT_EN_SET)** (See **Note 3**.)	R/W1S NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: These bits may also be set via each channel's RX Channel *x* Descriptor Tail Register (RX_*TAILx*).

3: This bit may also be set via the TX Channel *x* Descriptor Tail Register (TX_TAILx).

10.0.7 DMA CONTROLLER INTERRUPT ENABLE CLEAR REGISTER (DMAC_INT_EN_CLR)

Offset: 0C18h
Size: 32 bit

This register is used to clear the interrupt enables for the corresponding bits in the DMA Controller Interrupt Status Register (DMAC_INT_STS). Writing a '1' to a bit clears the corresponding enable. Writing a '0' has no effect. A read of this register returns the state of the interrupt enables. See Table 289.

Note:	There is no longer a "suspended" interrupt.

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TABLE 289: DMA CONTROLLER INTERRUPT ENABLE CLEAR REGISTER (DMAC_INT_EN_CLR) SPECIFICATIONS

Bit	Description	Type	Default
31:22	**RESERVED**	RO	—
21	**DMA Error Interrupt Enable Clear (DMA_ERR_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
20	**RESERVED**	RO	—
19:16	**RX Frame x Interrupt Enable Clear (RXFRMx_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0000b
15:12	**RX DMA x Stopped Interrupt Enable Clear (RXx_STOP_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0000b
11:9	**RESERVED**	RO	—
8	**TX DMA 0 Stopped Interrupt Enable Clear (TX0_STOP_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b
7:1	**RESERVED**	RO	—
0	**TX 0 Interrupt Enable Clear (TX0_INT_EN_CLR)**	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

10.0.8 RX ABSOLUTE TIMER CONFIGURATION REGISTER (RX_ABSTMR_CFG)

Offset: 0C1Ch
Size: 32 bit

This register configures the RX Absolute Timers. See Table 290.

TABLE 290: RX ABSOLUTE TIMER CONFIGURATION REGISTER (RX_ABSTMR_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RESERVED**	RO	—
23:20	**Absolute Timer Share Map (ABSTMR_SHARE_MAP)** These bits specify which DMA channel(s) are assigned to the shared absolute timer. A one in a bit position enables the corresponding channel into the shared absolute timer. A one also maps a shared absolute timer terminal count back to the corresponding channels cache flushing.	R/W NASR (**Note 1**)	0000b
19	**RX Absolute Timer Write Mask (ABSTMR_WR)** When this register is written, this bit enables the writing of the RX Absolute Timer selected by RX Absolute Timer Select (ABSTMR_SEL) field. A one enables the selected timer to be written.	WO	0b

TABLE 290: RX ABSOLUTE TIMER CONFIGURATION REGISTER (RX_ABSTMR_CFG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
18:16	**RX Absolute Timer Select (ABSTMR_SEL)** When this register is written, the value being written to this field (not the currently stored value) specifies which channel's timer is to be loaded with the value specified in RX Absolute Timer Count (ABSTMR_CNT). The stored value of this field selects which channel's timer is read back. 000 – channel 0 absolute timer 001 – channel 1 absolute timer 010 – channel 2 absolute timer 011 – channel 3 absolute timer 100 – shared absolute timer 101 – 111 – Reserved	R/W NASR (Note 1)	000b
15:0	**RX Absolute Timer Count (ABSTMR_CNT)** This field supports a time quantity. Each count represents 1 µs. A value of zero for a given timer disables that timer. There is a timer per channel, plus a timer shared amongst all channels. When this register is read, the read back value is the current value of the timer. The timer that is read or written is selected using the RX Absolute Timer Select (ABSTMR_SEL) field. (See Note 2.)	R/W	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The actual time can be low by up to 1 µs.

10.0.9 RX RELATIVE TIMER CONFIGURATION REGISTER (RXRELTMR_CFG)

Offset: 0C20h
Size: 32 bit

This register configures the operating mode of the RX Relative Timers. See Table 291.

TABLE 291: RX RELATIVE TIMER CONFIGURATION REGISTER (RXRELTMR_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:29	**Reserved**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The actual time can be low by up to 1 µs.

3: The upper bit of this field controls the shared relative timer/counter.

4: Software should not modify a bit for a given timer/counter while that timer/counter is running.

5: If RELTMR_CNT for a given timer/counter equals "0", that timer/counter is disabled.

TABLE 291: RX RELATIVE TIMER CONFIGURATION REGISTER (RXRELTMR_CFG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
28:24	**RX Relative Timer Operating Mode (RXRELTMR_MODE)** This field determines the operating mode of the RX Relative Timers. The semantic interpretation of the RELTMR_CNT field is determined by the contents of this field as follows: 0 = Timer is expired after the inactivity time specified by RELTMR_CNT has passed (time since last RX frame written into host memory). 1 = Counter is finished after the number of frames specified by RELTMR_CNT have been written into host memory. There is one mode bit per channel, plus a mode bit for the shared relative timer/counter. (See **Note 3**, **Note 4**, and **Note 5**.)	R/W NASR (**Note 1**)	0_0000b
23:20	**Relative Timer Share Map (RELTMR_SHARE_MAP)** These bits specify which DMA channel(s) are assigned to the shared relative timer. A “1” in a bit position enables the corresponding channel into the shared relative timer. A “1” also maps a shared relative timer terminal count back to the corresponding channels cache flushing.	R/W NASR (**Note 1**)	0000b
19	**RX Relative Timer Write Mask (RELTMR_WR)** When this register is written, this bit enables the writing of the RX Relative Timer selected by RX Relative Timer Select (RELTMR_SEL) field. A “1” enables the selected timer to be written.	WO	0b
18:16	**RX Relative Timer Select (RELTMR_SEL)** When this register is written, the value being written to this field (not the currently stored value) specifies which channel’s timer/counter is to be loaded with the value specified in RX Relative Timer Count (RELTMR_CNT). The stored value of this field selects which channel’s timer/counter is read back. 000 – channel 0 relative timer 001 – channel 1 relative timer 010 – channel 2 relative timer 011 – channel 3 relative timer 100 – shared relative timer 101 – 111 – Reserved	R/W NASR (**Note 1**)	000b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The actual time can be low by up to 1 µs.

3: The upper bit of this field controls the shared relative timer/counter.

4: Software should not modify a bit for a given timer/counter while that timer/counter is running.

5: If RELTMR_CNT for a given timer/counter equals “0”, that timer/counter is disabled.

TABLE 291: RX RELATIVE TIMER CONFIGURATION REGISTER (RXRELTMR_CFG) SPECIFICATIONS (CONTINUED)

Bit	Description	Type	Default
15:0	**RX Relative Timer Count (RELTMR_CNT)** The interpretation of this field depends on RX Relative Timer Operating mode (RXRELTMR_MODE). This field supports either a packet count or a time quantity. For time quantities, each count represents 1 µs. There is a timer/counter per channel, plus a timer/counter shared amongst all channels. When this register is read, the read back value is the current value of the timer/counter. The timer/counter that is read or written is selected using the RX Relative Timer Select (RELTMR_SEL) field. (See **Note 2**.)	R/W	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The actual time can be low by up to 1 µs.

3: The upper bit of this field controls the shared relative timer/counter.

4: Software should not modify a bit for a given timer/counter while that timer/counter is running.

5: If RELTMR_CNT for a given timer/counter equals “0”, that timer/counter is disabled.

10.0.10 TX DELAY TIMER CONFIGURATION REGISTER (TXTMR_CFG)

Offset: 0C24h
Size: 32 bit

This register configures the TX Delay Timer. See Table 292.

TABLE 292: TX DELAY TIMER CONFIGURATION REGISTER (TXTMR_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**RESERVED**	RO	—
19	**TX Delay Count Write Mask (TXDELAY_WR)** When this register is written, this bit enables the writing of the TX Delay Count. A “1” enables the count to be written.	WO	0b
18:16	**RESERVED**	RO	—
15:0	**TX Delay Count (TXDELAY_CNT)** This field supports a time quantity. Each count represents 1 µs. A value of zero disables the timer. When this register is read, the read back value is the current value of the timer. (See **Note 1**.)	R/W	0000h

Note 1: The actual time can be low by up to 1 µs.

10.0.11 TX ABSOLUTE TIMER CONFIGURATION REGISTER (TX_ABSTMR_CFG)

Offset: 0C28h
Size: 32 bit

This register configures the TX Absolute Timer. See Table 293.

TABLE 293: TX ABSOLUTE TIMER CONFIGURATION REGISTER (TX_ABSTMR_CFG) SPECIFICATIONS

Bit	Description	Type	Default
31:20	**RESERVED**	RO	—
19	**TX Absolute Timer Write Mask (TX_ABSTMR_WR)** When this register is written, this bit enables the writing of the TX Delay Count. A one enables the count to be written.	WO	0b
18:16	**RESERVED**	RO	—
15:0	**TX Absolute Timer Count (TX_ABSTMR_CNT)** This field supports a time quantity. Each count represents 1 µs. A value of zero disables the timer. When this register is read, the read back value is the current value of the timer. (See **Note 1**.)	R/W	0000h

Note 1: The actual time can be low by up to 1 µs.

10.0.12 DMA CONTROLLER INTERRUPT STATUS READ TO CLEAR REGISTER (DMAC_INT_STS_R2C)

Offset: 0C2Ch
Size: 32 bit
See Table 294.

This register contains the same information as the DMAC_INT_STS Register.

The value in this register and the DMAC_INT_STS Register will always match. Bits that are cleared by reading this register will also be cleared in the DMAC_INT_STS Register. Bits that are cleared by writing the DMAC_INT_STS Register will also be cleared in this register.

As with the DMAC_INT_STS Register, interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

Reading the interrupt status through this register may cause the indicated bits to be cleared.

For each DMA channel, based on the RX/TX_INT_STS_R2C_MODE bits in the RX Channel *x* Configuration C Register (RX_CFG_C*x*) or TX Channel *x* Configuration C Register (TX_CFG_C*x*), the Read to Clear may be enabled, disabled or gated by the interrupt enables in the DMAC_INT_EN_SET register.

If the host reads this register on the same clock cycle as a new interrupt condition (a pulse or a level event) corresponding to the same bit occurs, the bit will remain set. If a level event remains asserted, then the corresponding bit will remain set.

TABLE 294: DMA CONTROLLER INTERRUPT STATUS READ TO CLEAR REGISTER (DMAC_INT_STS_R2C) SPECIFICATIONS

Bit	Description	Type	Default
31:28	**RESERVED**	RO	—
27:24	**RX Priority Frame x Status (RXPRIx)** In addition to other clearing methods, these bits are cleared when the RXFRMx_INT bits are cleared by reading from this register.	RO NASR (**Note 1**) (**Note 2**)	0000b
23:22	**RESERVED**	RO	—
21	**DMA Error Interrupt (DMA_ERR_INT)** This bit is not cleared when this register is read.	RO NASR (**Note 1**)	0b
20	**RESERVED**	RO	—
19:16	**RX Frame x Interrupt (RXFRMx_INT)** In addition to other clearing methods, these bits are optionally cleared when this register is read.	RO/RC (**Note 2**) NASR (**Note 1**)	0000b
15:12	**RX DMA x Stopped Interrupt (RXx_STOP_INT)** These bits are not cleared when this register is read.	RO NASR	1111b
11:9	**RESERVED**	RO	—
8	**TX DMA x Stopped Interrupt (TXx_STOP_INT)** This bit is not cleared when this register is read.	RO NASR	1b
7:1	**RESERVED**	RO	—
0	**TX x Interrupt (TXx_INT)** In addition to other clearing methods, this bit is optionally cleared when this register is read.	RO/RC (**Note 2**) NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Bit type (RO vs. RC) depends on the RX/TX_INT_STS_R2C_MODE bits in the RX/TX_CFG_Cx register.

10.0.13 RX CHANNEL *X* CONFIGURATION A REGISTER (RX_CFG_A*X*)

Offset:

0C40h (ch 0)
0C80h (ch 1)
0CC0h (ch 2)
0D00h (ch 3)
Size: 32 bits

This register is used to configure RX DMA channel *x*. See Table 295.

TABLE 295: RX CHANNEL X CONFIGURATION A REGISTER (RX_CFG_AX) SPECIFICATIONS

Bit	Description	TYPE	DEFAULT
31	**RX Write-back Software Flush (RX_WB_SWFLUSH)** Writing a “1” causes an RX descriptor cache write-back flush cycle to occur. All used descriptors in the cache, at the time that this bit is set, are written back. The bit self clears after the write-back flush cycle and subsequent head pointer write back (if enabled) are performed. (See **Note 2**.)	W1S/SC	0b
30	**RX Write-back Software Flush (RX_WB_SWFLUSH)** Writing a “1” causes an RX descriptor cache write-back flush cycle to occur. All used descriptors in the cache, at the time that this bit is set, are written back. The bit self clears after the write-back flush cycle and subsequent head pointer write back (if enabled) are performed. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
29	**RESERVED**	RO	—
28:24	**RX Write-back Threshold (RX_WB_THRES)** Specifies the threshold when to write-back the RX descriptors. The write-back occurs when the number of cached descriptors to be written back exceeds this value. (See **Note 3** and **Note 4**.)	R/W NASR (**Note 1**)	00000b
23:21	**RESERVED**	RO	—
20:16	**RX Prefetch Threshold (RX_PF_THRES)** Specifies the threshold when the DMA controller will start prefetching receive descriptors. This value is compared to the number of cached descriptors on-chip. When the on-chip count is equal to or below RX_PF_THRESH descriptors will be prefetched. (See **Note 3**.)	R/W NASR (**Note 1**)	00000b
15:13	**RESERVED**	RO	—
12:8	**RX Prefetch Priority Threshold (RX_PF_PRI_THRES)** Specifies the threshold when the DMA controller descriptor prefetch is considered a high priority. (See **Note 3**.)	R/W NASR (**Note 1**)	00000b
7:6	**RESERVED**	RO	—
5	**RX Head Pointer Write-back Enable (RX_HP_WB_EN)** This bit enables the write-back of the RX Head pointer. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
4:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: If there are no used descriptors in the cache at the time that this bit is set, then a write-back flush cycle (and potential head pointer write back) is not performed and this bit immediately self-clears.

3: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x) / Stop Receive x (STP_R_x) bits.

4: A setting of zero will cause write-backs to happen immediately.

10.0.14 RX CHANNEL *X* CONFIGURATION B REGISTER (RX_CFG_B*X*)

Offset:

0C44h (ch 0)
0C84h (ch 1)
0CC4h (ch 2)
0D04h (ch 3)

Size: 32 bits

This register is used to configure RX DMA channel *x*. See Table 296.

TABLE 296: RX CHANNEL X CONFIGURATION B REGISTER (RX_CFG_BX) SPECIFICATIONS

Bit	Description	TYPE	DEFAULT
31:30	**RESERVED**	RO	—
29	**Time-Stamp all Receive (TS_ALL_RX)** (See **Note 2**.)	R/W NASR (**Note 1**)	0b
28	**Time-Stamp in Descriptor Enable (TS_DECR_EN)** (See **Note 3**.)	R/W NASR (**Note 1**)	0b
27:26	**RESERVED**	RO	—
25:24	**RX Data Pad (RX_PAD)** This field specifies the starting alignment of receive data in the first buffer. 00 = no padding 01 = reserved 10 = 2-byte pad 11 = reserved (See **Note 4**.)	R/W NASR (**Note 1**)	10b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Enables storing the receive time-stamp for all frames.

3: Enables storing the receive time-stamp in an extension descriptor.

4: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

5: This parameter as well as the Max_Payload_Size field in the PCIe Device Control Register determine the maximum burst size, with the lowest value prevailing.

6: The DMAC also terminates and starts a new transfer at the Max_Payload_Size and RX DMA Burst Length (RDMABL) address boundaries.

7: This parameter applies only to frame data writes and does not apply to descriptor write backs.

8: When the RX_TAILx and RX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of usable entries to RX_RING_LENx - 1 to prevent a full ring from being interpreted as an empty one.

TABLE 296: RX CHANNEL X CONFIGURATION B REGISTER (RX_CFG_BX) SPECIFICATIONS

Bit	Description	TYPE	DEFAULT
23	**RX DMAC Coalescing Disable (RX_COAL_DIS)** This bit disables DMA coalescing for RX channel x. 0 = DMA coalescing enabled if DMA Coalescing Enable (DMA_COAL_EN) is set. 1 = DMA coalescing is disabled for this channel. If the DMAC is in the coalescing state due to other channels, activity on this channel will cause an exit of the coalescing state. (See **Note 4**.)	R/W NASR (**Note 1**)	0b
22	**RESERVED**	RO	—
21	**RX Descriptor Read Reordering Enable (RX_DESCR_RO_EN)** This bit enables relaxed ordering rules for receive descriptor read. (See **Note 4**.)	R/W NASR (**Note 1**)	0b
20	**RX Data Write Reordering Enable (RX_DATA_RO_EN)** This bit enables relaxed ordering rules for receive data write. (See **Note 4**.)	R/W NASR (**Note 1**)	0b
19	**RESERVED**	RO	—
18:16	**RX DMA Burst Length (RDMABL)** Indicates the maximum number of bytes to be transferred in one RX DMA write transaction (maximum write size). (See **Note 5**, **Note 6**, and **Note 7**.) **Note:** 000 = 32 001 = 64 010 = 128 011 = 256 100 = 512 101 = 1024 (ineffective) 110 = 2048 (ineffective) 111 = 4096 (ineffective) (See **Note 4**.)	R/W NASR (**Note 1**)	100b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Enables storing the receive time-stamp for all frames.

3: Enables storing the receive time-stamp in an extension descriptor.

4: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

5: This parameter as well as the Max_Payload_Size field in the PCIe Device Control Register determine the maximum burst size, with the lowest value prevailing.

6: The DMAC also terminates and starts a new transfer at the Max_Payload_Size and RX DMA Burst Length (RDMABL) address boundaries.

7: This parameter applies only to frame data writes and does not apply to descriptor write backs.

8: When the RX_TAILx and RX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of usable entries to RX_RING_LENx - 1 to prevent a full ring from being interpreted as an empty one.

TABLE 296: RX CHANNEL X CONFIGURATION B REGISTER (RX_CFG_BX) SPECIFICATIONS

Bit	Description	TYPE	DEFAULT
15:0	**RX Descriptor Ring Length (RX_RING_LEN)** Specifies the number of Receive Descriptors constituting the ring. From 2 to 65535 descriptors are supported. (See **Note 7** and **Note 4**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Enables storing the receive time-stamp for all frames.

3: Enables storing the receive time-stamp in an extension descriptor.

4: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

5: This parameter as well as the Max_Payload_Size field in the PCIe Device Control Register determine the maximum burst size, with the lowest value prevailing.

6: The DMAC also terminates and starts a new transfer at the Max_Payload_Size and RX DMA Burst Length (RDMABL) address boundaries.

7: This parameter applies only to frame data writes and does not apply to descriptor write backs.

8: When the RX_TAILx and RX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of usable entries to RX_RING_LENx - 1 to prevent a full ring from being interpreted as an empty one.

10.0.15 RX CHANNEL *X* RING BASE ADDRESS HIGH REGISTER (RX_BASE_ADDRH*X*)

Offset:

0C48h (ch 0)
0C88h (ch 1)
0CC8h (ch 2)
0D08h (ch 3)

Size: 32 bits

This register specifies the high order 32 bits of the 64-bit starting address of receive channel *x*'s descriptor ring. See Table 297.

TABLE 297: RX CHANNEL X RING BASE ADDRESS HIGH REGISTER (RX_BASE_ADDRHX) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Channel Descriptor Ring Address[63:32]** This field is the high order 32-bits of the 64-bit starting address of receive channel *X's* descriptor ring. The descriptor ring resides in the system memory. (See **Note 2**.)	R/W NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x) / Stop Receive x (STP_R_x) bits.

10.0.16 RX CHANNEL *X* RING BASE ADDRESS LOW REGISTER (RX_BASE_ADDRL*X*)

Offset:

0C4Ch (ch 0)
0C8Ch (ch 1)
0CCCh (ch 2)
0D0Ch (ch 3)

Size: 32 bits

This register specifies the low order 32 bits of the 64-bit starting address of receive channel *x*'s descriptor ring. (See Table 298.)

The base address of the descriptor ring must be DWORD (4 byte) aligned (e.g. RX_BASE_ADDRLx[1:0] must be 0).

The H/W will not handle a 4 kB boundary crossing when accessing within a descriptor, therefore S/W must set the alignment on a Descriptor Spacing (DSPACE) boundary (i.e. the base must be DSPACE aligned).

Note:	An RX Extension Descriptor is considered a separate descriptor and may be in the next 4 kB boundary from its base descriptor.

Writing this register causes the RX Channel *x* Descriptor Head Register (RX_HEAD*x*) and RX Channel *x* Descriptor Tail Register (RX_*TAILx*) to be set to their default values.

TABLE 298: RX CHANNEL X RING BASE ADDRESS LOW REGISTER (RX_BASE_ADDRLX) SPECIFICATIONS

Bit	Description	Type	Default
31:2	**RX Channel Descriptor Ring Address[31:2]** This field is bits 31:2 of the 64-bit starting address of receive channel *x*'s descriptor ring. The descriptor ring resides in the system memory. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00000000h
1:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Internally, bits 1:0 are fixed at "0", in order to preserve DWORD alignment.

3: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

10.0.17 RX CHANNEL *X* HEAD WRITE-BACK ADDRESS HIGH REGISTER (RX_HEAD_WRITEBACK_ADDRH*X*)

Offset:
0C50h (ch 0)
0C90h (ch 1)
0CD0h (ch 2)
0D10h (ch 3)
Size: 32 bits

This register specifies the high order 32 bits of the 64-bit address of receive channel *x*'s Head pointer write-back location. See Table 299.

TABLE 299: RX CHANNEL *X* HEAD WRITE-BACK ADDRESS HIGH REGISTER (RX_HEAD_WRITEBACK_ADDRH*X*) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**RX Channel Write-back Address[63:32]** This field is the high order 32 bits of the 64-bit starting address of receive channel *x*'s write-back location. (See **Note 2**.)	R/W NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resetss

2: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Receive x (STRT_R_x)/Stop Receive x (STP_R_x) bits.

10.0.18 RX CHANNEL *X* HEAD WRITE-BACK ADDRESS LOW REGISTER (RX_HEAD_WRITEBACK_ADDRL*X*)

Offset:
0C54h (ch 0)
0C94h (ch 1)
0CD4h (ch 2)
0D14h (ch 3)
Size: 32 bits

This register specifies the low order 32 bits of the 64-bit starting address of receive channel *x*'s write-back location. The address must be DWORD (4 byte) aligned (e.g. RX_HEAD_WRITEBACK_ADDRLx[1:0] must be 0). See Table 300.

Note:	Although the RX Head pointer is 16 bits wide, all 32 bits of the Write-back location are written.

TABLE 300: RX CHANNEL X HEAD WRITE-BACK ADDRESS LOW REGISTER (RX_HEAD_WRITEBACK_ADDRLX) SPECIFICATIONS

Bit	Description	Type	Default
31:2	**RX Channel Write-back Address [31:2]** This field is the low order 32 bits of the 64-bit starting address of receive channel *x*'s write-back location. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00000000h
1:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Internally, bits 1:0 are fixed at 0, in order to preserve DWORD alignment.

3: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Receive x (STRT_R_x) / Stop Receive x (STP_R_x) bits.

10.0.19 RX CHANNEL *X* DESCRIPTOR HEAD REGISTER (RX_HEAD*X*)

Offset:
0C58h (ch 0)
0C98h (ch 1)
0CD8h (ch 2)
0D18h (ch 3)
Size: 32 bits

This register contains the head pointer into receive channel x's descriptor ring. The pointer is a zero-based index and not a memory address or offset. See Table 301.

Hardware owns all descriptors between head and tail—1. Any descriptor not in this range is owned by software. H/W maintains this pointer and increments it as buffers are filled and descriptors are written back.

Note 1: Due to PCIe I/O write buffering, this register may not reflect the current state of descriptors in the host's main memory. Therefore the host should not rely on this register to determine which descriptors to release. It should make use of the head pointer write-back mechanism instead.

2: This register is reset to the default value whenever the RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) is written.

TABLE 301: RX CHANNEL X DESCRIPTOR HEAD REGISTER (RX_HEADX) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**Current Receive Descriptor Head (RX_HEAD)**	RO	0000h

10.0.20 RX CHANNEL *X* DESCRIPTOR TAIL REGISTER (RX_TAIL*X*)

Offset:
0C5Ch (ch 0)
0C9Ch (ch 1)
0CDCh (ch 2)
0D1Ch (ch 3)
Size: 32 bits

This register contains the tail pointer into receive channel x's descriptor ring. The pointer is a zero based index and not a memory address or offset. See Table 302.

Hardware owns all descriptors between head and tail—1. The tail pointer points to one entry beyond the last hardware owned descriptor. Any descriptor not in this range is owned by software. S/W maintains this pointer and writes it to add free buffers to the end of the ring.

Note 1: When the RX_TAILx and RX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of used entries to RX_RING_LENx—1.

2: Once descriptors have been handed to hardware, the software must not attempt to take any of them back by reducing this value. The only way to stop processing descriptors that have already been transferred to hardware is for the software to stop and then reset the channel.

3: This register is reset to the default value whenever the RX Channel *x* Ring Base Address Low Register (RX_BASE_ADDRL*x*) is written.

TABLE 302: RX CHANNEL X DESCRIPTOR TAIL REGISTER (RX_TAILX)SPECIFICATIONS

Bit	Description	Type	Default
31	**Set DMAC Interrupt Enable (SET_DMAC_INT_EN)** When this field is written with a “1”, the channel’s RX Frame Interrupt Enable bit in the DMA Controller Interrupt Enable Set Register (DMAC_INT_EN_SET) is set. Writing a 0 has no effect.	WO	0b
30	**Set Top Level Interrupt Enable (SET_TOP_INT_EN)** When this field is written with a “1”, the DMA RX Channel x Interrupt Enable bit in the Interrupt Enable Set Register (INT_EN_SET) is set. Writing a 0 has no effect.	WO	0b
29	**Set Top Level Interrupt Vector Enable (SET_TOP_INT_VEC_EN)** When this field is written with a “1”, the Interrupt Vector Enable bit in the Interrupt Vector Enable Set Register (INT_VEC_EN_SET), for the vector that is mapped to this channel, is set. Writing a “0” has no effect. (See **Note 2**.)	WO	0b
28:16	**RESERVED**	RO	—
15:0	**Current Receive Descriptor Tail (RX_TAIL)** (See **Note 3**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The vector mapping is specified in the Interrupt Vector Mapping Table Registers (INT_VEC_MAPX).

3: The separate bytes in this field should not be written individually (by using BYTE enables within a DWORD write). Otherwise a incorrect intermediate value may be inferred).

10.0.21 RX CHANNEL *X* ERROR STATUS REGISTER (RX_ERR_STS*X*)

Offset:
0C60h (ch 0)
0CA0h (ch 1)
0CE0h (ch 2)
0D20h (ch 3)
Size: 32 bits

This register contains error status and information for the receive channel.

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 304.

TABLE 303: RX CHANNEL X ERROR STATUS REGISTER (RX_ERR_STSX) SPECIFICATIONS

Bit	Description	Type	Default
31:22	**RESERVED**	RO	—
21	**Enable RX Descriptor Tail Error (RX_DESC_TAIL_ERR_EN)** This bit controls if the DMAC attempts to continue operation after detecting a Tail Pointer was set out of the bounds of the ring. 0 = report error and attempt to continue operation 1 = report error and halt	R/W NASR (**Note 1**)	0b
20:7	**RESERVED**	RO	—
6	**RX Descriptor Read Retry Error (RX_DESC_READ_ERR)** This bit is set if the H/W a PCIe read error while fetching descriptors and all retries have been used. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register.	R/W1C NASR (**Note 1**)	0b
5	**RX Descriptor Tail Error (RX_DESC_TAIL_ERR)** This bit is set if the H/W encounters that the Tail Pointer was set out of the bounds of the ring. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above RX_DESC_TAIL_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b
4:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

10.0.22 RX CHANNEL *X* CONFIGURATION C REGISTER (RX_CFG_C*X*)

Offset:
0C64h (ch 0)
0CA4h (ch 1)
0CE4h (ch 2)
0D24h (ch 3)
Size: 32 bits

This register is used to configure RX DMA channel *x*. See Table 304.

TABLE 304: RX CHANNEL X CONFIGURATION C REGISTER (RX_CFG_CX) SPECIFICATIONS

Bit	Description	Type	Default
31:7	**RESERVED**	RO	—
6	**RX Top Level Interrupt Enable Auto Clear (RX_TOP_INT_EN_AUTO_CLR)** When set to a '1' the channel's Interrupt Enable (in INT_EN_SET) is cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
5	**RX DMA Interrupt Enable Auto Clear (RX_DMA_INT_EN_AUTO_CLR)** When set to a '1' the channel's Interrupt Enable (in DMAC_INT_EN_SET) is cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
4	**RX Interrupt Enable Read to Clear (RX_INT_EN_R2C)** When set to a '1': The channel's interrupt enable (in INT_EN_SET) is cleared when the INT_STS_R2C register is read if the channel's status (in INT_STS_R2C) was set at the time. The channel's interrupt enable (in DMAC_INT_EN_SET) is cleared when the DMAC_INT_STS_R2C register is read if the channel's status (in DMAC_INT_STS_R2C) was set at the time.	R/W NASR (**Note 1**)	0b
3	**RX DMA Interrupt Status Auto Clear (RX_DMA_INT_STS_AUTO_CLR)** When set to a '1' the channel's RX Frame x Interrupt (RXFRMx_INT) status and RX Priority Frame x Status (RXPRIx) bits are cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The vector mapping is specified in the Interrupt Vector Mapping Table Registers (INT_VEC_MAPX).

TABLE 304: RX CHANNEL X CONFIGURATION C REGISTER (RX_CFG_CX) SPECIFICATIONS

Bit	Description	Type	Default
2:0	**RX Interrupt Status Read to Clear Mode (RX_INT_STS_R2C_MODE)** These bits determine the operation, for this channel, when the Interrupt Status Read to Clear Register (INT_STS_R2C) or DMA Controller Interrupt Status Read to Clear Register (DMAC_INT_STS_R2C) is read. Read of DMAC_INT_STS_R2C: 000 = Interrupt status does not clear on a read 1x0 = Interrupt status clears on a read 1x1 = Interrupt status clears on a read only if the channel's interrupt enable in DMAC_INT_EN_SET is set Read of INT_STS_R2C: 000 = Interrupt status does not clear on a read 100 = Interrupt status clears on a read 101 = Interrupt status clears on a read only if the channel's interrupt enable in DMAC_INT_EN_SET is set 110 = Interrupt status clears on a read only if the channel's interrupt enable in INT_EN_SET is set 111 = Interrupt status clears on a read only if the channel's interrupt enables in both DMAC_INT_EN_SET and INT_EN_SET are set	R/W NASR (Note 1)	000b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The vector mapping is specified in the Interrupt Vector Mapping Table Registers (INT_VEC_MAPX).

10.0.23 TX CHANNEL *X* CONFIGURATION A REGISTER (TX_CFG_A*X*)

Offset:
0D40h (ch 0)
0D80h (ch 1)
0DC0h (ch 2)
0E00h (ch 3)
Size: 32 bits

This register is used to configure TX DMA channel *x*. See Table 305.

TABLE 305: TX CHANNEL *X* CONFIGURATION A REGISTER (TX_CFG_A*X*) SPECIFICATIONS

Bit	Description	Type	Default
31	**TX Head Pointer Write-back Software Flush (TX_HP_WB_SWFLUSH)** Writing a "1" causes a TX head pointer write-back flush cycle to occur. The bit self clears after the head pointer write-back is performed. (See **Note 2**.)	W1S/SC	0b
30	**TX Head Pointer Write-back on Interrupt Moderation Expiration (TX_HP_WB_ON_INT_TMR)** This bit enables the write-back of the TX head pointer when the interrupt moderation timer assigned to the channel is expired. If there is no moderation timer assigned to the channel, then this function is disabled regardless of the setting of this bit. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
29:28	**TX Timer and Head Pointer Write-back Select (TX_TMR_HPWB_SEL)** This field determines if TX Head Pointer Write-backs, TX timers and TX interrupts are triggered based on the IOC or LS bit in the TX descriptor. 00 – trigger disabled 01 – trigger on descriptors that have the IOC bit set 10 – trigger on descriptors that have the LS bit set 11 – trigger on descriptors that have either the IOC or LS bit set (See **Note 4** and **Note 3**.)	R/W NASR (**Note 1**)	00b
27:21	**RESERVED**	RO	—
20:16	**TX Prefetch Threshold (TX_PF_THRES)** This specifies the threshold when the DMA controller will start prefetching transmit descriptors. This value is compared to the number of cached descriptors on-chip. When the on-chip count is equal to or below TX_PF_THRESH, descriptors will be prefetched.	R/W NASR (**Note 1**)	00000b
15:13	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: If there are no coalesced head pointer write-backs at the time that this bit is set, then a write-back is not performed and this bit immediately self-clears.

3: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

4: A setting of 00b effectively disables the generation of TX Head Pointer write-backs and the triggering of the TX timers and TX interrupts.

5: A setting of zero will cause write-backs to happen immediately.

6: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

7: Only descriptors which have their IOC or LS bit set (as determined by the TX Timer and Head Pointer Write-back Select (TX_TMR_HPWB_SEL) field) are counted towards this threshold.

TABLE 305: TX CHANNEL *X* CONFIGURATION A REGISTER (TX_CFG_A*X*) SPECIFICATIONS

Bit	Description	Type	Default
12:8	**TX Prefetch Priority Threshold (TX_PF_PRI_THRES)** Specifies the threshold when the DMA controller descriptor prefetch is considered a high priority. (See **Note 3**.)	R/W NASR (**Note 1**)	00000b
7	**TX Stop on Transmit Error (TX_STOP_TXE)** This bit controls the operation of the DMA when the TX FCT detects the loss of sync condition. 0 – Stop the DMA when loss of sync is detected. 1 – Do not stop the DMA when loss of sync is detected. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
6	**RESERVED**	RO	—
5	**TX Head Pointer Write-back Enable (TX_HP_WB_EN)** This bit enables the write-back of the TX Head pointer (as determined by the TX Timer and Head Pointer Write-back Select (TX_TMR_HPWB_SEL) field). (See **Note 3**.)	R/W NASR (**Note 1**)	0b
4	**TX Head Pointer Write-back on TX Delay Timer (TX_HP_WB_ON_TXTMR)** This bit enables the write-back of the TX Head pointer when the TX Delay Timer expires. (See **Note 3**.)	R/W NASR (**Note 1**)	0b
3:0	**TX Head Pointer Write-back Threshold (TX_HP_WB_THRES)** Specifies the threshold when to write-back the TX Head pointer. The write-back occurs when the number of pending write back requests exceeds this value. (See **Note 5**, **Note 6** and **Note 7**.)	R/W NASR (**Note 1**)	0000b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: If there are no coalesced head pointer write-backs at the time that this bit is set, then a write-back is not performed and this bit immediately self-clears.

3: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

4: A setting of 00b effectively disables the generation of TX Head Pointer write-backs and the triggering of the TX timers and TX interrupts.

5: A setting of zero will cause write-backs to happen immediately.

6: Software should not modify this field unless DMA for the channel is in the Initial state as indicated by the Start Transmit x (STRT_T_x)/Stop Transmit x (STP_T_x) bits.

7: Only descriptors which have their IOC or LS bit set (as determined by the TX Timer and Head Pointer Write-back Select (TX_TMR_HPWB_SEL) field) are counted towards this threshold.

10.0.24 TX CHANNEL *X* CONFIGURATION B REGISTER (TX_CFG_B*X*)

Offset:
0D44h (ch 0)
0D84h (ch 1)
0DC4h (ch 2)
0E04h (ch 3)
Size: 32 bits

This register is used to configure TX DMA Channel *x*. See Table 306.

TABLE 306: TX CHANNEL X CONFIGURATION B REGISTER (TX_CFG_BX) SPECIFICATIONS

Bit	Description	Type	Default
31:24	**RESERVED**	RO	—
23	**TX DMAC Coalescing Disable (TX_COAL_DIS)** This bit disables DMA coalescing for TX channel x. 0 = DMA Coalescing enabled if DMA Coalescing Enable (DMA_COAL_EN) is set. 1 = DMA Coalescing is disabled for this channel. If the DMAC is in the Coalescing state due to other channels, activity on this channel will cause an exit of the Coalescing state. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
22	**TX Descriptor Read Reordering Enable (TX_DESCR_RO_EN)** This bit enables relaxed ordering rules for transmit descriptor read. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
21	**TX Data Read Reordering Enable (TX_DATA_RO_EN)** This bit enables relaxed ordering rules for transmit data read. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
20	**TX Head Pointer Write Reordering Enable (TX_HEAD_RO_EN)** This bit enables relaxed ordering rules for transmit descriptor head pointer write-back. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
19	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

3: This parameter as well as the Max_Read_Request_Size field in the PCIe Device Control Register determine the maximum burst size, with the lowest value prevailing.

4: The DMAC also terminates and starts a new transfer at the Max_Read_Request_Size and TX DMA Burst Length (TDMABL) address boundaries.

5: This parameter applies only to frame data reads and does not apply to descriptor reads.

6: When the TX_TAILx and TX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of used entries to TX_RING_LENx - 1 to prevent a full ring from being interpreted as an empty one.

TABLE 306: TX CHANNEL X CONFIGURATION B REGISTER (TX_CFG_BX) SPECIFICATIONS

Bit	Description	Type	Default
18:16	**TX DMA Burst Length (TDMABL)** Indicates the maximum number of bytes requested to be transferred in one TX DMA read transaction (maximum read request size). (See **Note 3**, **Note 4**, and **Note 5**.) 000 = 32 001 = 64 010 = 128 011 = 256 100 = 512 101 = 1024 (ineffective) 110 = 2048 (ineffective) 111 = 4096 (ineffective) (See **Note 2**.)	R/W NASR (**Note 1**)	100b
15:0	**TX Descriptor Ring Length (TX_RING_LEN)** Specifies the number of Transmit Descriptors constituting the ring. From 2 to 65535 descriptors are supported. (See **Note 6** and **Note 2**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

3: This parameter as well as the Max_Read_Request_Size field in the PCIe Device Control Register determine the maximum burst size, with the lowest value prevailing.

4: The DMAC also terminates and starts a new transfer at the Max_Read_Request_Size and TX DMA Burst Length (TDMABL) address boundaries.

5: This parameter applies only to frame data reads and does not apply to descriptor reads.

6: When the TX_TAILx and TX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of used entries to TX_RING_LENx - 1 to prevent a full ring from being interpreted as an empty one.

10.0.25 TX CHANNEL *X* RING BASE ADDRESS HIGH REGISTER (TX_BASE_ADDRH*X*)

Offset:
0D48h (ch 0)
0D88h (ch 1)
0DC8h (ch 2)
0E08h (ch 3)
Size: 32 bits

This register specifies the high order 32-bits of the 64-bit starting address of transmit channel x's descriptor ring. See Table 307.

TABLE 307: X CHANNEL X RING BASE ADDRESS HIGH REGISTER (TX_BASE_ADDRHX) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Channel Descriptor Ring Address[63:32]** This field is the high order 32-bits of the 64-bit starting address of transmit channel *x*'s descriptor ring. (See **Note 2**.)	R/W NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

10.0.26 TX CHANNEL *X* RING BASE ADDRESS LOW REGISTER (TX_BASE_ADDRL*X*)

Offset:
0D4Ch (ch 0)
0D8Ch (ch 1)
0DCCh (ch 2)
0E0Ch (ch 3)
Size: 32 bits

This register specifies the low order 32-bits of the 64-bit starting address of transmit channel *x*'s descriptor ring.

The base address of the descriptor ring must be DWORD (4 byte) aligned (e.g. TX_BASE_ADDRLx[1:0] must be 0).

The H/W will not handle a 4 kB boundary crossing when accessing within a descriptor, therefore S/W must set the alignment on a Descriptor Spacing (DSPACE) boundary (i.e. the base must be DSPACE aligned). See Table 308.

Note: A TX Extension Descriptor is considered a separate descriptor and may be in the next 4 kB boundary from its base descriptor.

Writing this register causes the TX Channel *x* Descriptor Head Register (TX_HEAD*x*) and TX Channel *x* Descriptor Tail Register (TX_TAILx) to be set to their default values.

TABLE 308: TX CHANNEL X RING BASE ADDRESS LOW REGISTER (TX_BASE_ADDRLX) SPECIFICATIONS

Bit	Description	Type	Default
31:2	**TX Channel Descriptor Ring Address[31:2]** This field is bits 31:2 of the 64-bit starting address of transmit channel *x*'s descriptor ring. The descriptor ring resides in the system memory. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00000000h
1:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Internally, bits 1:0 are fixed at 0, in order to preserve DWORD alignment.

3: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

10.0.27 TX CHANNEL *X* HEAD WRITE-BACK ADDRESS HIGH REGISTER (TX_HEAD_WRITEBACK_ADDRH*X*)

Offset:
0D50h (ch 0)
0D90h (ch 1)
0DD0h (ch 2)
0E10h (ch 3)
Size: 32 bits

This register specifies the high order 32 bits of the 64-bit address of transmit channel *x*'s Head pointer write-back location. See Table 309.

TABLE 309: TX CHANNEL X HEAD WRITE-BACK ADDRESS HIGH REGISTER (TX_HEAD_WRITEBACK_ADDRHX) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**TX Channel Write-back Address[63:32]** This field is the high order 32-bits of the 64-bit starting address of transmit channel *x*'s write-back location. (See **Note 2**.)	R/W NASR (**Note 1**)	00000000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

10.0.28 TX CHANNEL *X* HEAD WRITE-BACK ADDRESS LOW REGISTER (TX_HEAD_WRITEBACK_ADDRL*X*)

Offset:
0D54h (ch 0)
0D94h (ch 1)
0DD4h (ch 2)
0E14h (ch 3)
Size: 32 bits

This register specifies the low order 32 bits of the 64-bit starting address of transmit channel *x*'s write-back location. The address must be DWORD (4 byte) aligned (e.g. TX_HEAD_WRITEBACK_ADDRLx[1:0] must be 0). See Table 310.

Note:	Although the TX Head pointer is 16 bits wide, all 32 bits of the Write-back location are written.

TABLE 310: TX CHANNEL X HEAD WRITE-BACK ADDRESS LOW REGISTER (TX_HEAD_WRITEBACK_ADDRLX) SPECIFICATIONS

Bit	Description	Type	Default
31:2	**TX Channel Write-back Address[31:2]** This field is the low order 32 bits of the 64-bit starting address of transmit channel *x*'s write-back location. (See **Note 2** and **Note 3**.)	R/W NASR (**Note 1**)	00000000h
1:0	**RESERVED**	RO	—

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: Internally, bits 1:0 are fixed at 0, in order to preserve DWORD alignment.

3: Software should not modify this field unless DMA for the channel is in the Initial State as indicated by the Start Transmit x (STRT_T_x) / Stop Transmit x (STP_T_x) bits.

10.0.29 TX CHANNEL *X* DESCRIPTOR HEAD REGISTER (TX_HEAD*X*)

Offset:
0D58h (ch 0)
0D98h (ch 1)
0DD8h (ch 2)
0E18h (ch 3)
Size: 32 bits

This register contains the head pointer into transmit channel x's descriptor ring. The pointer is a zero-based index and not a memory address or offset.

Hardware owns all descriptors between head and tail—1. Any descriptor not in this range is owned by software. H/W maintains this pointer and increments it as buffers are read and released. See Table 311.

Note 1: Since TX descriptors are not written back to host memory, this register may be used to determine which descriptors to release. Alternately, the value of this register maybe written back into host memory using TX_HEAD_WRITEBACK_ADDRH/Lx.

2: This register is reset to the default value whenever the TX Channel x Ring Base Address Low Register (TX_BASE_ADDRLx) is written.

TABLE 311: TX CHANNEL X DESCRIPTOR HEAD REGISTER (TX_HEADX) SPECIFICATIONS

Bit	Description	Type	Default
31:16	**RESERVED**	RO	—
15:0	**Current Transmit Descriptor Head (TX_HEAD)**	RO	0000h

10.0.30 TX CHANNEL *X* DESCRIPTOR TAIL REGISTER (TX_TAIL*X*)

Offset:
0D5Ch (ch 0)
0D9Ch (ch 1)
0DDCh (ch 2)
0E1Ch (ch 3)
Size: 32 bits

This register contains the tail pointer into transmit channel x's descriptor ring. The pointer is a zero-based index and not a memory address or offset.

Hardware owns all descriptors between head and tail—1. The tail pointer points to one entry beyond the last hardware owned descriptor. Any descriptor not in this range is owned by software. S/W maintains this pointer and writes it to add filled buffers to the end of the ring. See Table 312.

Note 1: When the TX_TAILx and TX_HEADx pointers are equal, the ring is considered to be empty. S/W must limit the number of used entries to TX_RING_LENx - 1.

2: Once descriptors have been handed to hardware, the software must not attempt to take any of them back by reducing this value. The only way to stop processing descriptors that have already been transferred to hardware is for the software to stop and then reset the channel.

3: This register is reset to the default value whenever the TX Channel *x* Ring Base Address Low Register (TX_BASE_ADDRL*x*) is written.

TABLE 312: TX CHANNEL X DESCRIPTOR TAIL REGISTER (TX_TAIL*X*) SPECIFICATIONS

Bit	Description	Type	Default
31	**Set DMAC Interrupt Enable (SET_DMAC_INT_EN)** When this field is written with a "1", the TX Interrupt Enable bit in the DMA Controller Interrupt Enable Set Register (DMAC_INT_EN_SET) is set. Writing a "0" has no effect.	WO	0b
30	**Set Top Level Interrupt Enable (SET_TOP_INT_EN)** When this field is written with a "1", the DMA TX Channel x Interrupt Enable bit in the Interrupt Enable Set Register (INT_EN_SET) is set. Writing a "0" has no effect.	WO	0b
29	**Set Top Level Interrupt Vector Enable (SET_TOP_INT_VEC_EN)** When this field is written with a "1", the Interrupt Vector Enable bit in the Interrupt Vector Enable Set Register (INT_VEC_EN_SET) for the vector that is mapped to this channel is set. Writing a 0 has no effect. (See **Note 2**.)	WO	0b
28:16	**RESERVED**	RO	—
15:0	**Current Transmit Descriptor Tail (TX_TAIL)** (See **Note 3**.)	R/W NASR (**Note 1**)	0000h

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The vector mapping is specified in the Interrupt Vector Mapping Table Registers (INT_VEC_MAPX).

3: The separate bytes in this field should not be written individually (by using BYTE enables within a DWORD write). Otherwise, a incorrect intermediate value may be inferred).

10.0.31 TX CHANNEL *X* ERROR STATUS REGISTER (TX_ERR_STS*X*)

Offset:
0D60h (ch 0)
0DA0h (ch 1)
0DE0h (ch 2)
0E20h (ch 3)
Size: 32 bits

This register contains error status and information for the transmit channel.

If the host attempts to clear a R/W1C bit within this register on the same clock cycle as a new event occurs, the bit will remain set. See Table 313.

TABLE 313: TX CHANNEL *X* ERROR STATUS REGISTER (TX_ERR_STS*X*) SPECIFICATIONS

Bit	Description	Type	Default
31:22	**RESERVED**	RO	—
21	**Enable TX Descriptor Tail Error (TX_DESC_TAIL_ERR_EN)** This bit controls if the DMAC attempts to continue operation after detecting a Tail Pointer was set out of the bounds of the ring. 0 = report error and attempt to continue operation 1 = report error and halt	R/W NASR (**Note 1**)	0b
20:17	**RESERVED**	RO	—
16	**Enable TX Descriptor Sequence Error (TX_DESC_SEQ_ERR_EN)** This bit controls if the DMAC continues operation when detecting a Descriptor Sequence Error. 0 = report error(s) and attempt to continue operation 1 = report error(s) and halt	R/W NASR (**Note 1**)	0b
15:8	**RESERVED**	RO	—
7	**TX Data Buffer Read Retry Error (TX_DATA_READ_ERR)** This bit is set if the H/W a PCIe read error while reading a data buffer and all retries have been used. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register.	R/W1C NASR (**Note 1**)	0b
6	**TX Descriptor Read Retry Error (TX_DESC_READ_ERR)** This bit is set if the H/W a PCIe read error while fetching descriptors and all retries have been used. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register.	R/W1C NASR (**Note 1**)	0b
5	**TX Descriptor Tail Error (TX_DESC_TAIL_ERR)** This bit is set if the H/W encounters that the Tail Pointer was set out of the bounds of the ring. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above TX_DESC_TAIL_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

TABLE 313: TX CHANNEL *X* ERROR STATUS REGISTER (TX_ERR_STS*X*) SPECIFICATIONS

Bit	Description	Type	Default
4	**FCT TX Error (FCT_TXE)** This bit is set if the FCT basic sanity checks failed. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register.	R/W1C NASR (**Note 1**)	0b
3	**TX Data Descriptor Missing Sequence Error (TX_DESC_DATATYPE_ERR)** This bit is set if the H/W expected a Data Descriptor but did not receive such. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above TX_DESC_SEQ_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b
2	**TX Extension Descriptor Missing Sequence Error (TX_DESC_EXTNTYPE_ERR)** This bit is set if the H/W expected an Extension Descriptor but did not receive such. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above TX_DESC_SEQ_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b
1	**TX Descriptor Extraneous FS Sequence Error (TX_DESC_EXTRAFS_ERR)** This bit is set if the H/W encounters a Data Descriptor with the FS bit set but expected the FS bit to be cleared. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above TX_DESC_SEQ_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b
0	**TX Descriptor Missing FS Sequence Error (TX_DESC_NOFS_ERR)** This bit is set if the H/W encounters a Data Descriptor with the FS bit cleared but expected the FS bit to be set. This bit cascades to the DMA Error Interrupt (DMA_ERR_INT) bit in the DMAC_INT_STS register only if the above TX_DESC_SEQ_ERR_EN bit is set.	R/W1C NASR (**Note 1**)	0b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

10.0.32 TX CHANNEL *X* CONFIGURATION C REGISTER (TX_CFG_C*X*)

Offset:
0D64h
0DA4h
0DE4h
0E24h
Size: 32 bits

This register is used to configure TX DMA channel *x*. See Table 314.

TABLE 314: TX CHANNEL X CONFIGURATION C REGISTER (TX_CFG_CX) SPECIFICATIONS

Bit	Description	TYPE	DEFAULT
31:7	**RESERVED**	RO	—
6	**TX Top Level Interrupt Enable Auto Clear (TX_TOP_INT_EN_AUTO_CLR)** When set to a '1', the channel's Interrupt Enable (in INT_EN_SET) is cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
5	**TX DMA Interrupt Enable Auto Clear (TX_DMA_INT_EN_AUTO_CLR)** When set to a '1', the channel's Interrupt Enable (in DMAC_INT_EN_SET) is cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
4	**TX Interrupt Enable Read to Clear (TX_INT_EN_R2C)** When set to a '1', the channel's interrupt enable (in INT_EN_SET) is cleared when the INT_STS_R2C register is read if the channel's status (in INT_STS_R2C) was set at the time. The channel's interrupt enable (in DMAC_INT_EN_SET) is cleared when the DMAC_INT_STS_R2C register is read if the channel's status (in DMAC_INT_STS_R2C) was set at the time.	R/W NASR (**Note 1**)	0b
3	**TX DMA Interrupt Status Auto Clear (TX_DMA_INT_STS_AUTO_CLR)** When set to a '1,' the channel's TX x Interrupt (TXx_INT) status bit is cleared when an MSI/MSI-X message is sent for the interrupt vector assigned to the channel. (See **Note 2**.)	R/W NASR (**Note 1**)	0b
2:0	**TX Interrupt Status Read to Clear Mode (TX_INT_STS_R2C_MODE)** These bits determine the operation, for this channel, when the Interrupt Status Read to Clear Register (INT_STS_R2C) or DMA Controller Interrupt Status Read to Clear Register (DMAC_INT_STS_R2C) is read. Read of DMAC_INT_STS_R2C: 000 = Interrupt status does not clear on a read. 1x0 = Interrupt status clears on a read. 1x1 = Interrupt status clears on a read only if the channel's interrupt enable in DMAC_INT_EN_SET is set. Read of INT_STS_R2C: 000 = Interrupt status does not clear on a read. 100 = Interrupt status clears on a read. 101 = Interrupt status clears on a read-only if the channel's interrupt enable in DMAC_INT_EN_SET is set. 110 = Interrupt status clears on a read only if the channel's interrupt enable in INT_EN_SET is set. 111 = Interrupt status clears on a read only if the channel's interrupt enables in both DMAC_INT_EN_SET and INT_EN_SET are set.	R/W NASR (**Note 1**)	000b

Note 1: The NASR designation is only applicable when the DMA Software Reset (DMAC_SWR), TX DMA Software Reset x (TX_SWR_x) or RX DMA Software Reset x (RX_SWR_x) bits of the DMA Controller Command Register (DMAC_CMD) are set. Register bits designated as NASR are reset via other chip level software initiated resets.

2: The vector mapping is specified in the Interrupt Vector Mapping Table Registers (INT_VEC_MAPX).

10.0.33 DMAC DEBUG REGISTER 0 (DMAC_DEBUG_0)

Offset: 0FF0h
Size: 32 bits

This register contains debug control information. See Table 315.

TABLE 315: DMAC DEBUG REGISTER 0 (DMAC_DEBUG_0) SPECIFICATIONS

Bit	Description	Type	Default
31	**Debug Capture (DEBUG_CAP)** When this bit is set, debug information for the indicated channel/block is captured.	WO/SC	0b
30:5	**RESERVED**	RO	—
4:0	**Debug Channel (DEBUG_CH)** This field specifies the channel/block that is captured. 0 – descriptor cache RX ch 0 1 – descriptor cache RX ch 1 2 – descriptor cache RX ch 2 3 – descriptor cache RX ch 3 8 – RX ch 0 9 – RX ch 1 10 – RX ch 2 11 – RX ch 3 12 – descriptor cache TX ch 0 13 – reserved 14 – reserved 15 – reserved 16 – TX ch 0 17 – reserved 18 – reserved 19 – reserved 20 – coalescing 21 – reorder buffer 22 – 31 reserved	WO/SC	00000b

10.0.34 DMAC DEBUG REGISTER 1 (DMAC_DEBUG_1)

Offset: 0FF4h
Size: 32 bits

This register along with DMAC Debug Register 2 (DMAC_DEBUG_2) contains the captured debug information. See Table 316.

TABLE 316: DMAC DEBUG REGISTER 1 (DMAC_DEBUG_1) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Debug Data (DEBUG_DATA_1)** When this bit is set, debug information for the indicated channel/block is captured.	RO	0000_0000h

10.0.35 DMAC DEBUG REGISTER 2 (DMAC_DEBUG_2)

Offset: 0FF8h
Size: 32 bits

This register along with DMAC Debug Register 1 (DMAC_DEBUG_1) contains the captured debug information. See Table 317.

TABLE 317: DMAC DEBUG REGISTER 2 (DMAC_DEBUG_2) SPECIFICATIONS

Bit	Description	Type	Default
31:0	**Debug Data (DEBUG_DATA_2)** When this bit is set, debug information for the indicated channel/block is captured.	RO	0000_0000h

11.0 OTP CONTROL AND STATUS REGISTERS

This section details the OTP registers. The OTP registers are at offsets 1000h through 1020h within the device. This range is for exclusive use of the OTP registers. See Table 318.

TABLE 318: OTP REGISTER MAP

Byte Offset	Register Name (Symbol)
1000h	OTP Power Down Register
1004h	OTP Address High Register
1008h	OTP Address Low Register
100Ch	OTP Address Bits Register
1010h	OTP Program Data Register
1014h	OTP Program Mode Register
1018h	OTP Read Data Register
101Ch	Reserved
1020h	OTP Function Command Register

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

11.1 OTP Power Down Register

Offset: 1000h
Size: 32 bits

See Table 319.

TABLE 319: OTP POWER DOWN REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:1	**RESERVED**	RO	—
0	**PWRDN_N** This active-low bit directly controls the CEB input into the OTP IP. 0: OTP is operational 1: OTP is in power down (See **Note 1**.)	R/W	1b

Note 1: Software should clear this bit before performing OTP operations and set it after all planned OTP programming and read operations have completed.

11.2 OTP Address High Register

Offset: 1004h
Size: 32 bits

See Table 320.

TABLE 320: OTP ADDRESS HIGH REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:2	**RESERVED**	RO	—
1:0	**OTP_ADDR[12:11]** Address input. Programs the address targeted by OTP operation. These bits are directly connected to the Kilopass IP input A[12:11]. (See **Note 1**.)	R/W	00b

Note 1: Software must not change this field while read and programming operations are pending.

11.3 OTP Address Low Register

Offset: 1008h
Size: 32 bits

See Table 321.

TABLE 321: OTP ADDRESS LOW REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**OTP_ADDR[10:3]** Address input. Programs the address targeted by OTP operation. These bits are directly connected to the Kilopass IP input A[10:3]. (See **Note 1**.)	R/W	00h

Note 1: Software must not change this field while read and programming operations are pending.

11.4 OTP Address Bits Register

Offset: 100Ch
Size: 32 bits

See Table 322.

TABLE 322: OTP ADDRESS BITS REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:3	**RESERVED**	RO	—
2:0	**OTP_ADDR[2:0]** Address input. Programs the address targeted by OTP operation. These bits are directly connected to the Kilopass IP input A[2:0]. (See **Note 1** and **Note 2**.)	R/W	000b

Note 1: Software must not change this field while read and programming operations are pending.
2: When a read operation or byte-wide program operation occurs, bits OTP_ADDR[2:0] are ignored.

11.5 OTP Program Data Register

Offset: 1010h
Size: 32 bits
See Table 323.

TABLE 323: OTP PROGRAM DATA REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**OTP_WR_DATA** Parallel data to be written to the DATA register. The DATA register is then transferred to the OTP at the OTP_ADDR location with a program command.	R/W	00h

Note 1: Software must not change this field while a programming operation is pending.

11.6 OTP Program Mode Register

Offset: 1014h
Size: 32 bits
See Table 324.

TABLE 324: OTP PROGRAM MODE REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:1	**RESERVED**	RO	—
0	**PGM_MODE_BYTE** This indicates the units of a programming operation. 0 – Bit programming 1 – Byte programming The OTP IP can only be programmed on a bit basis. The OTP controller adjusts for this by issuing eight programming commands to implement byte programming. (See **Note 1** and **Note 2**.)	R/W	0b

Note 1: OTP reads are always byte wide.
2: Software must not change this field while a programming operation is pending.

11.7 OTP Read Data Register

Offset: 1018h
Size: 32 bits
See Table 325.

TABLE 325: OTP READ DATA REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:8	**RESERVED**	RO	—
7:0	**OTP_RD_DATA** This is the data from the OTP at the location pointed to by OTP_ADDR. To get fresh data a READ, PROGRAM, or PROGRAMVERIFY command operation must be issue before reading this register. (See **Note 1** and **Note 2**.)	RO	00h

Note 1: PROGRAM commands update this register, and the data bus output from OTP holds the value stored at the previously programmed location after the deassertion of PGMEN.

2: Since a data value of zero is not actually programmed, this field is not updated in such cases.

11.8 OTP Function Command Register

Offset: 1020h
Size: 32 bits
See Table 326.

Only a single bit in OTP Function Command register or OTP Test Command register must be set before initiating the OTP operation via the GO bit.

TABLE 326: OTP FUNCTION COMMAND REGISTER SPECIFICATIONS

Bit	Description	Type	Default
31:3	**RESERVED**	RO	—
2	**RESET** RESET command. Pulses the RSTB input into the OTP for a length specified in OTP Reset Pulse Width High Register. (See **Note 1**.)	R/W/SC	0b
1	**PROGRAM** Program OTP command.	R/W/SC	0b
0	**READ** Read OTP command.	R/W/SC	0b

Note 1: This bit clears after command is accepted by the OTP controller.

NOTES:

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002948A (2-11-19)	All	Initial release.

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