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COMPTE-RENDU TP ELEN2

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1.1. Astable with NAND Logic Gate (4093)

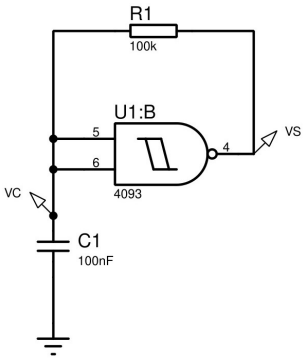

Figure 1.1. Astable NAND Logic Gate Circuit

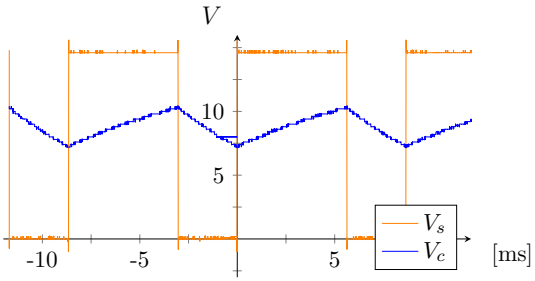

Figure 1.2. Signal Response V_c and V_s

According to theory, while the logic gate outputs $+15V$, pin 5 will be set to `HIGH`, and the capacitor will start charging itself. When the capacitor meets its threshold voltage $9.4V$ the output flops to $0V$ at which point pin 5 is set to `LOW` and pin 6 discharges from `HIGH` until the negative threshold volatge of $7.3V$.

This cycle repeats itself indefinetely creating a clock which can be seen on the signal response graph, and corresponds to the theoretical values.

1.2. Astable with NAND Logic Gate (4011)

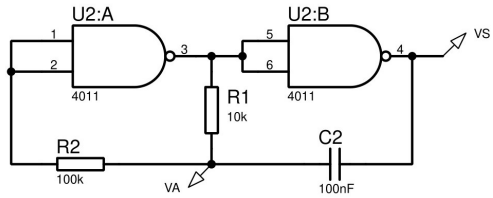

Figure 1.3. Astable NAND Logic Gate Circuit

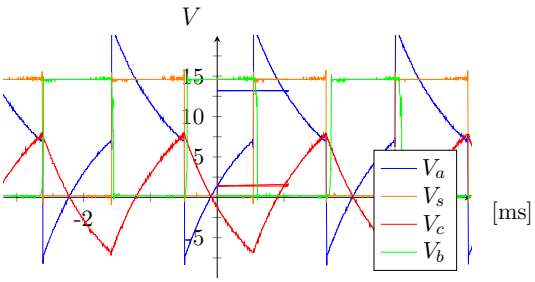

Figure 1.4. Signal Response V_a, V_b, V_c and V_s

Inicially the logic gates output $15V$ on pin 4 and pin 3. This in turn charges the capacitor allowing current to pass through and results in a spike in voltage at V_a, setting logic levels at pin 1 and 2 to `HIGH`, returning $0V$ at output 3.

As the voltage spike V_a falls down to the threshold $6.8V$ for pins 5 and 6 the logic gate outputs $0V$ on pin 4, discharging the capcitor. A negative voltage spike on V_a is then induced due to the capacitor, the output on pin 3 then flips to $15V$ setting pin 6 to a `LOW` logic level until the voltage rises to the $6.8V$ threshold as a result of the discharging capacitor.

This cycle repeats itself indefinetely creating a clock which can be seen on the signal response graph, and corresponds to the theoretical values.

As the probe `P1` is set to a `HIGH` logic state, the circuit appears to be functionning properly with no issues. The same however is not to be said when `P1` is at a `LOW` logic state, in which case the astable circuit no longer outputs a clock signal.

Due to this particular functionality we can quickly spot that `P1` acts as an enabling signal that can decide whether to turn the clock on or off.

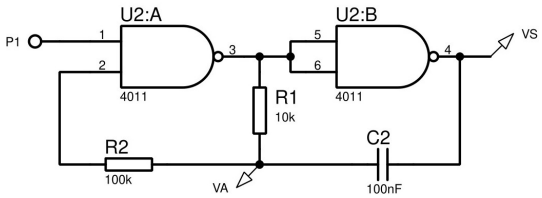

Figure 1.5. Astable NAND Logic Gate Circuit with Enable Probe

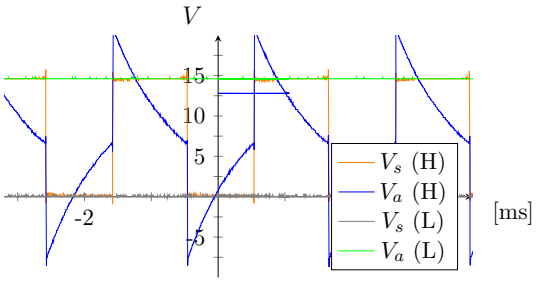

Figure 1.6. Signal Response V_a and V_s for P1 High and Low

1.3. Astable with NE555

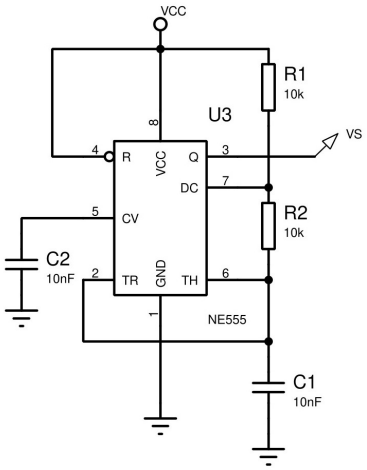

Figure 1.7. Astable NE555 Circuit

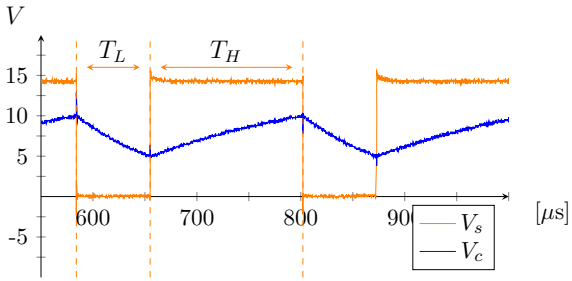

Figure 1.8. Signal Response V_c and V_s

After having set the circuit up, we carefully measure $T_L = 70\ \mu s$ and $T_H = 148\ \mu s$ with which we deduce the period $T = T_H + T_L = 218\ \mu s$ and by extension the frequency $f = \frac{1}{T} = 4.6\ kH_z$. The duty cycle can be easily obtained as $\tau = \frac{T_H}{T} = 67.9\%$
Level triggers are also measured to be around $10.2V$ for the positive threshold and $4.8V$ for the negative threshold.

Properties	Values
T_H	148 μs
T_L	70 μs
Period	218 μs
Duty Cycle	67.9 %
Frequency	4.6 kH_z
Positive Trigger	10.2 V
Negative Trigger	4.8 V

Figure 1.9. Measured Properties Summary

Properties	Values
T_H	138 μs
T_L	69.3 μs
Period	231 μs
Duty Cycle	66.5 %
Frequency	4.5 kH_z
Positive Trigger	10 V
Negative Trigger	5 V

Figure 1.10. Datasheet Properties Summary

All mesured values correspond with those from the datasheet.

As the `Trigger` voltage rises due to the charging capacitor, the comparator compares its value to the threshold $\frac{2}{3}V_{CC}$, as it does the voltage outputed to the flipflop sets the `Output` to `+VCC`.

Once it reaches the threshold the capacitor starts to discharge and the comparator no longer outputs to the flipflop causing the second comparator to compare its value to the `Threshold`, and since the latter is alway above $\frac{1}{3}V_{CC}$ the `Output` signal is set to $0V$. Upon meeting the $\frac{1}{3}V_{CC}$ threshold the cycle then repeats itself as the capcitor charges and `Output` is set back to `+VCC`.

This process can be seen on the signal response graph, as the capacitor charges, V_s is at $15V$, and as it discharges, iV_s falls down to $0V$.

This type of astable circuit is particularly useful since the pulse width can easily be modulated by changing the values of the resistors or capacitors using the datasheet as a refferal.

1.4. Astable with Operational Amplifier

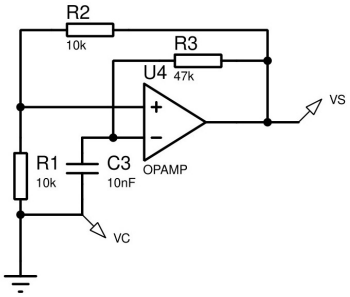

Figure 1.11. Astable Operational Amplifier Circuit

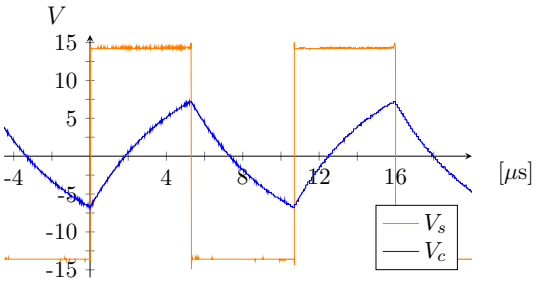

Figure 1.12. Signal Response V_c and V_s

As the operational amplifier incicially outputs $15V$, a positive threshold value $7.5V$ is set on the positive input pin whilst on the negative pin the capacitor charges itself from $0V$. Upon reaching the set threshold, the output flops to $-15V$ setting the negative threshold value at $-7.5V$.

As a result of the negative voltage the capacitor discharges itself until the negative threshold to which point the cycle repeats itself as the output of the operational amplifier is back at $15V$.

This process can be seen on the signal response graph, as the capacitor charges, V_s is at $15V$, and as it discharges, V_s falls down to $-15V$.

2. Summary

1. The first circuit with the NAND logic gate (4093) is convenient as it requires minimal component to set a function clock, with so however, the pulse width modulation needs to be repeatedly calculated and the circuit itself offers no signal input that can act as an enbaling function for the clock.

2. The second circuit with the NAND logic gate (4011) offer the same features as the previous 4093 NAND gate, in addition to the possibility to enable to clock using an external signal input at `P1`. The main drawback being that it requires two logic gates which can result in being more costly for extensive fabrication.

3. The NE555 Circuit is much more expensive in terms of cost as the component alone uses 1 flipflop, 2 comparators, and 2 transistor. This comes with a glad payoff were the clock itself can be easily mended with as the pulse width modulation is documented as well as its frequency and trigger levels. The component itself is very versatile and offers many more adjustable functions that other circuits do not have.

4. Lastly, the astable operational amplifier circuit allows for a similar clock as the NAND logic gate (4093), although benefiting from high slew rate and wide output voltage range. With its counterpart it still lacks an enabling input and requires manual computation for its pulse width modulation.