# VHDL Synthesis The IEEE Std. 1076.3 (summary)

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# **Interpretation of vector**

Given the variables:

v1 : std\_logic\_vector(1 DOWNTO 0); v2 : std\_logic\_vector(2 DOWNTO 0); res : std\_logic\_vector(2 DOWNTO 0);

v1 := "11"; v2 := "000";

res := v1 + v2;





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# **IEEE "synthesis packages"**

- An IEEE standard Std 1076.3 1997
- Two similar packages:
  - numeric\_bit: vector is based on type bit use ieee.numeric bit.all:
  - numeric\_std: vector is based on type std\_(u)logic use ieee.numeric\_std.all;
- Two types are declared in these packages:
  - signed: twos complement representation type SIGNED is array (NATURAL range <>) of STD\_LOGIC;
  - unsigned: unsigned representation type UNSIGNED is array (NATURAL range <>>) of STD\_LOGIC;

Use at most <u>one</u> of these packages in a design unit.





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## The subprograms in numeric\_std and numeric\_bit

- Arithmetic
- Comparison
- Shift/rotate
- Resize
- Conversion
- Std\_match



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# **Arithmetic**

Type of operands	signed	unsigned	natural	integer
signed	Std. 1076.3	not supported	Std. 1076.3	Std. 1076.3
unsigned	not supported	Std. 1076.3	Std. 1076.3	not supported
natural	Std. 1076.3	Std. 1076.3	Std. 1076	Std. 1076
integer	Std. 1076.3	not supported	Std. 1076	Std. 1076

unary: abs, - (both only for type signed)

binary: +, -, \*, /, rem, mod



# Arithmetic /3

#### Range of the result of addition and subtraction

R	signed	integer
L		
signed	max(L'length,R'length)-1 downto 0	L'length-1 downto 0
integer	R'length-1 downto 0	Std. 1076-1987/1993

#### Range of the result of multiplication

R	signed	integer
L		
signed	L'length + R'length-1 downto 0	2×L'length-1 downto 0
integer	2×R'length-1 downto 0	Std. 1076-1987/1993



## **Arithmetic /6**

#### Range of the result of division, mod, rem

R	signed	integer
L		
signed	L'length -1 downto 0	L'length-1 downto 0
integer	R'length-1 downto 0	Std. 1076-1987/1993



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#### functions Shift/Rotate

- shift\_left (vec, pos);
  - vec is shifted 'pos' to the left. Vacated positions filled with '0'.
  - pos should be >= 0.
- shift\_right (vec, pos);
  - vec is shifted 'pos' to the right. Vacated positions filled with:

'0' for unsigned vec vec(vec'left) for signed vec

- pos should be >= 0.
- rotate\_left (vec, pos); rotate\_right (vec, pos);
  - rotate\_left or rotate\_right over 'pos' positions.
  - pos should be >= 0.

Also overloaded the predefined functions sll, srl, rol, ror (std. 1076-1993). In these functions "pos" may also be negative.



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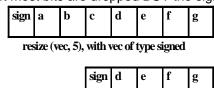
#### **Function** Resize

- Resize (vec, length);
  - result is a vector of the specified length.
  - unsigned:

if length > vec'length then left most bit positions filled with '0'. otherwise left most bits are dropped.

- signed:
  - if length > vec'length then left most bit positions filled with vec(vec'left).

otherwise left most bits are dropped BUT the sign bit is retained.





# **Conversion functions**

- to\_integer(vec);
  - · returns the integer value of 'vec'. Two overloaded functions for vec of type signed and unsigned.
  - if 'vec' contains other values then '0','1','L','H' then the result is 0, and
- to\_unsigned(value,length);

a warning is raised

- · returns an unsigned vector of the specified length.
- if value is out of range a warning raised.
- to\_signed(value,length);
  - · returns a signed vector of the specified length.
  - if value is out of range a warning raised.



# Omission in the package std\_logic\_1164

```
SIGNAL a : std_logic_vector(0 TO 2);
IF a = "1-1" THEN ..
```

# equal?

```
SIGNAL a : std_logic_vector(0 TO 2);
IF a(0)='1' AND a(2)='1' THEN ..
```



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### Std\_match

- Numeric\_std contains a functions std\_match, input of type:
   std\_ulogic
   std\_logic

  - unsigned
  - signed std\_logic\_vector
  - std\_ulogic\_vector

SIGNAL a : std\_logic\_vector(0 TO 2);

IF std\_match(a, "1-1") THEN ..

- Functions returns TRUE only if:
  - both values are logical values ('0', '1', 'L', 'H') and the same.
  - one value is '0' and the other is 'L'
  - one value is '1' and the other is 'H'
  - at least one of the values is '-'
- If the two arguments are vectors:
  - · the operands should be of the same length, and
  - the function is applied on each element

