Design of Digital Systems

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- **Goal: to become familiar with the design flow of a digital system:**
  - **Design decisions**
  - **Correctness/Assertion Based Verification/Testing/PSL**
- **Hardware description language VHDL**
  - **Simulation**
  - **Synthesis**
- **Case: design your own subset MIPS processor**

Personal involved

- **Lecturers**
  - **Bert Molenkamp, ZI-4051,**
    coordinator of this course
    email: e.molenkamp@utwente.nl
  - **Sabih Gerez, ZI-4033, lecture: low power**
    email: s.h.gerez@utwente.nl
  - **Jan Kuper, ZI-4102, lecture: PSL**
    email: j.kuper@utwente.nl

- **Lab. assistant (for questions about your project)**
  - **Marco Gerards, ZI-4090**
    email: m.e.t.gerards@utwente.nl

Topics of the lecture

- Introduction VHDL
- VHDL in more detail (some slides)
- Synthesis of VHDL
- Behaviour, algorithm, datapath & control
- Assertion Based Verification (PSL) (Jan Kuper)
- Low power (Sabih Gerez)
- Verilog

Practical training

- First two weeks
  - Introduction in the environment and language (VHDL simulation and synthesis)
  - Advice: work in teams of two persons
  - Additional lectures on Fridays

    7 September 13.45 in ZI-4126 and ~15.00 Lab

    14 September 13.45 in ZI-5126 and ~15.00 Lab
  - No grade
- The other weeks
  - Form teams of up to 4 students (your action!).
  - Design your own MIPS processor

Tooling

- QuestaSim; VHDL simulator (available in the lab).
  ModelSim-Altera starter can be legally used at home (see BlackBoard).

- QuartusII; VHDL synthesis tool.
  Web Edition of QuartusII can be legally used at home (see BlackBoard).

- MIPS tooling (assembler, simulator):
  - Tool developed by EPFL Lausanne (http://www.perseguers.ch/epfl/mips/), or
  - SPIM http://spimsimulator.sourceforge.net/)

QuestaSim ~ Modelsim with PSL support

Grading

- **Based on the MIPS processor design**
  - **The design; include the design steps (all steps in VHDL!)**
    - Behavior
    - Algorithm
    - Datapath & Controller
    - Synthesis of datapath (and postsimulation)
  - **Design decisions (alternatives and motivation) made in all design steps (in your report!).**
  - **Motivation of the test (including test procedures for sub designs) and including useful PSL properties.**
  - **The report (include a CD or other media with the design steps and how to reproduce the tests).**
  - **And the the time your project is finished.**

- **If you want in-between comment on your work send it to me by email before the date listed in the roster.**

BlackBoard

- **Many information (slides, etc) is available, e.g.**
  - **Slides**
  - **Books**
  - **Example of a design flow of a simple ALU. Study it because you have to make similar design steps**
  - **Interesting links**