# Register file

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
ENTITY register_file IS
  PORT (aa,ba,da : IN  unsigned(3 DOWNTO 0);
        d        : IN  std_logic_vector(7 DOWNTO 0);
        a,b      : OUT std_logic_vector(7 DOWNTO 0);
        rw, clk  : IN  std_logic);
END register_file;

ARCHITECTURE behavior OF register_file IS
  TYPE mem_type IS ARRAY(0 TO 15) OF std_logic_vector(7 DOWNTO 0);
  SIGNAL reg_file : mem_type;
BEGIN
  write:PROCESS(clk)
  BEGIN
    IF rising_edge(clk) THEN
      IF rw='1' THEN
        reg_file(to_integer(da))<=d;
      END IF;
    END IF;
  END PROCESS;
  a <= reg_file(to_integer(aa));
  b <= reg_file(to_integer(ba));
END behavior;
```