UNIVERSITY OF TWENTE.

Study guide

Fundamentals of Digital Logic

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March 2013

Contents

Course material in detail

1.1 Course material

Book used in this course:

Logic and Computer Design Fundamentals, fourth edition
M. Morris Mano en Charles R. Kime
Prentice-Hall, Upper Saddle River, New Jersey, USA.
ISBN: 0-13-198926-X (hard cover)
ISBN: 0-13-206711-0 (paperback) (International edition)

Note the page numbers in both books are not the same:
Page number paperback = page number hard cover + 18

Errata is available: http://www.prenhall.com/mano/

On, and via, blackboard additional reading material is available.

1.2 Assessment

The written examination is based on:
- material presented at the lectures
- slides, exercises, labs and additional reading material on Blackboard.
- the following additional reading material provided by the publisher:
  http://www.prenhall.com/mano/ ➔fourth edition➔"Reading Supplements":
  - Design & Analysis Using JK & T-Flip-flops,
  - Error Detection and Correction,
  - Logic Analysis,
  - Carry-Lookahead Adder
- the book *Logic and Computer Design Fundamentals, fourth edition* the chapters 1 until 7 (inclusive) and chapter 8 until section 8.4 (inclusive).

1.3 Book in detail: sections of the book not for exam

From the chapters 1 until 8 of the book not all the material is to be known for the written examination.

Here some details:

Section 1-5, 'Alphanumeric Codes'.
The principles of the alphanumeric codes (ASCII code) should be understood, of course, the table 1.5 need not be learned.

Section 2-6, 'Pragmatic Two-Level Optimization'
Not for written exam.

Section 2-7, 'Multiple-Level Optimization.
Multi-level optimization not for written exam.

Section 4-8 "HDL Representations for Combinational Circuits-Verilog"
Not for written exam.

Section 5-3 subsection “Master-Slave Flip-Flops”

The pulse-triggered flip-flop is not for written exam.

Section 5-3 figure 5-13

Second row in this figure (pulse-triggered flip-flops) not for written exam.

Section 5-9 “HDL Representations-Verilog”

Not for written exam.

Section 6-1 “The Design Space”.

Not for written exam.

Section 6-3 “Flip-Flop Timing”

The text on ‘pulse-triggered’ flipflops is not part of the examination material (e.g. figure 6-7a and figure 6-8b) . The Edge triggered flipflop IS part the examination material.

Section 7-12 “HDL Representations for Shift Registers and Counters-Verilog”

Not for written exam

2 Organization of the course

The assessment of this course is based on the lab and the written exam.

1) **The Lab (practical training).**

   The practical training consists of two parts:

   a) The intermediate assignment
   The intermediate assignment is compulsory. You cannot attend the written examination if this assignment is not finished successfully.

   This intermediate assignment must be completed at latest in lab session 7 (Wednesday June 19, 2013).

   b) The final assignment.
   The final assignment is optional. The final assignment is graded with 0 or 10 point! These points are only valid for the written exam immediately after the lecture period and not for the resit.

   For a successful completion of the final assignment you must have finished your intermediate assign at latest in lab session 5 (Wednesday June 12, 2013).

   Unfortunately, it appears that about 50% of the students do not finish the final assignment in time due to a poor preparation.

2) **Written exam.**
   You must have completed the intermediate assignment before you can attend the written exam and the resit.

3 Course grading

The course is not graded if the intermediate assignment is not finished successfully.

3.1 Written exam immediately after the lecture period

Points for written exam (WE): 0 until 90
Points for final assignment (FA): 0 OR 10

Grade = round to nearest integer ((WE + FA)/10)

3.2 Written exam (RESIT)

Points for written exam (WE): 0 until 100

Grade = round to nearest integer (WE/10)