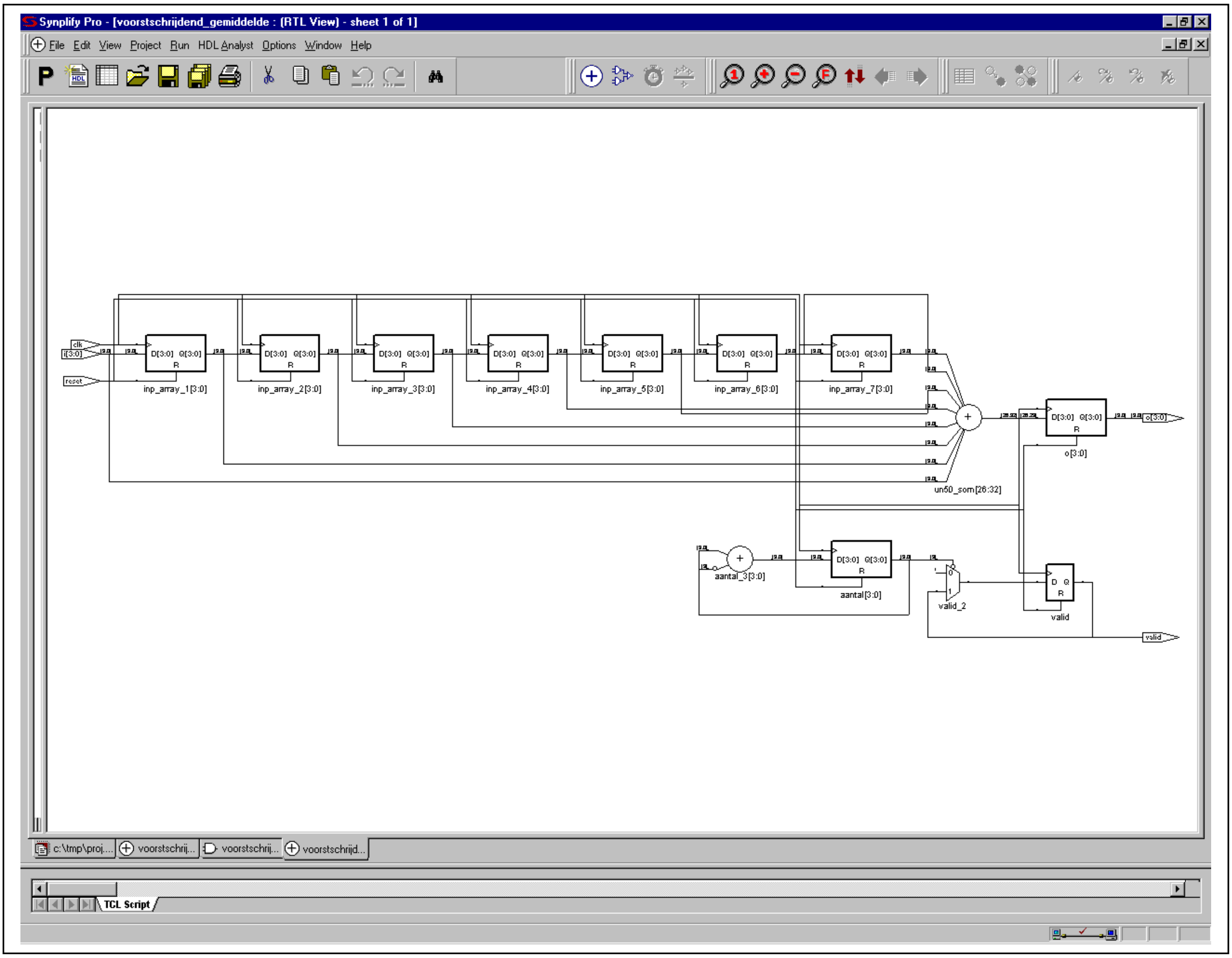
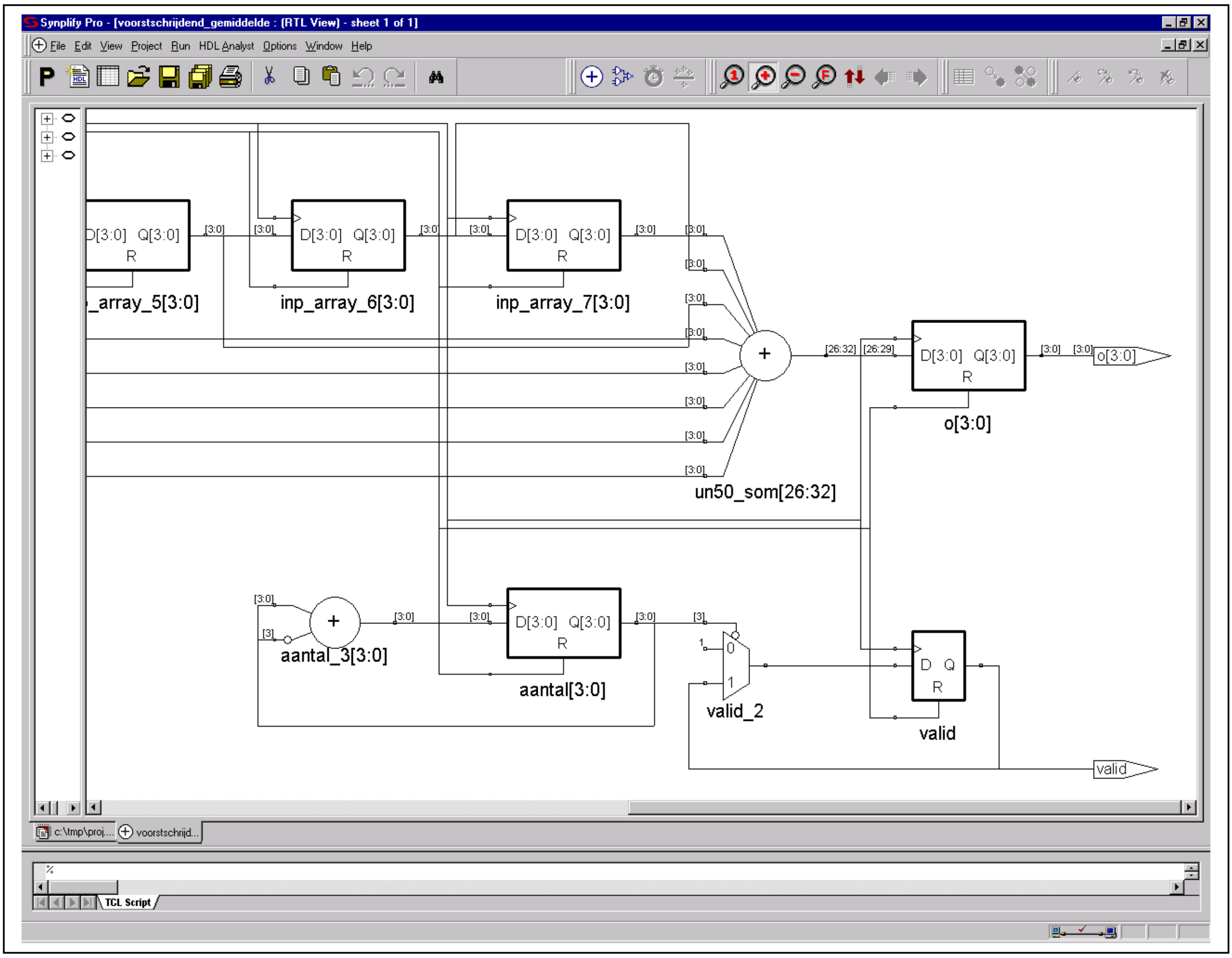
Resultaten november 2001

```
ENTITY voorstschrijdend_gemiddelde IS
  GENERIC (n : positive := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit; -- synchroon
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde;

ARCHITECTURE gedrag OF voorstschrijdend_gemiddelde IS
BEGIN
  PROCESS (reset,clk)
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    FUNCTION gemiddeld(inp : integer_array)
             RETURN integer IS
      VARIABLE som : integer RANGE 0 TO inp'LENGTH*max;
    BEGIN
      som := 0;
      FOR i IN inp'RANGE LOOP som:=som+inp(i); END LOOP;
      RETURN som/inp'LENGTH;
    END gemiddeld;
    VARIABLE inp_array : integer_array(1 TO n);
    VARIABLE aantal : integer RANGE 0 TO n*max;
  BEGIN
    IF reset='1'
      THEN valid <='0'; aantal := 0; inp_array := (OTHERS=>0); o <= 0;
    ELSIF clk='1' and clk'EVENT THEN
        IF aantal < n
          THEN aantal:=aantal+1;
          ELSE valid <= '1';
        END IF;
        inp_array := i & inp_array(1 TO n-1);
        o <= gemiddeld (inp_array);
    END IF;
  END PROCESS;
END gedrag;
```

```
$ Start of Compile
#Thu Nov 29 11:49:06 2001

Synplicity VHDL Compiler, version 6.1.0, Build 067R, built Oct 20 2000
Synplicity ProAsic Technology Mapper, version 6.1.0, Build 068R, built Oct 23 2000
Requested     Estimated     Requested     Estimated
Clock     Frequency     Frequency     Period        Period        Slack
-----------------------------------------------------------------------
clk       1.0 MHz       51.5 MHz      1000.0        19.4          980.6
=======================================================================
```



Synplify Pro - [voorstschrijdend_gemiddelde : (RTL View) - sheet 1 of 1]
File
Edit
View
Project
Run
HDL Analyst
Options
Window
Help
clk
i[3:0]
reset
D[3:0] Q[3:0]
R
inp_array_1[3:0]
inp_array_2[3:0]
inp_array_3[3:0]
inp_array_4[3:0]
inp_array_5[3:0]
inp_array_6[3:0]
inp_array_7[3:0]
un50_som[26:32]
o[3:0]
aantal_3[3:0]
aantal[3:0]
valid_2
valid
D Q
0
1
c:\tmp\proj....
voorstschrij...
voorstschrij...
voorstschrijd...
TCL Script


Synplify Pro - [voorstschrijdend_gemiddelde : (RTL View) - sheet 1 of 1]
File Edit View Project Run HDL Analyst Options Window Help
D[3:0] Q[3:0]
R
_array_5[3:0]
D[3:0] Q[3:0]
R
inp_array_6[3:0]
D[3:0] Q[3:0]
R
inp_array_7[3:0]
[3:0]
+
un50_som[26:32]
[26:32]
[26:29]
D[3:0] Q[3:0]
R
o[3:0]
o[3:0]
[3:0]
[3]
+
aantal_3[3:0]
D[3:0] Q[3:0]
R
aantal[3:0]
0
1
valid_2
D Q
R
valid
valid
c:\tmp\proj...
voorstschrijd...
%
TCL Script

```
ENTITY voorstschrijdend_gemiddelde_rec IS
  GENERIC (n : positive := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit; -- synchroon
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde_rec;

ARCHITECTURE recursief OF voorstschrijdend_gemiddelde_rec IS
BEGIN
  PROCESS (reset,clk)
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    FUNCTION som(inp : integer_array)
             RETURN integer IS
      CONSTANT midden : integer := inp'LENGTH/2;
--      CONSTANT inpi : integer_array(1 TO inp'LENGTH) := inp;  -- synthesis complains
      VARIABLE inpi : integer_array(1 TO inp'LENGTH);
    BEGIN
      inpi := inp;
      IF inpi'LENGTH=1 THEN
        RETURN inpi(1);
      ELSE
        RETURN som(inpi(1 TO midden)) + som(inpi(midden+1 TO inpi'LENGTH));
      END IF;
    END som;
    VARIABLE inp_array : integer_array(1 TO n);
    VARIABLE aantal : integer RANGE 0 TO n*max;
  BEGIN
    IF reset='1'
      THEN valid <='0'; aantal := 0; inp_array := (OTHERS=>0); o <= 0;
    ELSIF clk='1' and clk'EVENT THEN
        IF aantal < n
          THEN aantal:=aantal+1;
          ELSE valid <= '1';
        END IF;
        inp_array := i & inp_array(1 TO n-1);
        o <= som(inp_array)/n;
    END IF;
  END PROCESS;
END recursief;
```

```
$ Start of Compile
#Thu Nov 29 11:42:31 2001

Synplicity VHDL Compiler, version 6.1.0, Build 067R, built Oct 20 2000
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VHDL syntax check successful!
Synthesizing work.voorstschrijdend_gemiddelde_rec.recursief
\\synnac\syn\george\nt\syn610\src\compilers\lsynth\lctx.c:396 Compiler Error: Could not delete binding for
variable inp_1
Probably near:
@E:"c:\tmp\gemid_recursief.vhd":24:30:24:35|Compiler Error - please check end of log for more information
Please call Synplicity Support (USA) at (408) 548-6000 or send
email including this log and test case to support@synplicity.com
Process took 0.11 seconds realtime, 0.13 seconds cputime
```
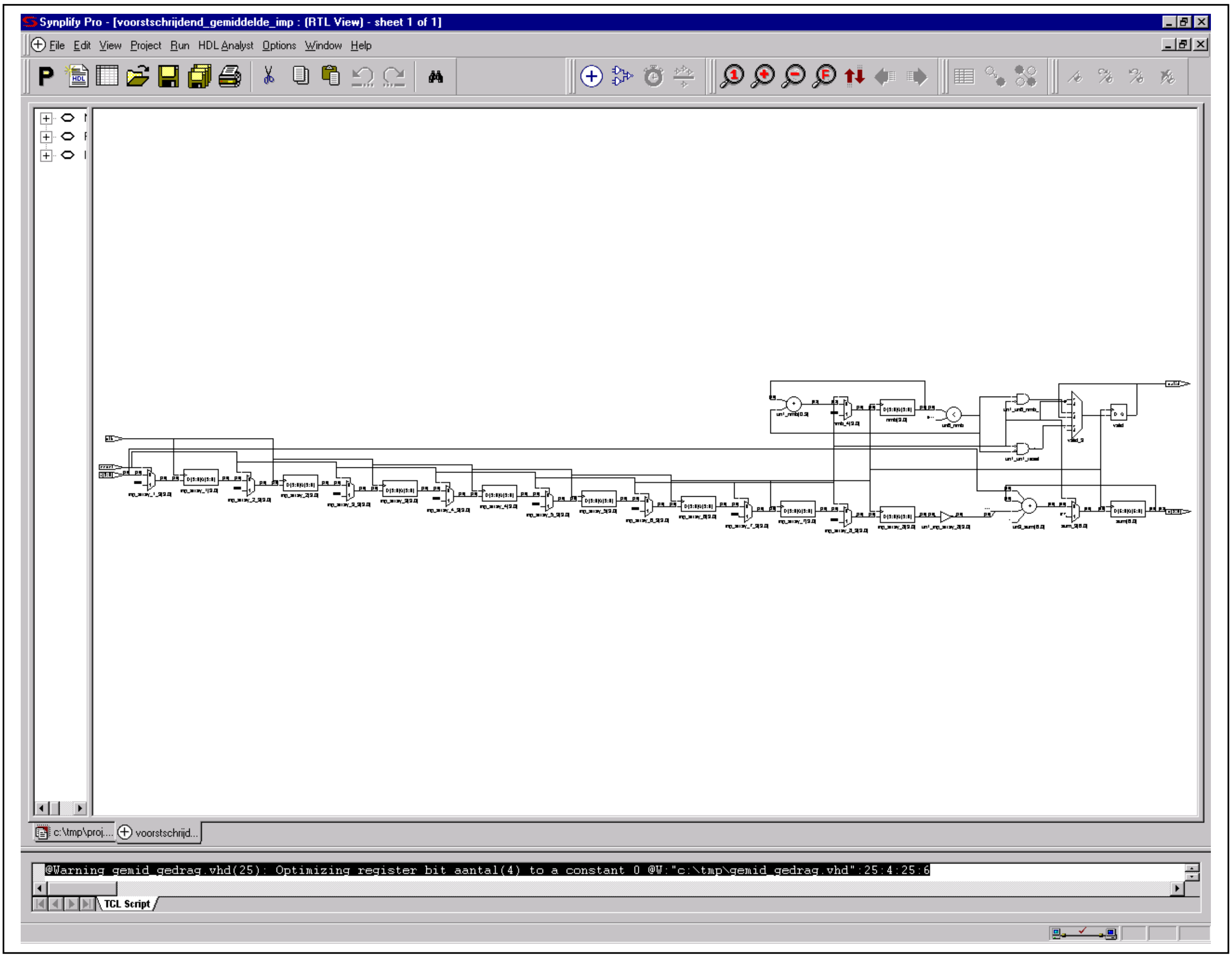
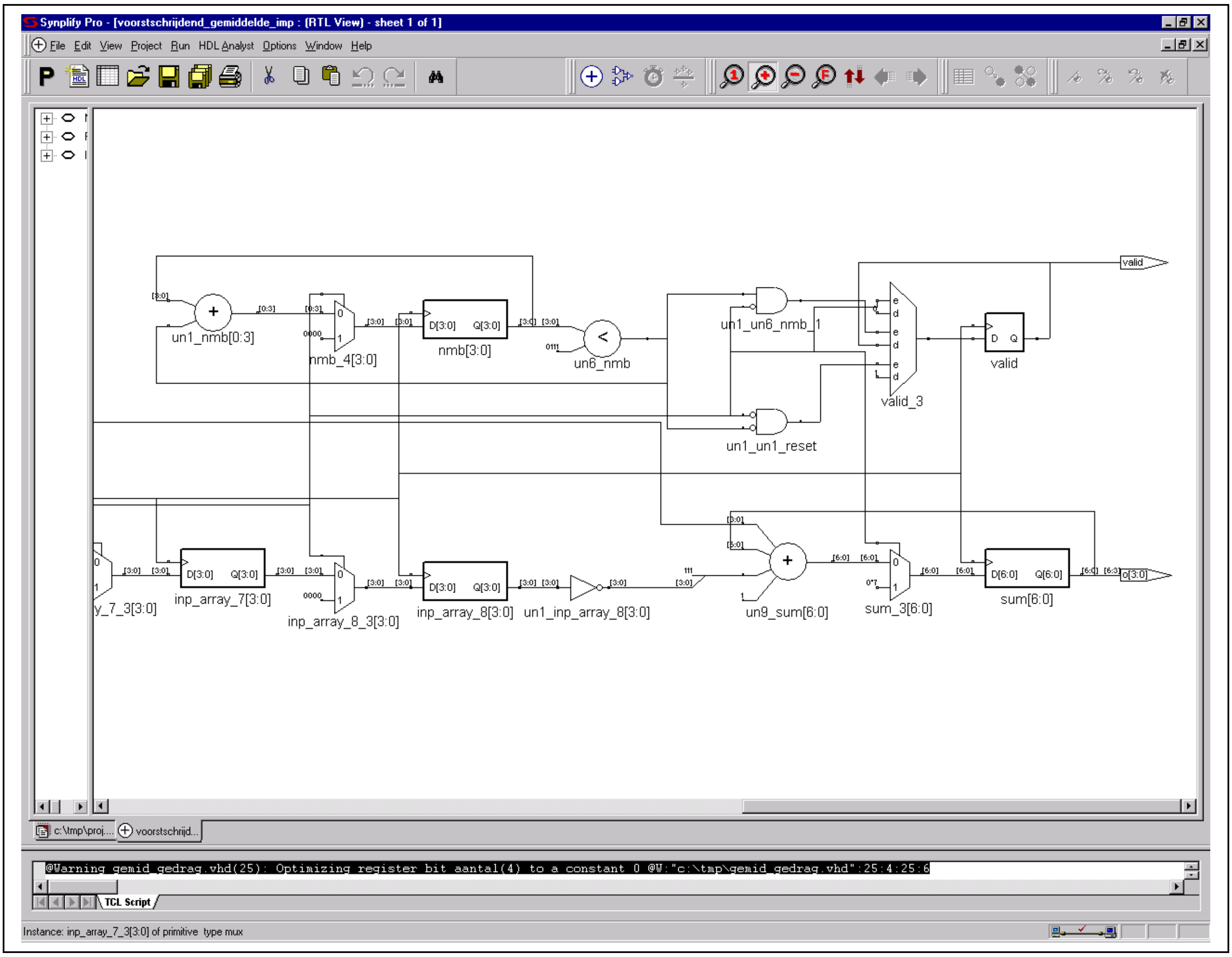

```
 ENTITY voorstschrijdend_gemiddelde_imp IS
  GENERIC (n : integer := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit;
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde_imp;

ARCHITECTURE implementatie OF voorstschrijdend_gemiddelde_imp IS
BEGIN
  PROCESS
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    VARIABLE inp_array : integer_array(1 TO n);
    VARIABLE index : integer RANGE 0 TO n -1;
    VARIABLE nmb : integer RANGE 0 TO n;
    VARIABLE sum : integer RANGE 0 TO max*(n+1);
  BEGIN
    WAIT UNTIL clk='1';
    IF reset='1' THEN
      valid <='0'; nmb := 0; sum := 0; index:=0; o <=0; inp_array:=(OTHERS=>0);
    ELSE
      IF nmb < n-1 THEN
        nmb:=nmb+1;
      ELSE
        valid <= '1';
      END IF;
      sum := sum + i - inp_array(n);
      o <= sum / n;
      inp_array := i & inp_array(1 TO n-1);
    END IF;
  END PROCESS;
END implementatie;
```

```
          Requested     Estimated     Requested     Estimated
Clock     Frequency     Frequency     Period        Period        Slack
-----------------------------------------------------------------------
clk       1.0 MHz       73.9 MHz      1000.0        13.5          986.5
=======================================================================
```



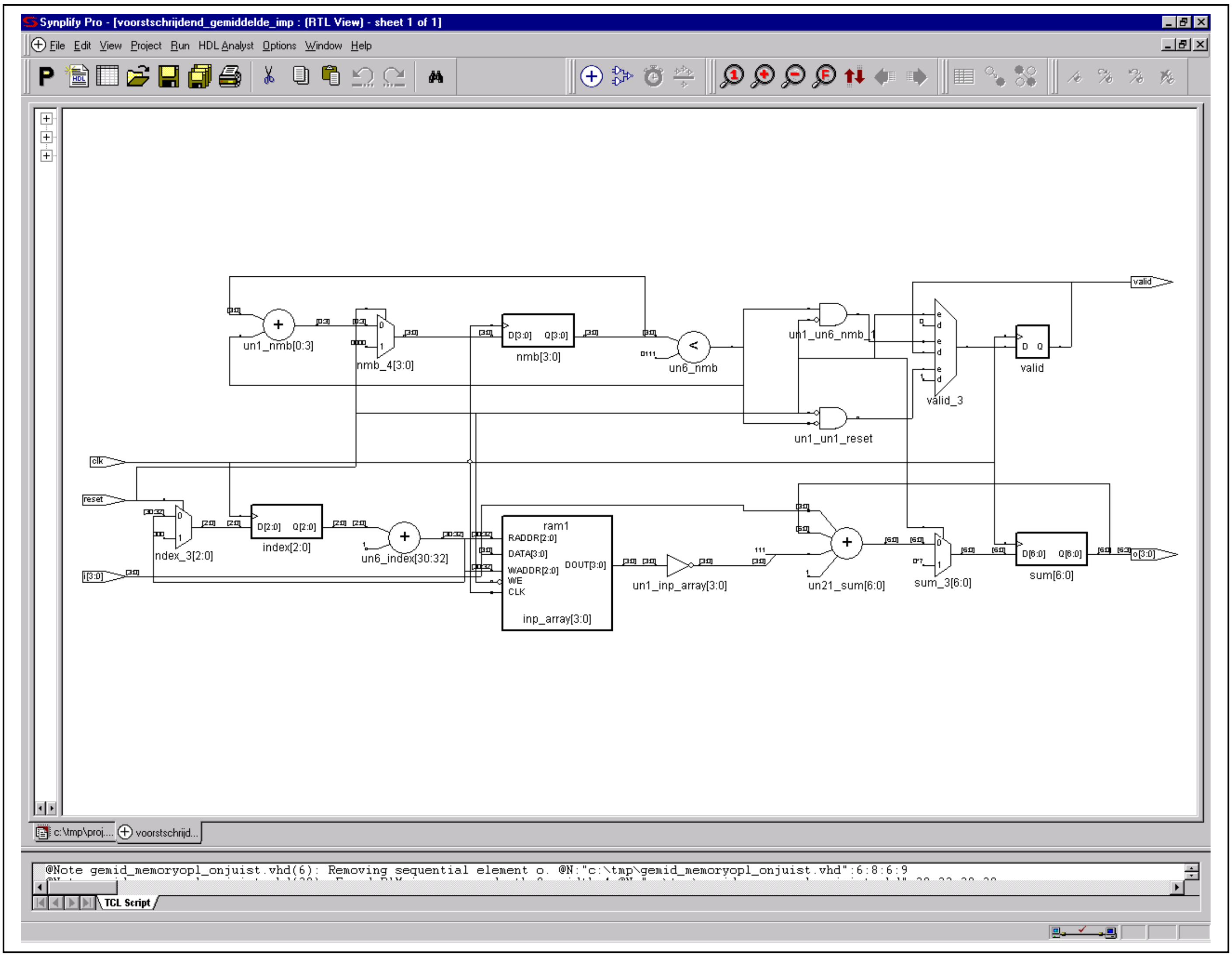
```
@Warning gemid_gedrag.vhd(25): Optimizing register bit aantal(4) to a constant 0 @W:"c:\tmp\gemid_gedrag.vhd":25:4:25:6
```



```
@Warning gemid_gedrag.vhd(25): Optimizing register bit aantal(4) to a constant 0 @W:"c:\tmp\gemid_gedrag.vhd":25:4:25:6
```

Instance: inp_array_7_3[3:0] of primitive type mux

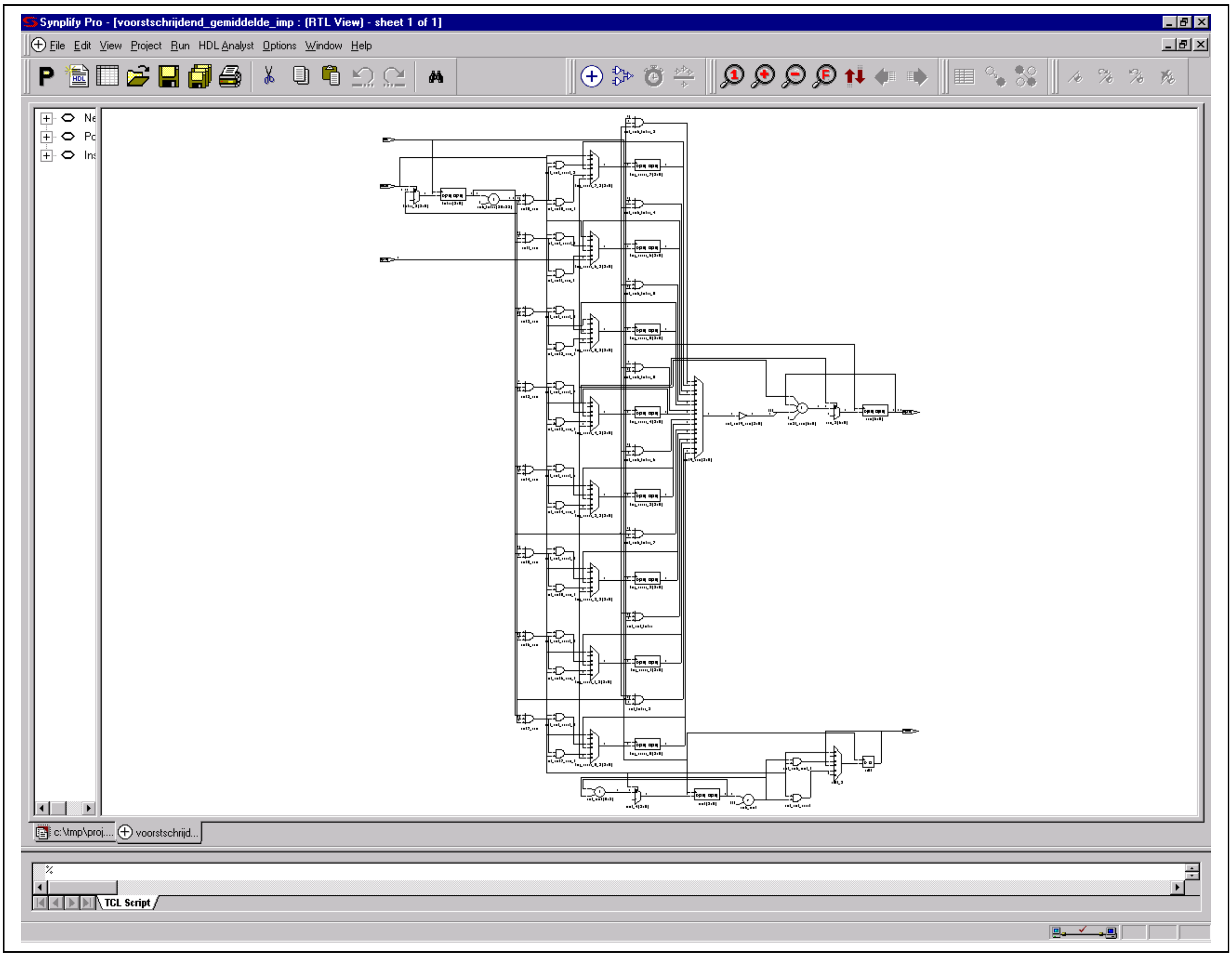
```
ENTITY voorstschrijdend_gemiddelde_imp IS
  GENERIC (n : integer := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit;
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde_imp;

ARCHITECTURE implementatie OF voorstschrijdend_gemiddelde_imp IS
BEGIN
  PROCESS
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    VARIABLE inp_array : integer_array(0 TO n-1);
    VARIABLE index : integer RANGE 0 TO n -1;
    VARIABLE nmb : integer RANGE 0 TO n;
    VARIABLE sum : integer RANGE 0 TO max*(n+1);
  BEGIN
    WAIT UNTIL clk='1';
    IF reset='1' THEN
      valid <='0'; nmb := 0; sum := 0; index:=0; o <=0; -- inp_array:=(OTHERS=>0);
    ELSE
      IF nmb < n-1 THEN
        nmb:=nmb+1;
      ELSE
        valid <= '1';
      END IF;
      index := (index + 1) MOD n;
      sum := sum + i - inp_array(index); -- moet sum 1 bit groter worden?
      o <= sum / n;
      inp_array(index):= i;
    END IF;
  END PROCESS;
END implementatie;

-- Bij deze oplossing wordt het geheugen niet expliciet op nul gezet.
-- Dit betekent dat de som 'biased' is met het gemiddelde van de
-- initiele waarde van de registers.
               *********************

          Requested     Estimated     Requested     Estimated
Clock     Frequency     Frequency     Period        Period        Slack
-----------------------------------------------------------------------
clk       1.0 MHz       47.7 MHz      1000.0        21.0          979.0
=======================================================================
```

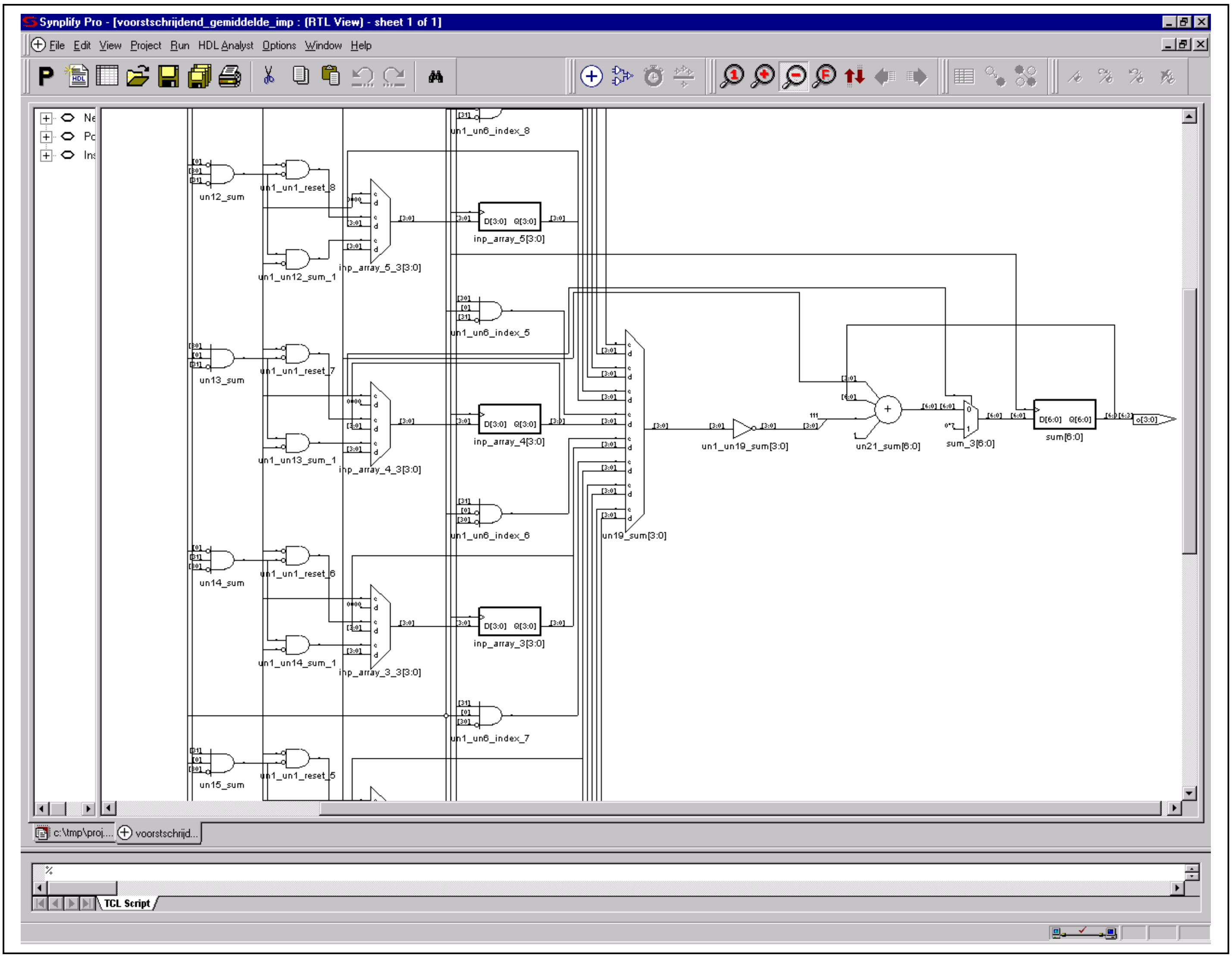


```
@Note gemid_memoryopl_onjuist.vhd(6): Removing sequential element o. @N:"c:\tmp\gemid_memoryopl_onjuist.vhd":6:8:6:9
```

```
ENTITY voorstschrijdend_gemiddelde_imp IS
  GENERIC (n : integer := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit;
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde_imp;

ARCHITECTURE implementatie OF voorstschrijdend_gemiddelde_imp IS
BEGIN
  PROCESS
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    VARIABLE inp_array : integer_array(0 TO n-1);
    VARIABLE index : integer RANGE 0 TO n -1;
    VARIABLE nmb : integer RANGE 0 TO n;
    VARIABLE sum : integer RANGE 0 TO max*(n+1);
  BEGIN
    WAIT UNTIL clk='1';
    IF reset='1' THEN
      valid <='0'; nmb := 0; sum := 0; index:=0; o <=0; inp_array:=(OTHERS=>0);
    ELSE
      IF nmb < n-1 THEN
        nmb:=nmb+1;
      ELSE
        valid <= '1';
      END IF;
      index := (index + 1) MOD n;
      sum := sum + i - inp_array(index);
      o <= sum / n;
      inp_array(index):= i;
    END IF;
  END PROCESS;
END implementatie;

-- Bij deze oplossing wordt het geheugen niet expliciet op nul gezet.
-- Dit betekent dat de som 'biased' is met het gemiddelde van de
-- initiele waarde van de registers.
-- inp_array:=(OTHERS=>0); initialeert geheugen ==> geen memory meer.
```

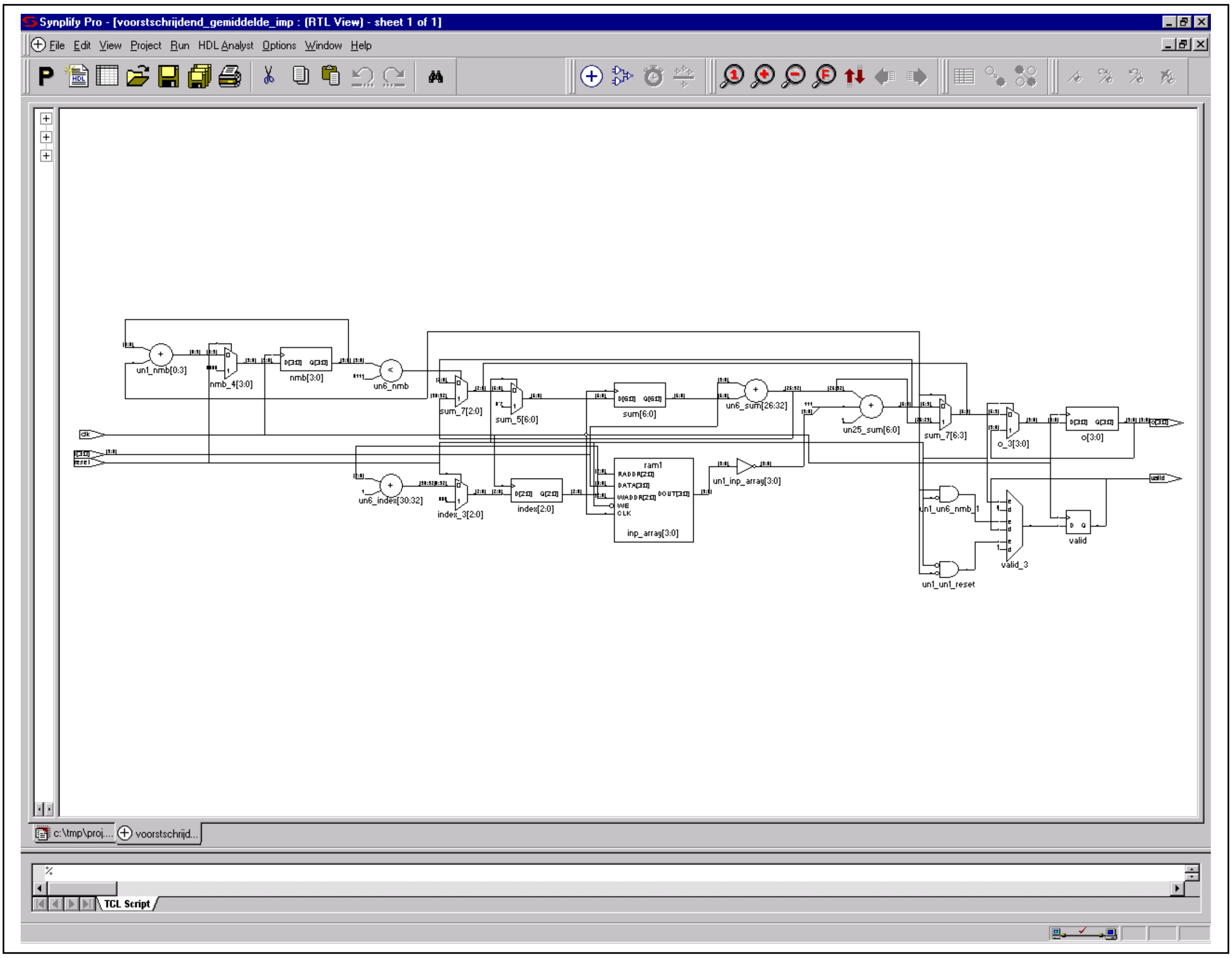
```
          Requested     Estimated     Requested     Estimated
Clock     Frequency     Frequency     Period        Period        Slack
-----------------------------------------------------------------------
clk       1.0 MHz       42.2 MHz      1000.0        23.7          976.3
=======================================================================
```

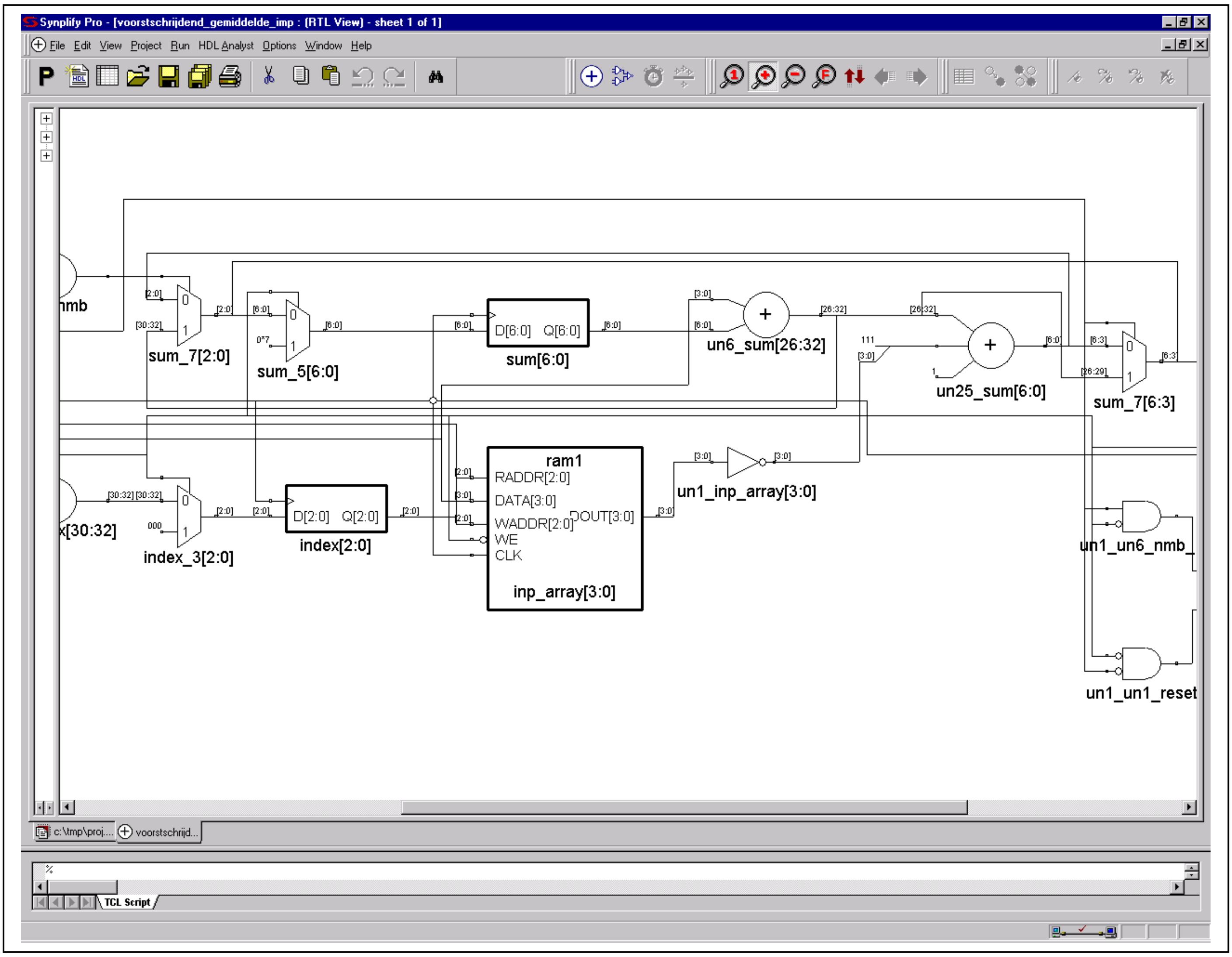

Synplify Pro - [voorstschrijdend_gemiddelde_imp : (RTL View) - sheet 1 of 1]
File Edit View Project Run HDL Analyst Options Window Help
Ne
Pc
Ins
c:\tmp\proj....
voorstschrijd...
%
TCL Script


Synplify Pro - [voorstschrijdend_gemiddelde_imp : (RTL View) - sheet 1 of 1]
File Edit View Project Run HDL Analyst Options Window Help
Ne
Pc
Ins
un1_un6_index_8
un12_sum
un1_un1_reset_8
un1_un12_sum_1
inp_array_5_3[3:0]
D[3:0] Q[3:0]
inp_array_5[3:0]
un1_un6_index_5
un13_sum
un1_un1_reset_7
un1_un13_sum_1
inp_array_4_3[3:0]
inp_array_4[3:0]
un1_un6_index_6
un19_sum[3:0]
un1_un19_sum[3:0]
un21_sum[6:0]
sum_3[6:0]
D[6:0] Q[6:0]
sum[6:0]
o[3:0]
un14_sum
un1_un1_reset_6
un1_un14_sum_1
inp_array_3_3[3:0]
inp_array_3[3:0]
un1_un6_index_7
un15_sum
un1_un1_reset_5
c:\tmp\proj...
voorstschrijd...
TCL Script

```
ENTITY voorstschrijdend_gemiddelde_imp IS
  GENERIC (n : integer := 8; max : positive := 15);
  PORT (i     : IN integer RANGE 0 TO max;
        reset : IN bit; -- synchroon
        clk   : IN bit;
        o     : OUT integer RANGE 0 TO max;
        valid : OUT bit);
END voorstschrijdend_gemiddelde_imp;

ARCHITECTURE implementatie OF voorstschrijdend_gemiddelde_imp IS
BEGIN
  PROCESS
    TYPE integer_array IS ARRAY (natural RANGE <>) OF integer RANGE 0 TO max;
    VARIABLE inp_array : integer_array(0 TO n-1);
    VARIABLE index : integer RANGE 0 TO n -1;
    VARIABLE nmb : integer RANGE 0 TO n;
    VARIABLE sum : integer RANGE 0 TO max*(n+1);
  BEGIN
    WAIT UNTIL clk='1';
    IF reset='1' THEN
      valid <='0'; nmb := 0; sum := 0; index:=0;
    ELSE
      sum := sum + i;
      IF nmb < n-1 THEN -- inhoud geheugen mag willekeurig zijn
        nmb:=nmb+1;
      ELSE
        valid <= '1';
        sum := sum - inp_array(index);
      END IF;
      inp_array(index):= i;
      o <= sum / n;
      index := (index + 1) MOD n;
    END IF;
  END PROCESS;
END implementatie;
```

```
          Requested     Estimated     Requested     Estimated
Clock     Frequency     Frequency     Period        Period        Slack
-----------------------------------------------------------------------
clk       1.0 MHz       51.0 MHz      1000.0        19.6          980.4
=======================================================================
```


Synplify Pro - [voorstschrijdend_gemiddelde_imp : (RTL View) - sheet 1 of 1]
File Edit View Project Run HDL Analyst Options Window Help
un1_nmb[0:3]
nmb_4[3:0]
D[3:0] Q[3:0]
nmb[3:0]
un6_nmb
sum_7[2:0]
sum_5[6:0]
D[6:0] Q[6:0]
sum[6:0]
un6_sum[26:32]
un25_sum[6:0]
sum_7[6:3]
o_3[3:0]
D[3:0] Q[3:0]
o[3:0]
clk
reset
un6_index[30:32]
index_3[2:0]
D[2:0] Q[2:0]
index[2:0]
ram1
RADDR[2:0]
DATA[3:0]
WADDR[2:0]
WE
CLK
DOUT[3:0]
inp_array[3:0]
un1_inp_array[3:0]
un1_un6_nmb_1
un1_un1_reset
valid_3
D Q
valid
c:\tmp\proj...
voorstschrijd...
TCL Script


Synplify Pro - [voorstschrijdend_gemiddelde_imp : (RTL View) - sheet 1 of 1]
File Edit View Project Run HDL Analyst Options Window Help
nmb
sum_7[2:0]
sum_5[6:0]
0*7
D[6:0] Q[6:0]
sum[6:0]
un6_sum[26:32]
111
un25_sum[6:0]
sum_7[6:3]
ram1
RADDR[2:0]
DATA[3:0]
WADDR[2:0]
WE
CLK
DOUT[3:0]
inp_array[3:0]
un1_inp_array[3:0]
x[30:32]
000
index_3[2:0]
D[2:0] Q[2:0]
index[2:0]
un1_un6_nmb_
un1_un1_reset
c:\tmp\proj...
voorstschrijd...
TCL Script