

# Chenyang Zhu

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## EDUCATION

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### ZHEJIANG UNIVERISTY

#### *Bachelor of Computer Science and Technology*

Hangzhou, China

Sep 2020 – present

- **Academic:** Overall GPA 3.90/4.0 (88.63/100)
- **English Proficiency:** Toefl 104
- **Honor:**
  - Zhejiang Provincial Government Scholarship
  - Outstanding Student of Zhejiang University
- **Research Interests:**
  - IoT Security, Cloud Native Security, Software Security, Network Security

## RESEARCH EXPERIENCE

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### **Get to know whether the vulnerable package in your supply chain is dangerous at low cost**

Hangzhou, China

*Zhejiang University, Supervisor: Dr. Wenbo Shen*

Aug 2022 – present

- Measure the accuracy of supply chain vulnerability detection tool which usually runs on a coarse grain (parse metadata only)
- Currently proposing a method to describe module to realize cross-module analysis with low cost
- Provide open source databases derived from large-scale analysis to facilitate future research

## PROJECTS

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### **Detect Vulnerability in Google Blockly Code Generator**

Hangzhou, China

*Project of Student Research Train Program*

Apr 2022 – present

- Improved the solidity code generator for *Google Blockly*, enabling it to dynamically store key syntax information
- Summarized the characteristics of some classic vulnerabilities, and developed a tool to automatically detect them based on that syntax information. Currently working on improving it

### **Single-User Compact Database Engine**

Hangzhou, China

*Coursework of Database System*

May 2022

- Designed and implemented a singer-user database engine which includes five modules: disk and buffer pool manager, catalog manager, record manager, index manager, executor engine and SQL parser. User can enter SQL language through CLI
- The engine supports basic CRUD operations, three data types (int, float, char), multiple tables and multiple databases
- Accelerated searching based on automatically built B+ tree index on primary key

### **Dynamically Scheduled Risc-V CPU Design**

Hangzhou, China

*Coursework of Computer Architecture*

Dec 2022

- Using Verilog to design Pipelined CPU with IF/IS/RO/FU/WB stages which supports multicycle operations
- Designed dynamically scheduled pipeline with Scoreboard
- Designed different function units with state machine

## SKILLS

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- Programming Language: C/C++, Python, Verilog, X86 & Risc-V Assembly Language, SQL
- Other: Linux, CodeQL, SOOT