Innovus Tutorial

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Outline

- **Preparation**

- **Import Design & Floorplan**

- **Place & Power plan**

- **Clock Tree Synthesis**

- **Power Route & NanoRoute**

- **Save Out & Post-sim**

Lab for Data Processing System

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Lab for Data Processing System

Preparation

- **Copy your syn. files to syn/**

- **Adjust timing constraint in file:**
  - layout/IG_APR.sdc
  - set cycle 8.0

- **Select server with CentOS**
  - source /usr/cad/innovus/CIC/license.cshrc
  - source /usr/cad/innovus/CIC/innovus.cshrc

- **$ cd layout/**

- **$ innovus**
  - DON'T use '&', we will use the terminal interface

Lab for Data Processing System

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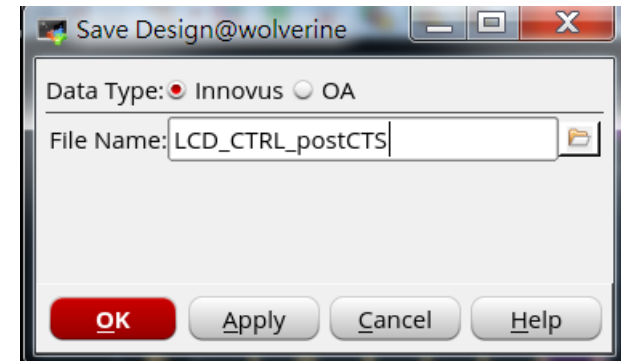
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Design import

- File → Import Design → Load

- Load → IG.globals → Open → OK

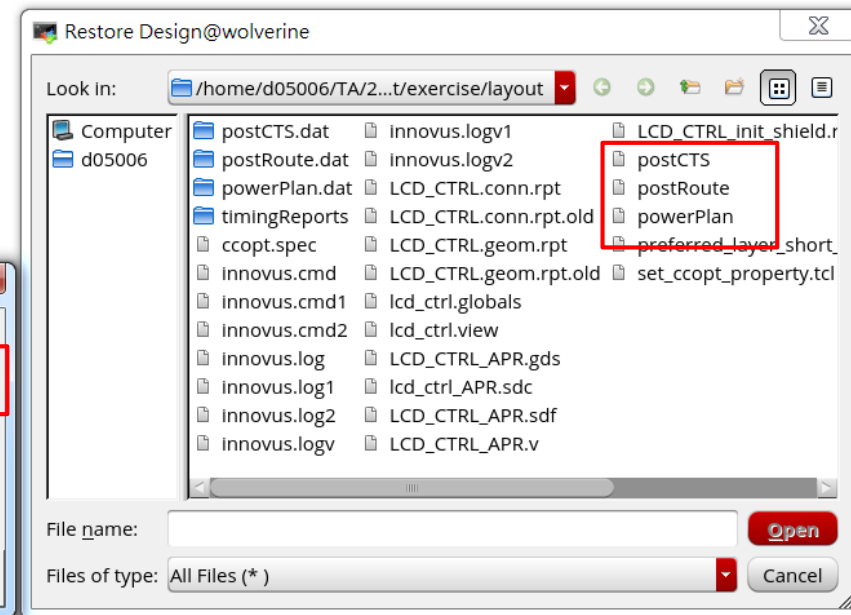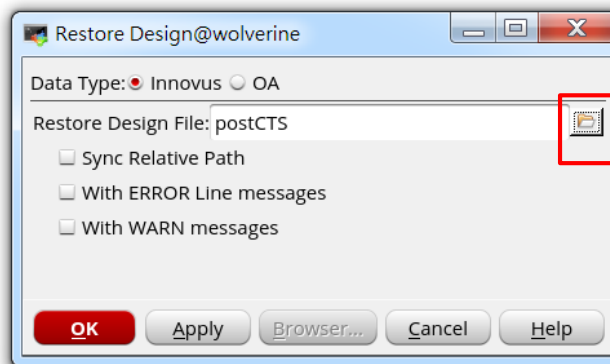Lab for Data Processing System

Save/Load

- 進行到任何步驟都可以儲存目前狀態
  - File → Save Design
  - 勾選'Innovus'，輸入 File Name
  - OK

- 隨時中斷/不滿意可讀檔繼續步驟
  - File → Restore Design
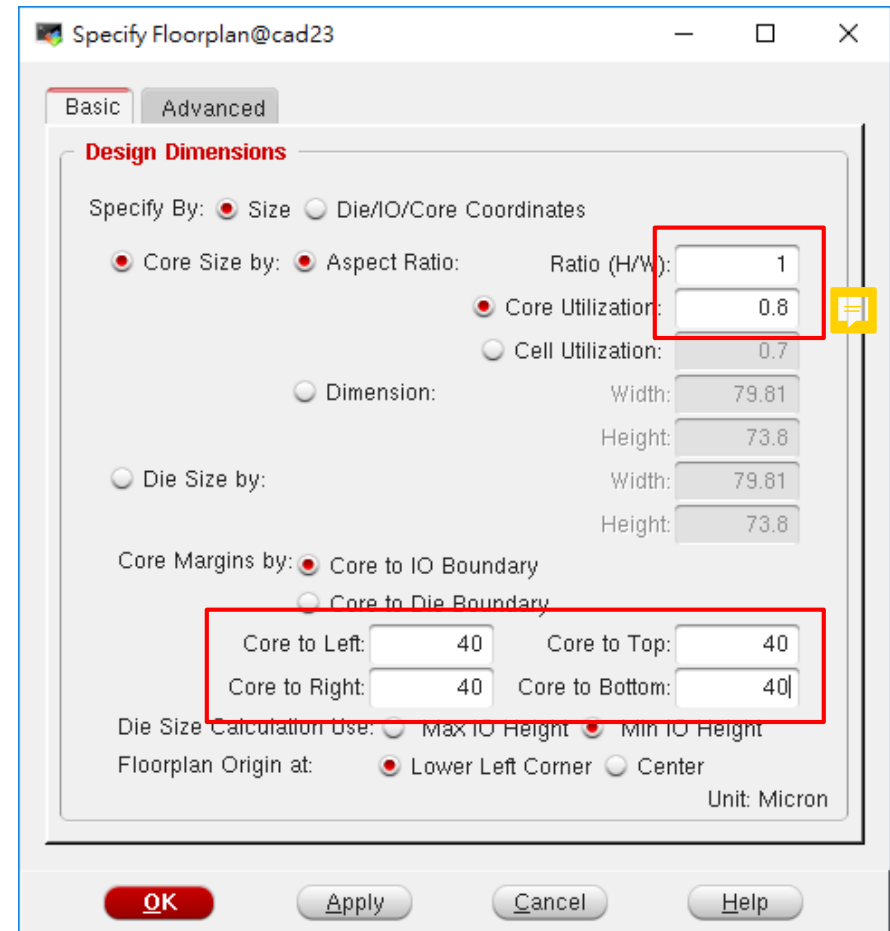 - 勾選 'Innovus'，按browse
  - Open → OK

Global Net Connect

- 目的：把所有的 **Standard cell** 的 **power/ground pin** 連接到 **VDD/VSS**

- **Power → Connect Global Nets**

  - Connect選Pin，Pin Name(s)填入VDD，Scope選Apply All，To Global Net填入VDD，按Add to List

  - Connect選Pin，Pin Name(s)填入VSS，Scope選Apply All，To Global Net填入VSS，按Add to List

  - 將1'b1/1'b0連接至VDD/VSS

    – Connect選Tie High，Scope選Apply All，To Global Net填入VDD，按下Add to List

    – Connect選Tie Low，Scope選Apply All，To Global Net填入VSS，按下Add to List

  - 按下Apply，再按Check，再關閉視窗

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Floorplan

■ **Floorplan → Specify Floorplan**

- 填入數值（可自行調整）

- OK

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Placement In Floorplan Mode

- **Place → Place Standard Cell**

  - 選擇Run Placement In Floorplan Mode (Optimization Options的選項取消勾選: Include Pre-Place Optimization，按OK

  - 執行完之後可以選擇不同的design view (下圖紅框處)，會看到tool已經幫我們把所有的cell擺進去core裡面

Notice →

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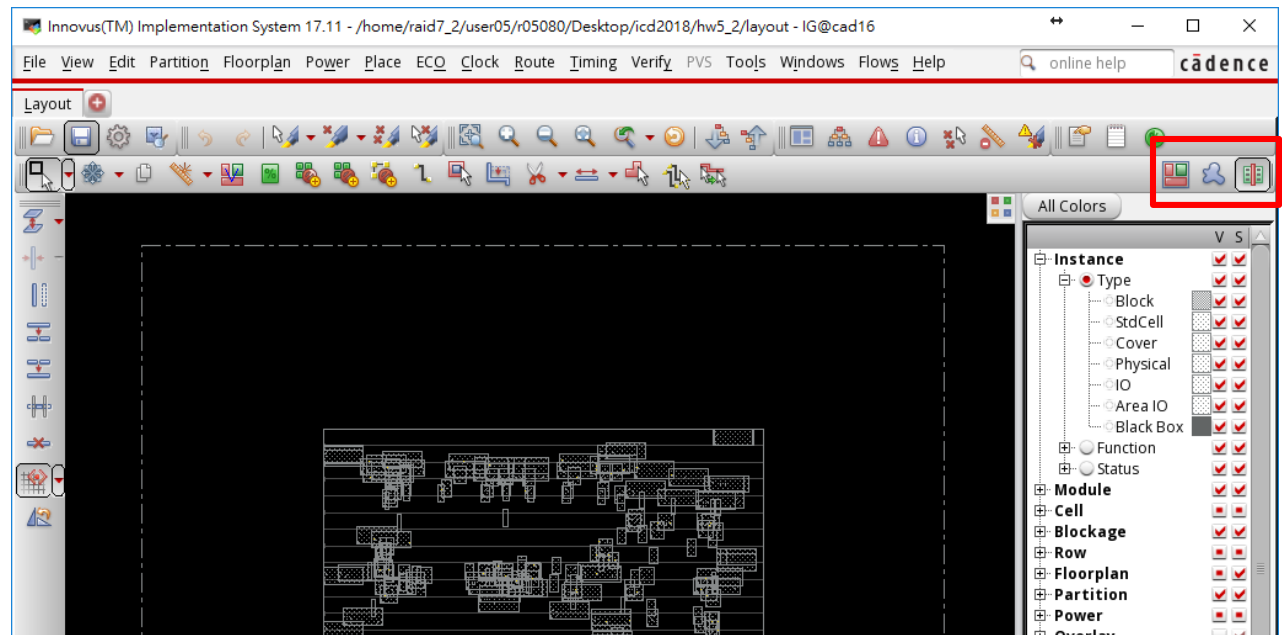
Timing analysis

▪ Timing → Report Timing

- Design Stage選擇Pre-Place，按下OK

  – 此時Tool會開始分析trial route與RC Extraction，計算出各點的delay後再使用STA (Static timing analysis)分析Data path

  – Tool跑完之後可以在Terminal看到分析之後的結果，主要是WNS (Worst Negative Slack)，如果這個值是負的，則表示目前的Placement結果無法達到IG_APR.sdc裡面的Timing constraint

  – 如果WNS是負的，Innovus有補救的方法，就是執行Timing Optimization (後面會講解步驟，這裡先不用做)

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Full mode place

▪ **Place ➔ Place Standard Cell**

- 選擇Run Full Placement，取消Include Pre-Place Optimization
- 按Mode，加選Enable Clock Gating Awareness，按OK
- 按OK開始跑Placement

▪ **執行Place ➔ Refine Placement來讓cell擺置的方向正確**

▪ **Timing ➔ Report Timing**

- Design Stage選擇Pre-CTS
- 如果WNS為負，則進行Timing Optimization
  - ECO ➔ Optimize Design
  - Design Stage選擇Pre-CTS，按OK

Lab for Data Processing System
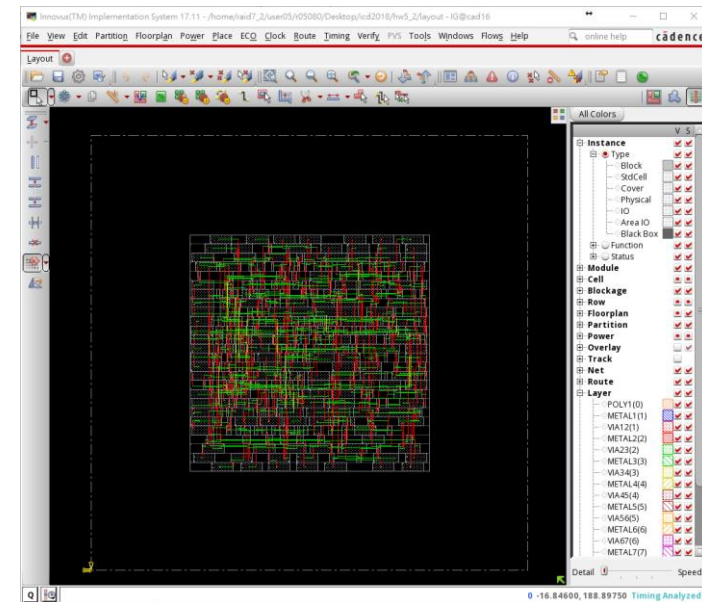
Power ring

- 目的：在core周圍建立一圈Power ring，讓晶片內部供電電壓均勻，避免IR drop

- **Place → Refine Placement ，直接按OK**

  - 此步驟主要是先拿掉timing analysis產生的trial route的結果，以免影響Powerplan，做完這步之後會發現Physical view裡面原本有的繞線都被移除了

Data Processing System
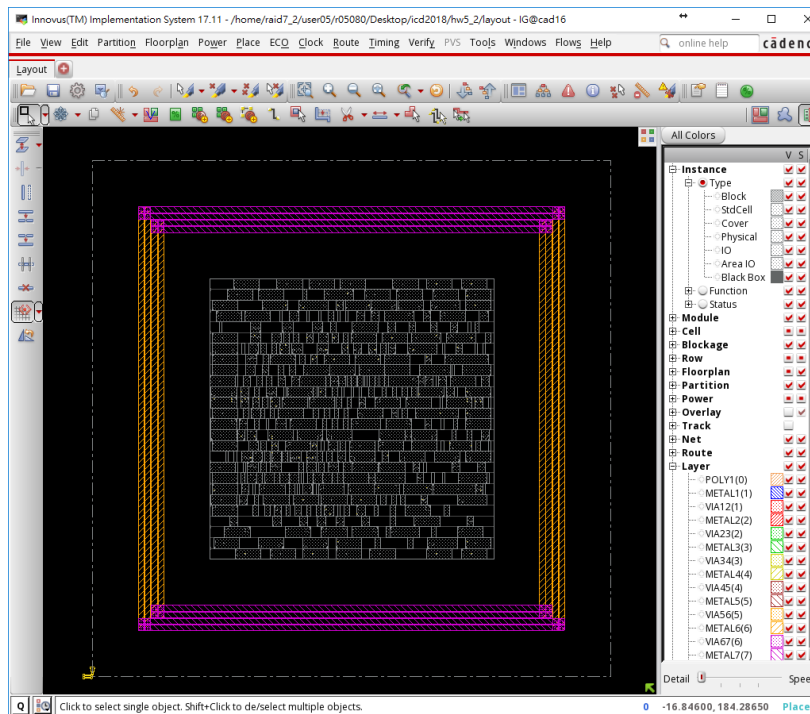
Power ring

- **Power → Power Planning → Add Ring**
  - Net(s)選VDD VSS
  - Ring Configuration
    - Top/Bottom Layer改成METAL7 H
    - Left/Right Layer改成METAL6 V
    - Width都改成2
    - 填完之後按一下Spacing下面的Update
    - 勾選Offset: Center in channel
  - 切換到Advanced
    - 勾選wire group
    - 勾選Interleaving
    - Number of bits填入2，按OK 💬
  - 做完之後可以看到Core跟I/O Pad之間多了一圈Power ring

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Power stripe

- 目的：加入垂直方向的**Power stripe**，也是用來使**core**內部的供電電壓均勻

Lab for Data Processing System
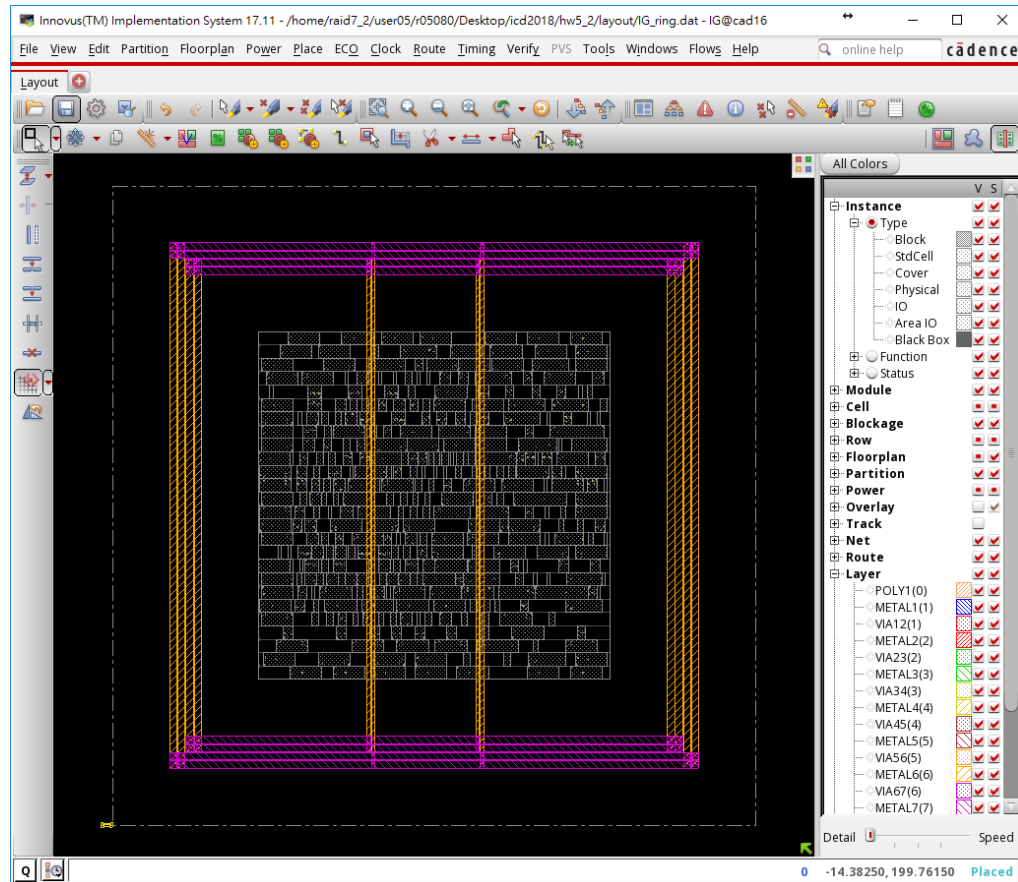
Power stripe

▪ Power → Power Planning → Add Stripe

- Net(s) 選VDD VSS
- Layer選擇METAL6 (由於我們想要create的是直的stripe，所以在這裡我們選擇METAL6，若是要打上橫的stripe，則選擇METAL7)
- Width設定為1，按下Update
- 選擇Set-to-set distance，並設定為30
- 下方First/Last Stripe 的start設定為30，Stop設定為30
- 切換到Advanced
  - 勾選Switch layer over obstructions
  - 勾選wire group與Interleaving，Number of bits設定為1
- 按OK

Lab for Data Processing System

DRC Check

▪ **Verify → Verify Geometry，按OK**

- 看terminal是否有任何的Violations，在這裡出現的Violation最好要解決掉(可以重新做placement或是手動移動block)，否則留到後面就很難解決了

- 在layout上面如果有出現X的圖案，則表示那邊有DRC error

Lab for Data Processing System

Add Tie High/Low Cell

- **先做一下timing analysis**

  - Timing →Report Timing

  - Design Stage選擇Pre-CTS，按下OK

  - 若 WNS是負的，則必須做 optimization，或是DRC有max fanout violation也可以用optimization來修

    - ECO → Optimize Design，在Optimization Type裡加選Max Fanout，OK

    - 如果Optimization作完後仍然WNS為負，則加選Incremental繼續執行Optimization，直到修到WNS為正

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Add Tie High/Low Cell

- **將1'b0及1'b1連到tie high或tie low cell上**

  - 執行 Place → Tie Hi/Lo Cell → Add → Mode，左欄選 TieHiLo， Cell Name 輸入TIEHI TIELO，勾選Specify Maximum Fanout 設 10，勾選 Specify Maximum Distance設100，OK。

  - Cell Name已設為TIEHI TIELO，OK (TIEHI TIELO 中間有空格，外面不要有大括號)

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Clock Tree Synthesis (CTS)

■ 本步驟都在**terminal**輸入指令

■ 設定**ccopt**的基本參數，直接**source**以下檔案

- $ source set_ccopt_property.tcl

■ 產生對應的**ccopt**參數

- $ create_ccopt_clock_tree_spec -file ccopt.spec

- $ source ccopt.spec

■ 進行**Clock Tree Synthesis**

- $ ccopt_design –cts

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Post-CTS Timing analysis

- **Timing ➜ Report Timing，Design Stage 選 Post-CTS，Analysis Type選Setup，OK**
  - 若 WNS 是負的，做 ECO ➜ Optimize Design…，選 Post-CTS，OK
  - 重複直到 WNS 為正

- **Timing ➜Report Timing，Design Stage 選 Post-CTS，Analysis Type選Hold，OK。**
  - 若 WNS 是負的，做 ECO ➜ Optimize Design…，選 Post-CTS，OK
  - 重複 11.4 直到 WNS 為正

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Lab for Data Processing System

Route Power

- **Route →Special Route**

  - Basic → Net(s) → …→加入 VSS VDD

  - SRoute 只留下 Follow pins → OK

  - 可以看到core cell的power(藍色的線) 都連到左右的power ring上

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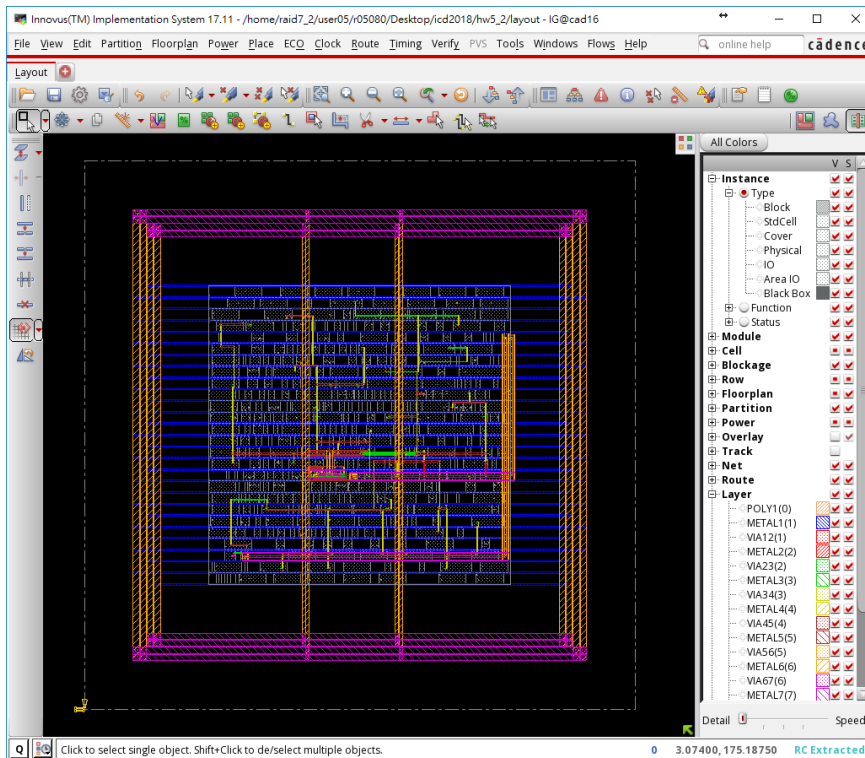
檢查 Special Net 的 DRC 及 connectivity

- **Place ➔Refine Placement, OK**

  - 將 trial route 的 signal net 移除

- **Verify Connectivity, Net type 選 Special Only, Check 取消 unrouted net, OK**

  - 如果有任何的 violation，每一個都用滑鼠點擊選取 violation 的繞線檢查問題

  - 修正完後可以重複本投影片確認不再有violation

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Routing

- **Route➔NanoRoute➔Route**

  - 勾選Insert Diodes，Diode Cell Name輸入ANTENNA
  - 勾選Timing driven
  - 勾選SI Driven
  - 點選Attribute
    - 選 Nettype(s), Clock Nets
    - Weight: 10
    - Spacing: 1
    - Avoid Detour: True (意思是 Route as short as possible)
    - 按 OK
  - 按OK，開始routing，看看有沒有violation

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Routing

Lab for Data Processing System
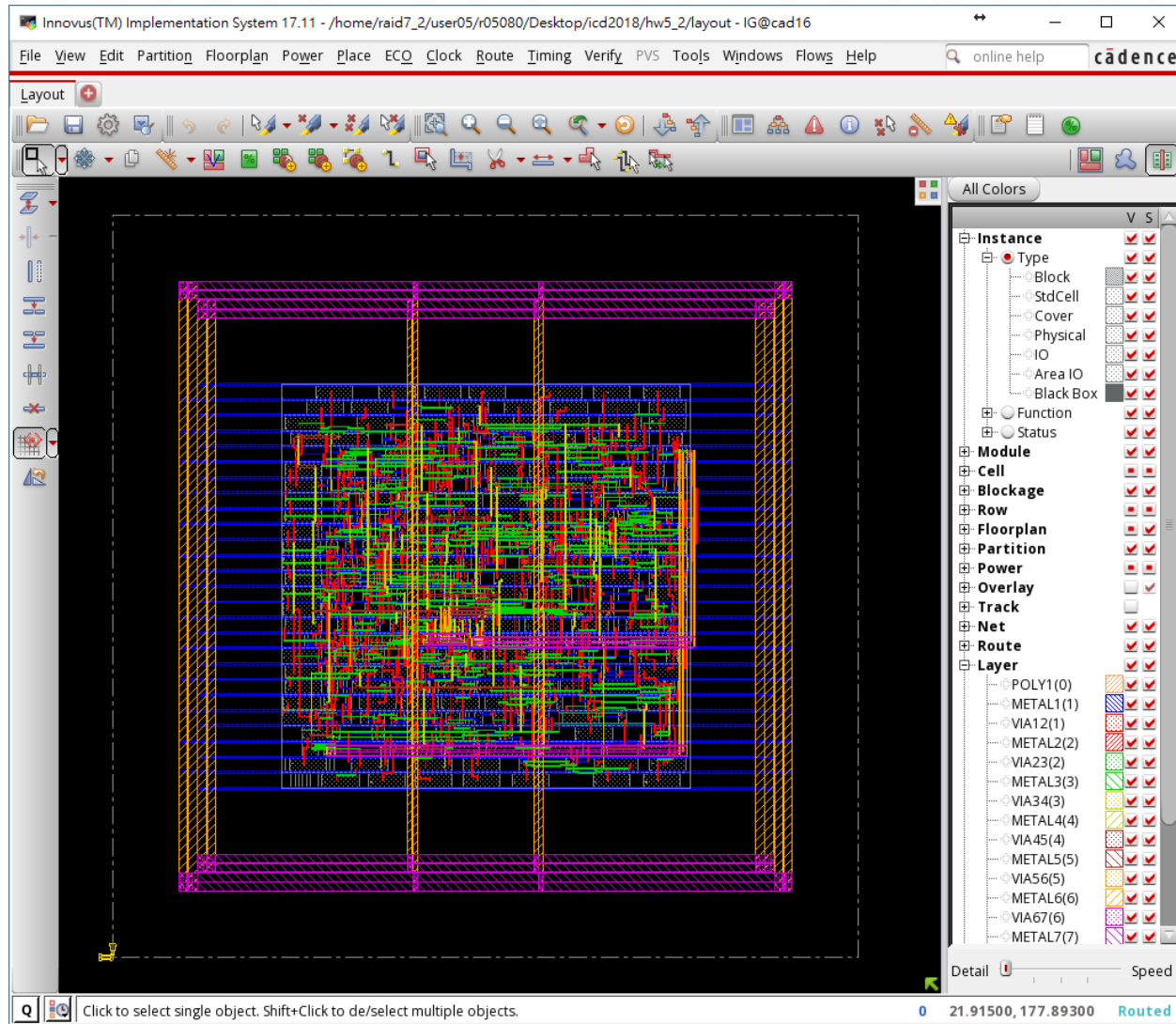
Post route Timing Analysis

▪ **在terminal輸入指令**

- $ setAnalysisMode -analysisType onChipVariation

▪ **Timing → Report Timing**

- Design Stage 選 Post-Route，Analysis Type: <u>Setup</u>，OK

- 若 WNS 為負的則：

  - Optimize → Optimize Design，Design Stage選Post-route，加選Max Fanout，OK。一直重覆到WNS為正的為止

- Design Stage 選 Post-Route，Analysis Type: <u>Hold</u>，OK

Lab for Data Processing System

DRC Check

- **Verify → Verify Geometry，按OK**

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Finish

- **Generate files for post-sim**
  - File→Save →Netlist…
    - Netlist File 填 IG_APR.v，OK
    - Timing→Write SDF
      - » 取消 Ideal Clock，SDF Output File 填 IG_APR.sdf，OK
- **Generate area report**
  - File→Report→Summary…
    - 選 Text Only，檔名為 summaryReport.rpt，OK
      - » 通常會以 Total area of Core

Finish

- **Stream out GDS**

  - Tool → Set Mode → Mode Setup

    - 左欄選StreamOut，取消Virtual Connection，OK

  - File →Save →GDS/OASIS

    - Output File填入IG_APR.gds

    - Map File填入 ../library/streamOut.map

    - 勾選Merge File，填入 ../library/gds/tpz013g3_v1.1.gds 和 ../library/gds/tsmc13gfsg_fram.gds (兩個檔案用空格隔開)

    - 勾選Write abstract information for LEF Macros，Unit: 1000

    - OK

- **關閉Innovus**

Post-layout simulation

- **Check your APR Verilog netlist (2 way)**

  - $ ncverilog -f run_apr.f

    +ncmaxdelays testfixture_APR.v layout/IG_APR.v -v syn/tsmc13_neg.v +define+SDF

  - 如果模擬沒過，可以慢慢提高testbench中的cycle time，直到通過為止

```
Warning!  Timing violation
          $setuphold<setup>( posedge CLK:12 NS, posedge CEN:11960 PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IROM.v, line = 326
          Scope: test.IROM_1.irom_1
           Time: 12 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:12 NS, posedge WEN:11452 PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 419
          Scope: test.IRB_1
           Time: 12 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:12 NS, negedge A[5]:11552 PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 432
          Scope: test.IRB_1
           Time: 12 NS

All data have been generated successfully!

------------------PASS------------------

Simulation complete via $finish(1) at time 1447683 PS + 0
./testfixture.v:137            #10 $finish;
ncsim> exit
[d05006@wolverine ICD]$ ncverilog testfixture.v ../exercise/layout/LCD_CTRL_APR.v -v ../exercise/syn/tsmc13_neg.v +define+SDF+tb2 +ncmaxdelays
```

Lab for Data Processing System

Some common questions

- **Clock cycle in transistor level simulation should be consistent with synthesis and layout step**

- **Remember to select APR.sdf/.v file instead of syn.sdf/.v file when performing transistor level simulation**

- **You should redo the synthesis process if you want to relax the timing constraint**

- **What can I do when simulation fail?**

  - Make sure all the Verilog and SDF file, relative path and linking are correct

  - Relax the timing constraint and repeat synthesis and layout

  - You may try 2x constraint cycle time when simulating

  - Open nWave and debug

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