hw1 report

b06901063 電機二 黃士豪

一、 RTL-Level 模擬結果

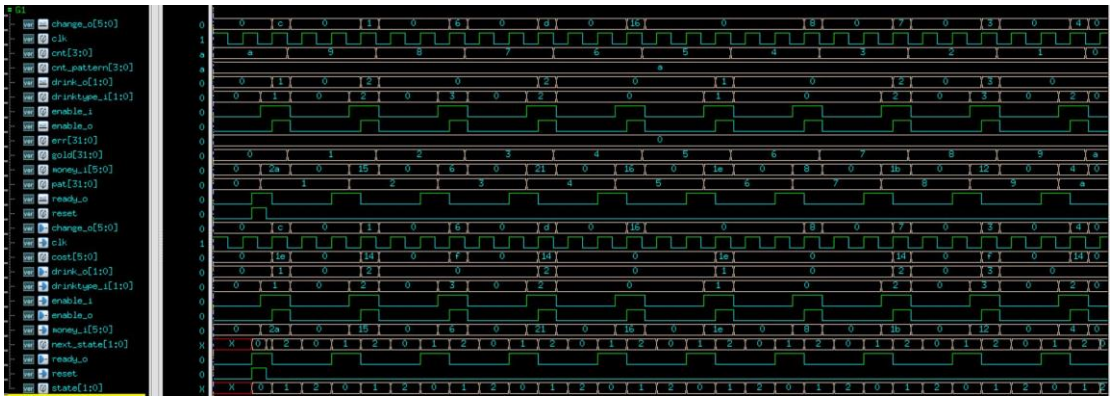
1. testbench1

```
================ 2014 Spring ICD HW4 - Automatic Selling Machine ================
 At    25 NS Correct! The change, type should be:   5, 01 Your:   5, 01


                  ****************************
                  **                        **       /|__/|
                  **  Congratulations !!    **      / 0,0  |
                  **                        **    /_____   |
                  **  You pass this test!!  **   /^ ^ ^ \  |
                  **                        **  |^ ^ ^ ^ |w|
                  ****************************   \m___m__|_|


Simulation complete via $finish(1) at time 35 NS + 0
./testbench1.v:144        $finish;
ncsim> exit
```

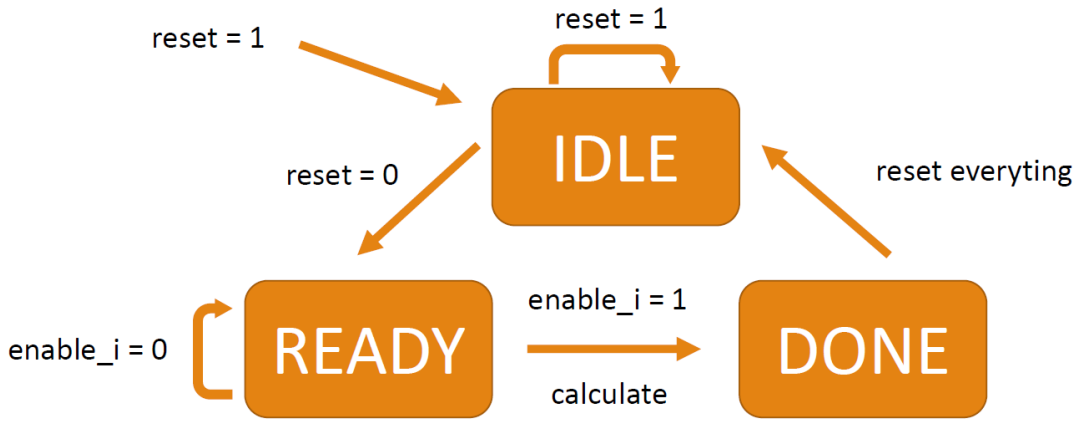
2. testbench2

```
================ 2014 Spring ICD HW4 - Automatic Selling Machine ================
 At     9 NS Correct! The change, type should be:  12, 01 Your:  12, 01
 At    15 NS Correct! The change, type should be:   1, 10 Your:   1, 10
 At    21 NS Correct! The change, type should be:   6, 00 Your:   6, 00
 At    27 NS Correct! The change, type should be:  13, 10 Your:  13, 10
 At    33 NS Correct! The change, type should be:  22, 00 Your:  22, 00
 At    39 NS Correct! The change, type should be:   0, 01 Your:   0, 01
 At    45 NS Correct! The change, type should be:   8, 00 Your:   8, 00
 At    51 NS Correct! The change, type should be:   7, 10 Your:   7, 10
 At    57 NS Correct! The change, type should be:   3, 11 Your:   3, 11
 At    63 NS Correct! The change, type should be:   4, 00 Your:   4, 00


                  ****************************
                  **                        **       /|__/|
                  **  Congratulations !!    **      / 0,0  |
                  **                        **    /_____   |
                  **  You pass this test!!  **   /^ ^ ^ \  |
                  **                        **  |^ ^ ^ ^ |w|
                  ****************************   \m___m__|_|


Simulation complete via $finish(1) at time 65 NS + 0
./testbench2.v:140        $finish;
ncsim> exit
```

3. 波形圖



二、 Finite State Machine 設計圖與設計理念



當 reset 被設成 1 時 machine 開始運作，進入 state ILDE，在 reset 回歸 0 之前都仍然維持在 IDLE。當 reset 變成 0 之後進入 state READY，並在吃到 enable_i=1 之後開始計算，進入 state DONE 進行歸零，最後回到 state IDLE。