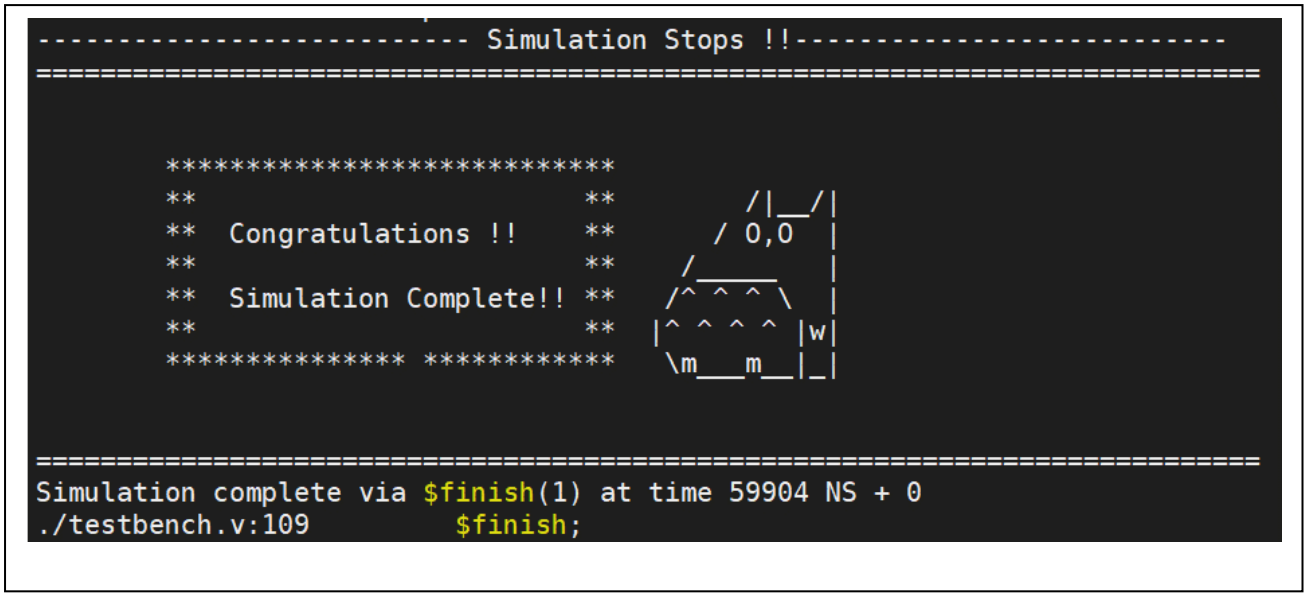
2020 Fall Verilog Project

HW1 Counting the Number of Vertex Covers by Circle Graph

Verilog - RTL and Synthesis Report

Student ID	B07901021	Name	潘世軒
Testbench(RTL)	Pass		
Testbench(Syn)	Pass		
Clock Cycle(Syn)	6(ns)		
Cell Area(Syn)	4778.180988		
Total Time(Syn)	59904(ns)		
Area*Time(Syn)	286232152.905152		

Synthesis Result (截圖)



Timing Report

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****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : SET
Version: N-2017.09-SP2
Date   : Tue Nov 24 23:13:24 2020
****************************************

Operating Conditions: slow     Library: slow
Wire Load Model Mode: top

  Startpoint: i_reg[1] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: candidate_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  SET                tsmc13_wl10           slow

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              1.00       1.00
  i_reg[1]/CK (DFFRX1)                     0.00       1.00 r
  i_reg[1]/QN (DFFRX1)                     0.64       1.64 r
  U205/CO (ADDFX2)                         0.37       2.01 r
  U148/CO (ADDFXL)                         0.28       2.29 r
  U150/S (ADDFXL)                          0.62       2.91 r
```

U180/Y (CLKINVX1)	0.22	3.13 f
U320/Y (NOR2X1)	0.18	3.31 r
mult_pow_129/U5/CO (ADDFXL)	0.52	3.83 r
mult_pow_129/U4/S (ADDFXL)	0.37	4.20 r
U155/S (ADDFXL)	0.59	4.80 f
U348/Y (OAI222XL)	0.59	5.39 r
U349/Y (OAI222XL)	0.25	5.63 f
U350/Y (OA21XL)	0.22	5.85 f
U351/Y (AOI211X1)	0.21	6.06 r
U195/Y (CLKINVX1)	0.11	6.18 f
U144/Y (OAI31X1)	0.20	6.38 r
U167/Y (AND2X2)	0.32	6.70 r
U203/Y (AO22X1)	0.19	6.89 r
candidate_reg[0]/D (DFFRX1)	0.00	6.89 r
data arrival time		6.89
clock clk (rise edge)	10.00	10.00
clock network delay (ideal)	1.00	11.00
clock uncertainty	-0.10	10.90
candidate_reg[0]/CK (DFFRX1)	0.00	10.90 r
library setup time	-0.12	10.78
data required time		10.78
---		
data required time		10.78
data arrival time		-6.89
---		
slack (MET)		3.89

Area Report

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****************************************
Report : area
Design : SET
Version: N-2017.09-SP2
Date   : Tue Nov 24 23:12:56 2020
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          121
Number of nets:                           493
Number of cells:                          342
Number of combinational cells:            284
Number of sequential cells:               53
Number of macros/black boxes:             0
Number of buf/inv:                        50
Number of references:                     53

Combinational area:            3262.402839
Buf/Inv area:                   191.806197
Noncombinational area:         1515.778149
Macro/Black Box area:             0.000000
Net Interconnect area:        40833.536591

Total cell area:               4778.180988
Total area:                   45611.717579
```

Power Report

```
Loading db file '/home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
            -analysis_effort low
Design : SET
Version: N-2017.09-SP2
Date   : Tue Nov 24 23:13:11 2020
****************************************


Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design             Wire Load Model                Library
------------------------------------------------
SET                            tsmc13_wl10          slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

Cell Internal Power = 160.2389 uW (74%)
Net Switching Power = 57.6749 uW (26%)

Total Dynamic Power = 217.9139 uW (100%)

Cell Leakage Power = 1.2658 uW

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)
register	0.1336	7.5533e-03	4.1246e+05	0.1415	(64.57%)
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)
combinational	2.6670e-02	5.0122e-02	8.5334e+05	7.7645e-02	(35.43%)
Total	0.1602 mW	5.7675e-02 mW	1.2658e+06 pW	0.2192 mW	