#### 2020 Fall Verilog Project

## **HW1** Counting the Number of Vertex Covers by Circle Graph

## Verilog - RTL and Synthesis Report

Student ID	B07901021	Name	潘世軒	
Testbench(RTL)	Pass			
Testbench(Syn)	Pass			
Clock Cycle(Syn)	6(ns)			
Cell Area(Syn)	4778.180988			
Total Time(Syn)	59904(ns)			
Area*Time(Syn)	286232152.905152			

#### Synthesis Result (截圖)

# **Timing Report**

*******	*******	****	
Report : timing			
-path full			
-delay max	<b>(</b>		
-max_path	is 1		
-sort_by g	roup		
Design : SET			
Version: N-2017.09-			
	4 23:13:24 2020		
******	*******	****	
Operating Condition	or closer Library of Service		
_	s: slow Library: slow		
Wire Load Model M	ode. top		
Startpoint: i_reg[^	1] (rising edge-triggered	flin-flon clocke	ed by clk)
Endpoint: candida		mp nop oloom	ou by only
•	g edge-triggered flip-flo	p clocked by cl	k)
Path Group: clk	,		•
Path Type: max			
Des/Clust/Port	Wire Load Model	Library	
SET	tsmc13_wl10	slow	
Point		Incr	Path
clock clk (rise edge)			0.00
clock clk (rise edg	e)	0.00	0.00
clock clk (rise edg clock network del		0.00 1.00	1.00
	ay (ideal)		
clock network del	ay (ideal) X1)	1.00	1.00
clock network del i_reg[1]/CK (DFFR	ay (ideal) X1) RX1)	1.00 0.00	1.00 1.00 r
clock network del i_reg[1]/CK (DFFR i_reg[1]/QN (DFFF	ay (ideal) X1) RX1) 2)	1.00 0.00 0.64	1.00 1.00 r 1.64 r

U180/Y (CLKINVX1)       0.22       3.13 f         U320/Y (NOR2X1)       0.18       3.31 r         mult_pow_129/U5/CO (ADDFXL)       0.52       3.83 r         mult_pow_129/U4/S (ADDFXL)       0.37       4.20 r         U155/S (ADDFXL)       0.59       4.80 f         U348/Y (OAI222XL)       0.59       5.39 r         U349/Y (OAI222XL)       0.25       5.63 f         U350/Y (OA21XL)       0.22       5.85 f         U351/Y (AOI21X1)       0.21       6.06 r         U195/Y (CLKINVX1)       0.11       6.18 f         U144/Y (OAI31X1)       0.20       6.38 r         U167/Y (AND2X2)       0.32       6.70 r         U203/Y (AO22X1)       0.19       6.89 r         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90 r         clock uncertainty       -0.10       10.78         data required time       -0.12       10.78         data required time       10.78         data arrival time       -6.89			
mult_pow_129/U5/CO (ADDFXL) 0.52 3.83 r mult_pow_129/U4/S (ADDFXL) 0.37 4.20 r U155/S (ADDFXL) 0.59 4.80 f U348/Y (OAI222XL) 0.59 5.39 r U349/Y (OAI222XL) 0.25 5.63 f U350/Y (OA21XL) 0.22 5.85 f U351/Y (AOI211X1) 0.21 6.06 r U195/Y (CLKINVX1) 0.11 6.18 f U144/Y (OAI31X1) 0.20 6.38 r U167/Y (AND2X2) 0.32 6.70 r U203/Y (AO22X1) 0.19 6.89 r candidate_reg[0]/D (DFFRX1) 0.00 6.89 r data arrival time 6.89  clock clk (rise edge) 10.00 10.00 clock uncertainty -0.10 10.90 clock uncertainty -0.10 10.90 r clibrary setup time -0.12 10.78 data required time 10.78	J180/Y (CLKINVX1)	0.22	3.13 f
mult_pow_129/U4/S (ADDFXL)       0.37       4.20 r         U155/S (ADDFXL)       0.59       4.80 f         U348/Y (OAI222XL)       0.59       5.39 r         U349/Y (OAI222XL)       0.25       5.63 f         U350/Y (OA21XL)       0.22       5.85 f         U351/Y (AOI211X1)       0.21       6.06 r         U195/Y (CLKINVX1)       0.11       6.18 f         U144/Y (OAI31X1)       0.20       6.38 r         U167/Y (AND2X2)       0.32       6.70 r         U203/Y (AO22X1)       0.19       6.89 r         candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       10.90         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78	J320/Y (NOR2X1)	0.18	3.31 r
U155/S (ADDFXL)  U348/Y (OAI222XL)  U349/Y (OAI222XL)  U350/Y (OA21XL)  U350/Y (OA21XL)  U351/Y (AOI211X1)  U195/Y (CLKINVX1)  U1144/Y (OAI31X1)  U167/Y (AND2X2)  U203/Y (AO22X1)  candidate_reg[0]/D (DFFRX1)  data arrival time  Clock clk (rise edge)  clock network delay (ideal)  clock uncertainty  candidate_reg[0]/CK (DFFRX1)  data required time  10.78  data required time  10.78	nult_pow_129/U5/CO (ADDFXL)	0.52	3.83 r
U348/Y (OAI222XL) U349/Y (OAI222XL) U350/Y (OA21XL) U350/Y (OA21XL) U351/Y (AOI211X1) U195/Y (CLKINVX1) U1144/Y (OAI31X1) U167/Y (AND2X2) U203/Y (AO22X1) Candidate_reg[0]/D (DFFRX1) Clock clk (rise edge) Clock clk (rise edge) Clock network delay (ideal) Clock uncertainty Candidate_reg[0]/CK (DFFRX1) Clock uncertainty Candidate_reg[0]/CK (DFFRX1) Clock uncertainty Clock	nult_pow_129/U4/S (ADDFXL)	0.37	4.20 r
U349/Y (OAI222XL) U350/Y (OA21XL) U350/Y (OA21XL) U351/Y (AOI211X1) U195/Y (CLKINVX1) U144/Y (OAI31X1) U167/Y (AND2X2) U203/Y (AO22X1) Candidate_reg[0]/D (DFFRX1) Odata arrival time  Clock clk (rise edge) Clock network delay (ideal) Clock uncertainty Candidate_reg[0]/CK (DFFRX1) U100 Clock uncertainty Candidate_reg[0]/CK (DFFRX1) U100 Clock uncertainty U1000 Clock uncertainty U1000 Clock uncertainty U100 Clock uncertainty U100 Clock	J155/S (ADDFXL)	0.59	4.80 f
U350/Y (OA21XL)  U351/Y (AOI211X1)  U195/Y (CLKINVX1)  U144/Y (OAI31X1)  U167/Y (AND2X2)  U203/Y (AO22X1)  candidate_reg[0]/D (DFFRX1)  data arrival time  0.89  clock clk (rise edge)  clock network delay (ideal)  clock uncertainty  candidate_reg[0]/CK (DFFRX1)  0.00  10.00  10.00  clock uncertainty  -0.10  10.90  candidate_reg[0]/CK (DFFRX1)  0.00  10.90  clock uncertainty  -0.12  10.78  data required time  10.78	J348/Y (OAI222XL)	0.59	5.39 r
U351/Y (AOI211X1)  U195/Y (CLKINVX1)  U105/Y (CLKINVX1)  U167/Y (AND2X2)  U203/Y (AO22X1)  Candidate_reg[0]/D (DFFRX1)  data arrival time  Clock clk (rise edge)  clock network delay (ideal)  clock uncertainty  candidate_reg[0]/CK (DFFRX1)  D.00  D.00  D.00  Clock uncertainty  Cl	J349/Y (OAI222XL)	0.25	5.63 f
U195/Y (CLKINVX1)       0.11       6.18 f         U144/Y (OAI31X1)       0.20       6.38 r         U167/Y (AND2X2)       0.32       6.70 r         U203/Y (AO22X1)       0.19       6.89 r         candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J350/Y (OA21XL)	0.22	5.85 f
U144/Y (OAI31X1)       0.20       6.38 r         U167/Y (AND2X2)       0.32       6.70 r         U203/Y (AO22X1)       0.19       6.89 r         candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J351/Y (AOI211X1)	0.21	6.06 r
U167/Y (AND2X2)       0.32       6.70 r         U203/Y (AO22X1)       0.19       6.89 r         candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J195/Y (CLKINVX1)	0.11	6.18 f
U203/Y (AO22X1)       0.19       6.89 r         candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J144/Y (OAI31X1)	0.20	6.38 r
candidate_reg[0]/D (DFFRX1)       0.00       6.89 r         data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J167/Y (AND2X2)	0.32	6.70 r
data arrival time       6.89         clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	J203/Y (AO22X1)	0.19	6.89 r
clock clk (rise edge)       10.00       10.00         clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	candidate_reg[0]/D (DFFRX1)	0.00	6.89 r
clock network delay (ideal)       1.00       11.00         clock uncertainty       -0.10       10.90         candidate_reg[0]/CK (DFFRX1)       0.00       10.90 r         library setup time       -0.12       10.78         data required time       10.78         data required time       10.78	data arrival time		6.89
clock uncertainty         -0.10         10.90           candidate_reg[0]/CK (DFFRX1)         0.00         10.90 r           library setup time         -0.12         10.78           data required time         10.78           data required time         10.78	clock clk (rise edge)	10.00	10.00
candidate_reg[0]/CK (DFFRX1) 0.00 10.90 r library setup time -0.12 10.78 data required time 10.78 data required time 10.78	clock network delay (ideal)	1.00	11.00
library setup time -0.12 10.78 data required time 10.78 data required time 10.78	clock uncertainty	-0.10	10.90
data required time 10.78  data required time 10.78	candidate_reg[0]/CK (DFFRX1)	0.00	10.90 r
data required time 10.78	ibrary setup time	-0.12	10.78
·	data required time		10.78
data arrival time -6.89	data required time		10.78
	data arrival time		-6.89
slack (MET) 3.89	slack (MET)		3.89

#### **Area Report**

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Report : area Design : SET

Version: N-2017.09-SP2

Date : Tue Nov 24 23:12:56 2020

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Information: Updating design information... (UID-85)

Library(s) Used:

typical (File: /home/raid7\_2/course/cvsd/CBDK\_IC\_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports: 121

Number of nets: 493

Number of cells: 342

Number of combinational cells: 284

Number of sequential cells: 53

Number of macros/black boxes: 0

Number of buf/inv: 50

Number of references: 53

Combinational area: 3262.402839

Buf/Inv area: 191.806197

Noncombinational area: 1515.778149

Macro/Black Box area: 0.000000

Net Interconnect area: 40833.536591

Total cell area: 4778.180988

Total area: 45611.717579

## **Power Report**

Loading db file '/home/raid7 2/course/cvsd/CBDK IC Contest/CIC/SynopsysDC/db/typical.db' Information: Propagating switching activity (low effort zero delay simulation). (PWR-6) Warning: Design has unannotated primary inputs. (PWR-414) Warning: Design has unannotated sequential cell outputs. (PWR-415) \*\*\*\*\*\*\*\*\*\* Report: power -analysis\_effort low Design: SET Version: N-2017.09-SP2 Date : Tue Nov 24 23:13:11 2020 \*\*\*\*\*\*\*\*\*\*\* Library(s) Used: typical (File: /home/raid7 2/course/cvsd/CBDK IC Contest/CIC/SynopsysDC/db/typical.db) Operating Conditions: slow Library: slow Wire Load Model Mode: top Design Wire Load Model Library tsmc13 wl10 slow SET Global Operating Voltage = 1.08 Power-specific unit information: Voltage Units = 1V Capacitance Units = 1.000000pf Time Units = 1ns Dynamic Power Units = 1mW (derived from V,C,T units) Leakage Power Units = 1pW

Cell Internal Power = 160.2389 uW (74%)

Net Switching Power = 57.6749 uW (26%)

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Total Dynamic Power = 217.9139 uW (100%)

Cell Leakage Power = 1.2658 uW

	Internal	Switching	Leakage	Total
Power Group	Power	Power	Power	Power
( % ) A	attrs			
io_pad	0.0000	0.0000	0.0000	0.0000
( 0.00%)				
memory	0.0000	0.0000	0.0000	0.0000
( 0.00%)				
black_box	0.0000	0.0000	0.0000	0.0000
( 0.00%)				
clock_network	0.0000	0.0000	0.0000	0.0000
( 0.00%)				
register	0.1336	7.5533e-03	4.1246e+05	0.1415
( 64.57%)				
sequential	0.0000	0.0000	0.0000	0.0000
( 0.00%)				
combinational	2.6670e-02	5.0122e-02	8.5334e+05	7.7645e-02
( 35.43%)				
Total	0.1602 mW	5.7675e-02 mW	1.2658e+06 pW	0.2192 mW