# SMDK2450 Evaluation Board for S3C2450X

| 1. PCB Revision | Date | Description |
|---|---|---|
| Rev 0.0 | 2007. 11. 22 | Preliminary Version |

## 2. Table of Contents

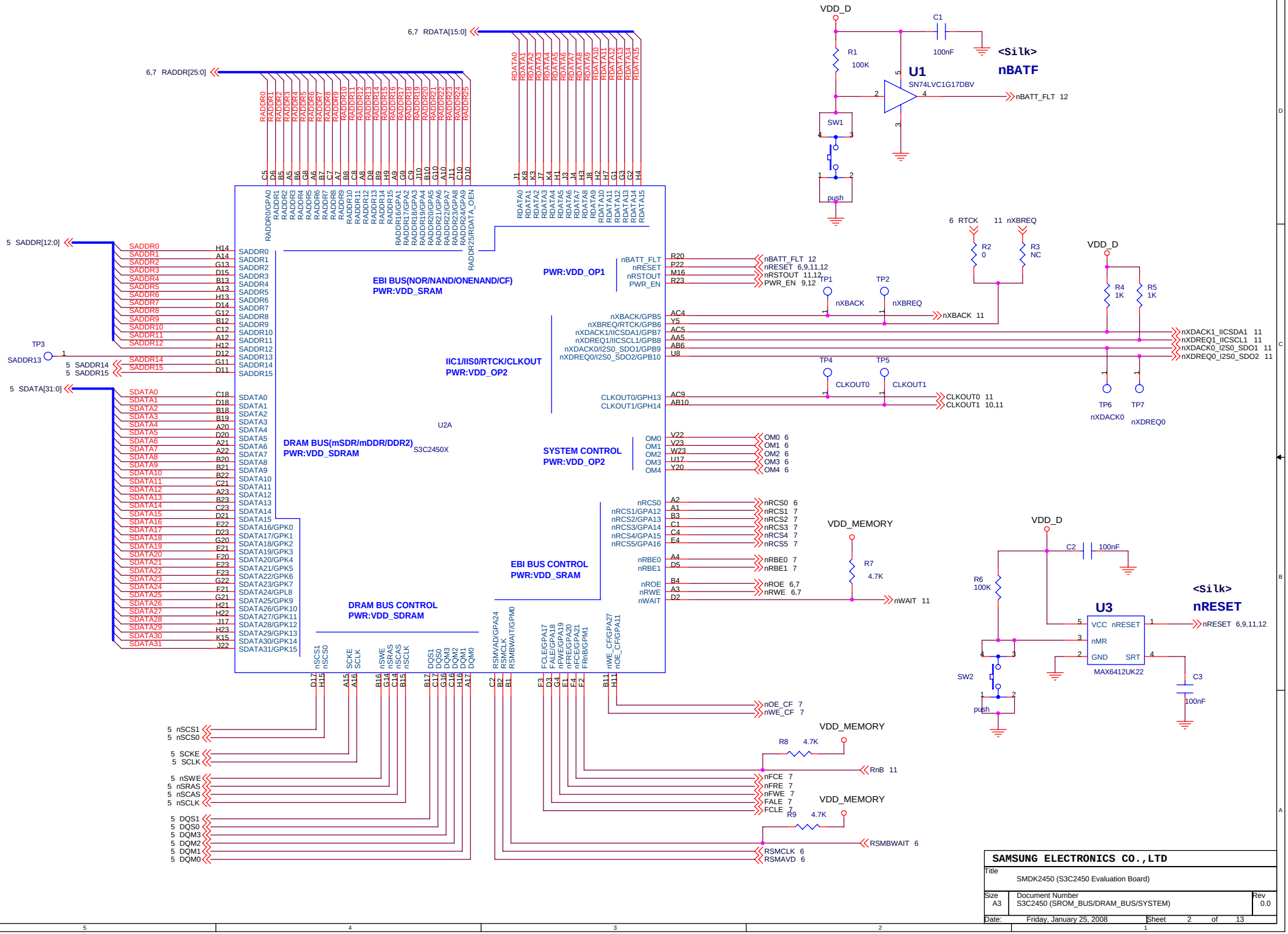


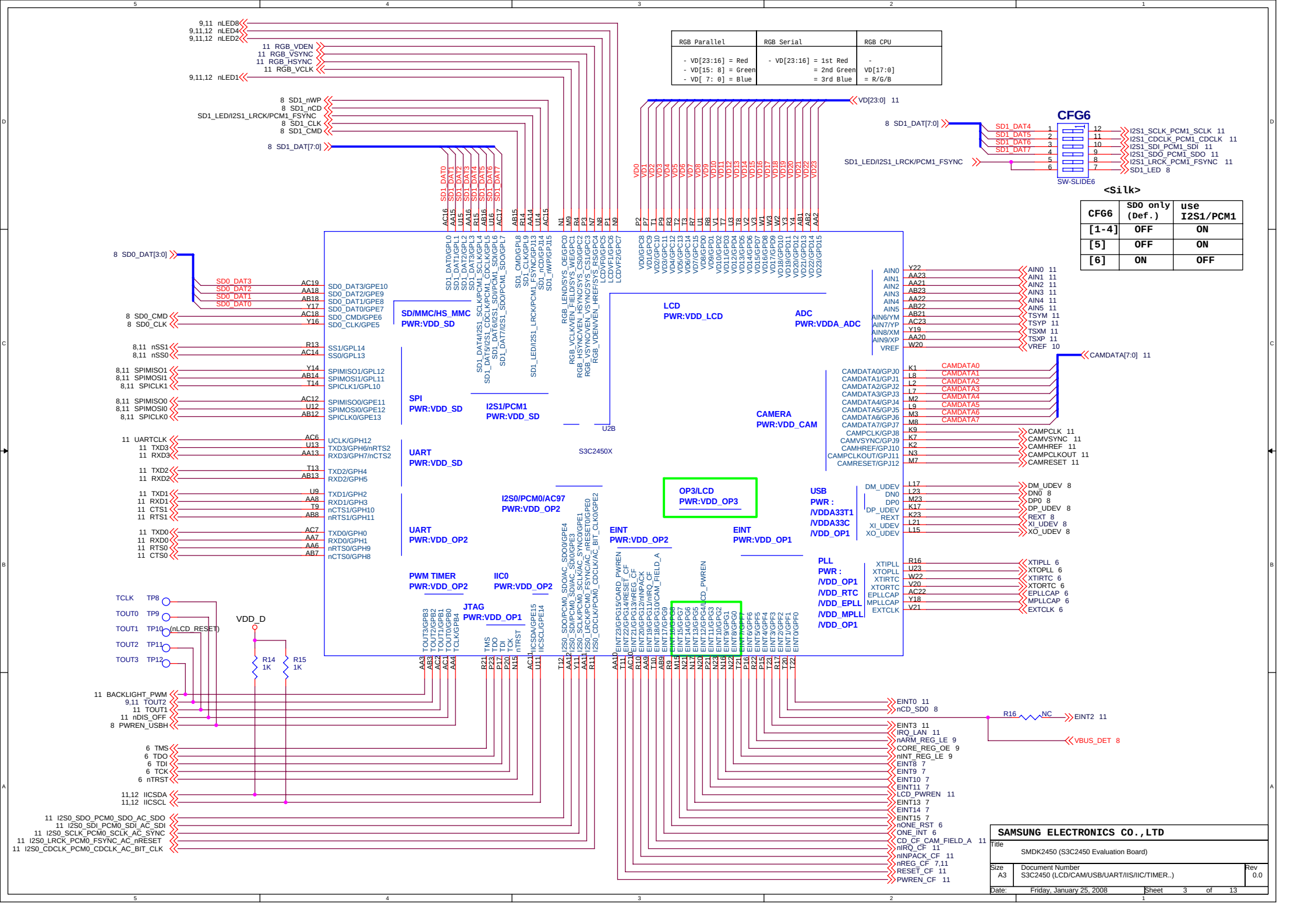
## 3. Part Reference

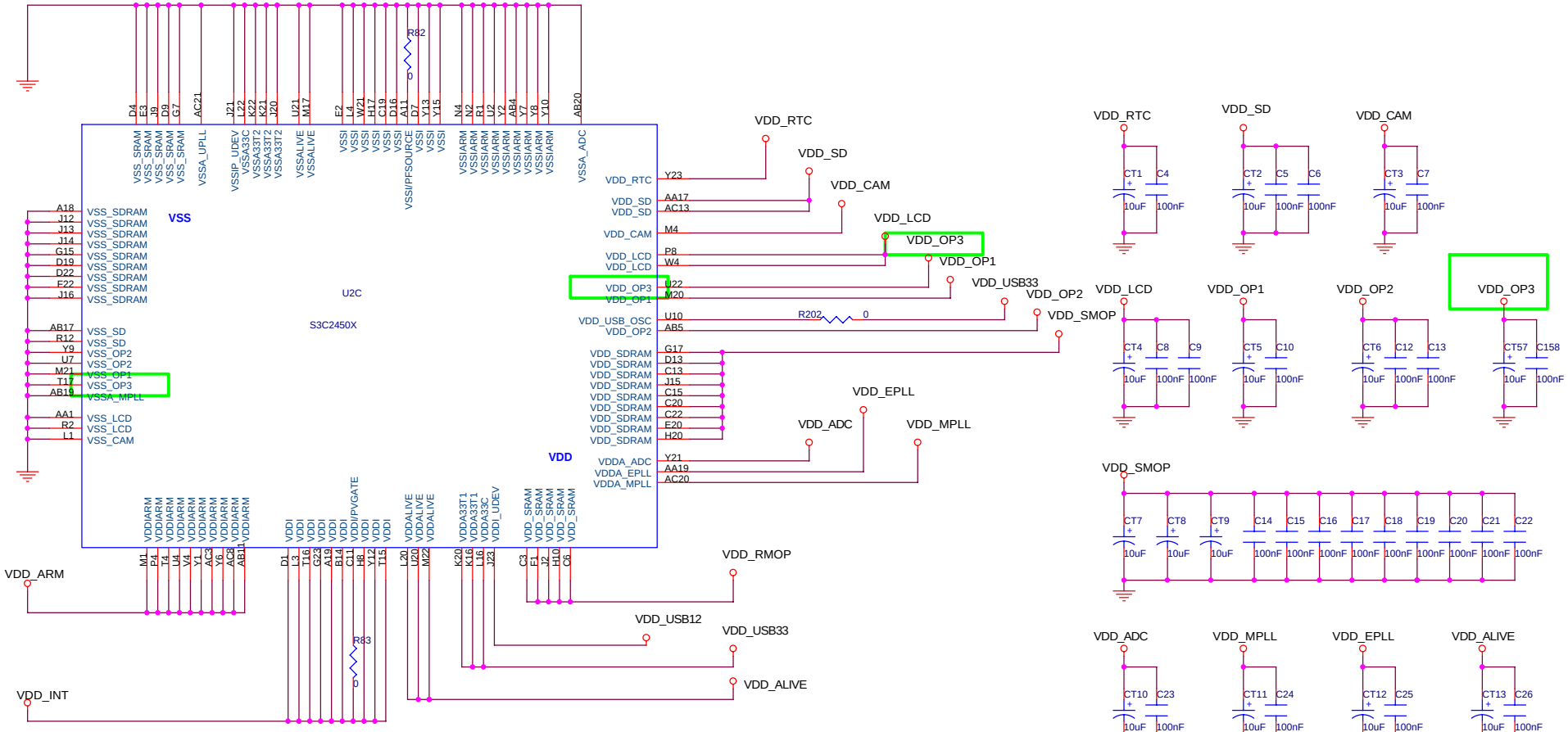
<Component><Number>

- U - COMPONENT IC & REGURATOR IC
- C - CAPACITOR
- CT- TANTAL CAPACITOR
- R - RESISTER
- RP - RESISTOR PACK
- VR - VARIABLE RESISTER
- J - JUMPER
- L - INDUCTOR
- F - FERRITE BEAD
- Y - OSCILLATOR
- X - CRYSTAL
- Q - TRANSISTOR/FET
- D - DIODE
- SW - TACT/PUSH SWITCH
- CON - CONNECTOR
- CFG - DIP SWITCH

| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: TITLE BLOCK | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 1 of 13 | |


6,7 RDATA[15:0]
6,7 RADDR[25:0]
5 SADDR[12:0]
5 SDATA[31:0]
EBI BUS(NOR/NAND/ONENAND/CF)
PWR:VDD_SRAM
PWR:VDD_OP1
IIC1/IIS0/RTCK/CLKOUT
PWR:VDD_OP2
U2A
S3C2450X
DRAM BUS(mSDR/mDDR/DDR2)
PWR:VDD_SDRAM
SYSTEM CONTROL
PWR:VDD_OP2
EBI BUS CONTROL
PWR:VDD_SRAM
DRAM BUS CONTROL
PWR:VDD_SDRAM
VDD_D
VDD_MEMORY
U1
SN74LVC1G17DBV
nBATF
U3
MAX6412UK22
nRESET
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
S3C2450 (SROM_BUS/DRAM_BUS/SYSTEM)
Friday, January 25, 2008


RGB Parallel
- VD[23:16] = Red
- VD[15: 8] = Green
- VD[ 7: 0] = Blue
RGB Serial
- VD[23:16] = 1st Red
= 2nd Green
= 3rd Blue
RGB CPU
- VD[17:0] = R/G/B
CFG6
SW-SLIDE6
<Silk>
CFG6 | SD0 only (Def.) | use I2S1/PCM1
[1-4] | OFF | ON
[5] | OFF | ON
[6] | ON | OFF
SD/MMC/HS_MMC PWR:VDD_SD
SPI PWR:VDD_SD
I2S1/PCM1 PWR:VDD_SD
UART PWR:VDD_SD
I2S0/PCM0/AC97 PWR:VDD_OP2
UART PWR:VDD_OP2
PWM TIMER PWR:VDD_OP2
IIC0 PWR:VDD_OP2
JTAG PWR:VDD_OP1
LCD PWR:VDD_LCD
ADC PWR:VDDA_ADC
CAMERA PWR:VDD_CAM
OP3/LCD PWR:VDD_OP3
USB PWR : /VDDA33T1 /VDDA33C /VDD_OP1
EINT PWR:VDD_OP2
EINT PWR:VDD_OP1
PLL PWR : /VDD_OP1 /VDD_RTC /VDD_EPLL /VDD_MPLL /VDD_OP1
U2B
S3C2450X
VDD_D
R14 1K
R15 1K
R16 NC
SAMSUNG ELECTRONICS CO.,LTD
Title: SMDK2450 (S3C2450 Evaluation Board)
Size: A3
Document Number: S3C2450 (LCD/CAM/USB/UART/IIS/IIC/TIMER..)
Rev: 0.0
Date: Friday, January 25, 2008
Sheet 3 of 13



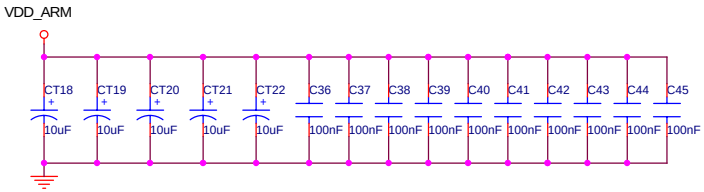


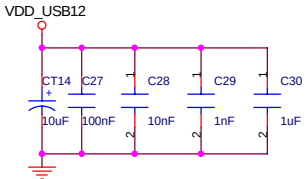


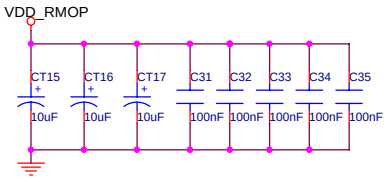


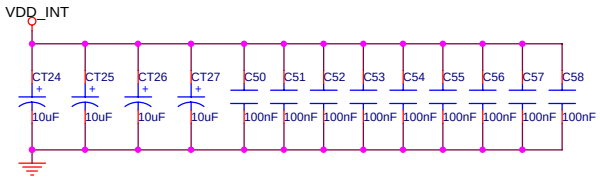


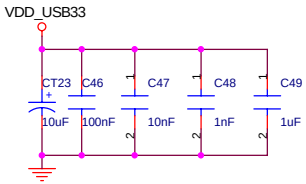




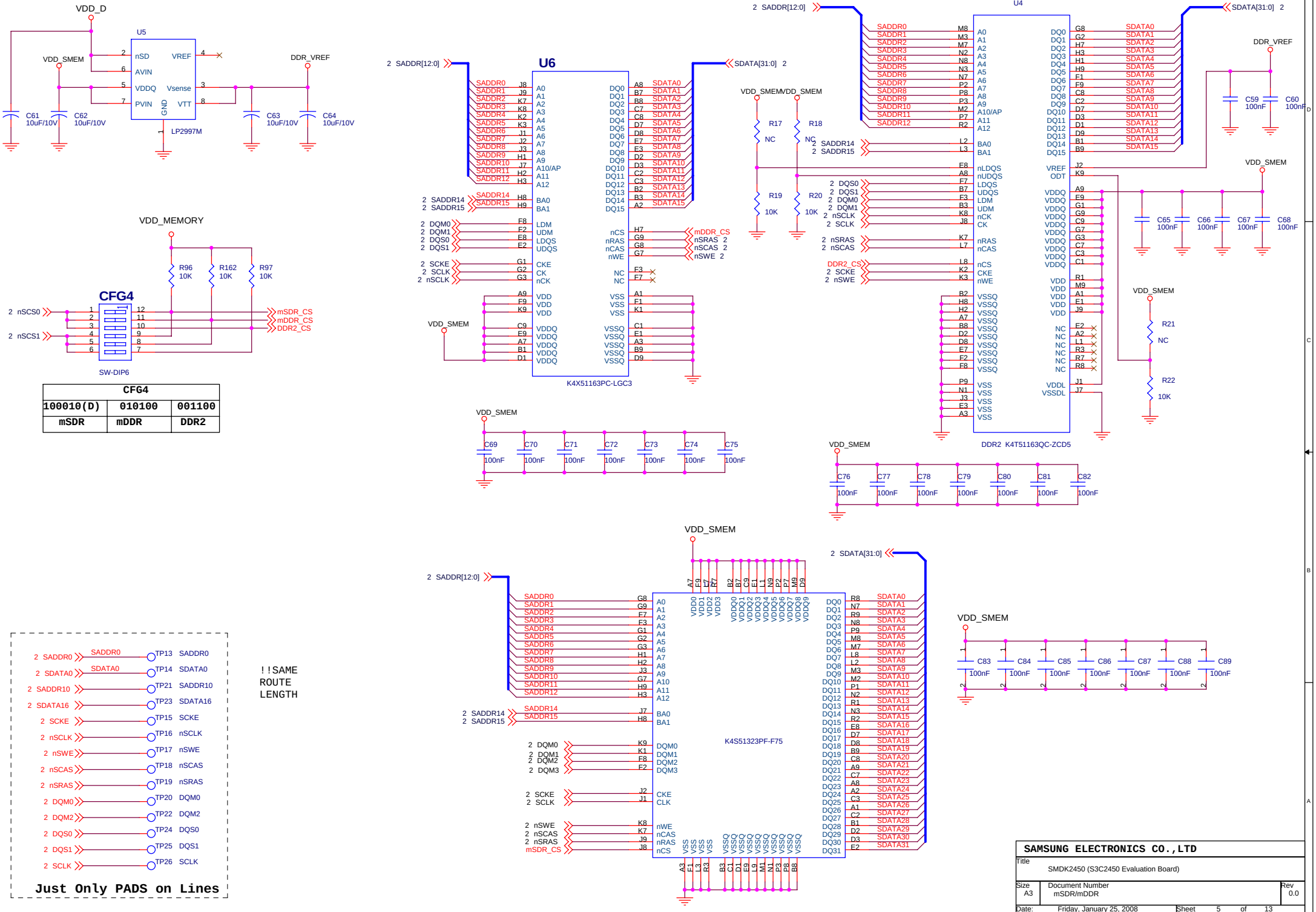




| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: S3C2450 (POWER) | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 4 of 13 | |


VDD_D
U5
VDD_SMEM
DDR_VREF
nSD
AVIN
VDDQ
PVIN
VREF
Vsense
VTT
GND
LP2997M
C61 10uF/10V
C62 10uF/10V
C63 10uF/10V
C64 10uF/10V
VDD_MEMORY
R96 10K
R162 10K
R97 10K
CFG4
2 nSCS0
2 nSCS1
mSDR_CS
mDDR_CS
DDR2_CS
SW-DIP6
CFG4
100010(D) 010100 001100
mSDR mDDR DDR2
U6
2 SADDR[12:0]
SDATA[31:0] 2
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
SADDR14 SADDR15
2 DQM0 2 DQM1 2 DQS0 2 DQS1
2 SCKE 2 SCLK 2 nSCLK
nCS nRAS nCAS nWE
mDDR_CS nSRAS 2 nSCAS 2 nSWE 2
NC NC
VDD VDD VDD
VDDQ VDDQ VDDQ VDDQ VDDQ
VSS VSS VSS
VSSQ VSSQ VSSQ VSSQ VSSQ
VDD_SMEM
K4X51163PC-LGC3
U4
VDD_SMEM/VDD_SMEM
R17 NC
R18 NC
R19 10K
R20 10K
2 SADDR14 2 SADDR15
2 DQS0 2 DQS1 2 DQM0 2 DQM1 2 nSCLK 2 SCLK
2 nSRAS 2 nSCAS
DDR2_CS 2 SCKE 2 nSWE
nLDQS nUDQS LDQS UDQS LDM UDM nCK CK
nRAS nCAS nCS CKE nWE
VSSQ VSS VSSDL
VDDQ VDD VDDL
DDR_VREF
VDD_SMEM
C59 100nF C60 100nF
C65 100nF C66 100nF C67 100nF C68 100nF
R21 NC
R22 10K
DDR2 K4T51163QC-ZCD5
C69 C70 C71 C72 C73 C74 C75 100nF
C76 C77 C78 C79 C80 C81 C82 100nF
VDD_SMEM
2 SADDR[12:0]
2 SDATA[31:0]
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
SADDR14 SADDR15
2 DQM0 2 DQM1 2 DQM2 2 DQM3
2 SCKE 2 SCLK
2 nSWE 2 nSCAS 2 nSRAS mSDR_CS
VDD0 VDD1 VDD2 VDD3
VDDQ0 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9
VSS VSS VSS VSS
VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ
K4S51323PF-F75
C83 C84 C85 C86 C87 C88 C89 100nF
2 SADDR0 SADDR0 TP13 SADDR0
2 SDATA0 SDATA0 TP14 SDATA0
2 SADDR10 TP21 SADDR10
2 SDATA16 TP23 SDATA16
2 SCKE TP15 SCKE
2 nSCLK TP16 nSCLK
2 nSWE TP17 nSWE
2 nSCAS TP18 nSCAS
2 nSRAS TP19 nSRAS
2 DQM0 TP20 DQM0
2 DQM2 TP22 DQM2
2 DQS0 TP24 DQS0
2 DQS1 TP25 DQS1
2 SCLK TP26 SCLK
Just Only PADS on Lines
!!SAME ROUTE LENGTH
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number mSDR/mDDR
Rev 0.0
Date: Friday, January 25, 2008
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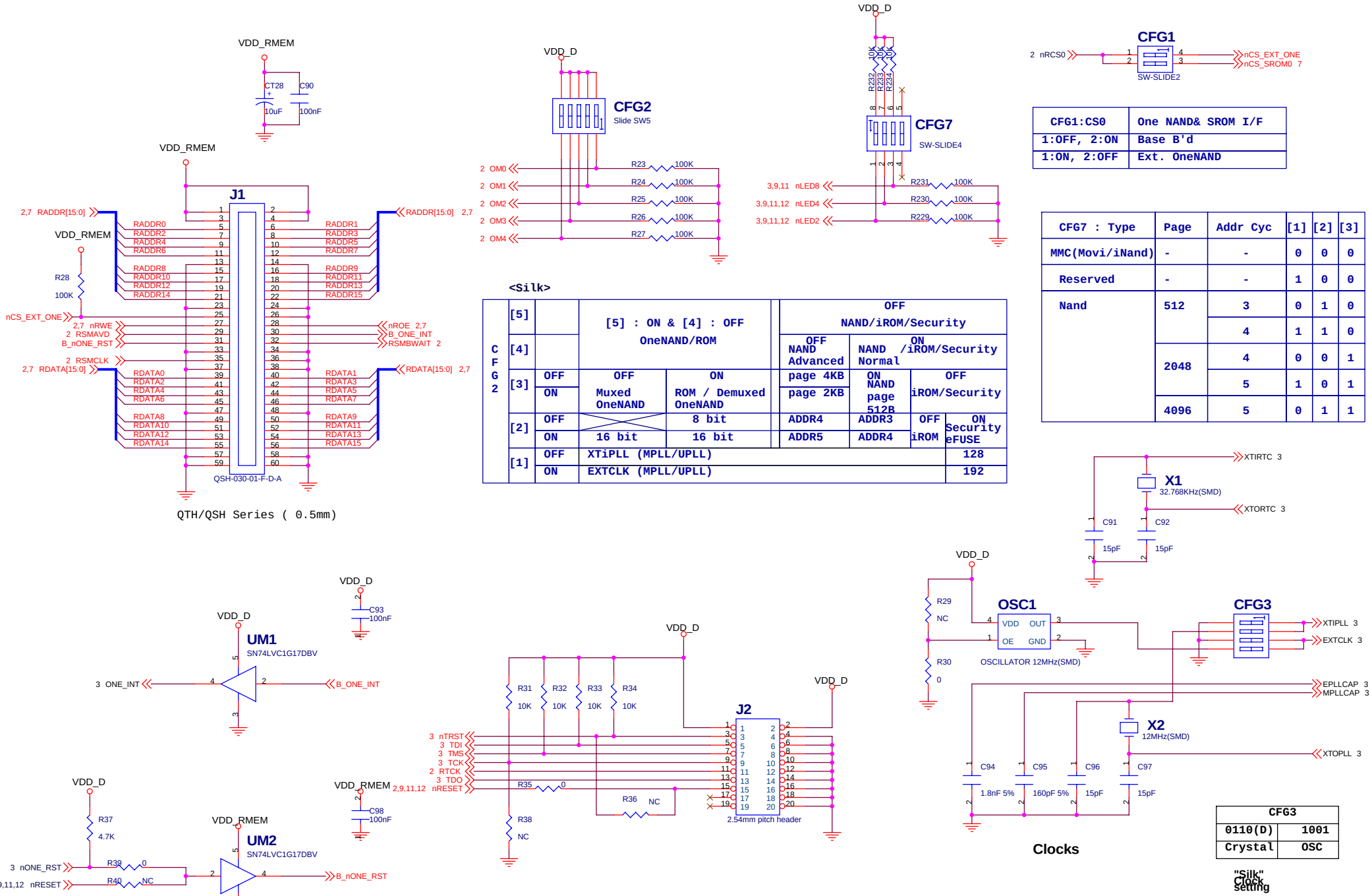
VDD_RMEM
CT28
C90
10uF
100nF
J1
QSH-030-01-F-D-A
QTH/QSH Series ( 0.5mm)
VDD_D
CFG2
Slide SW5
OM0
OM1
OM2
OM3
OM4
R23 100K
R24 100K
R25 100K
R26 100K
R27 100K
CFG7
SW-SLIDE4
nLED8
nLED4
nLED2
R231 100K
R230 100K
R229 100K
CFG1
SW-SLIDE2
nRCS0
nCS_EXT_ONE
nCS_SROM0
<Silk>
CFG2
[5] [4] [3] [2] [1]
[5] : ON & [4] : OFF
OneNAND/ROM
OFF
NAND/iROM/Security
NAND Advanced
NAND Normal
ON
/iROM/Security
Muxed OneNAND
ROM / Demuxed OneNAND
page 4KB
page 2KB
NAND page 512B
iROM/Security
8 bit
16 bit
ADDR4
ADDR5
ADDR3
ADDR4
iROM
Security eFUSE
XTiPLL (MPLL/UPLL)
EXTCLK (MPLL/UPLL)
128
192
CFG1:CS0 | One NAND& SROM I/F
1:OFF, 2:ON | Base B'd
1:ON, 2:OFF | Ext. OneNAND
CFG7 : Type | Page | Addr Cyc | [1] | [2] | [3]
MMC(Movi/iNand) | - | - | 0 | 0 | 0
Reserved | - | - | 1 | 0 | 0
Nand | 512 | 3 | 0 | 1 | 0
4 | 1 | 1 | 0
2048 | 4 | 0 | 0 | 1
5 | 1 | 0 | 1
4096 | 5 | 0 | 1 | 1
UM1
SN74LVC1G17DBV
ONE_INT
B_ONE_INT
UM2
SN74LVC1G17DBV
nONE_RST
B_nONE_RST
nRESET
J2
2.54mm pitch header
nTRST
TDI
TMS
TCK
RTCK
TDO
OSC1
OSCILLATOR 12MHz(SMD)
X1
32.768KHz(SMD)
X2
12MHz(SMD)
XTIRTC
XTORTC
XTIPLL
EXTCLK
XTOPLL
EPLLCAP
MPLLCAP
CFG3
0110(D) 1001
Crystal OSC
Clocks
"Silk" Clock Setting
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number MEMORY(OneNAND)/JTAG/CLK
Rev 0.0
Date: Friday, January 25, 2008
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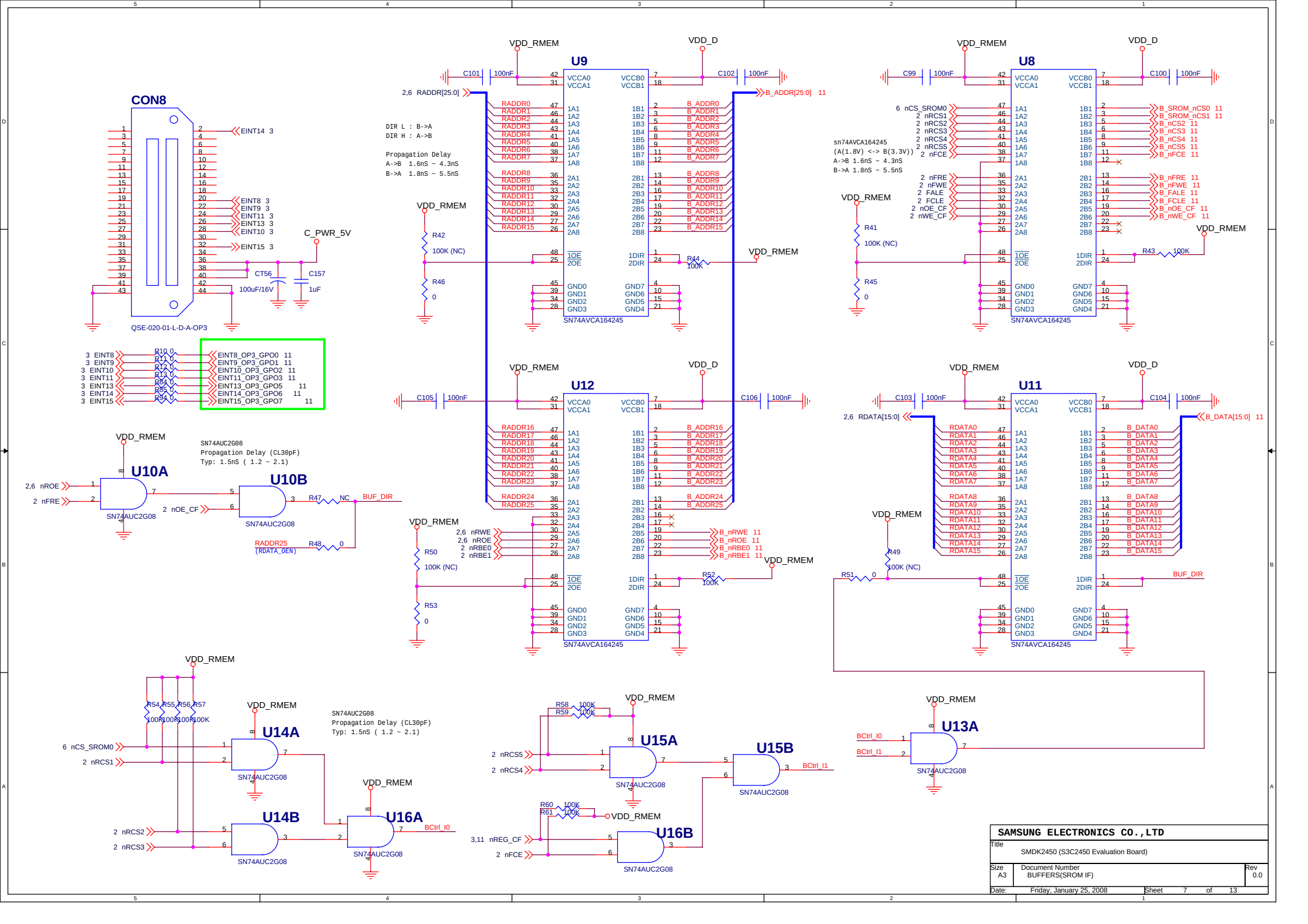
CON8
QSE-020-01-L-D-A-OP3
C_PWR_5V
CT56
100uF/16V
C157
1uF
EINT14 3
EINT8 3
EINT9 3
EINT11 3
EINT13 3
EINT10 3
EINT15 3
R10 0
R11 0
R12 0
R13 0
R84 0
R85 0
R86 0
EINT8_OP3_GPO0 11
EINT9_OP3_GPO1 11
EINT10_OP3_GPO2 11
EINT11_OP3_GPO3 11
EINT13_OP3_GPO5 11
EINT14_OP3_GPO6 11
EINT15_OP3_GPO7 11
U10A
U10B
SN74AUC2G08
SN74AUC2G08
Propagation Delay (CL30pF)
Typ: 1.5nS ( 1.2 ~ 2.1)
2,6 nROE
2 nFRE
2 nOE_CF
R47 NC
BUF_DIR
RADDR25
(RDATA_OEN)
R48 0
U9
U8
U12
U11
SN74AVCA164245
VDD_RMEM
VDD_D
C101 100nF
C102 100nF
C99 100nF
C100 100nF
C105 100nF
C106 100nF
C103 100nF
C104 100nF
2,6 RADDR[25:0]
B_ADDR[25:0] 11
DIR L : B->A
DIR H : A->B
Propagation Delay
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
sn74AVCA164245
(A(1.8V) <-> B(3.3V))
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
6 nCS_SROM0
2 nRCS1
2 nRCS2
2 nRCS3
2 nRCS4
2 nRCS5
2 nFCE
2 nFRE
2 nFWE
2 FALE
2 FCLE
2 nOE_CF
2 nWE_CF
B_SROM_nCS0 11
B_SROM_nCS1 11
B_nCS2 11
B_nCS3 11
B_nCS4 11
B_nCS5 11
B_nFCE 11
B_nFRE 11
B_nFWE 11
B_FALE 11
B_FCLE 11
B_nOE_CF 11
B_nWE_CF 11
R41 100K (NC)
R45 0
R43 100K
R42 100K (NC)
R46 0
R44 100K
R50 100K (NC)
R53 0
R52 100K
2,6 nRWE
2,6 nROE
2 nRBE0
2 nRBE1
B_nRWE 11
B_nROE 11
B_nRBE0 11
B_nRBE1 11
2,6 RDATA[15:0]
B_DATA[15:0] 11
R49 100K (NC)
R51 0
R54 100K
R55 100K
R56 100K
R57 100K
U14A
U14B
U16A
U15A
U15B
U16B
U13A
BCtrl_I0
BCtrl_I1
R58 100K
R59 100K
R60 100K
R61 100K
3,11 nREG_CF
2 nFCE
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number BUFFERS(SROM IF)
Rev 0.0
Date: Friday, January 25, 2008
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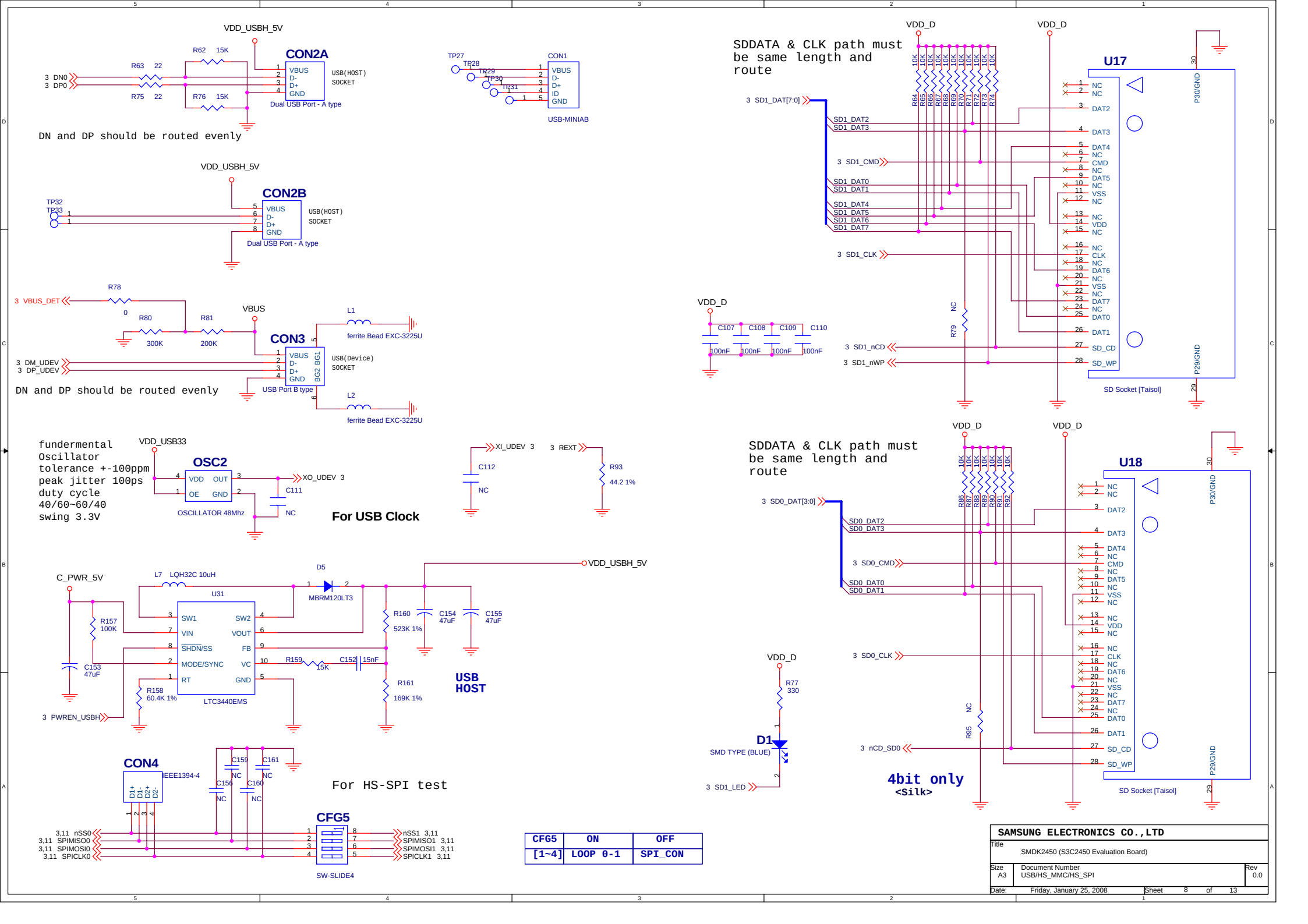
VDD_USBH_5V
R62 15K
R63 22
3 DN0
3 DP0
R75 22
R76 15K
CON2A
VBUS
D-
D+
GND
USB(HOST) SOCKET
Dual USB Port - A type
DN and DP should be routed evenly
TP27
TP28
TP29
TP30
TP31
CON1
VBUS
D-
D+
ID
GND
USB-MINIAB
VDD_USBH_5V
TP32
TP33
CON2B
VBUS
D-
D+
GND
USB(HOST) SOCKET
Dual USB Port - A type
R78
3 VBUS_DET
0
R80
300K
R81
200K
VBUS
CON3
VBUS
D-
D+
GND
BG2 BG1
USB(Device) SOCKET
USB Port B type
L1
ferrite Bead EXC-3225U
L2
ferrite Bead EXC-3225U
3 DM_UDEV
3 DP_UDEV
DN and DP should be routed evenly
SDDATA & CLK path must be same length and route
VDD_D
VDD_D
U17
3 SD1_DAT[7:0]
SD1_DAT2
SD1_DAT3
3 SD1_CMD
SD1_DAT0
SD1_DAT1
SD1_DAT4
SD1_DAT5
SD1_DAT6
SD1_DAT7
3 SD1_CLK
3 SD1_nCD
3 SD1_nWP
R64 10K
R65 10K
R66 10K
R67 10K
R68 10K
R70 10K
R71 10K
R72 10K
R73 10K
R74 10K
R79 NC
C107 100nF
C108 100nF
C109 100nF
C110 100nF
P30/GND
P29/GND
SD Socket [Taisol]
fundermental
Oscillator
tolerance +-100ppm
peak jitter 100ps
duty cycle
40/60~60/40
swing 3.3V
VDD_USB33
OSC2
VDD
OUT
OE
GND
OSCILLATOR 48Mhz
XO_UDEV 3
C111
NC
For USB Clock
XI_UDEV 3
C112
NC
3 REXT
R93
44.2 1%
C_PWR_5V
L7 LQH32C 10uH
U31
SW1
SW2
VIN
VOUT
SHDN/SS
FB
MODE/SYNC
VC
RT
GND
LTC3440EMS
D5
MBRM120LT3
VDD_USBH_5V
R157 100K
C153 47uF
R158 60.4K 1%
3 PWREN_USBH
R160 523K 1%
C154 47uF
C155 47uF
R159 15K
C152 15nF
R161 169K 1%
USB HOST
SDDATA & CLK path must be same length and route
VDD_D
VDD_D
U18
3 SD0_DAT[3:0]
SD0_DAT2
SD0_DAT3
3 SD0_CMD
SD0_DAT0
SD0_DAT1
3 SD0_CLK
3 nCD_SD0
R86 10K
R87 10K
R88 10K
R89 10K
R90 10K
R91 10K
R92 10K
R95 NC
P30/GND
P29/GND
SD Socket [Taisol]
4bit only
<Silk>
VDD_D
R77 330
D1
SMD TYPE (BLUE)
3 SD1_LED
CON4
IEEE1394-4
D1+
D1-
D2+
D2-
C159 NC
C161 NC
C156 NC
C160 NC
For HS-SPI test
CFG5
SW-SLIDE4
3,11 nSS0
3,11 SPIMISO0
3,11 SPIMOSI0
3,11 SPICLK0
nSS1 3,11
SPIMISO1 3,11
SPIMOSI1 3,11
SPICLK1 3,11
CFG5 | ON | OFF
[1~4] | LOOP 0-1 | SPI_CON
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number USB/HS_MMC/HS_SPI
Rev 0.0
Date: Friday, January 25, 2008
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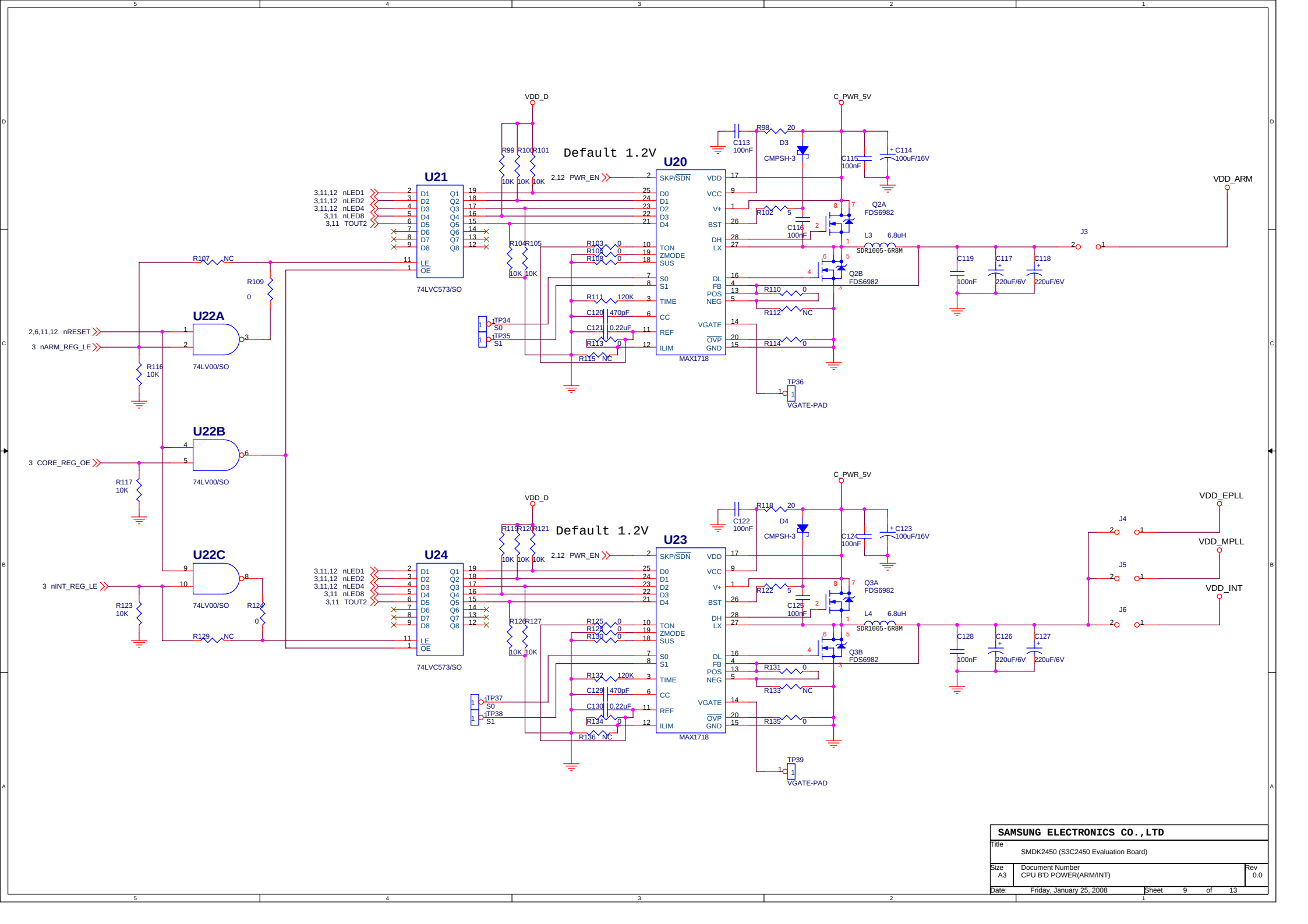
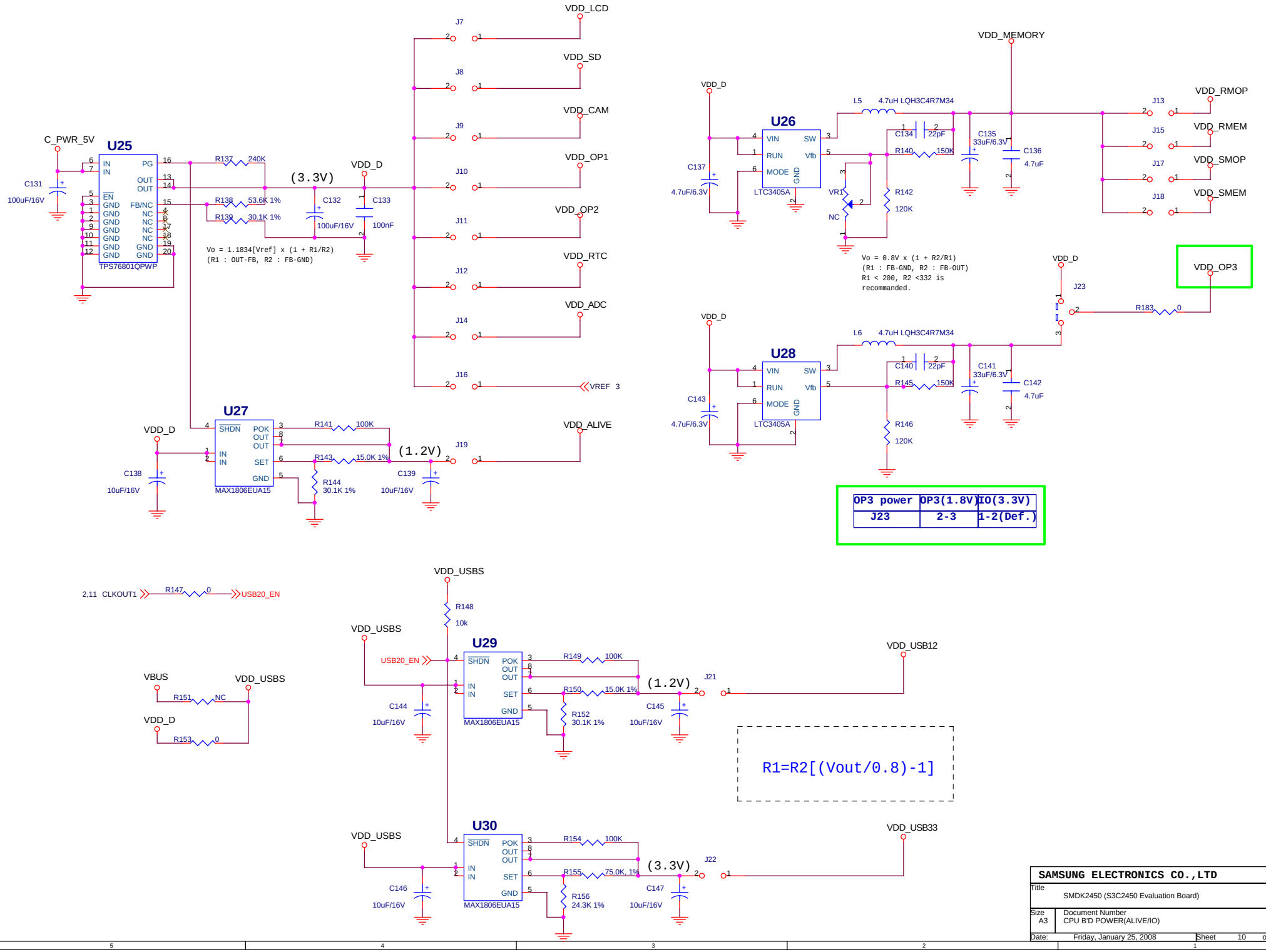
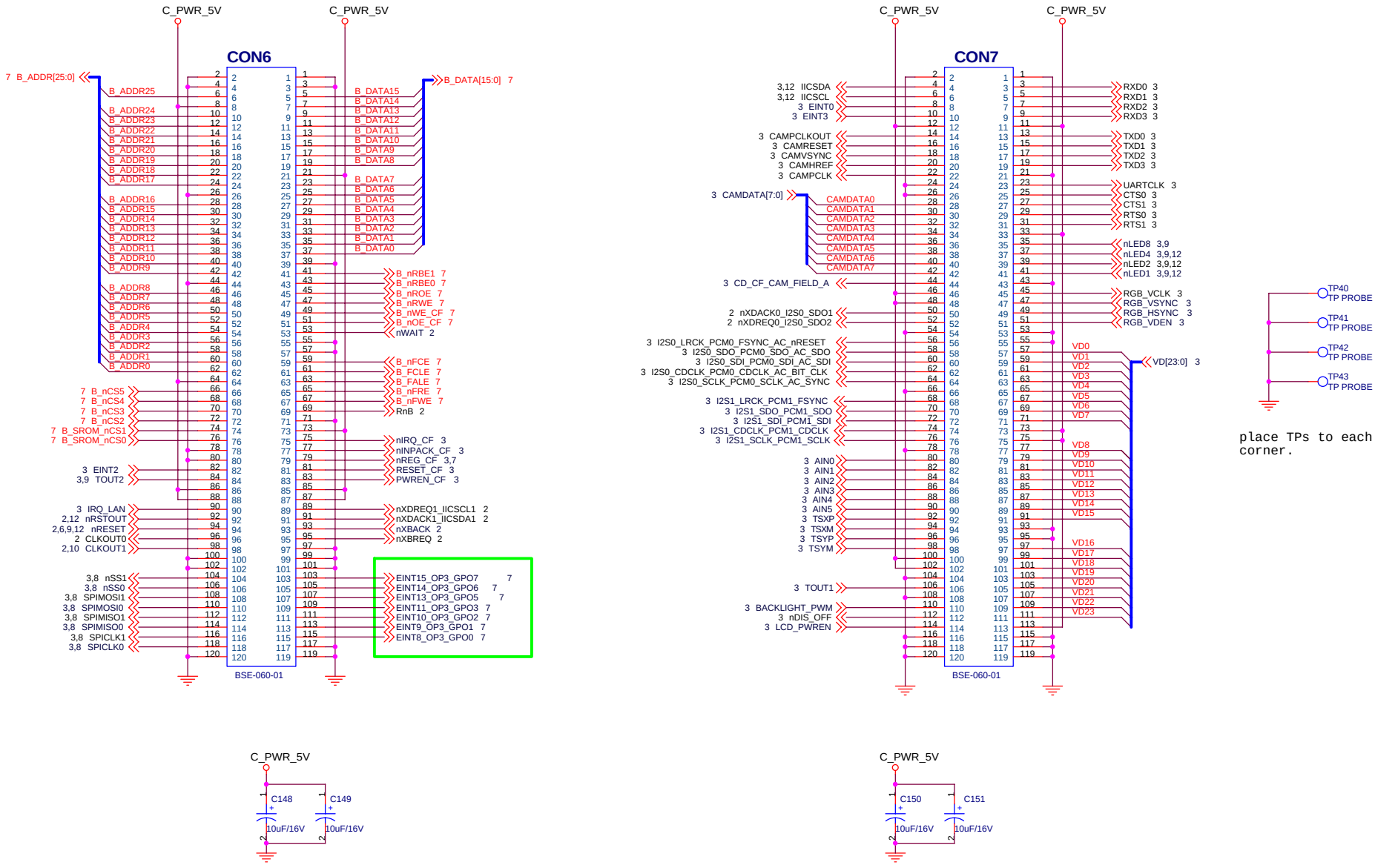
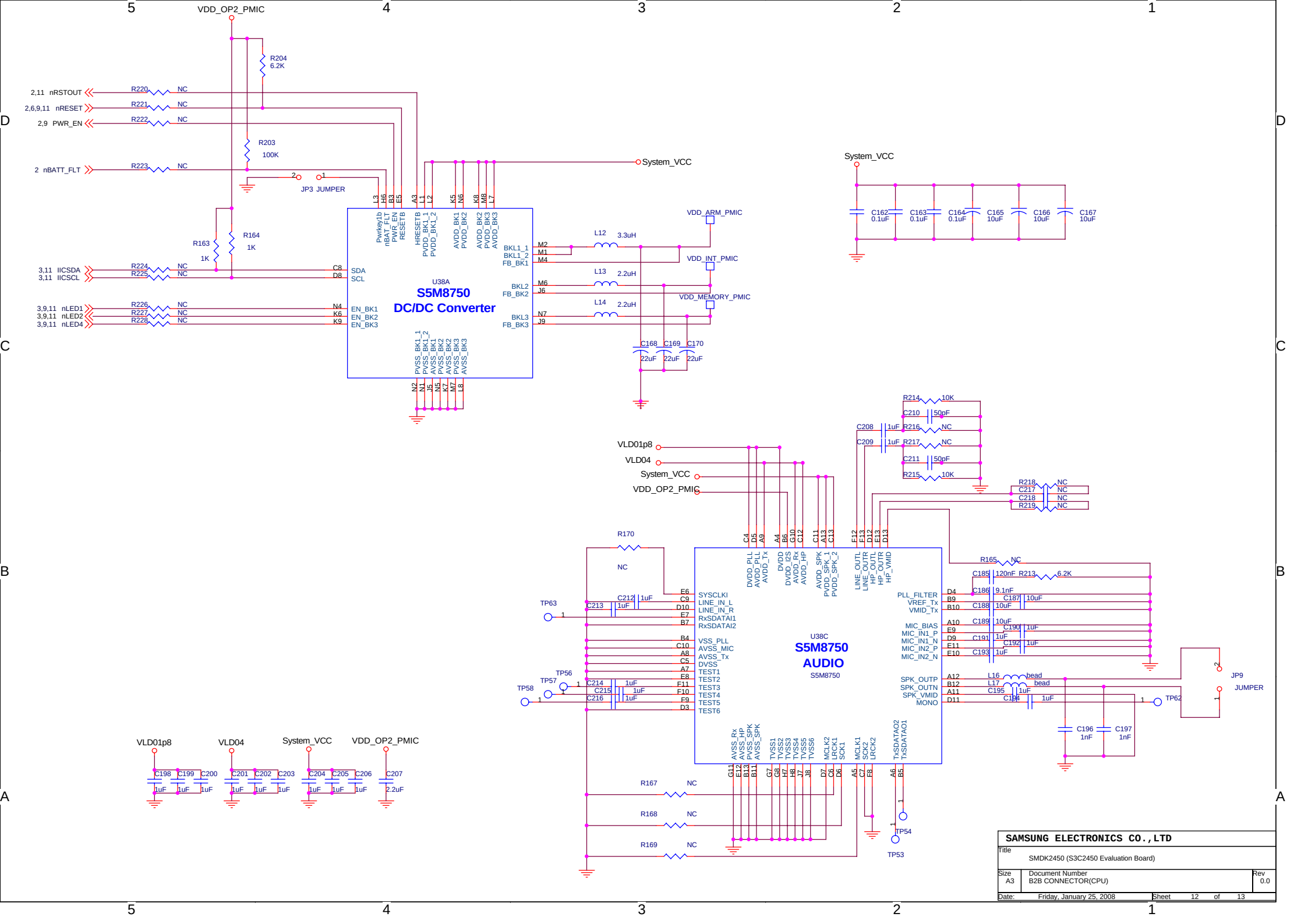

VDD_D
C_PWR_5V
Default 1.2V
U20
U21
U22A
U22B
U22C
U23
U24
MAX1718
74LVC573/SO
74LV00/SO
2,12 PWR_EN
3,11,12 nLED1
3,11,12 nLED2
3,11,12 nLED4
3,11 nLED8
3,11 TOUT2
2,6,11,12 nRESET
3 nARM_REG_LE
3 CORE_REG_OE
3 nINT_REG_LE
D3
CMPSH-3
D4
Q2A FDS6982
Q2B FDS6982
Q3A FDS6982
Q3B FDS6982
L3 6.8uH
L4 6.8uH
SDR1005-6R8M
VDD_ARM
VDD_EPLL
VDD_MPLL
VDD_INT
VGATE-PAD
J3
J4
J5
J6
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
CPU B'D POWER(ARM/INT)
Friday, January 25, 2008
Sheet 9 of 13

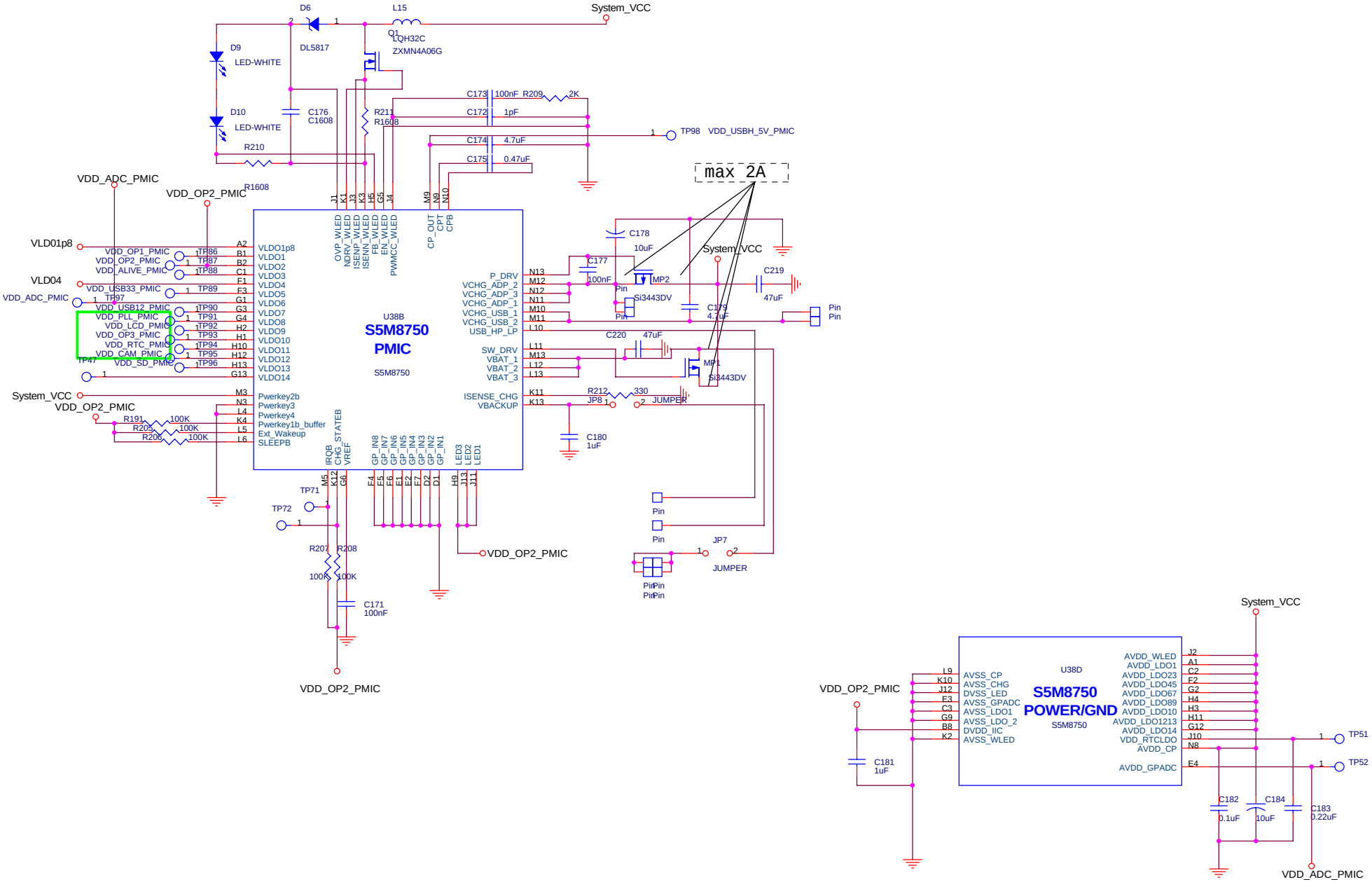



| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: CPU B'D POWER(ALIVE/IO) | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 10 of 13 | |



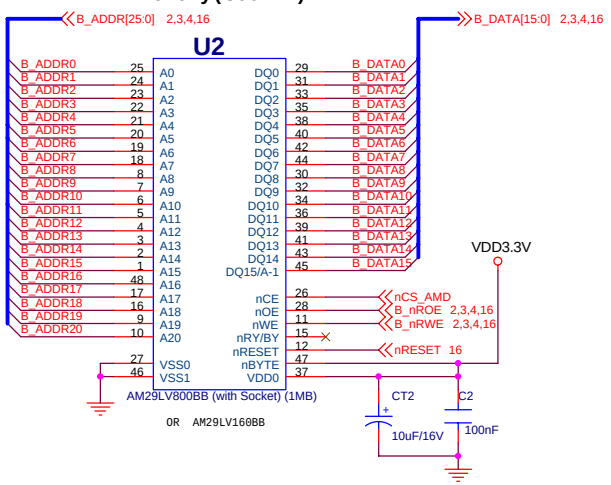

| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: C0B. PMIC DC-DC/Audio | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 11 of 13 | |


VDD_OP2_PMIC
R204 6.2K
2,11 nRSTOUT
2,6,9,11 nRESET
2,9 PWR_EN
R220 NC
R221 NC
R222 NC
R203 100K
2 nBATT_FLT
R223 NC
JP3 JUMPER
System_VCC
R163 1K
R164 1K
3,11 IICSDA
3,11 IICSCL
R224 NC
R225 NC
3,9,11 nLED1
3,9,11 nLED2
3,9,11 nLED4
R226 NC
R227 NC
R228 NC
U38A
S5M8750
DC/DC Converter
SDA
SCL
EN_BK1
EN_BK2
EN_BK3
VDD_ARM_PMIC
VDD_INT_PMIC
VDD_MEMORY_PMIC
L12 3.3uH
L13 2.2uH
L14 2.2uH
C168 22uF
C169 22uF
C170 22uF
C162 0.1uF
C163 0.1uF
C164 0.1uF
C165 10uF
C166 10uF
C167 10uF
VLD01p8
VLD04
R214 10K
C210 50pF
C208 1uF
R216 NC
C209 1uF
R217 NC
C211 50pF
R215 10K
R218 NC
C217 NC
C218 NC
R219 NC
R170 NC
U38C
S5M8750
AUDIO
S5M8750
SYSCLKI
LINE_IN_L
LINE_IN_R
RxSDATAI1
RxSDATAI2
VSS_PLL
AVSS_MIC
AVSS_Tx
DVSS
TEST1
TEST2
TEST3
TEST4
TEST5
TEST6
PLL_FILTER
VREF_Tx
VMID_Tx
MIC_BIAS
MIC_IN1_P
MIC_IN1_N
MIC_IN2_P
MIC_IN2_N
SPK_OUTP
SPK_OUTN
SPK_VMID
MONO
R165 NC
C185 120nF
R213 6.2K
C186 9.1nF
C187 10uF
C188 10uF
C189 10uF
C190 1uF
C191 1uF
C192 1uF
C193 1uF
L16 bead
L17 bead
C195 1uF
C194 1uF
C196 1nF
C197 1nF
JP9 JUMPER
TP62
TP63
TP56
TP57
TP58
TP54
TP53
C212 1uF
C213 1uF
C214 1uF
C215 1uF
C216 1uF
R167 NC
R168 NC
R169 NC
C198 1uF
C199 1uF
C200 1uF
C201 1uF
C202 1uF
C203 1uF
C204 1uF
C205 1uF
C206 1uF
C207 2.2uF
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number B2B CONNECTOR(CPU)
Rev 0.0
Date: Friday, January 25, 2008
Sheet 12 of 13

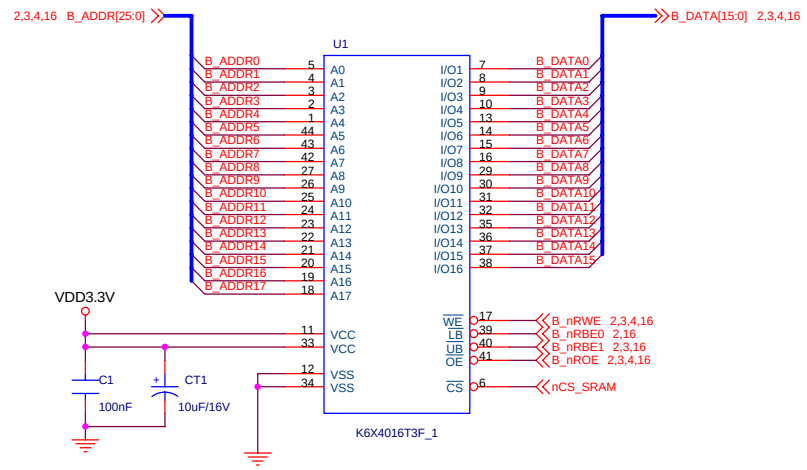


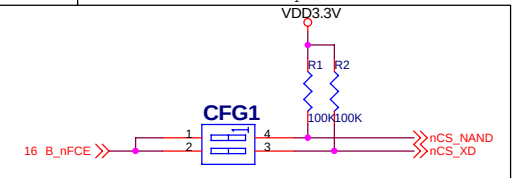

| | |
|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | |
| Title | SMDK2450 (S3C2450 Evaluation Board) |
| Size A3 | Document Number PMIC Power |
| Rev | 0.0 |
| Date: Friday, January 25, 2008 | Sheet 13 of 13 |

## AMD Flash Memory(SOCKET)



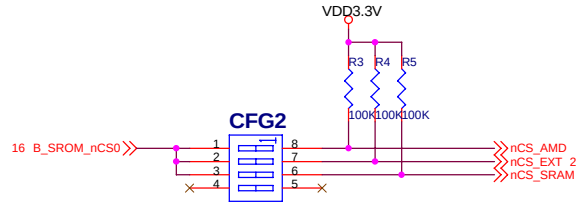

## SRAM




<Silk>

| CFG1: nFCE | SROM Selector |
|---|---|
| [2] | XD card |
| [1] | NAND |



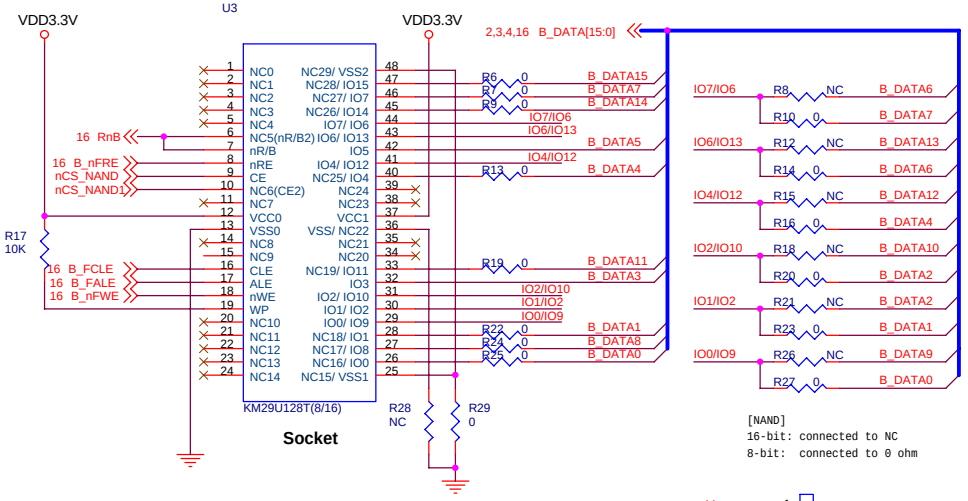

<Silk>

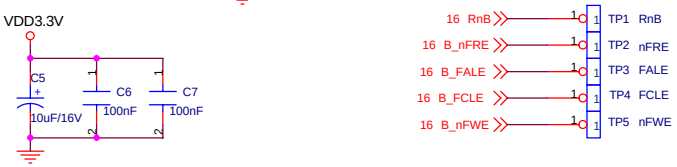
| CFG2: nCS0 | SROM Selector |
|---|---|
| [3] | External |
| [2] | SRAM |
| [1] | NOR(AMD) |

**S3C2450**
**Addition : NAND CS1 & RnB1**

**S3C2450**
**Addition : NAND CS1**
**SW(To Select Ethernet or Additional Nand CS)**

## NAND Flash memory (SOCKET )

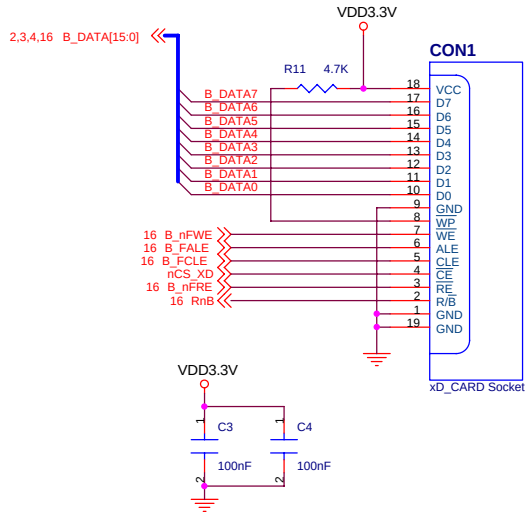


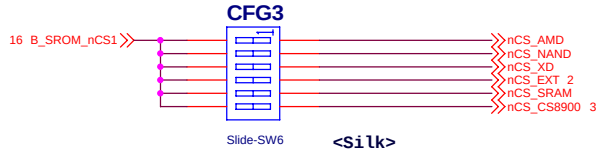







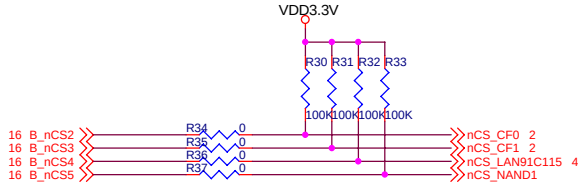
## XD PICTURE CARD



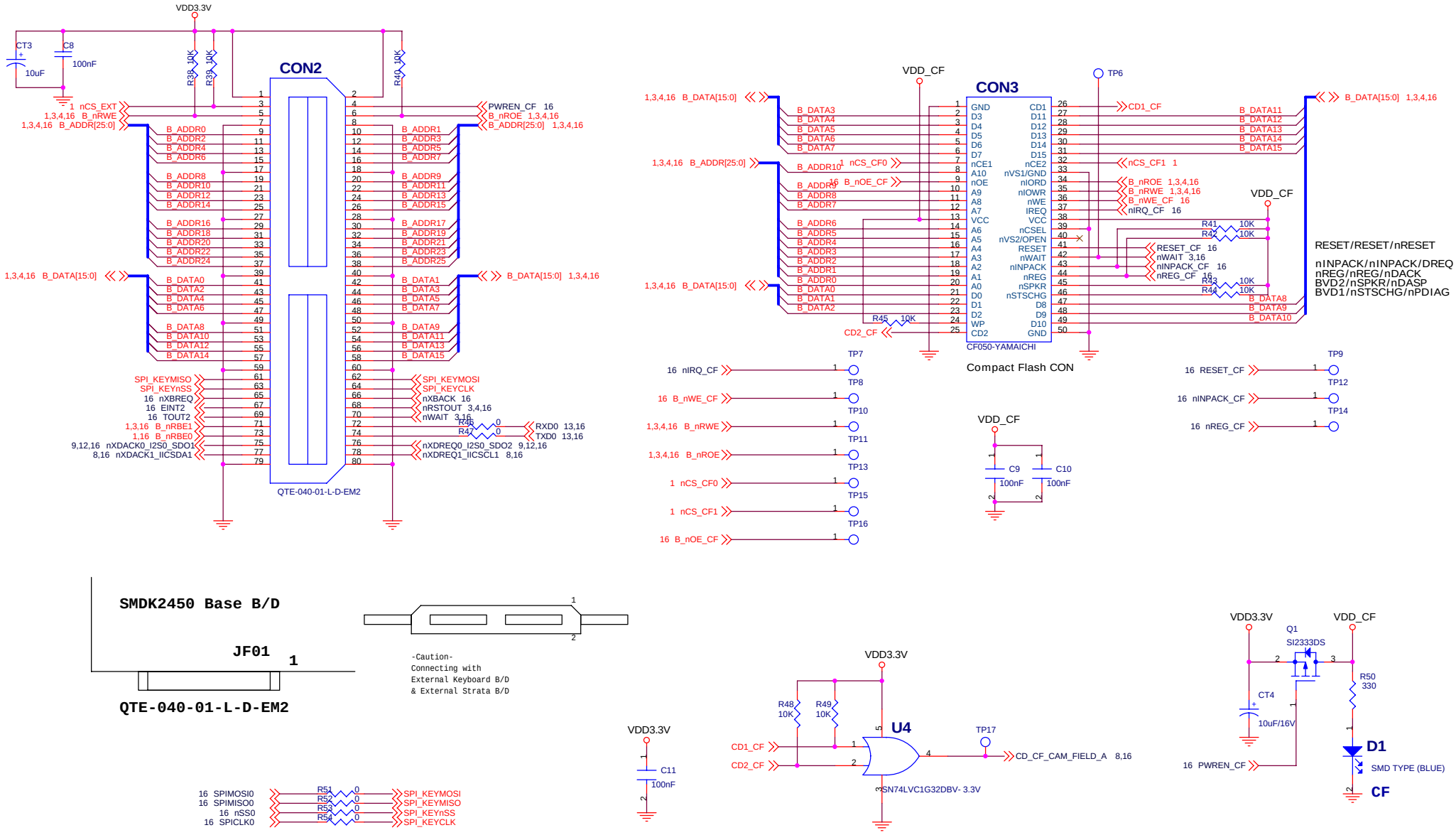

<Silk>

| CFG3: nCS1 | SROM Selector |
|---|---|
| [6] | CS8900(CS1) |
| [5] | SRAM |
| [4] | External |
| [3] | XD card |
| [2] | NAND |
| [1] | NOR(AMD) |

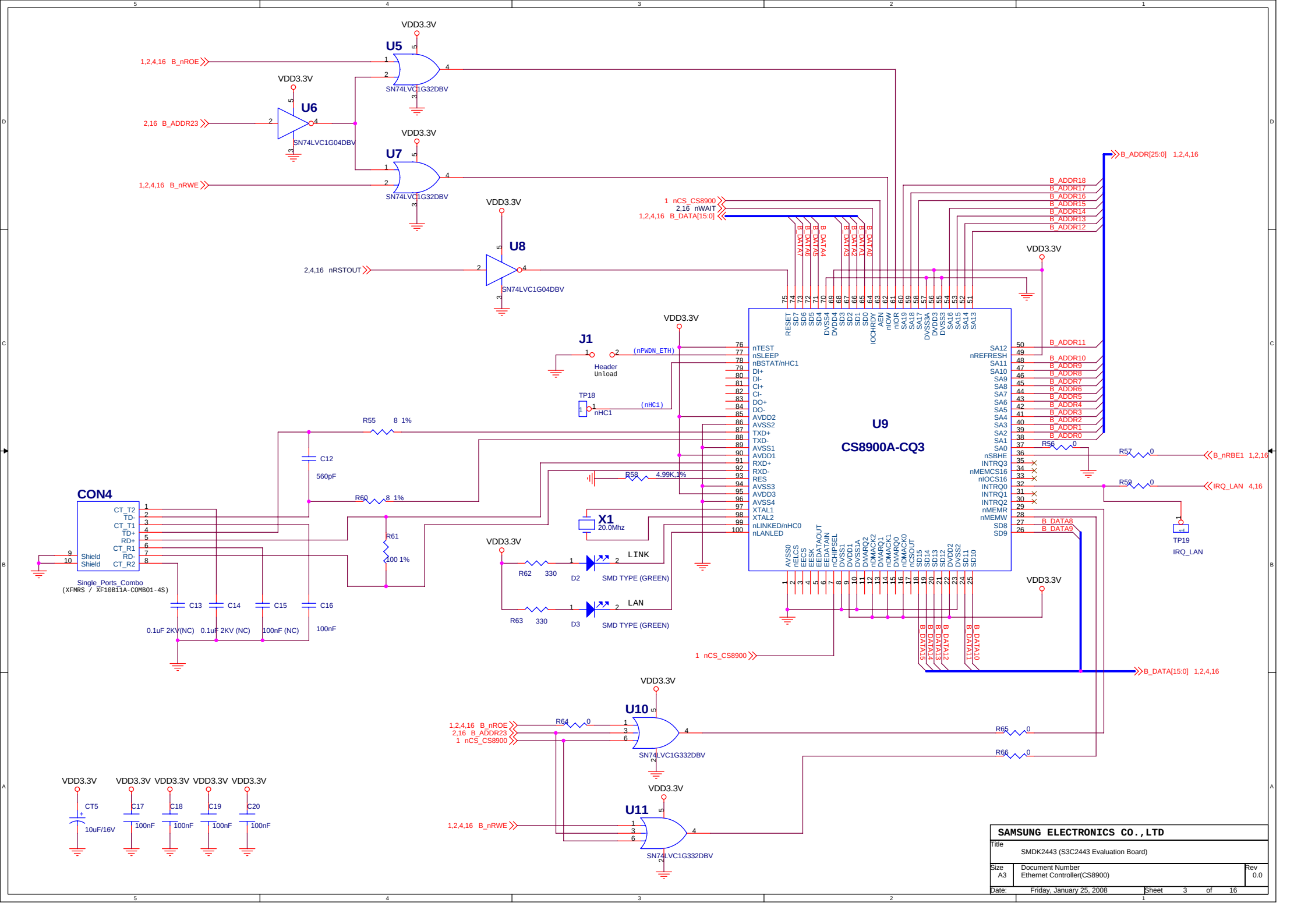



R281~R284 place on top

| SAMSUNG ELECTRONICS CO.,LTD | | |
|---|---|---|
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: NOR/NAND/SRAM/CONFIG | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 1 of 16 | |

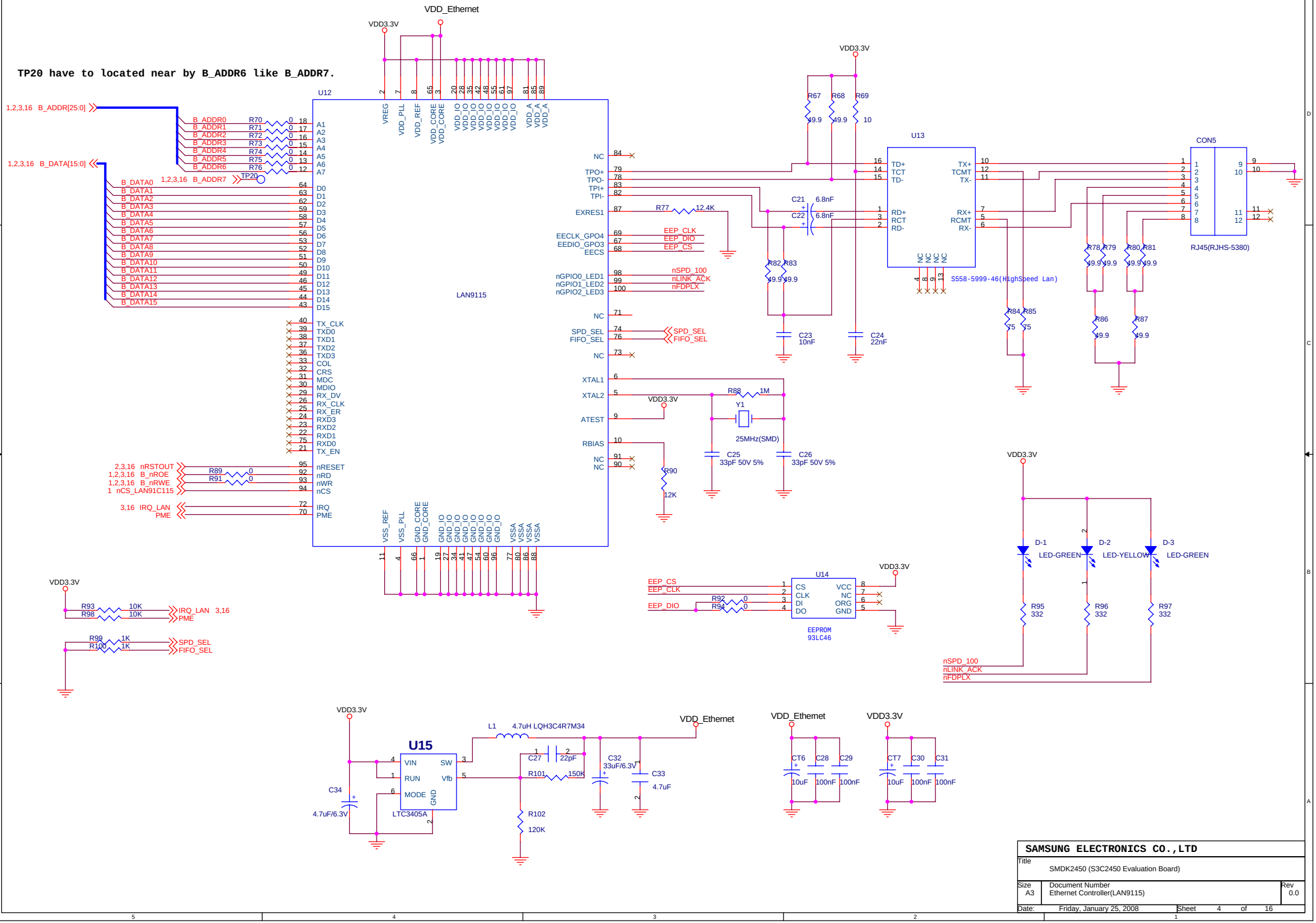


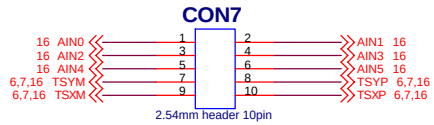

| | | |
|---|---|---|
| **SAMSUNG ELECTRONICS CO.,LTD** | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: External Bus connector & CF interface | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 2 of 16 | |



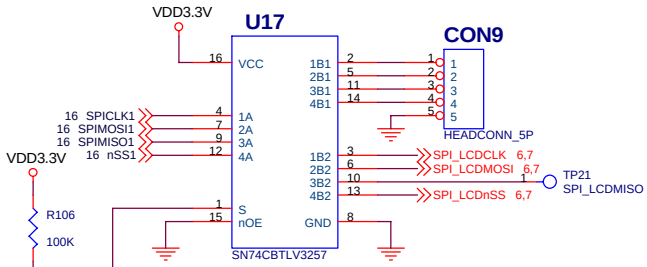

| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2443 (S3C2443 Evaluation Board) | | |
| Size: A3 | Document Number: Ethernet Controller(CS8900) | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 3 of 16 | |

**TP20 have to located near by B_ADDR6 like B_ADDR7.**





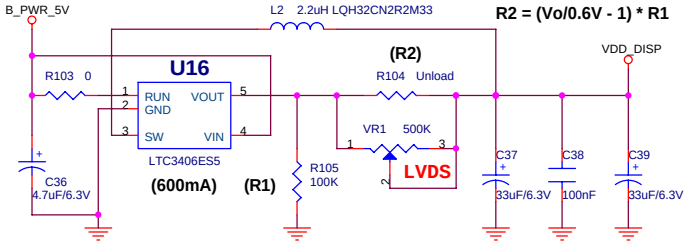

## ADC

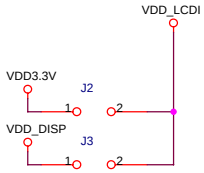


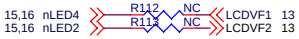

| | LCD_SPI | EXT_SPI |
|---|---|---|
| J4 | 1-2 | 2-3 |

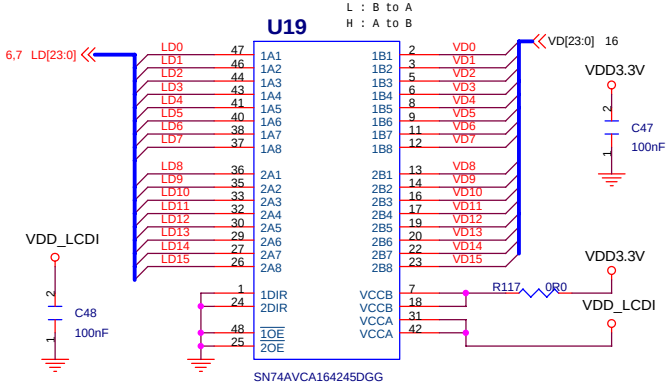
## EXT_SPI/LCD_SPI

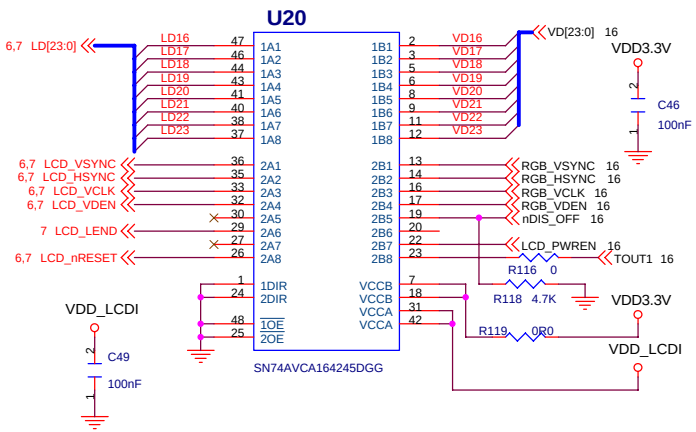
Vo = 0.6V * (1+R2/R1)= 2.8V
R2 = (Vo/0.6V - 1) * R1

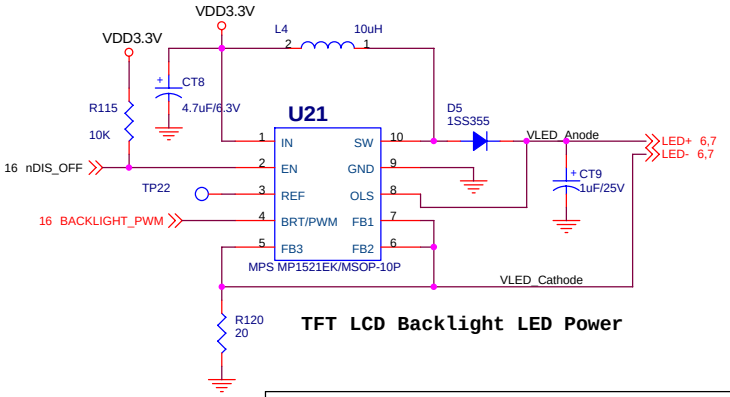


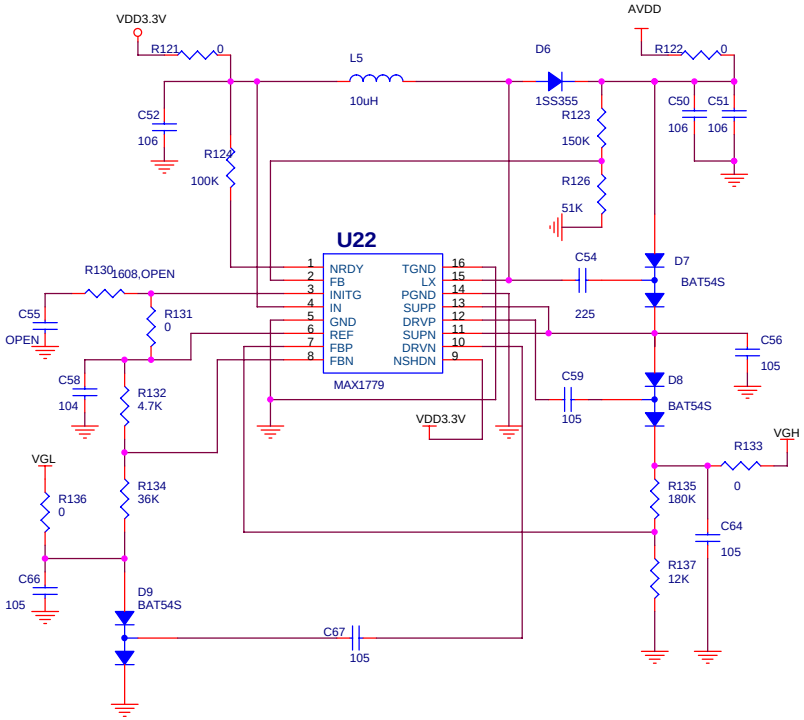



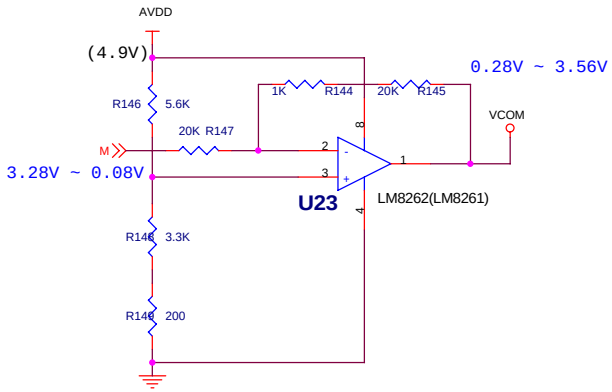



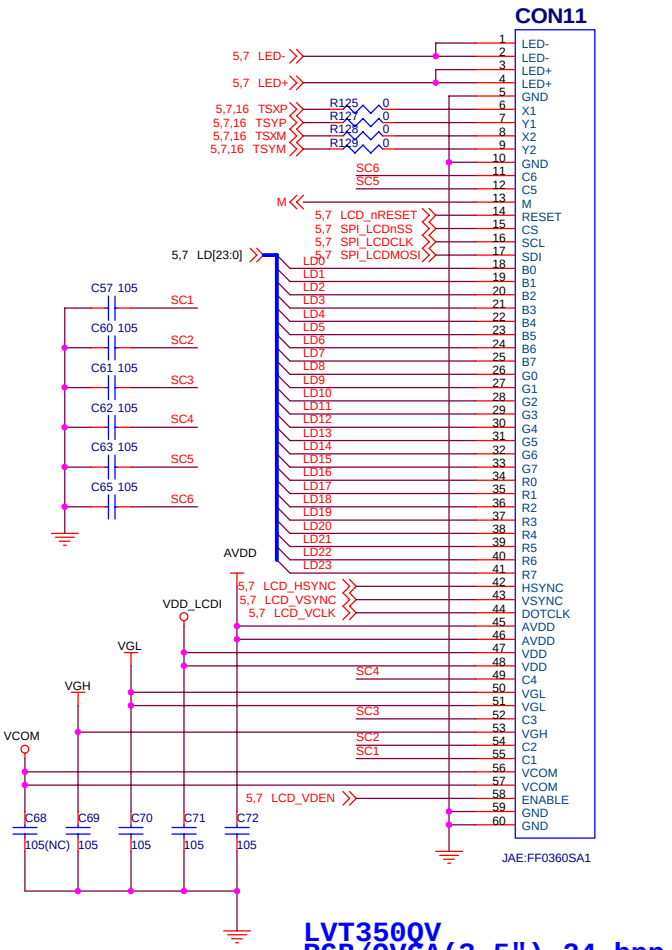




## TFT LCD Backlight LED Power

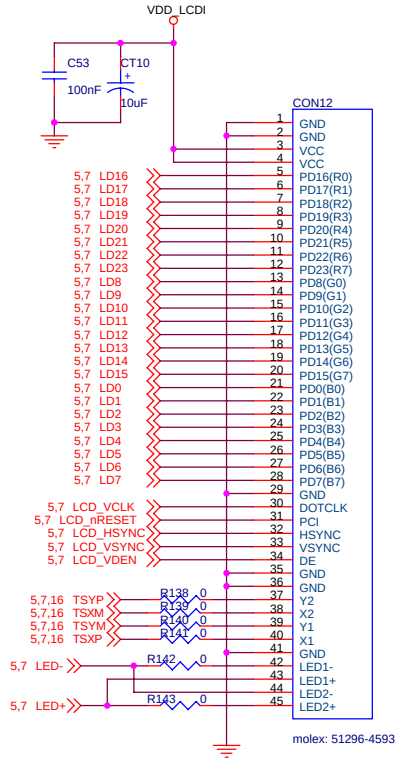
| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: B05. LCD General/SPI/ADC | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 5 of 16 | |




**LVT350QV**
**RGB/QVGA(3.5") 24-bpp**

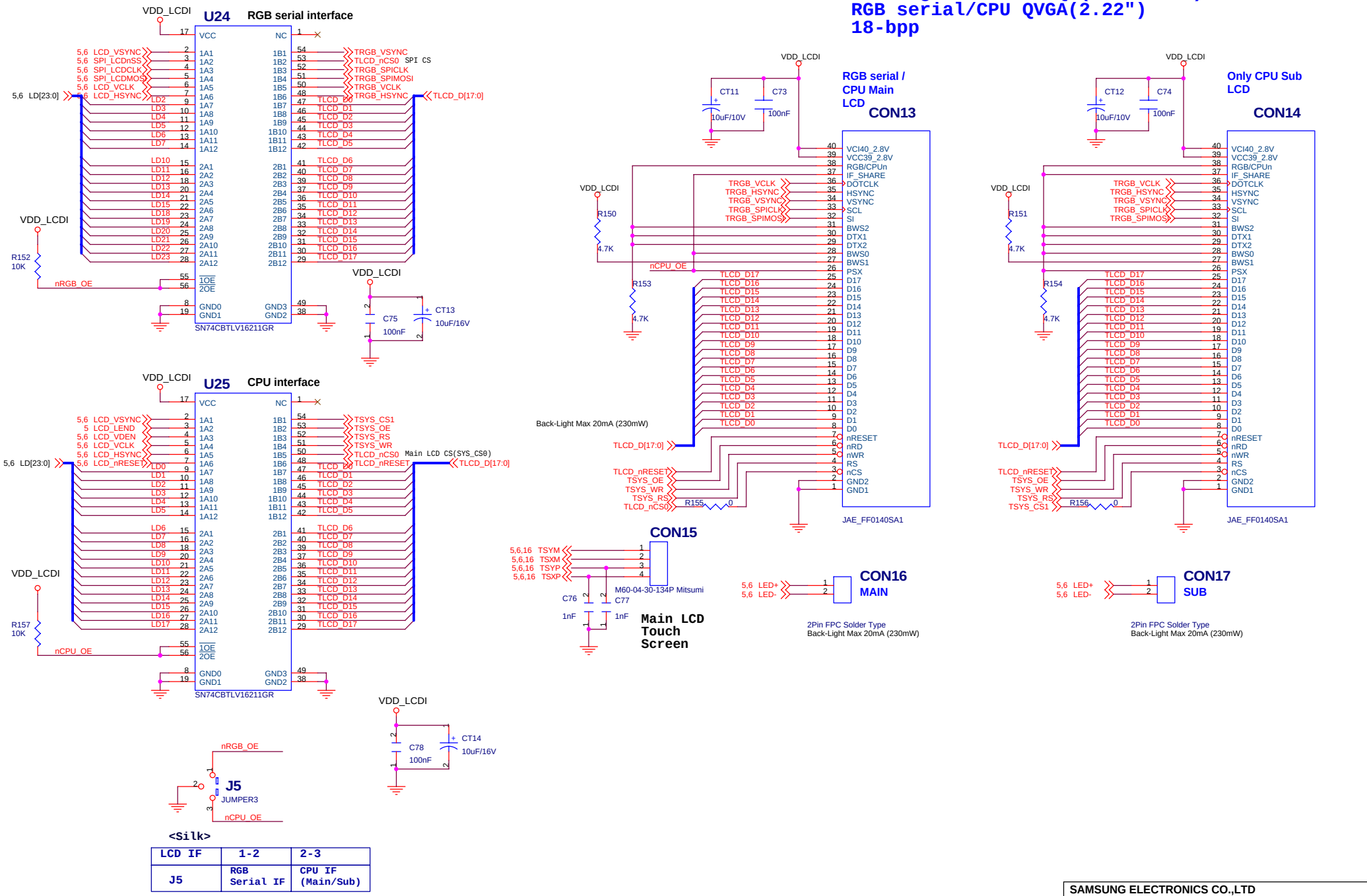



molex: 51296-4593

**LTE480WE**
**RGB/WVGA(4.8") 24-bpp**
**- Default**

| | | |
|---|---|---|
| **SAMSUNG ELECTRONICS CO.,LTD** | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: LCD interface & TFT LCD(Landscape type) | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 6 of 16 | |

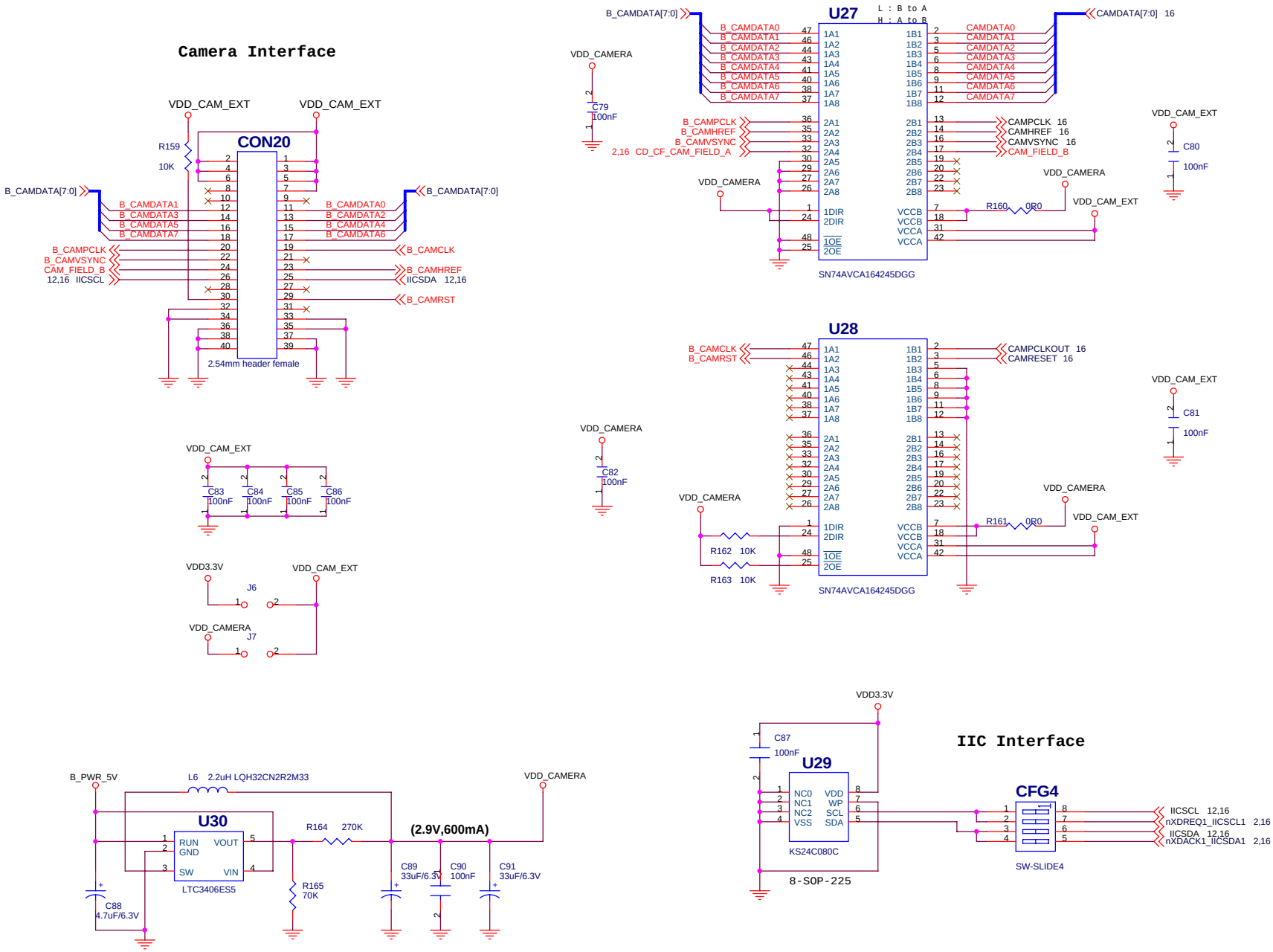
# Samsung LCD LTS222QV(1.7V~3.3V)
# RGB serial/CPU QVGA(2.22")
# 18-bpp




<Silk>

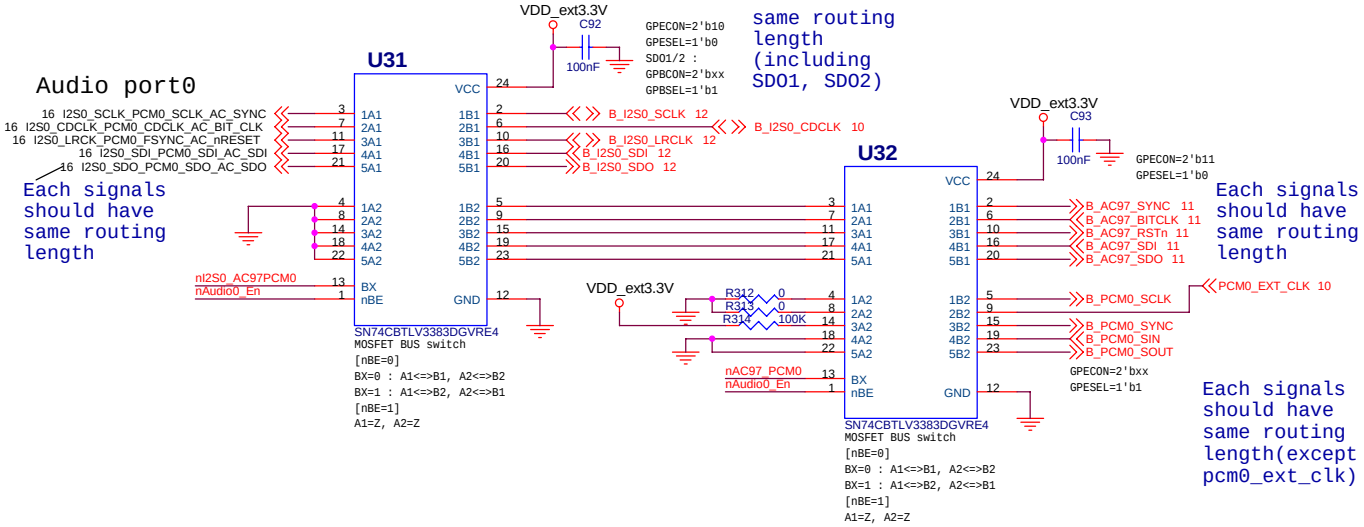
| LCD IF | 1-2 | 2-3 |
|---|---|---|
| J5 | RGB Serial IF | CPU IF (Main/Sub) |

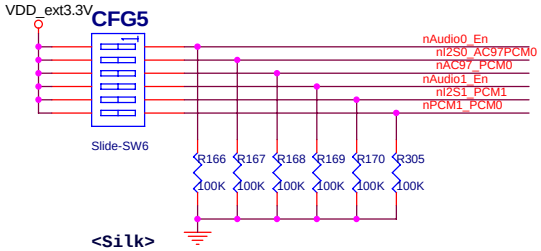
| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: TFT LCD(CPU/RGB portrait type) / CSTN LCD | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 7 of 16 | |




| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: Camera Interface | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 8 of 16 | |

## Audio port0

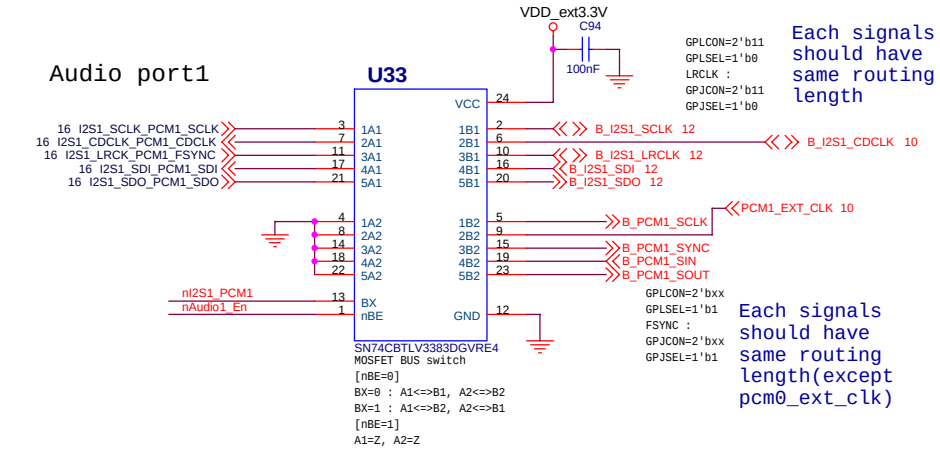


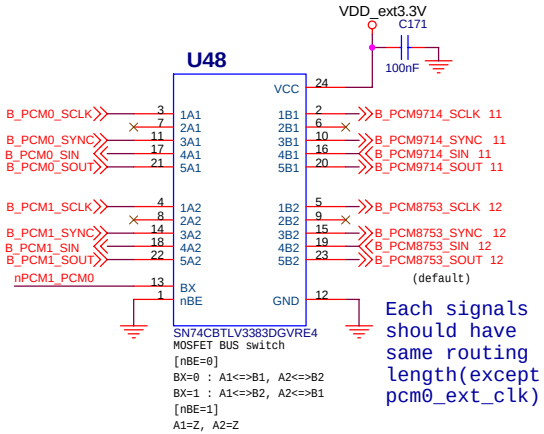




| CFG5: Audio port Enable/Demux | | | | | | |
|---|---|---|---|---|---|---|
| PORT # | Audio0 | | | Audio1 | | |
| En/Disable | [1] | | | [4] | | |
| Enable | OFF(Def.) | | | OFF(Def.) | | |
| Disable | ON | | | ON | | |
| Demux | [2] | [3] | [6] | Demux | [5] | [6] |
| I2S0 (Def) | OFF | X | X | IIS1* (Def) | OFF | X |
| AC97 | ON | OFF | X | PCM1* | ON | OFF (8753) |
| PCM0 | ON | ON | ON (8753) | | | |
| *For I2S1,PCM1 set CFG6 switch of CPU b'd | | | | | | |

<Pcm0/1 select>

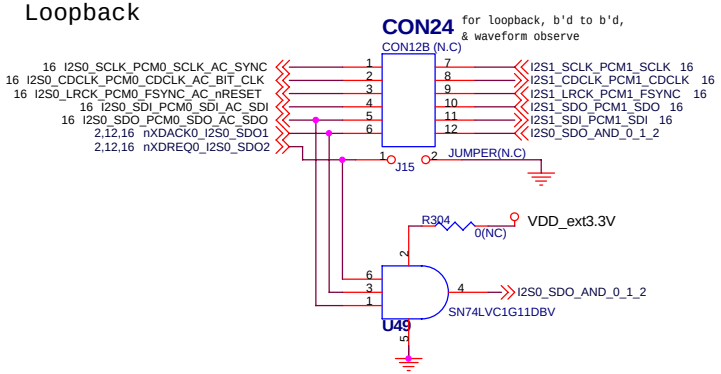
## Audio port1




Pcm0/1 are verified by 8753 codec(default)
but can be verified by 9714(sw setting is needed)

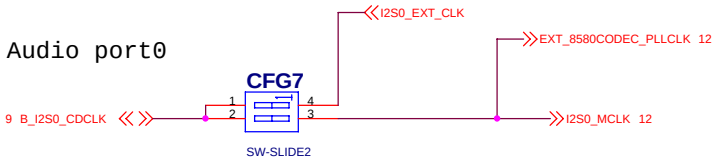
## Loopback




| | | | |
|---|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | | |
| Size: A3 | Document Number: Audio(Demux) | | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 9 of 16 | | |

<i2s cdclk select/codec operating clk supply>

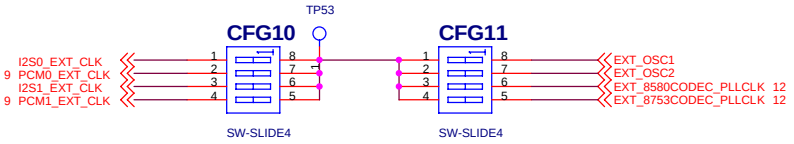
## Audio port0



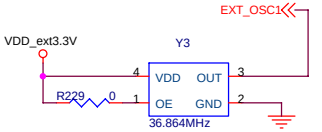

<Silk>

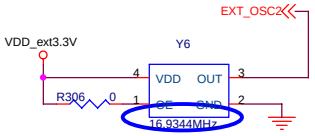
| I2S0 cdclk path select | | |
|---|---|---|
| CFG 7 | [1] | [2] |
| I2S0 Master(Def.) | OFF | ON |
| I2S0 Slave | OFF | OFF |
| I2S0 Master External clock | ON | OFF |

<External Clock select part>

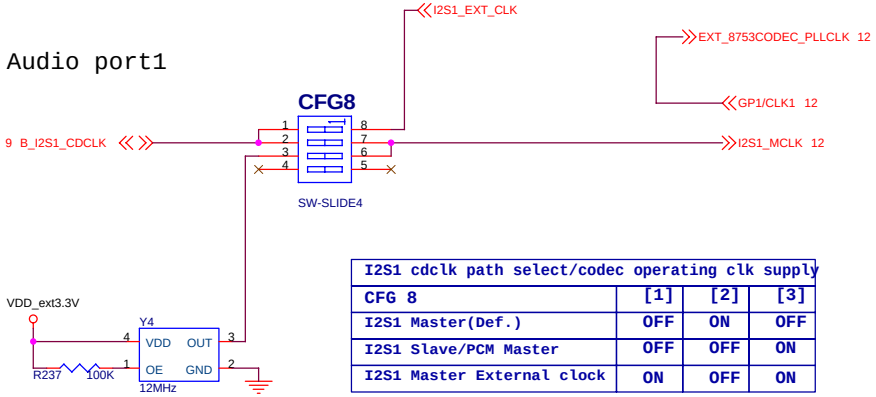



| Ext. Clk Sel. | CFG10 To. | CFG11 From |
|---|---|---|
| [1] | I2S0 | OSC1 |
| [2] | PCM0 | OSC2 |
| [3] | I2S1 | 8580PLL |
| [4] | PCM1 | 8753PLL |
| All Off (Default) | | |



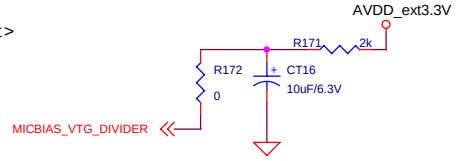



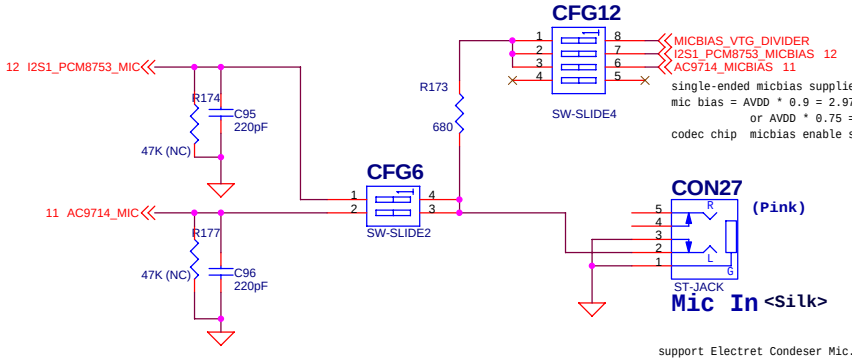

## Audio port1

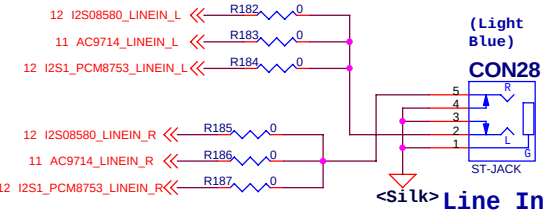



| I2S1 cdclk path select/codec operating clk supply | | | |
|---|---|---|---|
| CFG 8 | [1] | [2] | [3] |
| I2S1 Master(Def.) | OFF | ON | OFF |
| I2S1 Slave/PCM Master | OFF | OFF | ON |
| I2S1 Master External clock | ON | OFF | ON |

<mic bias part>




<Silk>

| Mic in direction select | | |
|---|---|---|
| CFG6 | [1] | [2] |
| IIS1_PCM8753 | ON | OFF |
| AC9714(Def.) | OFF | ON |

<Silk>

| CFG12 | Mic bias source |
|---|---|
| [1] | VTG div. (Def.) |
| [2] | 8753 Codec |
| [3] | 9714 Codec |

<Silk>
I2S FRONT
Speaker Out
-Front L,R
-WM8580 OUT1
CON21 PJ-327-2
(Green)
ST-JACKc
12 I2S08580_OUT1_L
12 I2S08580_OUT1_R

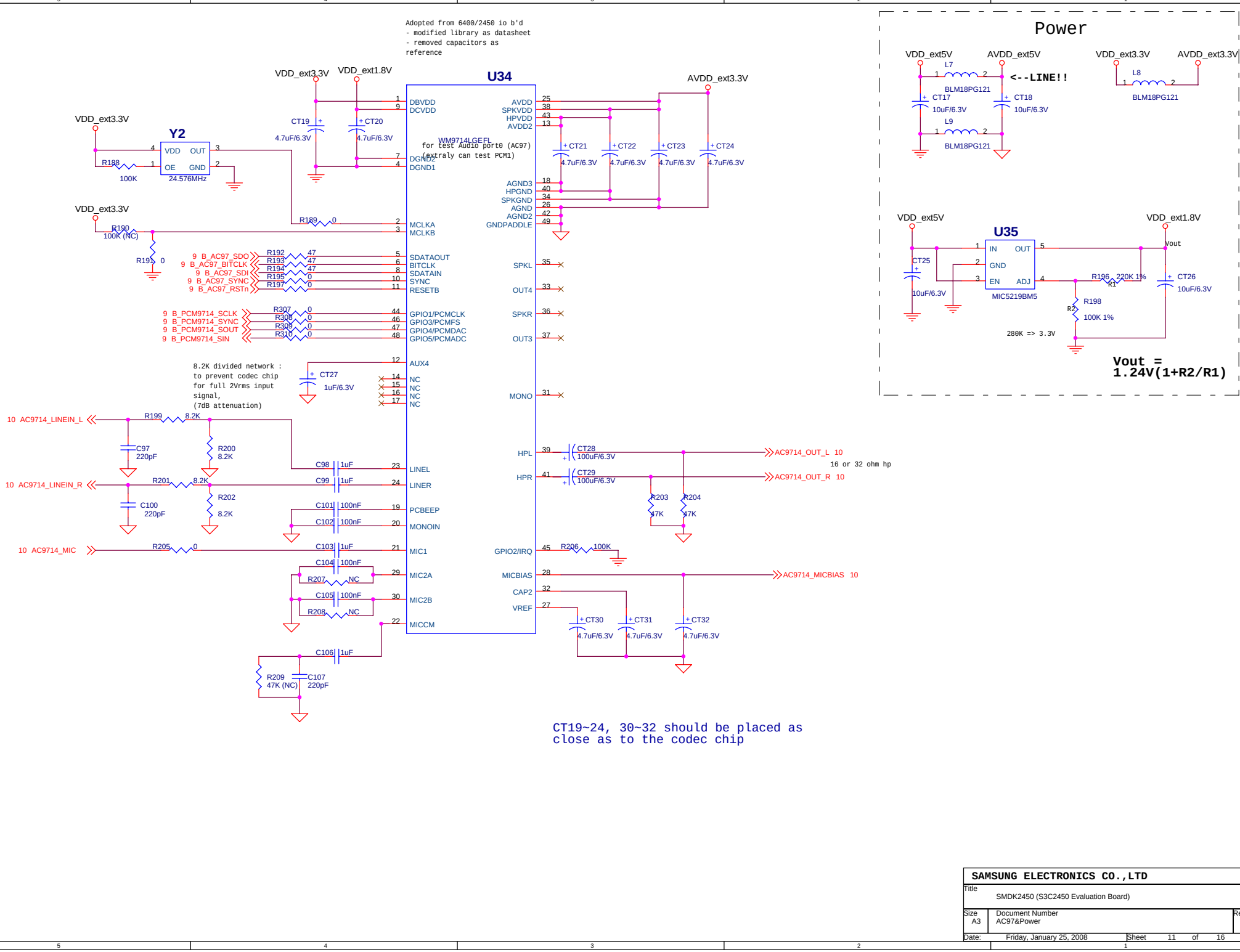
<Silk>
I2S CENTER
Speaker Out
-Center, LF
-WM8580 OUT2
CON22 PJ-327-2
(Orange)
ST-JACKc
12 I2S08580_OUT2_L
12 I2S08580_OUT2_R

<Silk>
I2S REAR
Speaker Out
-Rear L,R
-WM8580 OUT3
CON23 PJ-327-2
(Black)
ST-JACKc
12 I2S08580_OUT3_L
12 I2S08580_OUT3_R

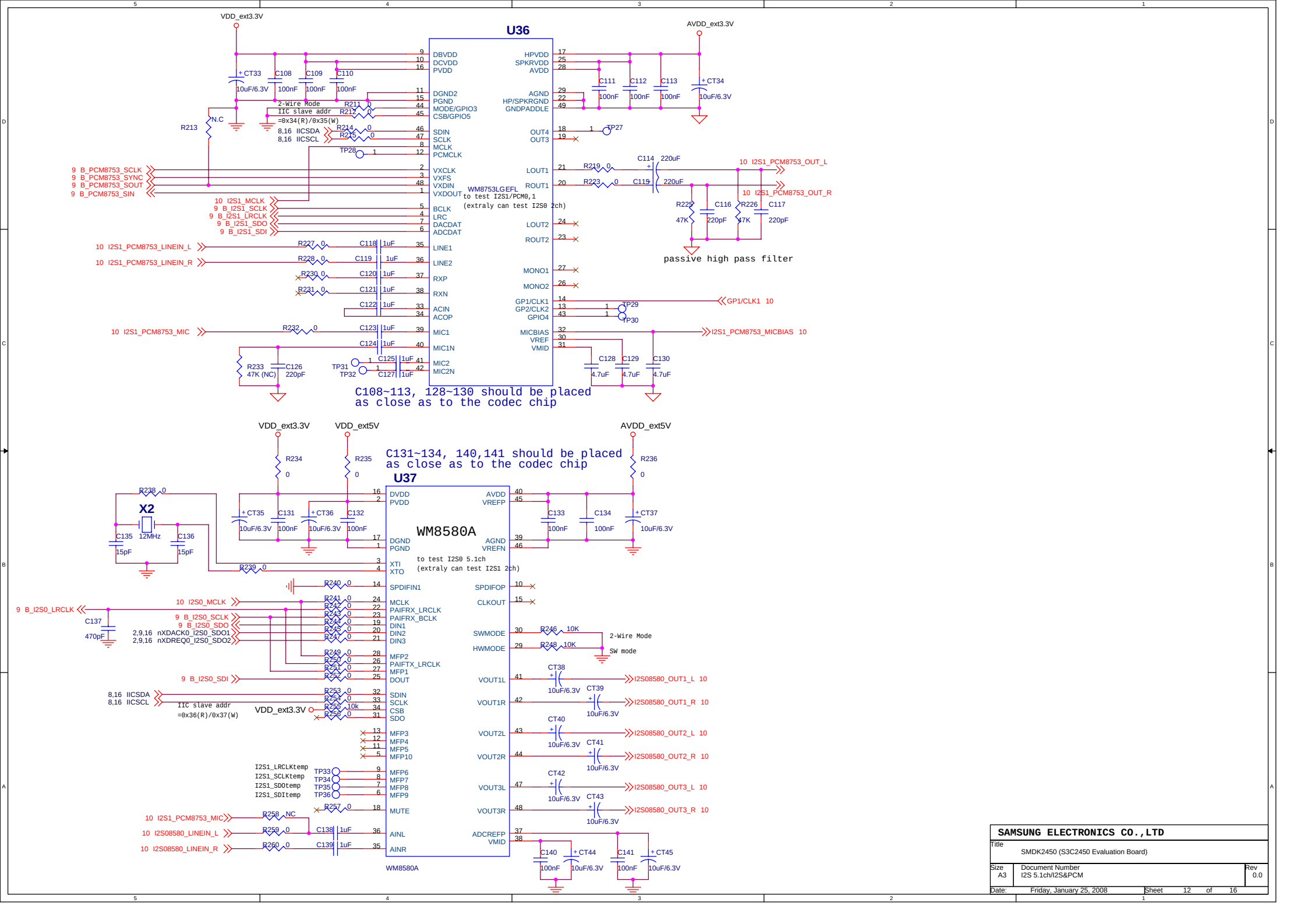
<Silk>
AC97 OUT
Speaker Out
-L,R
-WM9714
CON25 PJ-327-2
(Green)
ST-JACKc
11 AC9714_OUT_L
11 AC9714_OUT_R

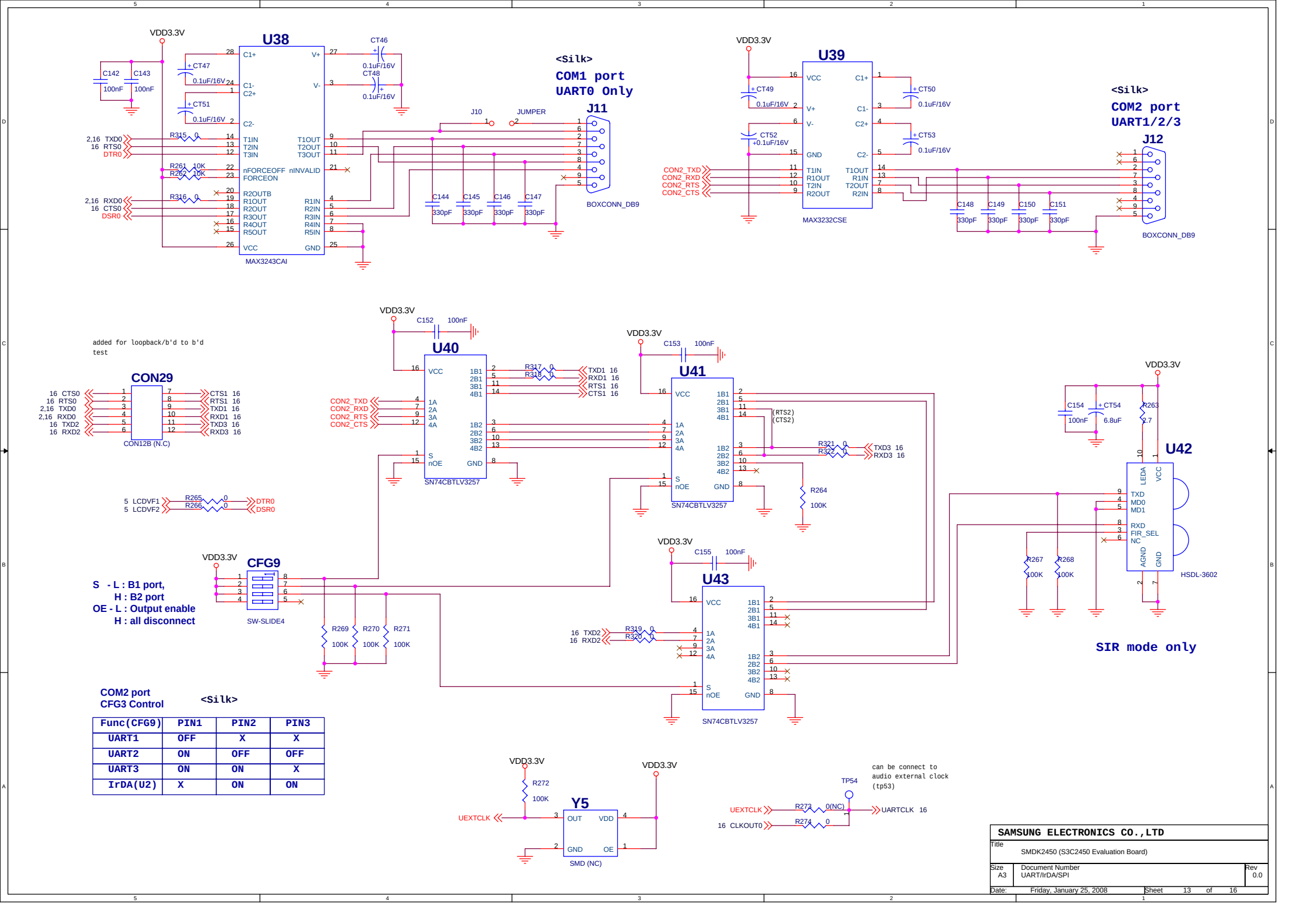
<Silk>
I2S1/PCM OUT
Speaker Out
-L,R
-WM8753
CON26 PJ-327-2
(Green)
ST-JACKc
12 I2S1_PCM8753_OUT_L
12 I2S1_PCM8753_OUT_R

| SAMSUNG ELECTRONICS CO.,LTD | | |
|---|---|---|
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: Audio(Ext. Clk & Conn) | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 10 of 16 | |




| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: AC97&Power | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 11 of 16 | |


U36
WM8753LGEFL
to test I2S1/PCM0,1
(extraly can test I2S0 2ch)
passive high pass filter
C108~113, 128~130 should be placed
as close as to the codec chip
C131~134, 140,141 should be placed
as close as to the codec chip
U37
WM8580A
to test I2S0 5.1ch
(extraly can test I2S1 2ch)
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
I2S 5.1ch/I2S&PCM
Friday, January 25, 2008


U38
MAX3243CAI
C142
C143
100nF
100nF
CT46
CT47
CT48
CT51
0.1uF/16V
VDD3.3V
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
T3IN
T1OUT
T2OUT
T3OUT
nFORCEOFF
nINVALID
FORCEON
R2OUTB
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
R1IN
R2IN
R3IN
R4IN
R5IN
VCC
GND
R315
R316
R261
R262
10K
2,16 TXD0
16 RTS0
DTR0
2,16 RXD0
16 CTS0
DSR0
<Silk>
COM1 port
UART0 Only
J10
JUMPER
J11
BOXCONN_DB9
C144
C145
C146
C147
330pF
U39
MAX3232CSE
CT49
CT50
CT52
CT53
+0.1uF/16V
CON2_TXD
CON2_RXD
CON2_RTS
CON2_CTS
T1IN
R1OUT
T2IN
R2OUT
T1OUT
R1IN
T2OUT
R2IN
<Silk>
COM2 port
UART1/2/3
J12
BOXCONN_DB9
C148
C149
C150
C151
added for loopback/b'd to b'd
test
CON29
CON12B (N.C)
16 CTS0
16 RTS0
2,16 TXD0
2,16 RXD0
16 TXD2
16 RXD2
CTS1 16
RTS1 16
TXD1 16
RXD1 16
TXD3 16
RXD3 16
U40
SN74CBTLV3257
C152
100nF
R317
R318
TXD1 16
RXD1 16
RTS1 16
CTS1 16
U41
C153
(RTS2)
(CTS2)
R321
R322
TXD3 16
RXD3 16
R264
100K
5 LCDVF1
5 LCDVF2
R265
R266
DTR0
DSR0
CFG9
SW-SLIDE4
S - L : B1 port,
H : B2 port
OE - L : Output enable
H : all disconnect
R269
R270
R271
100K
U43
C155
R319
R320
16 TXD2
16 RXD2
U42
HSDL-3602
C154
CT54
6.8uF
R263
2.7
LEDA
VCC
TXD
MD0
MD1
RXD
FIR_SEL
NC
AGND
GND
R267
R268
SIR mode only
COM2 port
CFG3 Control
<Silk>
Func(CFG9) | PIN1 | PIN2 | PIN3
UART1 | OFF | X | X
UART2 | ON | OFF | OFF
UART3 | ON | ON | X
IrDA(U2) | X | ON | ON
Y5
SMD (NC)
R272
UEXTCLK
OUT
VDD
GND
OE
TP54
R273
0(NC)
R274
16 CLKOUT0
UARTCLK 16
can be connect to
audio external clock
(tp53)
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
UART/IrDA/SPI
Rev
0.0
Date:
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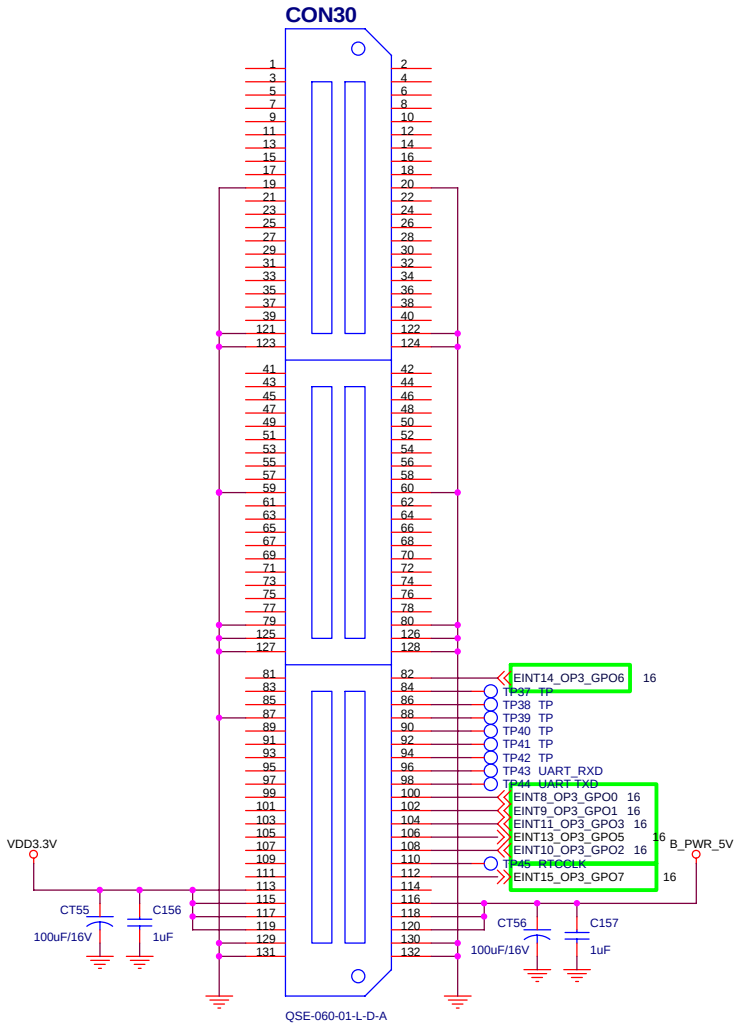
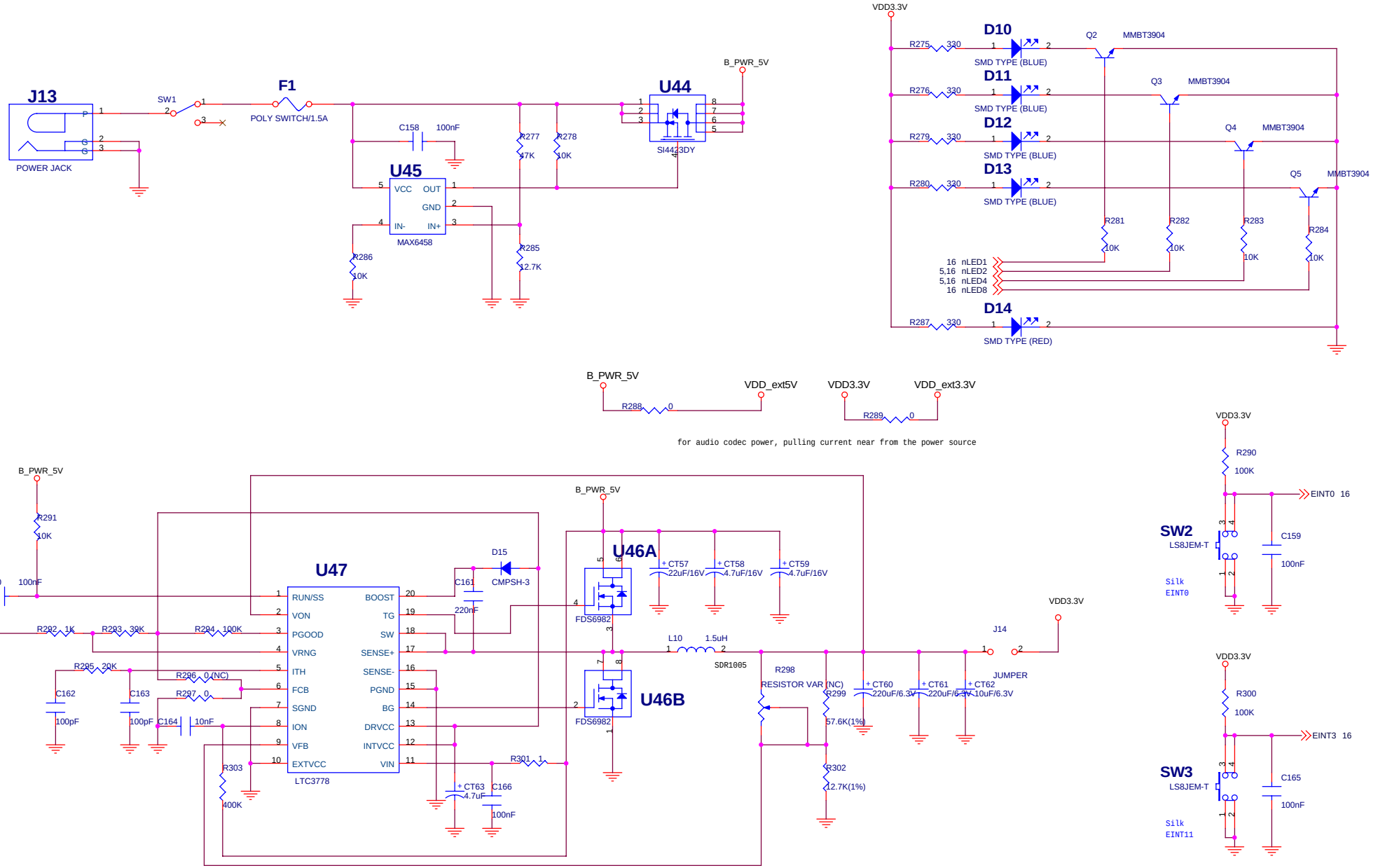
16

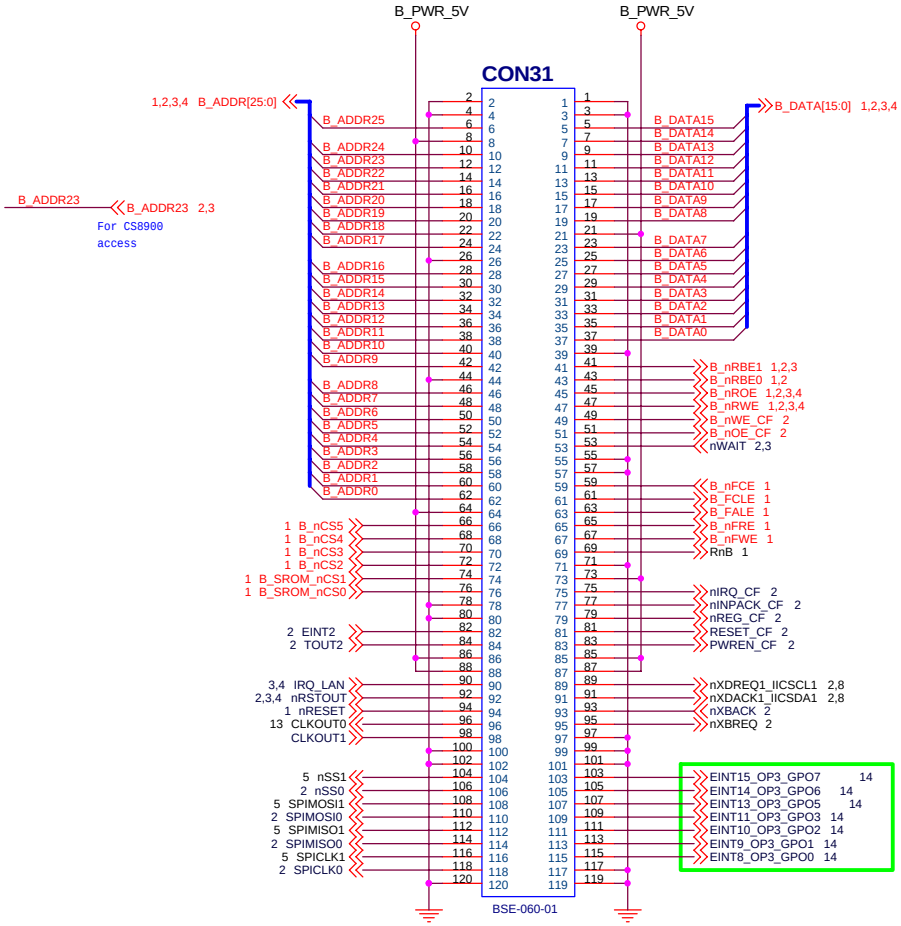


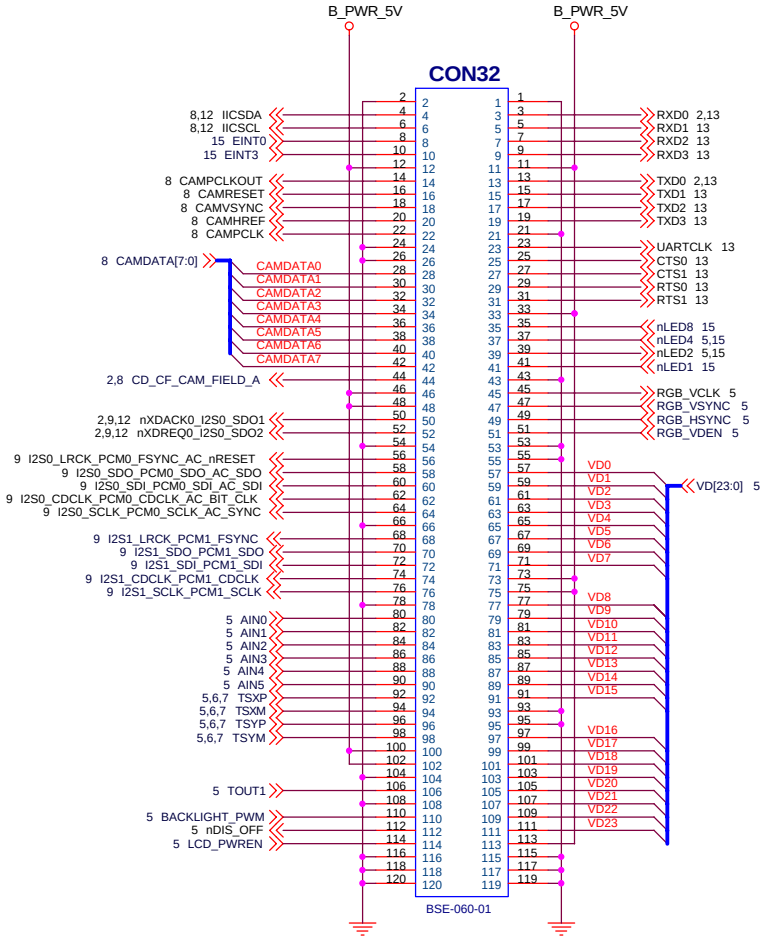

External I/O

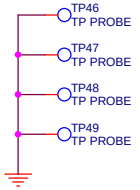
| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: External I/O | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 14 of 16 | |



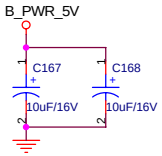

| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: Base board Power & LED | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 15 of 16 | |



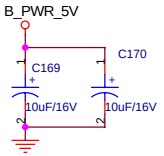




Place TPs to each corner








| | | |
|---|---|---|
| SAMSUNG ELECTRONICS CO.,LTD | | |
| Title: SMDK2450 (S3C2450 Evaluation Board) | | |
| Size: A3 | Document Number: Board to Board connector | Rev: 0.0 |
| Date: Friday, January 25, 2008 | Sheet 16 of 16 | |