SMDK2450 Evaluation Board for S3C2450X

1. PCB Revision

Revision	Date	Description
Rev 0.0	2007. 11. 22	Preliminary Version
Rev 0.1	2008. 2. 21	Modified in Cam/LCD(ref Red Circle/Rectangle)

2. Table of Contents

3. Part Reference

<Component><Number>

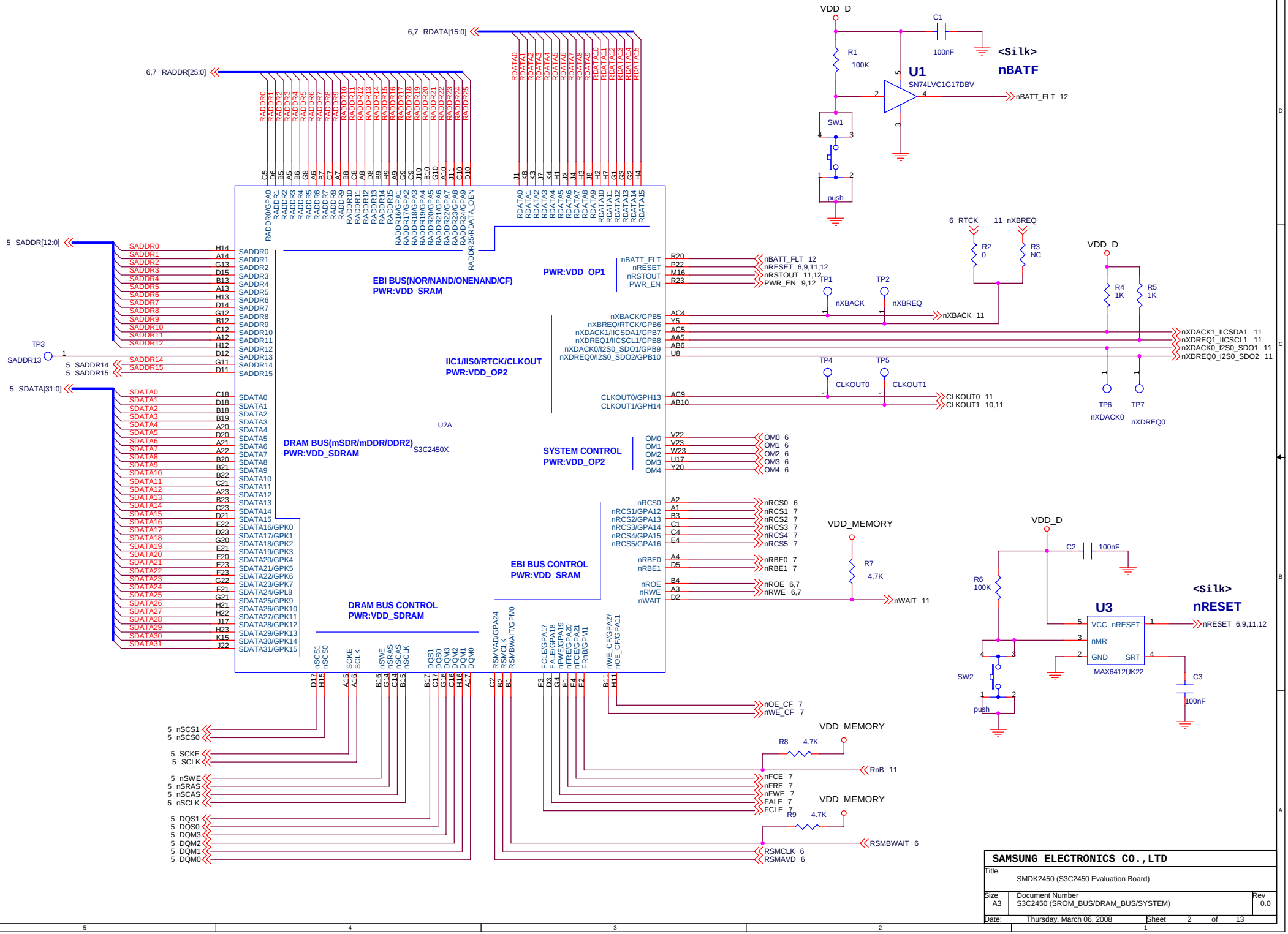
- U - COMPONENT IC & REGURATOR IC
- C - CAPACITOR
- CT- TANTAL CAPACITOR
- R - RESISTER
- RP - RESISTOR PACK
- VR - VARIABLE RESISTER
- J - JUMPER
- L - INDUCTOR
- F - FERRITE BEAD
- Y - OSCILLATOR
- X - CRYSTAL
- Q - TRANSISTOR/FET
- D - DIODE
- SW - TACT/PUSH SWITCH
- CON - CONNECTOR
- CFG - DIP SWITCH

SAMSUNG ELECTRONICS CO.,LTD

Title: SMDK2450 (S3C2450 Evaluation Board)

Size: A3 | Document Number: TITLE BLOCK | Rev: 0.1

Date: Thursday, March 06, 2008 | Sheet 1 of 13


6,7 RDATA[15:0]
6,7 RADDR[25:0]
5 SADDR[12:0]
5 SDATA[31:0]
SADDR13
5 SADDR14
5 SADDR15
TP3
EBI BUS(NOR/NAND/ONENAND/CF)
PWR:VDD_SRAM
PWR:VDD_OP1
IIC1/IIS0/RTCK/CLKOUT
PWR:VDD_OP2
U2A
S3C2450X
DRAM BUS(mSDR/mDDR/DDR2)
PWR:VDD_SDRAM
SYSTEM CONTROL
PWR:VDD_OP2
EBI BUS CONTROL
PWR:VDD_SRAM
DRAM BUS CONTROL
PWR:VDD_SDRAM
VDD_D
R1
100K
C1
100nF
U1
SN74LVC1G17DBV
<Silk>
nBATF
nBATT_FLT 12
SW1
push
6 RTCK
11 nXBREQ
R2
0
R3
NC
R4
1K
R5
1K
TP1
TP2
nXBACK
nXBREQ
nXBACK 11
TP4
TP5
CLKOUT0
CLKOUT1
TP6
TP7
nXDACK0
nXDREQ0
nXDACK1_IICSDA1 11
nXDREQ1_IICSCL1 11
nXDACK0_I2S0_SDO1 11
nXDREQ0_I2S0_SDO2 11
CLKOUT0 11
CLKOUT1 10,11
VDD_MEMORY
R7
4.7K
nWAIT 11
nOE_CF 7
nWE_CF 7
R8
4.7K
RnB 11
nFCE 7
nFRE 7
nFWE 7
FALE 7
FCLE 7
R9
4.7K
RSMBWAIT 6
RSMCLK 6
RSMAVD 6
R6
100K
C2
100nF
U3
MAX6412UK22
VCC
nRESET
nMR
GND
SRT
<Silk>
nRESET
nRESET 6,9,11,12
SW2
C3
100nF
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
S3C2450 (SROM_BUS/DRAM_BUS/SYSTEM)
Rev
0.0
Date:
Thursday, March 06, 2008
Sheet
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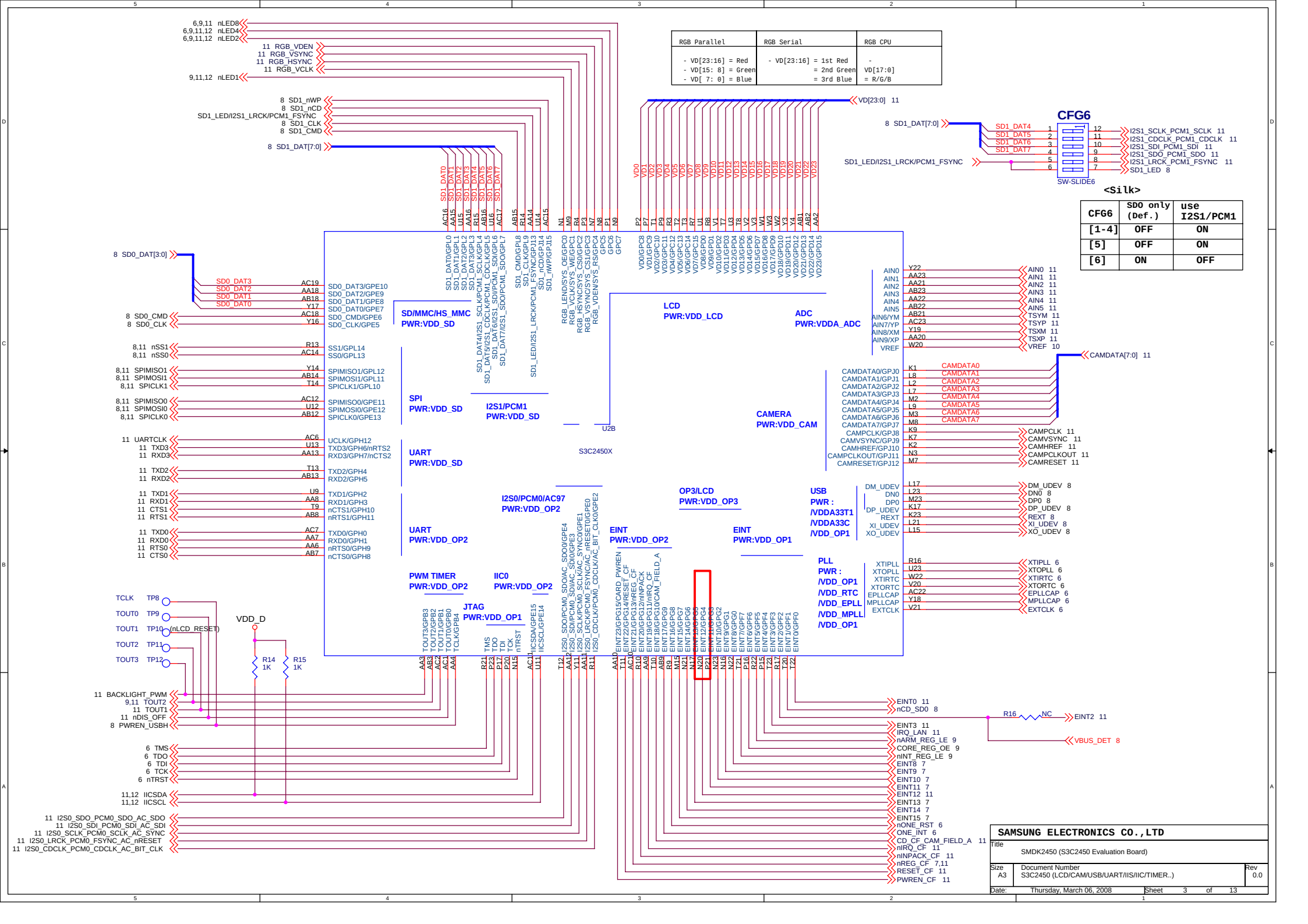
of
13


RGB Parallel
- VD[23:16] = Red
- VD[15: 8] = Green
- VD[7: 0] = Blue
RGB Serial
- VD[23:16] = 1st Red
= 2nd Green
= 3rd Blue
RGB CPU
-
VD[17:0]
= R/G/B
CFG6
SW-SLIDE6
<Silk>
CFG6 | SD0 only (Def.) | use I2S1/PCM1
[1-4] | OFF | ON
[5] | OFF | ON
[6] | ON | OFF
SD/MMC/HS_MMC
PWR:VDD_SD
SPI
PWR:VDD_SD
I2S1/PCM1
PWR:VDD_SD
UART
PWR:VDD_SD
I2S0/PCM0/AC97
PWR:VDD_OP2
UART
PWR:VDD_OP2
PWM TIMER
PWR:VDD_OP2
IIC0
PWR:VDD_OP2
JTAG
PWR:VDD_OP1
LCD
PWR:VDD_LCD
ADC
PWR:VDDA_ADC
CAMERA
PWR:VDD_CAM
OP3/LCD
PWR:VDD_OP3
USB
PWR :
/VDDA33T1
/VDDA33C
/VDD_OP1
EINT
PWR:VDD_OP2
EINT
PWR:VDD_OP1
PLL
PWR :
/VDD_OP1
/VDD_RTC
/VDD_EPLL
/VDD_MPLL
/VDD_OP1
U2B
S3C2450X
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
S3C2450 (LCD/CAM/USB/UART/IIS/IIC/TIMER..)
Rev
0.0
Date:
Thursday, March 06, 2008
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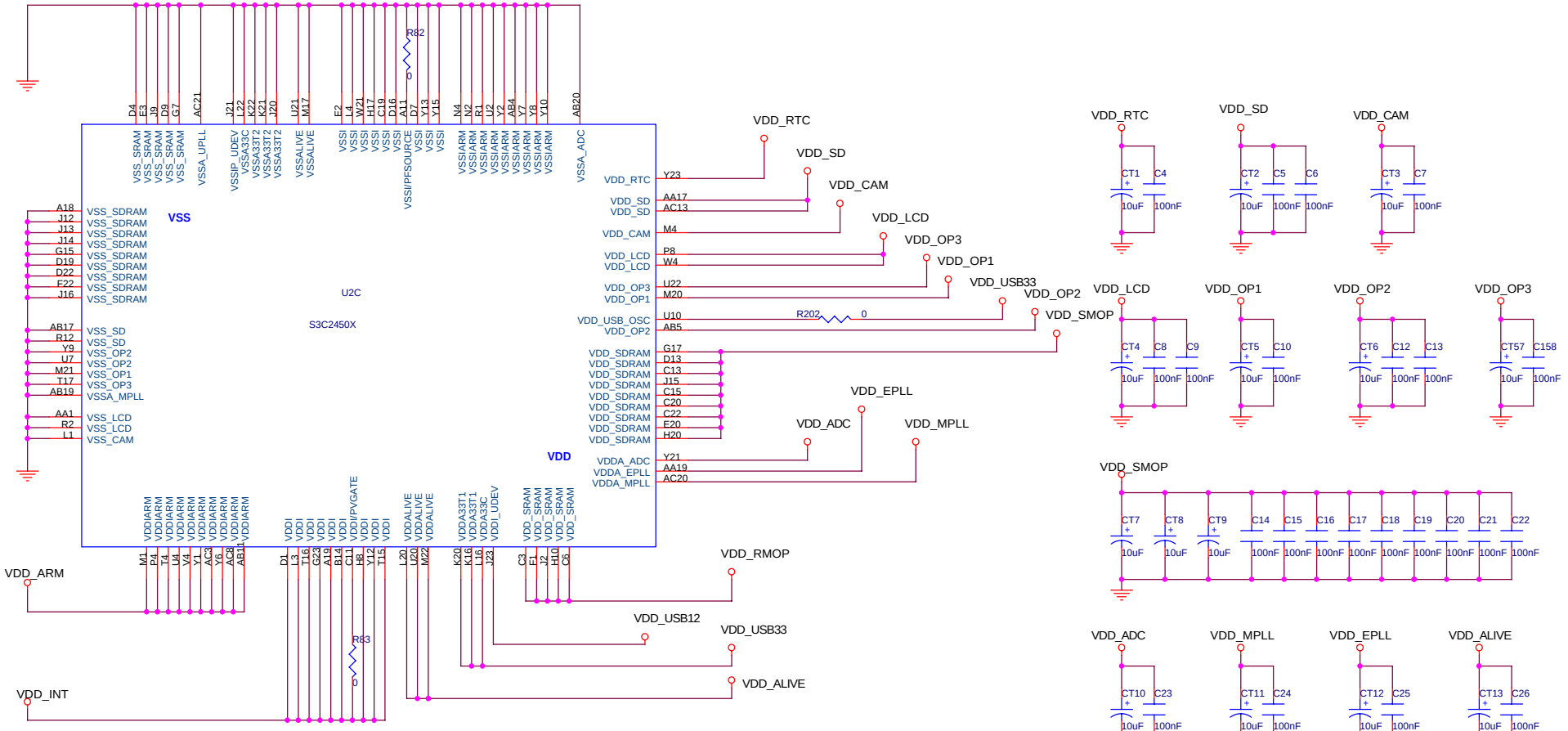
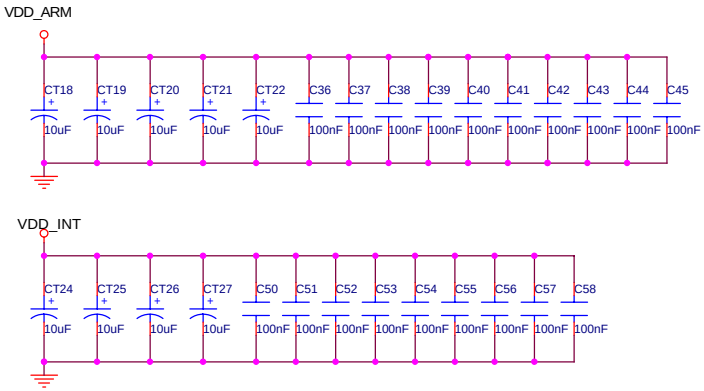
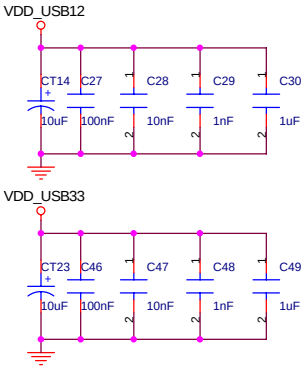
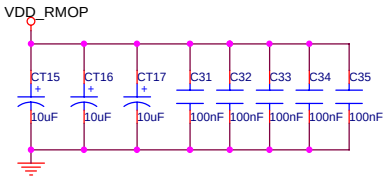
13

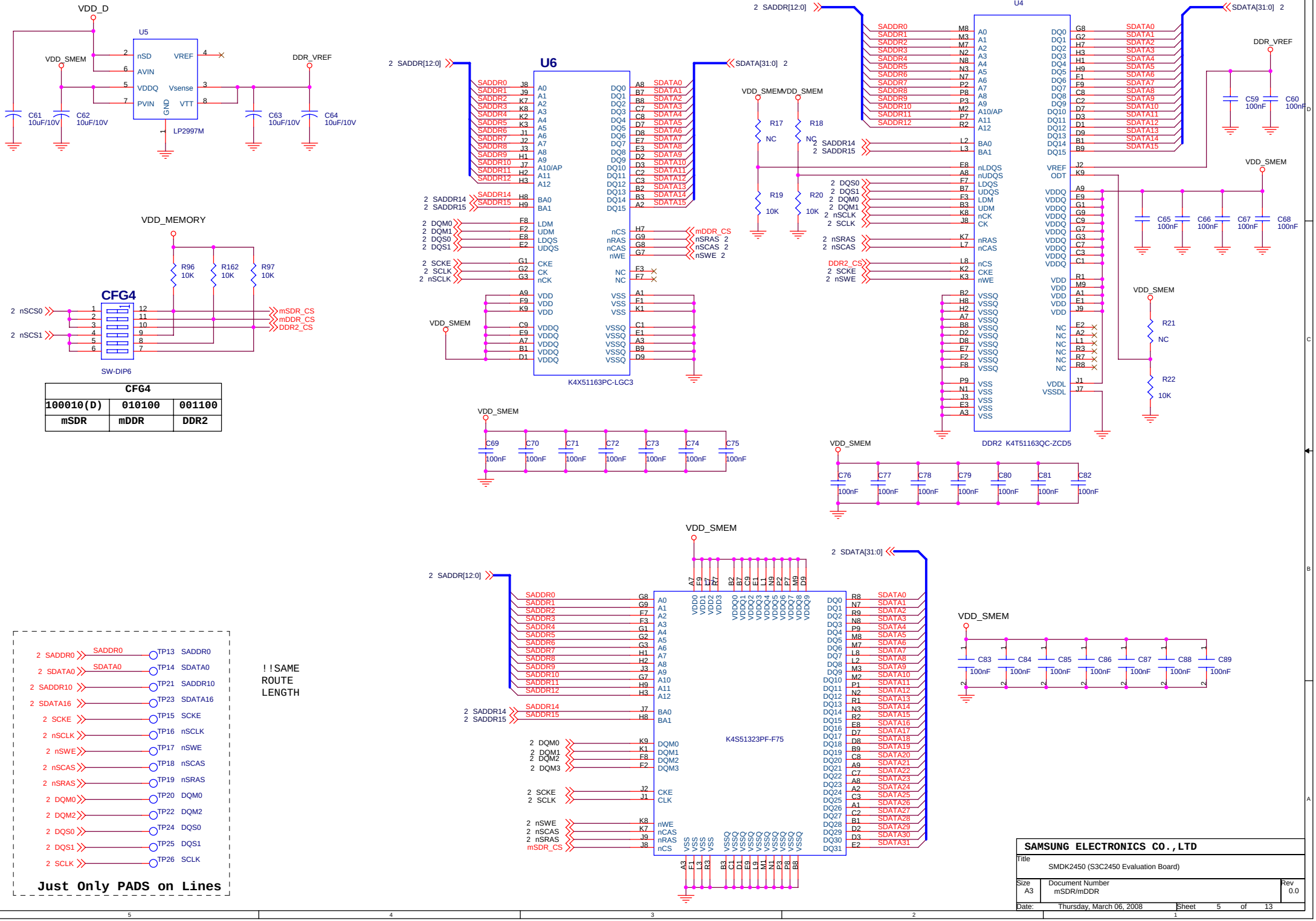








SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: S3C2450 (POWER)	Rev: 0.0
Date: Thursday, March 06, 2008	Sheet 4 of 13	


VDD_D
U5
VDD_SMEM
DDR_VREF
nSD
AVIN
VDDQ
PVIN
VREF
Vsense
VTT
GND
LP2997M
C61 10uF/10V
C62 10uF/10V
C63 10uF/10V
C64 10uF/10V
VDD_MEMORY
R96 10K
R162 10K
R97 10K
CFG4
2 nSCS0
2 nSCS1
mSDR_CS
mDDR_CS
DDR2_CS
SW-DIP6
CFG4
100010(D) 010100 001100
mSDR mDDR DDR2
U6
2 SADDR[12:0]
SDATA[31:0] 2
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
2 SADDR14 2 SADDR15
2 DQM0 2 DQM1 2 DQS0 2 DQS1
2 SCKE 2 SCLK 2 nSCLK
SDATA0 SDATA1 SDATA2 SDATA3 SDATA4 SDATA5 SDATA6 SDATA7 SDATA8 SDATA9 SDATA10 SDATA11 SDATA12 SDATA13 SDATA14 SDATA15
mDDR_CS
2 nSRAS
2 nSCAS
2 nSWE
K4X51163PC-LGC3
VDD_SMEM
C69 C70 C71 C72 C73 C74 C75 100nF
U4
VDD_SMEM/VDD_SMEM
R17 NC
R18 NC
R19 10K
R20 10K
DDR2_CS
DDR2 K4T51163QC-ZCD5
DDR_VREF
C59 C60 100nF
C65 C66 C67 C68 100nF
R21 NC
R22 10K
C76 C77 C78 C79 C80 C81 C82 100nF
2 SDATA[31:0]
K4S51323PF-F75
C83 C84 C85 C86 C87 C88 C89 100nF
SADDR0 SDATA0 SADDR10 SDATA16 SCKE nSCLK nSWE nSCAS nSRAS DQM0 DQM2 DQS0 DQS1 SCLK
TP13 TP14 TP21 TP23 TP15 TP16 TP17 TP18 TP19 TP20 TP22 TP24 TP25 TP26
Just Only PADS on Lines
!!SAME ROUTE LENGTH
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number mSDR/mDDR
Rev 0.0
Date: Thursday, March 06, 2008
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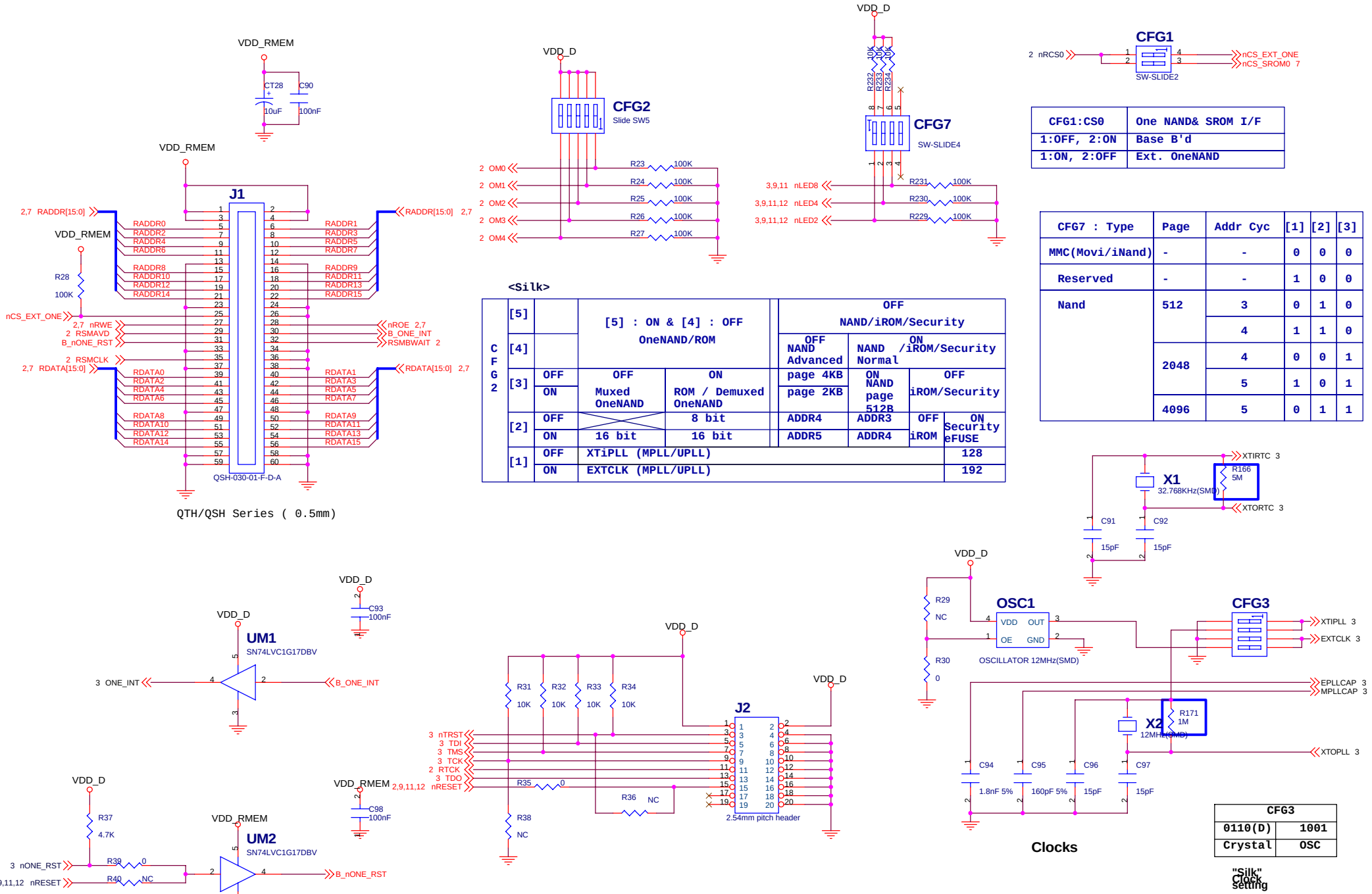


CFG1:CS0	One NAND& SROM I/F
1:OFF, 2:ON	Base B'd
1:ON, 2:OFF	Ext. OneNAND

CFG7 : Type	Page	Addr Cyc	[1]	[2]	[3]
MMC(Movi/iNand)	-	-	0	0	0
Reserved	-	-	1	0	0
Nand	512	3	0	1	0
		4	1	1	0
	2048	4	0	0	1
		5	1	0	1
	4096	5	0	1	1

CFG2					
[5]		[5] : ON & [4] : OFF OneNAND/ROM		OFF NAND/iROM/Security	
[4]				OFF NAND Advanced	ON NAND /iROM/Security Normal
[3]	OFF	OFF Muxed OneNAND	ON ROM / Demuxed OneNAND	page 4KB	ON NAND page 512B
	ON			page 2KB	OFF iROM/Security
[2]	OFF	8 bit		ADDR4	ADDR3
	ON	16 bit	16 bit	ADDR5	ADDR4
[1]	OFF	XTiPLL (MPLL/UPLL)			128
	ON	EXTCLK (MPLL/UPLL)			192

CFG3	
0110(D)	1001
Crystal	OSC

Clocks

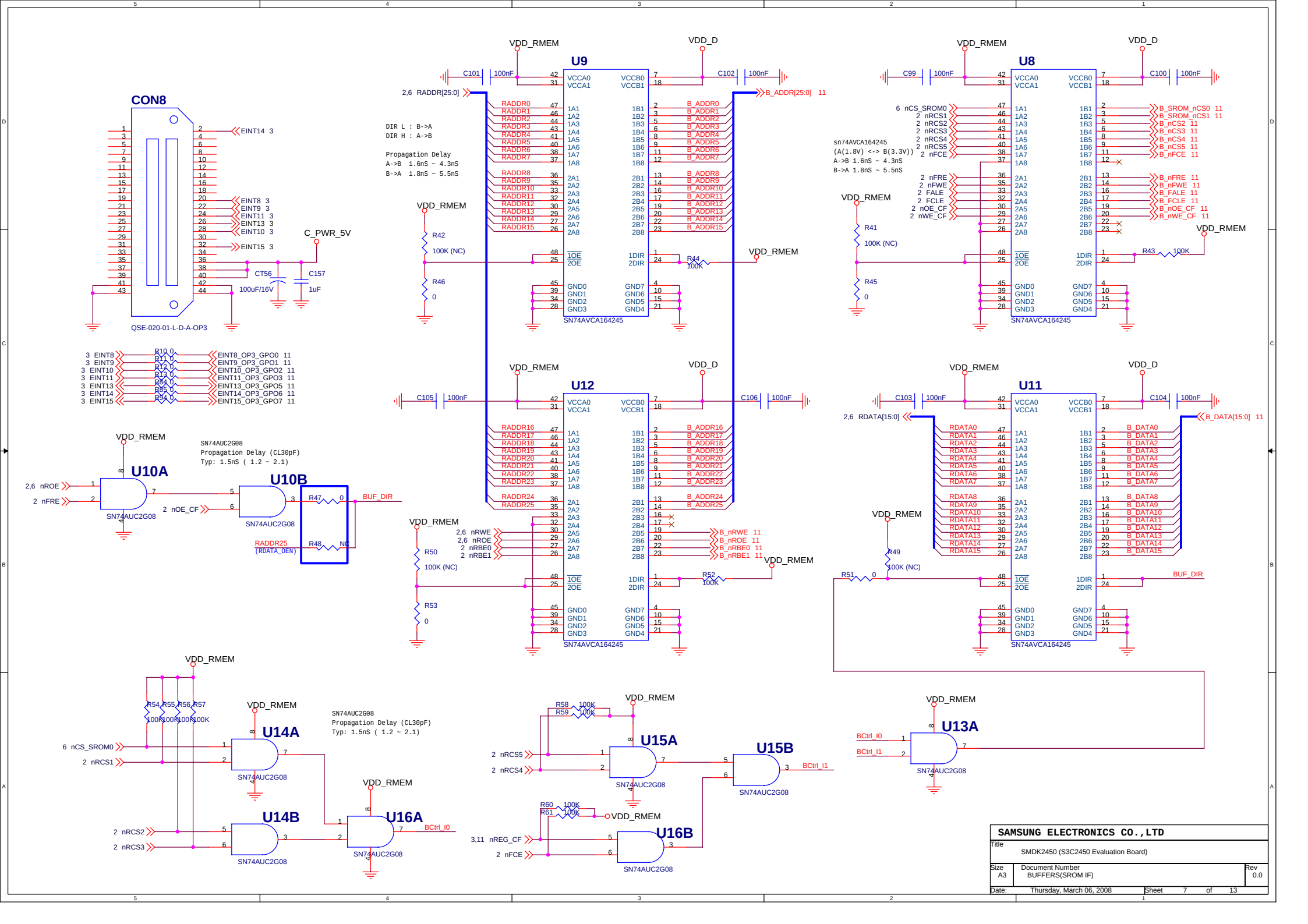
"Silk" Clock Setting

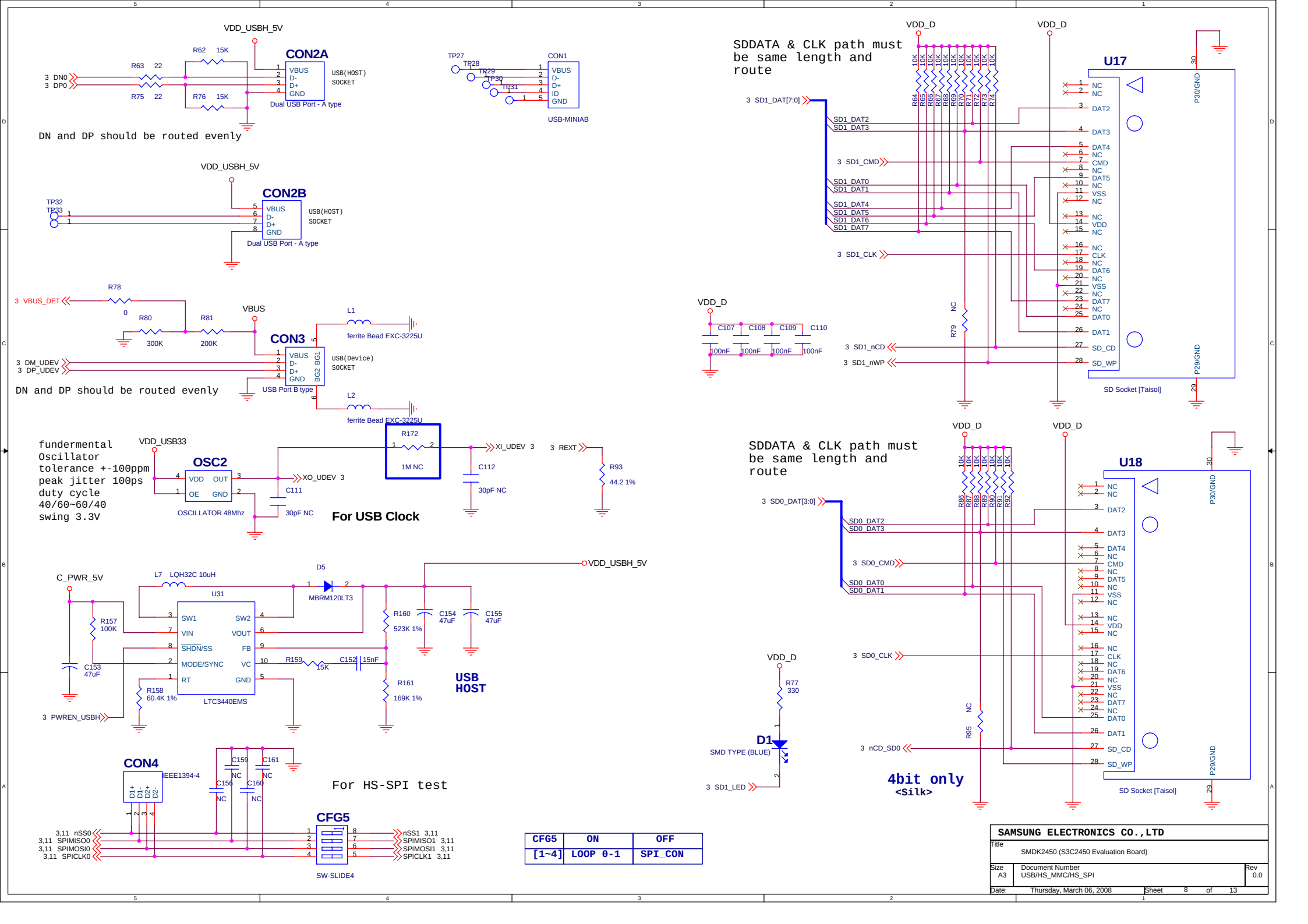
SAMSUNG ELECTRONICS CO.,LTD

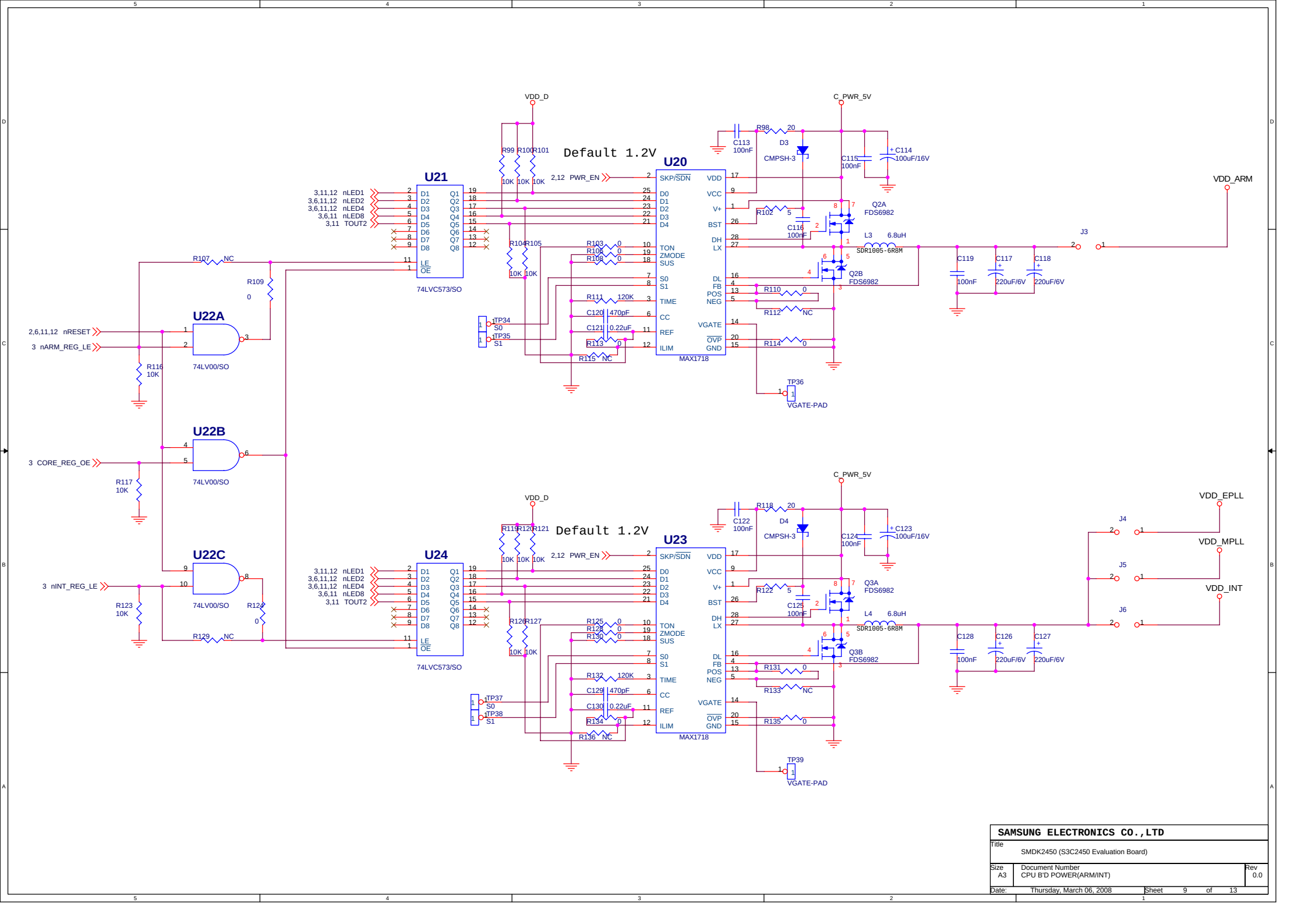
Title: SMDK2450 (S3C2450 Evaluation Board)

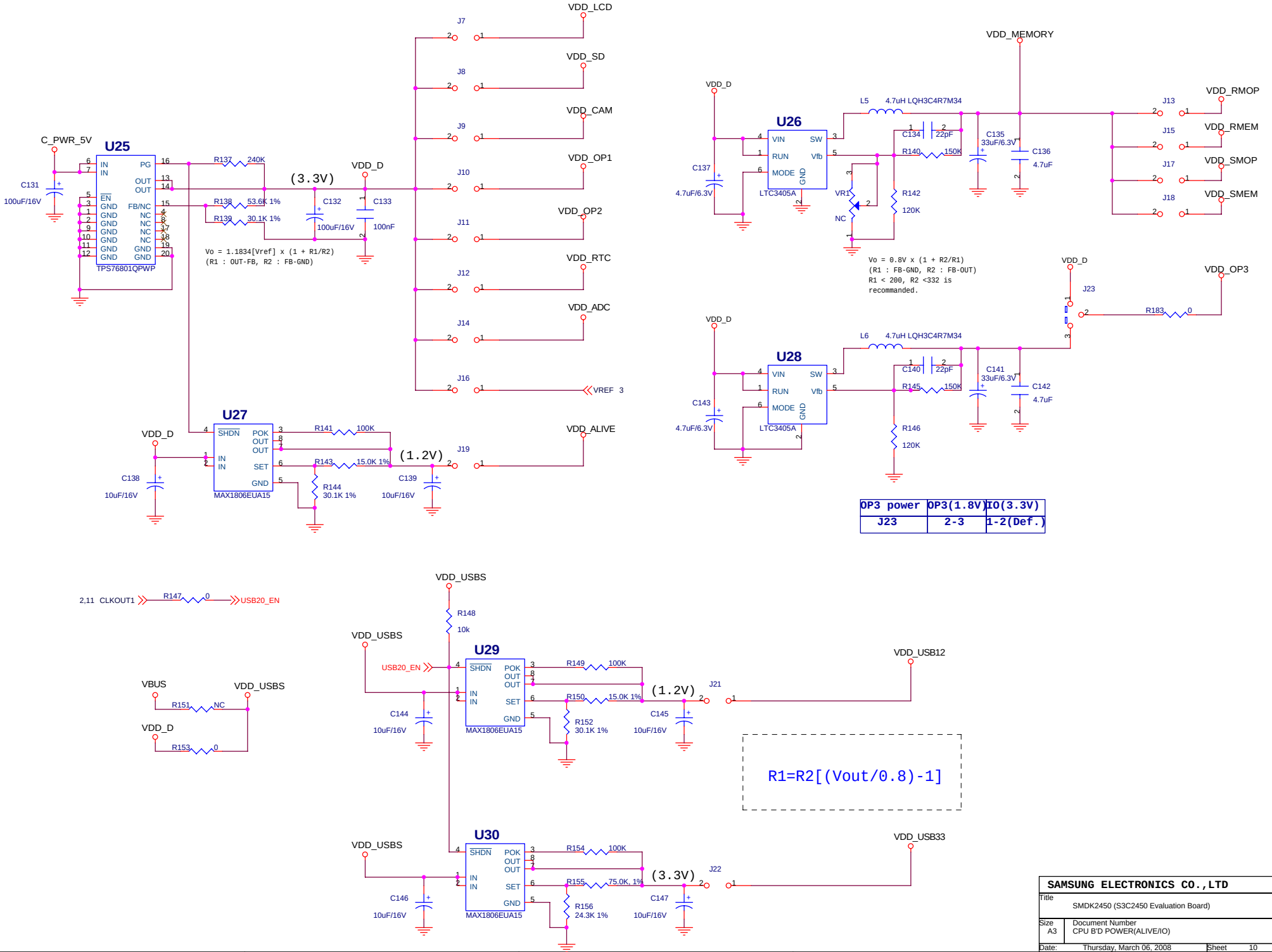
Size: A3 | Document Number: MEMORY(OneNAND)/JTAG/CLK | Rev: 0.0

Date: Thursday, March 06, 2008 | Sheet 6 of 13

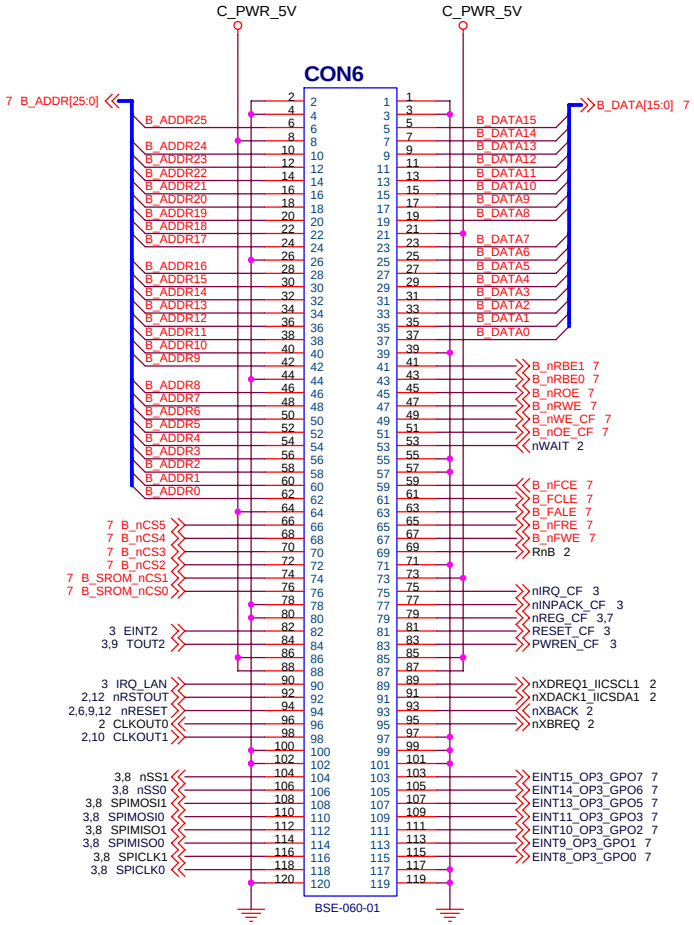

CON8
QSE-020-01-L-D-A-OP3
C_PWR_5V
CT56
100uF/16V
C157
1uF
U9
U8
U12
U11
SN74AVCA164245
VDD_RMEM
VDD_D
DIR L : B->A
DIR H : A->B
Propagation Delay
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
sn74AVCA164245
(A(1.8V) <-> B(3.3V))
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
U10A
U10B
U13A
U14A
U14B
U15A
U15B
U16A
U16B
SN74AUC2G08
Propagation Delay (CL30pF)
Typ: 1.5nS (1.2 ~ 2.1)
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
BUFFERS(SROM IF)
Thursday, March 06, 2008

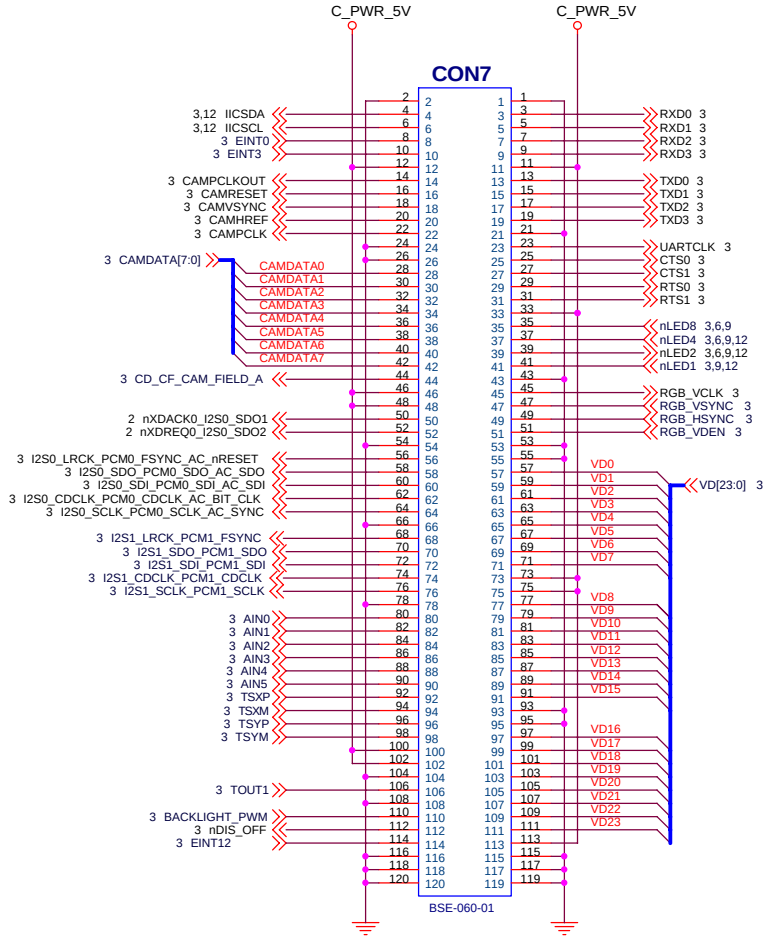

VDD_USBH_5V
R62 15K
R63 22
3 DN0
3 DP0
R75 22
R76 15K
CON2A
VBUS
D-
D+
GND
USB(HOST) SOCKET
Dual USB Port - A type
DN and DP should be routed evenly
TP27
TP28
TP29
TP30
TP31
CON1
VBUS
D-
D+
ID
GND
USB-MINIAB
VDD_USBH_5V
TP32
TP33
CON2B
VBUS
D-
D+
GND
USB(HOST) SOCKET
Dual USB Port - A type
R78
3 VBUS_DET
0
R80
300K
R81
200K
VBUS
CON3
VBUS
D-
D+
GND
BG2 BG1
USB(Device) SOCKET
USB Port B type
L1
ferrite Bead EXC-3225U
L2
ferrite Bead EXC-3225U
3 DM_UDEV
3 DP_UDEV
DN and DP should be routed evenly
fundermental
Oscillator
tolerance +-100ppm
peak jitter 100ps
duty cycle
40/60~60/40
swing 3.3V
VDD_USB33
OSC2
VDD
OUT
OE
GND
OSCILLATOR 48Mhz
XO_UDEV 3
C111
30pF NC
R172
1M NC
XI_UDEV 3
C112
30pF NC
3 REXT
R93
44.2 1%
For USB Clock
C_PWR_5V
L7 LQH32C 10uH
U31
SW1
SW2
VIN
VOUT
SHDN/SS
FB
MODE/SYNC
VC
RT
GND
LTC3440EMS
D5
MBRM120LT3
VDD_USBH_5V
R157
100K
C153
47uF
R158
60.4K 1%
3 PWREN_USBH
R159
15K
C152
15nF
R160
523K 1%
C154
47uF
C155
47uF
R161
169K 1%
USB HOST
CON4
IEEE1394-4
D1+
D1-
D2+
D2-
C159
NC
C161
NC
C156
NC
C160
NC
For HS-SPI test
CFG5
SW-SLIDE4
3,11 nSS0
3,11 SPIMISO0
3,11 SPIMOSI0
3,11 SPICLK0
nSS1 3,11
SPIMISO1 3,11
SPIMOSI1 3,11
SPICLK1 3,11
CFG5 | ON | OFF
[1~4] | LOOP 0-1 | SPI_CON
SDDATA & CLK path must be same length and route
VDD_D
R64 10K
R65 10K
R66 10K
R67 10K
R68 10K
R70 10K
R71 10K
R72 10K
R73 10K
R74 10K
3 SD1_DAT[7:0]
SD1_DAT2
SD1_DAT3
3 SD1_CMD
SD1_DAT0
SD1_DAT1
SD1_DAT4
SD1_DAT5
SD1_DAT6
SD1_DAT7
3 SD1_CLK
C107 100nF
C108 100nF
C109 100nF
C110 100nF
R79 NC
3 SD1_nCD
3 SD1_nWP
U17
NC
DAT2
DAT3
DAT4
CMD
DAT5
VSS
DAT7
DAT0
DAT1
SD_CD
SD_WP
VDD
CLK
P30/GND
P29/GND
SD Socket [Taisol]
SDDATA & CLK path must be same length and route
R86 10K
R87 10K
R88 10K
R89 10K
R90 10K
R91 10K
R92 10K
3 SD0_DAT[3:0]
SD0_DAT2
SD0_DAT3
3 SD0_CMD
SD0_DAT0
SD0_DAT1
3 SD0_CLK
R77 330
D1
SMD TYPE (BLUE)
3 SD1_LED
R95 NC
3 nCD_SD0
U18
4bit only
<Silk>
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number USB/HS_MMC/HS_SPI
Rev 0.0
Date: Thursday, March 06, 2008
Sheet 8 of 13

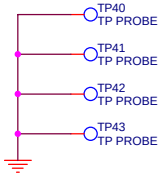

VDD_D
C_PWR_5V
Default 1.2V
U21
U20
74LVC573/SO
MAX1718
U22A
U22B
U22C
74LV00/SO
U24
U23
VDD_ARM
VDD_EPLL
VDD_MPLL
VDD_INT
VGATE-PAD
CMPSH-3
FDS6982
SDR1005-6R8M
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
CPU B'D POWER(ARM/INT)
Thursday, March 06, 2008
Sheet 9 of 13



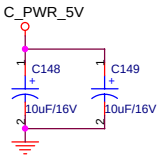
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: CPU B'D POWER(ALIVE/IO)	Rev: 0.0
Date: Thursday, March 06, 2008	Sheet 10 of 13	

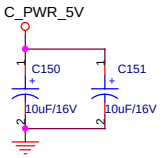




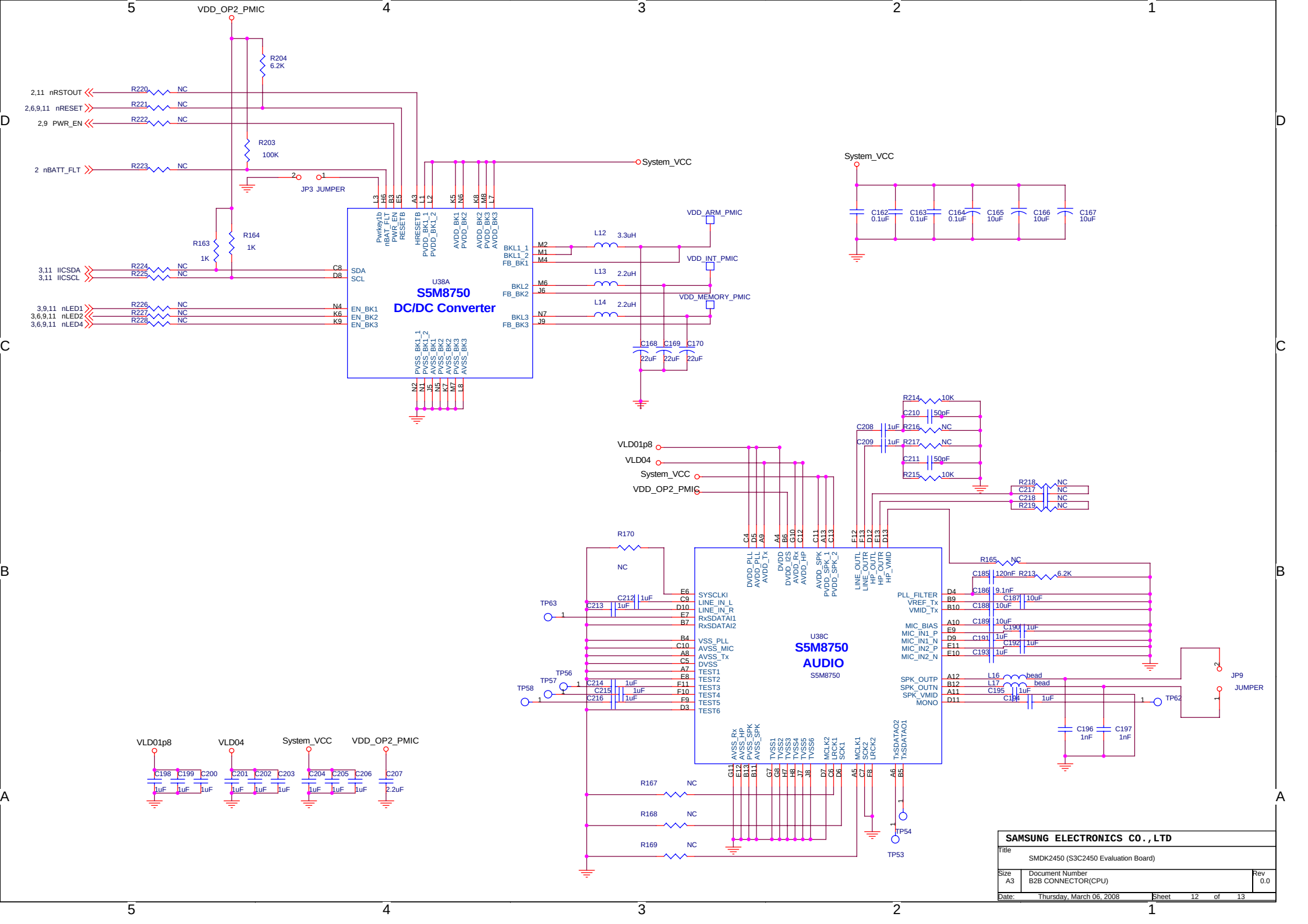


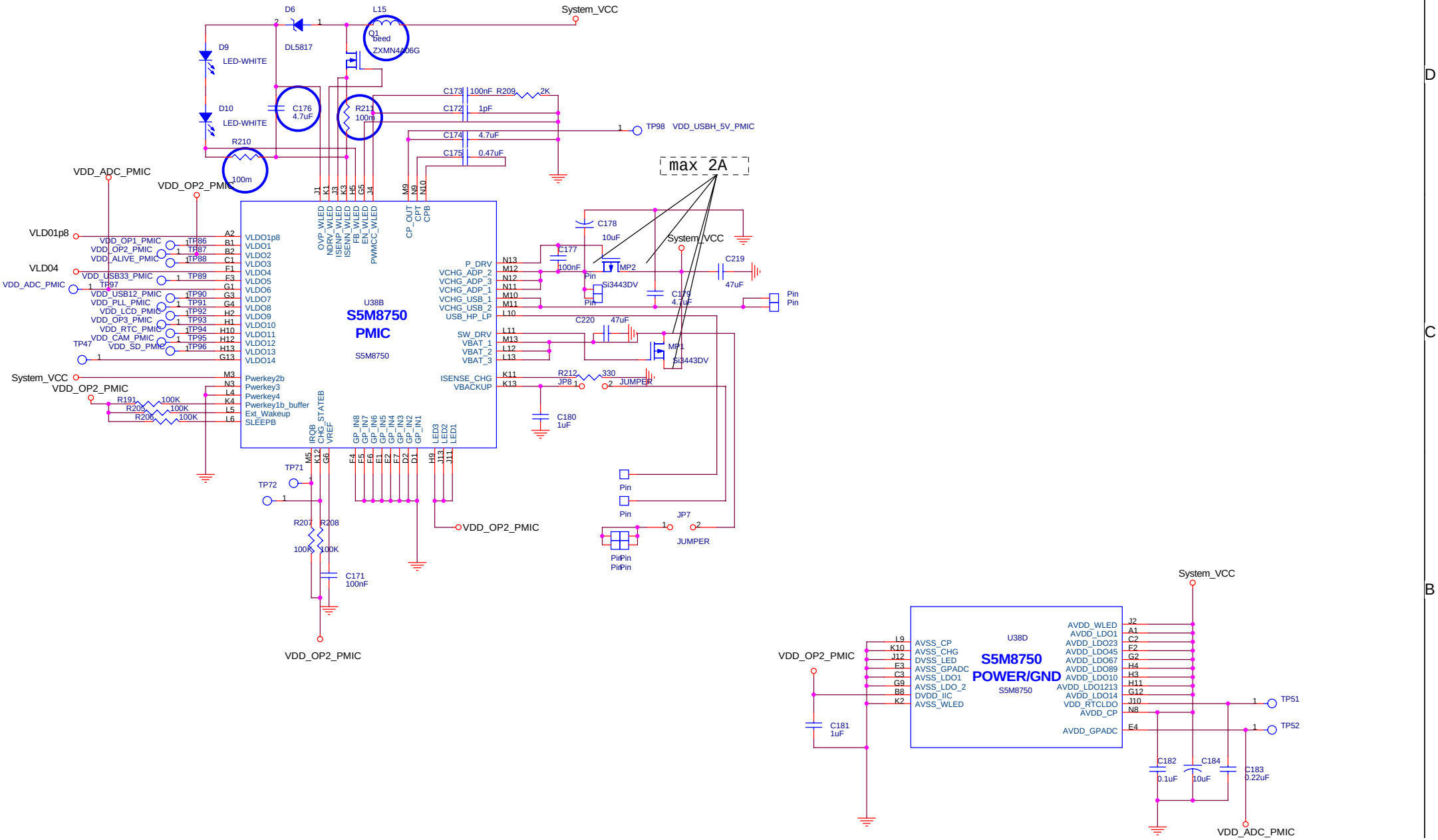
place TPs to each corner.





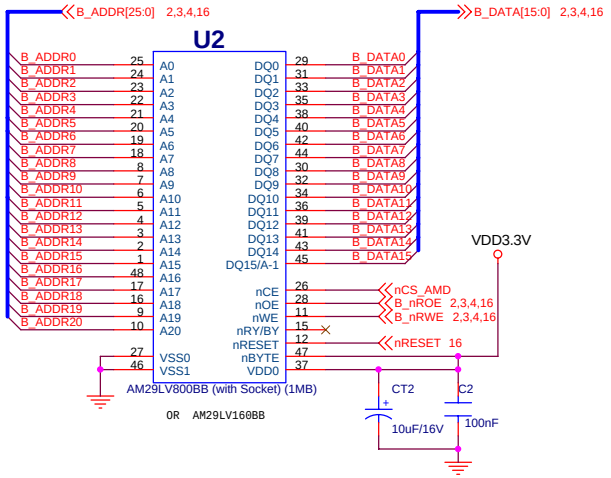
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: C0B. PMIC DC-DC/Audio	Rev: 0.0
Date: Thursday, March 06, 2008	Sheet 11 of 13	


VDD_OP2_PMIC
R204 6.2K
2,11 nRSTOUT
2,6,9,11 nRESET
2,9 PWR_EN
R220 NC
R221 NC
R222 NC
R203 100K
2 nBATT_FLT
R223 NC
JP3 JUMPER
System_VCC
R163 1K
R164 1K
3,11 IICSDA
3,11 IICSCL
R224 NC
R225 NC
3,9,11 nLED1
3,6,9,11 nLED2
3,6,9,11 nLED4
R226 NC
R227 NC
R228 NC
U38A
S5M8750
DC/DC Converter
SDA
SCL
EN_BK1
EN_BK2
EN_BK3
Pwrkey1b
nBAT_FLT
PWR_EN
RESETB
HRESETB
PVDD_BK1_1
PVDD_BK1_2
PVDD_BK2
AVDD_BK1
PVDD_BK2
AVDD_BK2
PVDD_BK3
AVDD_BK3
BKL1_1
BKL1_2
FB_BK1
BKL2
FB_BK2
BKL3
FB_BK3
PVSS_BK1_1
PVSS_BK1_2
AVSS_BK1
PVSS_BK2
AVSS_BK2
PVSS_BK3
AVSS_BK3
L12 3.3uH
L13 2.2uH
L14 2.2uH
VDD_ARM_PMIC
VDD_INT_PMIC
VDD_MEMORY_PMIC
C168 22uF
C169 22uF
C170 22uF
C162 0.1uF
C163 0.1uF
C164 0.1uF
C165 10uF
C166 10uF
C167 10uF
VLD01p8
VLD04
R214 10K
C210 50pF
C208 1uF
R216 NC
C209 1uF
R217 NC
C211 50pF
R215 10K
R218 NC
C217 NC
C218 NC
R219 NC
R170 NC
C212 1uF
C213 1uF
TP63
TP56
TP57
TP58
C214 1uF
C215 1uF
C216 1uF
U38C
S5M8750
AUDIO
S5M8750
SYSCLKI
LINE_IN_L
LINE_IN_R
RxSDATAI1
RxSDATAI2
VSS_PLL
AVSS_MIC
AVSS_Tx
DVSS
TEST1
TEST2
TEST3
TEST4
TEST5
TEST6
DVDD_PLL
AVDD_PLL
AVDD_Tx
DVDD
DVDD_I2S
AVDD_Rx
AVDD_HP
AVDD_SPK
PVDD_SPK_1
PVDD_SPK_2
LINE_OUTL
LINE_OUTR
HP_OUTL
HP_OUTR
HP_VMID
PLL_FILTER
VREF_Tx
VMID_Tx
MIC_BIAS
MIC_IN1_P
MIC_IN1_N
MIC_IN2_P
MIC_IN2_N
SPK_OUTP
SPK_OUTN
SPK_VMID
MONO
AVSS_Rx
AVSS_HP
PVSS_SPK
AVSS_SPK
TVSS1
TVSS2
TVSS3
TVSS4
TVSS5
TVSS6
MCLK2
LRCK1
SCK1
MCLK1
SCK2
LRCK2
TxSDATAO2
TxSDATAO1
R165 NC
C185 120nF
R213 6.2K
C186 9.1nF
C187 10uF
C188 10uF
C189 10uF
C190 1uF
C191 1uF
C192 1uF
C193 1uF
L16 bead
L17 bead
C195 1uF
C194 1uF
TP62
JP9
JUMPER
C196 1nF
C197 1nF
R167 NC
R168 NC
R169 NC
TP54
TP53
C198 1uF
C199 1uF
C200 1uF
C201 1uF
C202 1uF
C203 1uF
C204 1uF
C205 1uF
C206 1uF
C207 2.2uF
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number B2B CONNECTOR(CPU)
Rev 0.0
Date: Thursday, March 06, 2008
Sheet 12 of 13

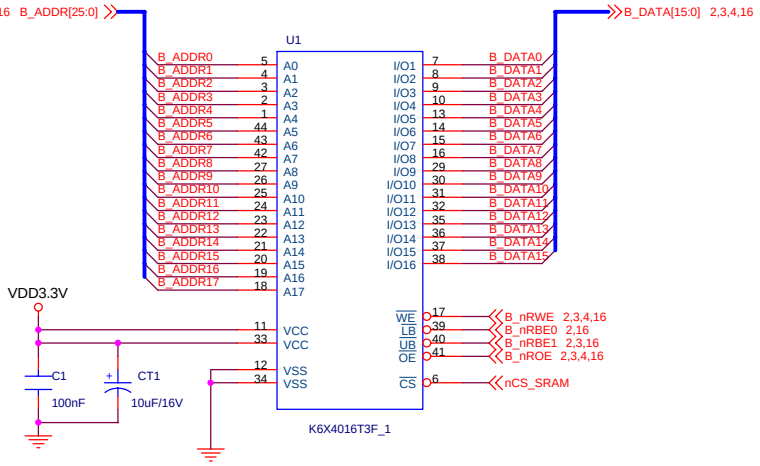


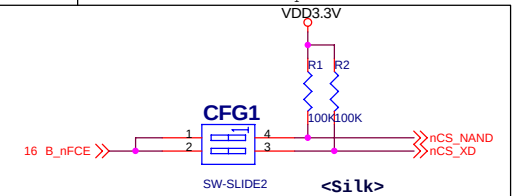
SAMSUNG ELECTRONICS CO.,LTD	
Title	SMDK2450 (S3C2450 Evaluation Board)
Size A3	Document Number PMIC Power
Rev	0.0
Date: Thursday, March 06, 2008	Sheet 13 of 13

AMD Flash Memory(SOCKET)



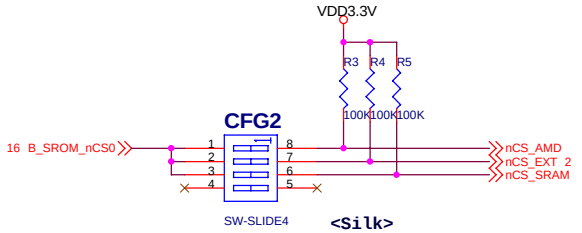
SRAM





<Silk>

CFG1: nFCE	SROM Selector
[2]	XD card
[1]	NAND



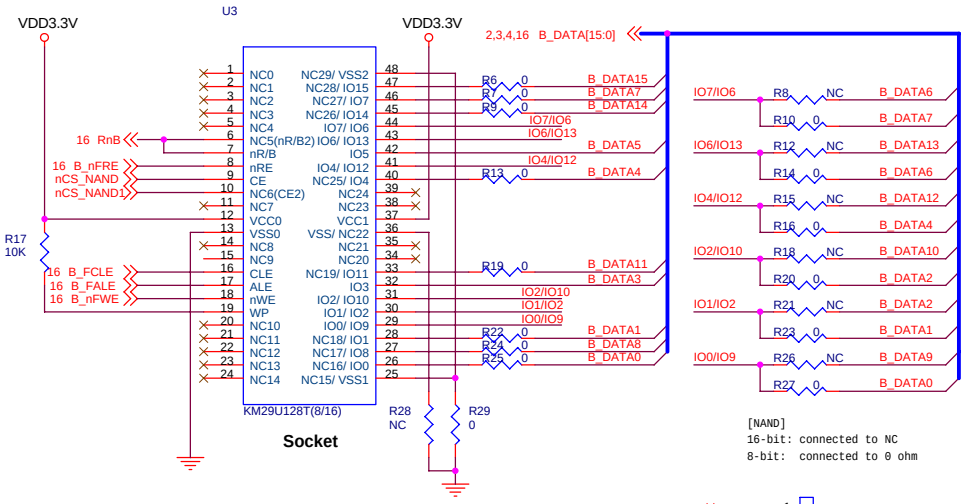
<Silk>

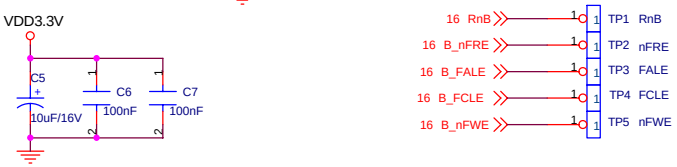
CFG2: nCS0	SROM Selector
[3]	External
[2]	SRAM
[1]	NOR(AMD)

S3C2450
Addition : NAND CS1 & RnB1

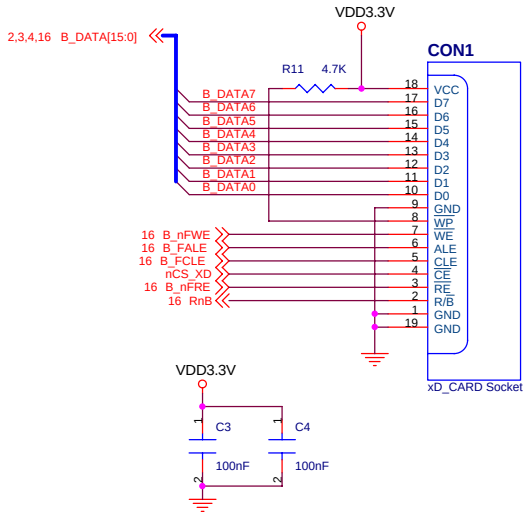
S3C2450
Addition : NAND CS1
SW(To Select Ethernet or Additional Nand CS)

NAND Flash memory (SOCKET)



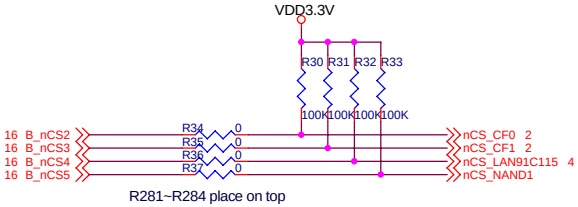


XD PICTURE CARD



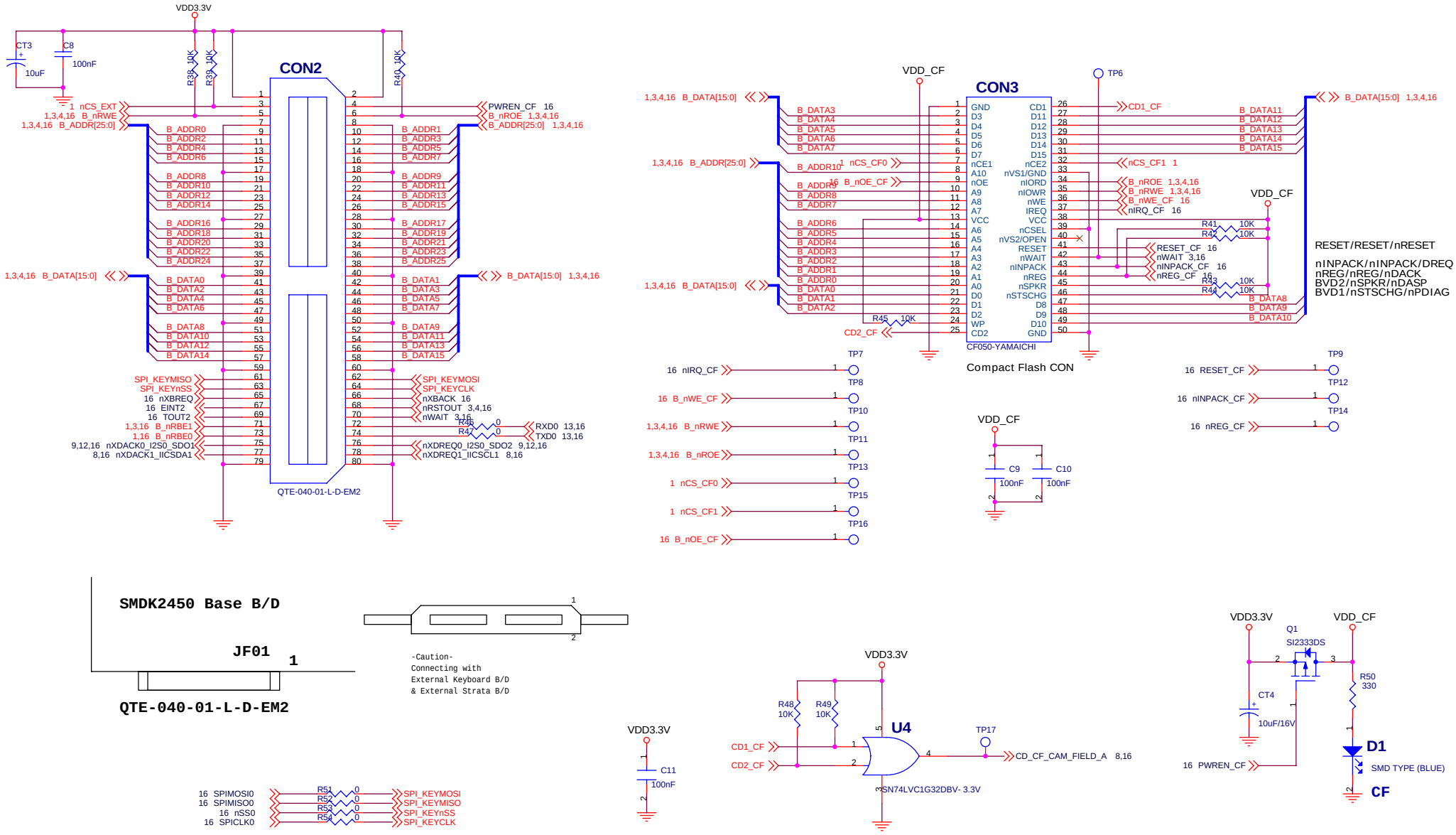
<Silk>

CFG3: nCS1	SROM Selector
[6]	CS8900(CS1)
[5]	SRAM
[4]	External
[3]	XD card
[2]	NAND
[1]	NOR(AMD)

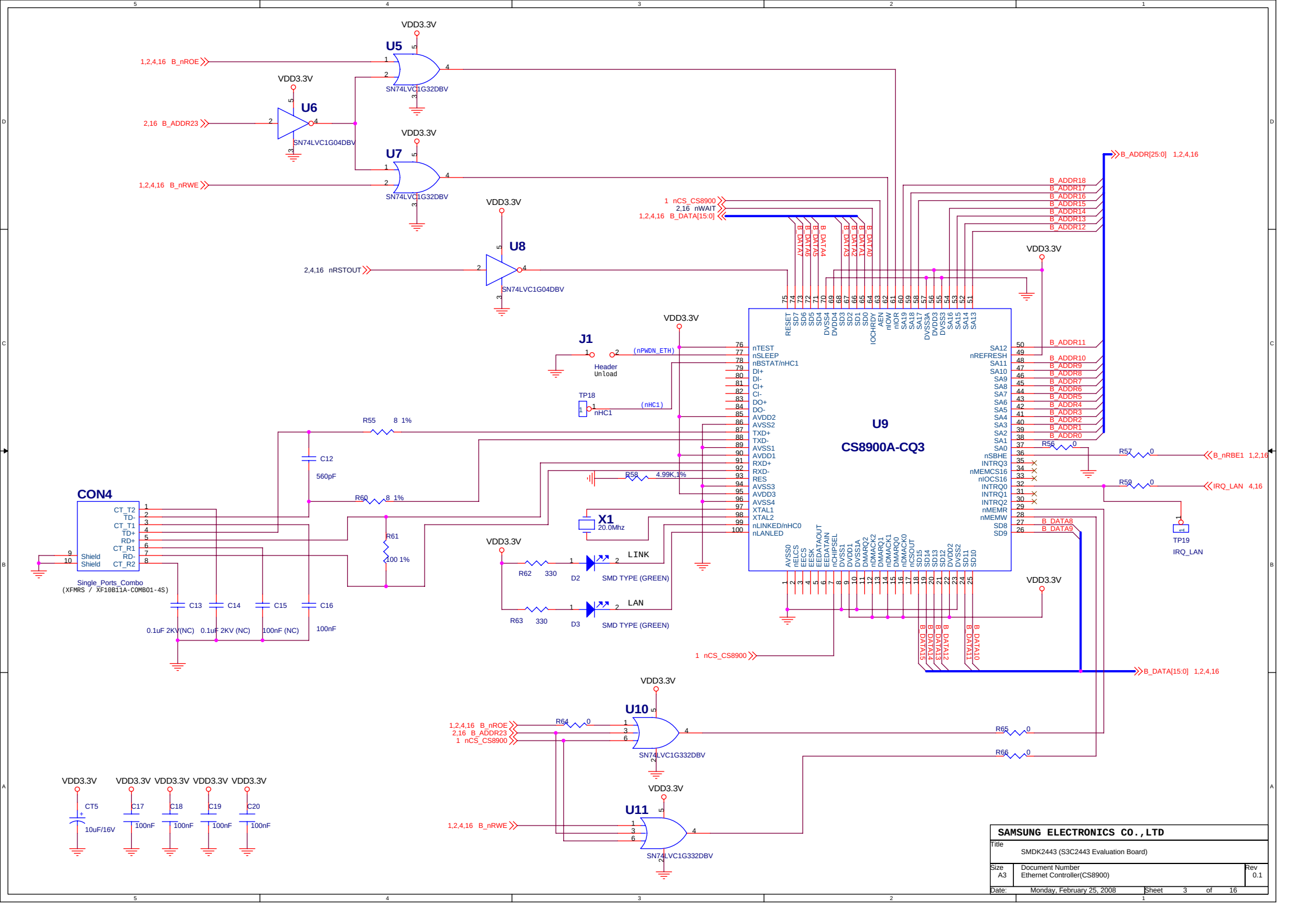


R281~R284 place on top

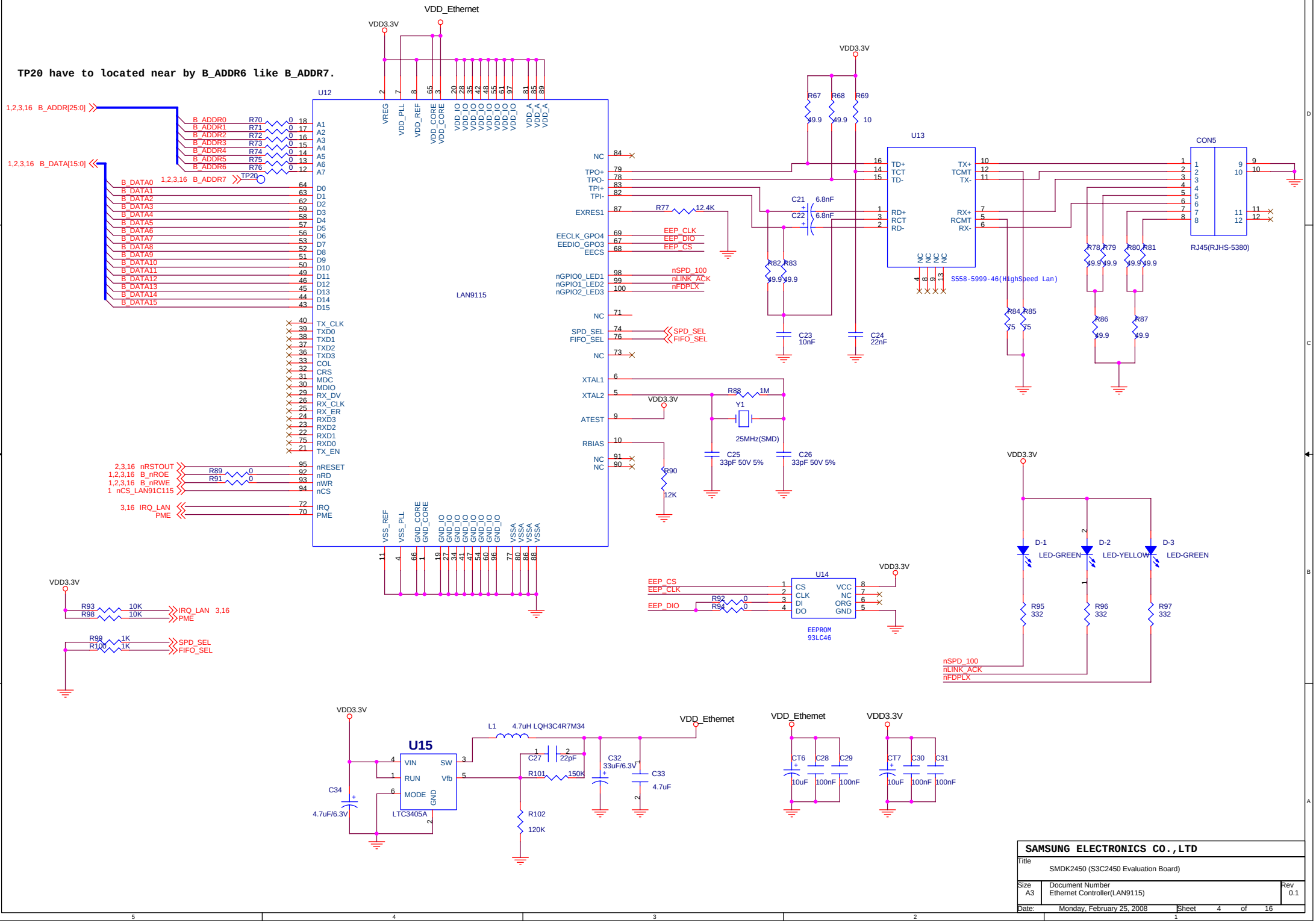
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: NOR/NAND/SRAM/CONFIG	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 1 of 16	



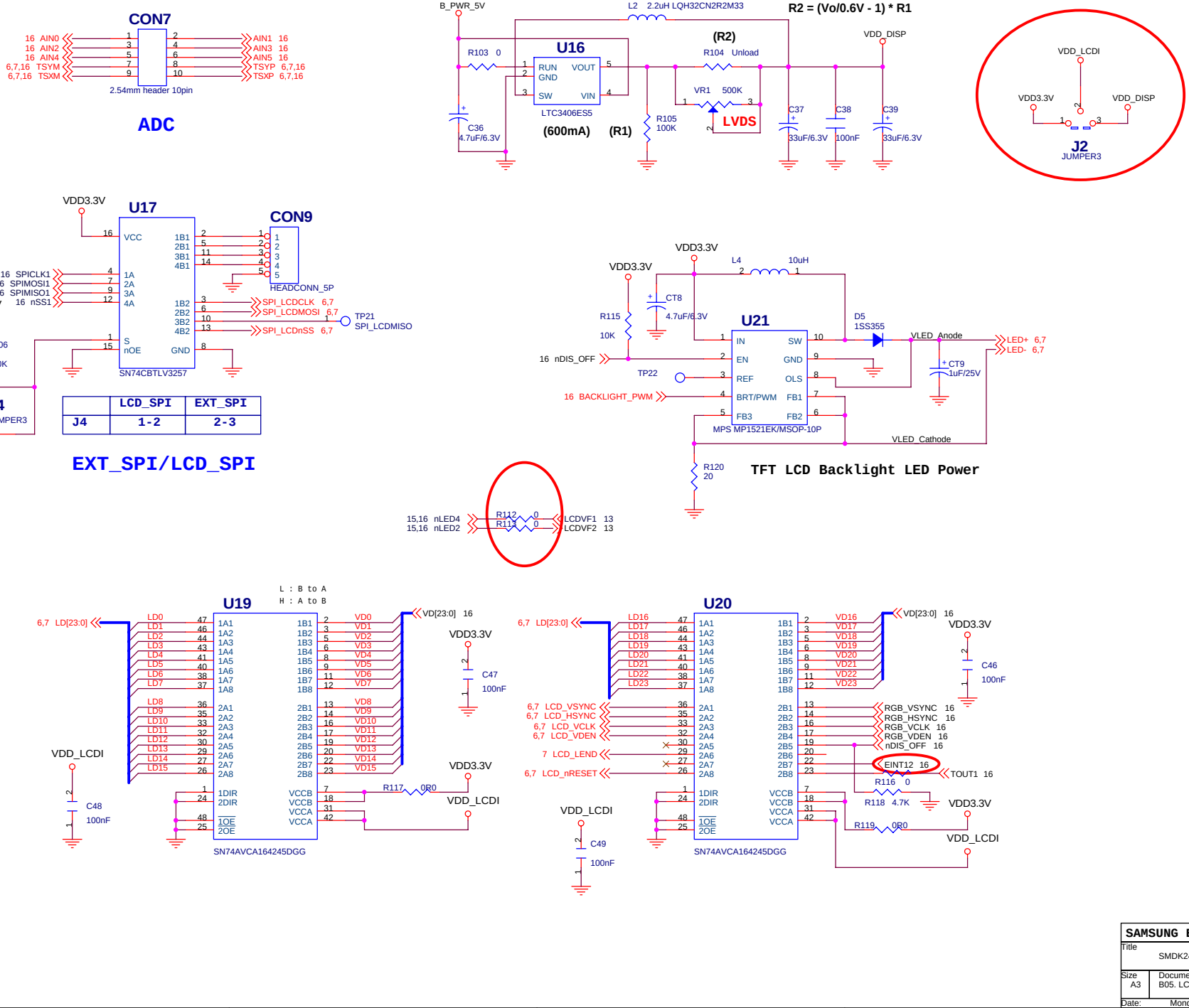
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: External Bus connector & CF interface	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 2 of 16	

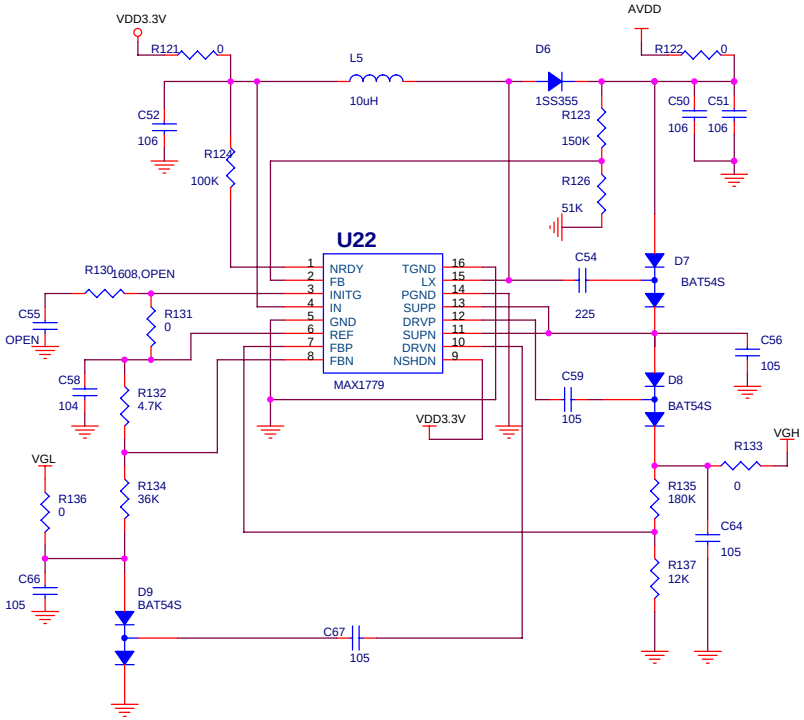

U5
SN74LVC1G32DBV
U6
SN74LVC1G04DBV
U7
SN74LVC1G32DBV
U8
SN74LVC1G04DBV
U9
CS8900A-CQ3
U10
SN74LVC1G332DBV
U11
SN74LVC1G332DBV
VDD3.3V
1,2,4,16 B_nROE
2,16 B_ADDR23
1,2,4,16 B_nRWE
2,4,16 nRSTOUT
1 nCS_CS8900
2,16 nWAIT
1,2,4,16 B_DATA[15:0]
B_ADDR[25:0] 1,2,4,16
J1
Header
Unload
(nPWDN_ETH)
TP18
nHC1
(nHC1)
R55 8 1%
R58 4.99K,1%
R60 8 1%
R61 100 1%
C12 560pF
X1 20.0Mhz
CON4
Single_Ports_Combo
(XFMRS / XF10B11A-COMB01-4S)
C13 0.1uF 2KV(NC)
C14 0.1uF 2KV (NC)
C15 100nF (NC)
C16 100nF
R62 330
R63 330
D2 SMD TYPE (GREEN)
D3 SMD TYPE (GREEN)
LINK
LAN
R56 0
R57 0
R59 0
B_nRBE1 1,2,16
IRQ_LAN 4,16
TP19
IRQ_LAN
R64 0
R65 0
R66 0
CT5 10uF/16V
C17 100nF
C18 100nF
C19 100nF
C20 100nF
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2443 (S3C2443 Evaluation Board)
Size A3
Document Number
Ethernet Controller(CS8900)
Rev 0.1
Date: Monday, February 25, 2008
Sheet 3 of 16

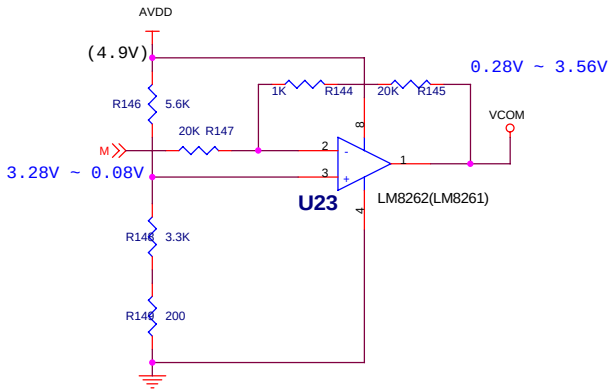
TP20 have to located near by B_ADDR6 like B_ADDR7.

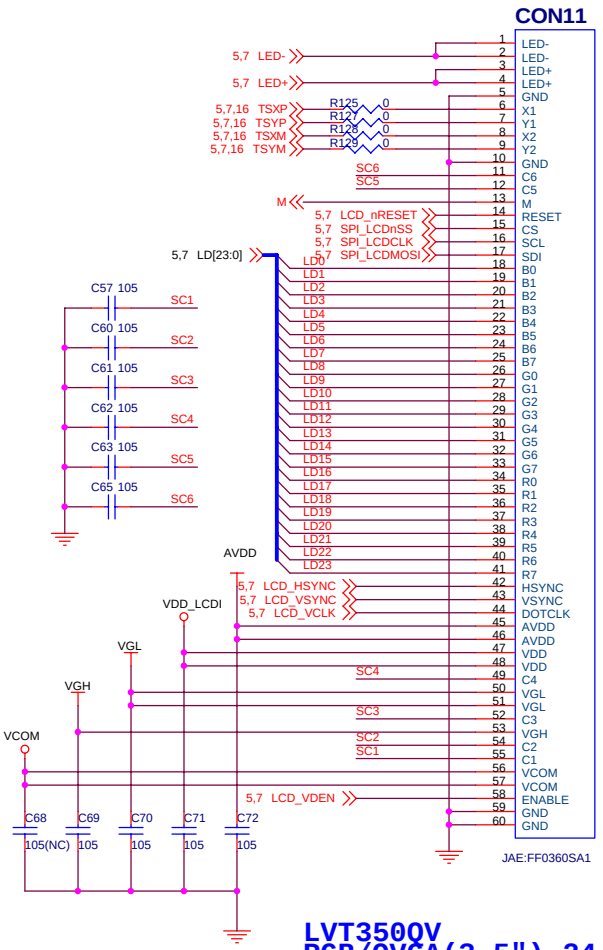


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Ethernet Controller(LAN9115)	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 4 of 16	

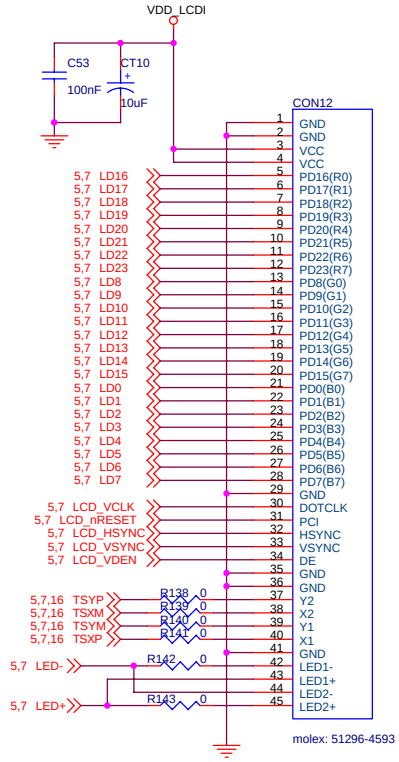

CON7
16 AIN0
16 AIN2
16 AIN4
6,7,16 TSYM
6,7,16 TSXM
AIN1 16
AIN3 16
AIN5 16
TSYP 6,7,16
TSXP 6,7,16
2.54mm header 10pin
ADC
B_PWR_5V
L2 2.2uH LQH32CN2R2M33
U16
R103 0
RUN
GND
SW
VOUT
VIN
LTC3406ES5
C36
4.7uF/6.3V
(600mA)
(R1)
R105
100K
(R2)
R104 Unload
VR1 500K
LVDS
VDD_DISP
C37
33uF/6.3V
C38
100nF
C39
33uF/6.3V
Vo = 0.6V * (1+R2/R1)= 2.8V
R2 = (Vo/0.6V - 1) * R1
VDD_LCDI
VDD3.3V
VDD_DISP
J2
JUMPER3
VDD3.3V
U17
CON9
16 SPICLK1
16 SPIMOSI1
16 SPIMISO1
16 nSS1
SPI_LCDCLK 6,7
SPI_LCDMOSI 6,7
SPI_LCDnSS 6,7
TP21
SPI_LCDMISO
HEADCONN_5P
SN74CBTLV3257
R106
100K
J4
JUMPER3
LCD_SPI
EXT_SPI
J4
1-2
2-3
EXT_SPI/LCD_SPI
VDD3.3V
L4
10uH
CT8
4.7uF/6.3V
R115
10K
U21
D5
1SS355
VLED_Anode
LED+ 6,7
LED- 6,7
CT9
1uF/25V
16 nDIS_OFF
TP22
16 BACKLIGHT_PWM
IN
EN
REF
BRT/PWM
FB3
SW
GND
OLS
FB1
FB2
MPS MP1521EK/MSOP-10P
VLED_Cathode
R120
20
TFT LCD Backlight LED Power
15,16 nLED4
15,16 nLED2
R112 0
R113 0
LCDVF1 13
LCDVF2 13
L : B to A
H : A to B
U19
6,7 LD[23:0]
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
LD11
LD12
LD13
LD14
LD15
1DIR
2DIR
1OE
2OE
VCCB
VCCA
VD[23:0] 16
VD0
VD1
VD2
VD3
VD4
VD5
VD6
VD7
VD8
VD9
VD10
VD11
VD12
VD13
VD14
VD15
VDD3.3V
C47
100nF
R117
0R0
VDD_LCDI
C48
100nF
SN74AVCA164245DGG
U20
6,7 LD[23:0]
LD16
LD17
LD18
LD19
LD20
LD21
LD22
LD23
6,7 LCD_VSYNC
6,7 LCD_HSYNC
6,7 LCD_VCLK
6,7 LCD_VDEN
7 LCD_LEND
6,7 LCD_nRESET
VD16
VD17
VD18
VD19
VD20
VD21
VD22
VD23
VD[23:0] 16
RGB_VSYNC 16
RGB_HSYNC 16
RGB_VCLK 16
RGB_VDEN 16
nDIS_OFF 16
EINT12 16
TOUT1 16
R116 0
R118 4.7K
R119 0R0
VDD3.3V
C46
100nF
VDD_LCDI
C49
100nF
SN74AVCA164245DGG
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
B05. LCD General/SPI/ADC
Rev
0.1
Date:
Monday, February 25, 2008
Sheet
5
of
16





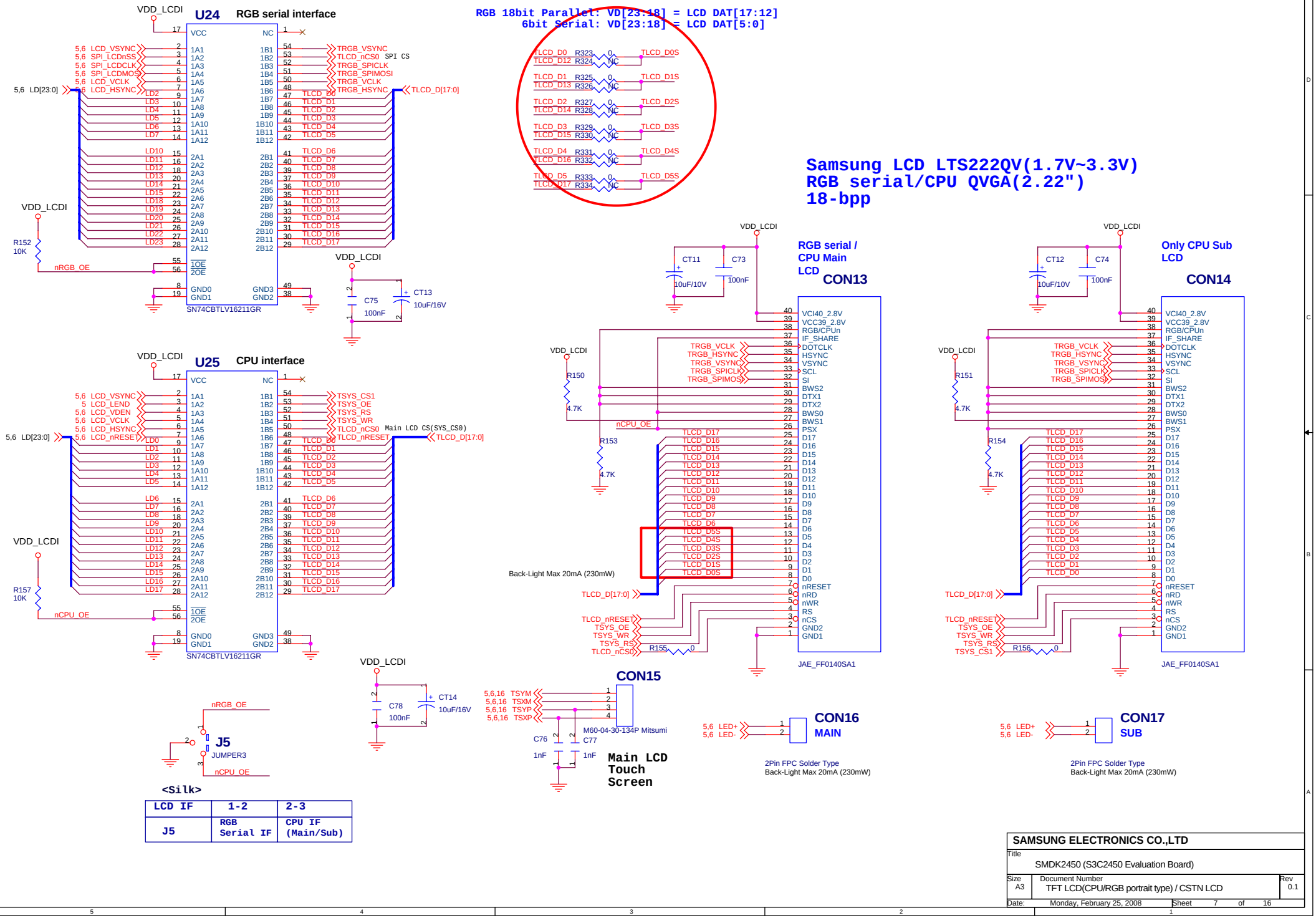


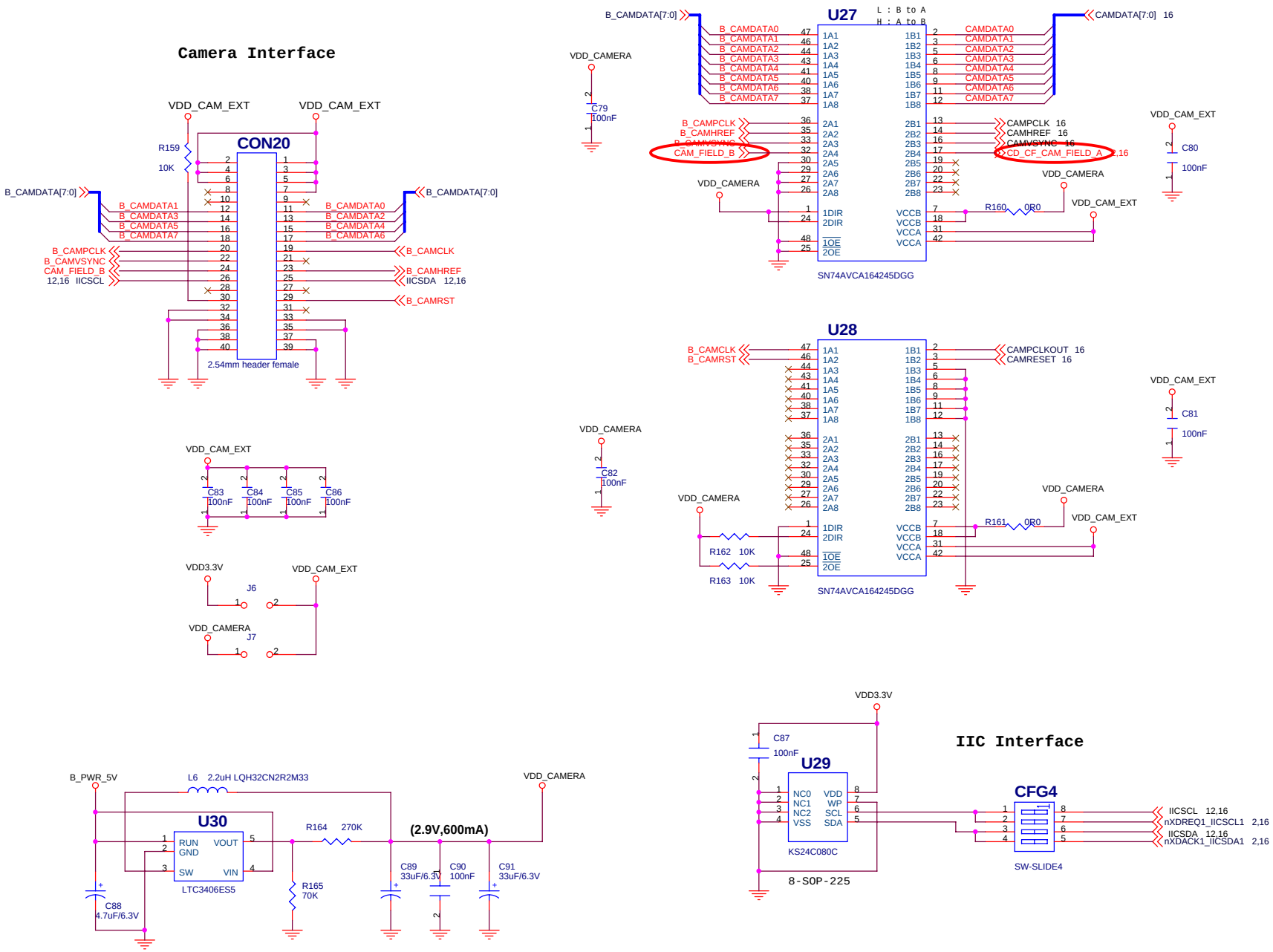
LVT350QV
RGB/QVGA(3.5") 24-bpp



LTE480WE
RGB/WVGA(4.8") 24-bpp
- Default

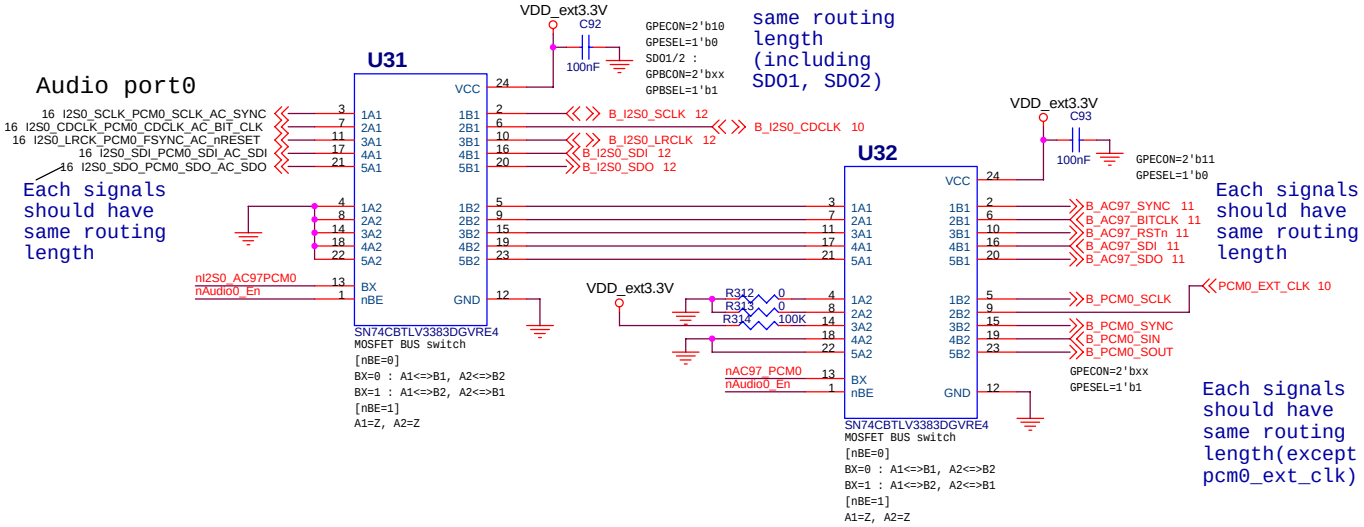
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: LCD interface & TFT LCD(Landscape type)	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 6 of 16	

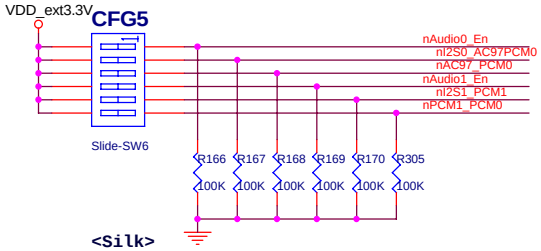

U24 RGB serial interface
SN74CBTLV16211GR
U25 CPU interface
SN74CBTLV16211GR
RGB 18bit Parallel: VD[23:18] = LCD DAT[17:12]
6bit Serial: VD[23:18] = LCD DAT[5:0]
Samsung LCD LTS222QV(1.7V~3.3V)
RGB serial/CPU QVGA(2.22")
18-bpp
RGB serial / CPU Main LCD
CON13
Only CPU Sub LCD
CON14
JAE_FF0140SA1
Back-Light Max 20mA (230mW)
CON15
M60-04-30-134P Mitsumi
Main LCD Touch Screen
CON16
MAIN
2Pin FPC Solder Type
Back-Light Max 20mA (230mW)
CON17
SUB
2Pin FPC Solder Type
Back-Light Max 20mA (230mW)
J5
JUMPER3
<Silk>
LCD IF | 1-2 | 2-3
J5 | RGB Serial IF | CPU IF (Main/Sub)
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
TFT LCD(CPU/RGB portrait type) / CSTN LCD
Monday, February 25, 2008



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Camera Interface	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 8 of 16	

Audio port0





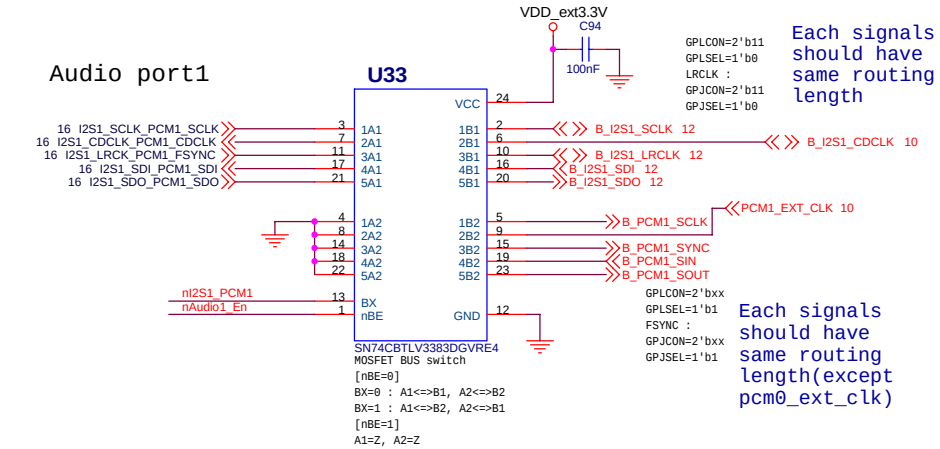
CFG5: Audio port Enable/Demux

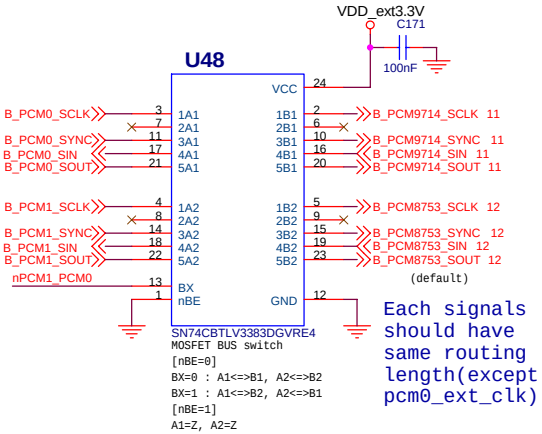
PORT #	Audio0			Audio1		
En/Disable	[1]			[4]		
Enable	OFF(Def.)			OFF(Def.)		
Disable	ON			ON		
Demux	[2]	[3]	[6]	Demux	[5]	[6]
I2S0 (Def)	OFF	X	X	IIS1* (Def)	OFF	X
AC97	ON	OFF	X	PCM1*	ON	OFF (8753)
PCM0	ON	ON	ON (8753)			

*For I2S1,PCM1 set CFG6 switch of CPU b'd

<Pcm0/1 select>

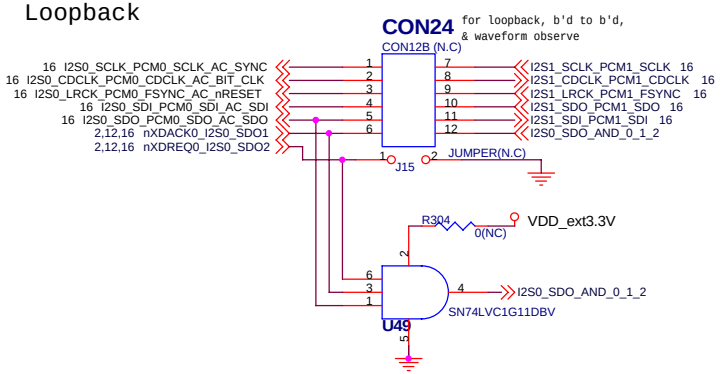
Audio port1





Pcm0/1 are verified by 8753 codec(default)
but can be verified by 9714(sw setting is needed)

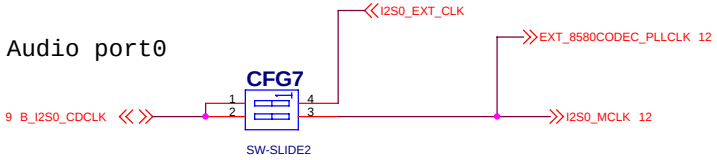
Loopback



SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2450 (S3C2450 Evaluation Board)			
Size: A3	Document Number: Audio(Demux)		Rev: 0.1
Date: Monday, February 25, 2008	Sheet 9 of 16		

<i2s cdclk select/codec operating clk supply>

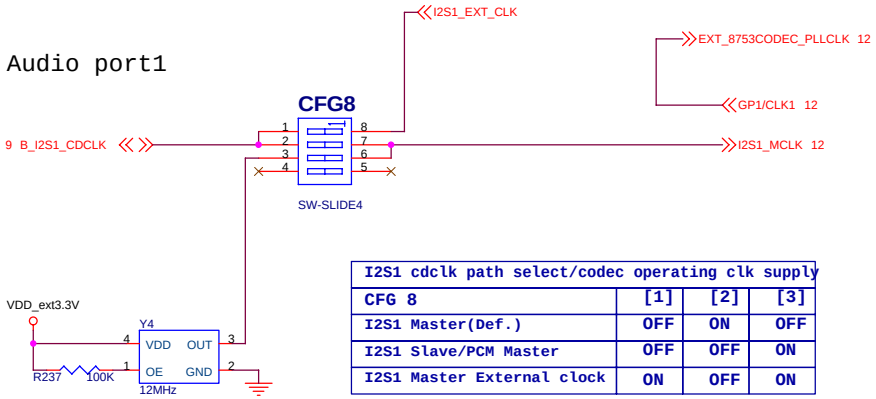
Audio port0



<Silk>

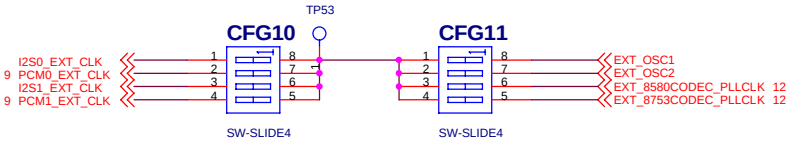
I2S0 cdclk path select		
CFG 7	[1]	[2]
I2S0 Master(Def.)	OFF	ON
I2S0 Slave	OFF	OFF
I2S0 Master External clock	ON	OFF

Audio port1

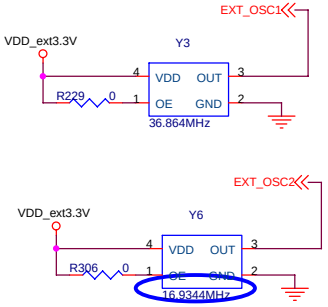


I2S1 cdclk path select/codec operating clk supply			
CFG 8	[1]	[2]	[3]
I2S1 Master(Def.)	OFF	ON	OFF
I2S1 Slave/PCM Master	OFF	OFF	ON
I2S1 Master External clock	ON	OFF	ON

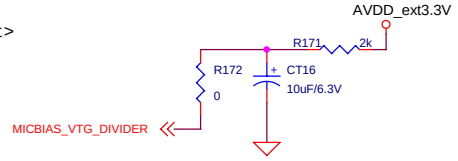
<External Clock select part>

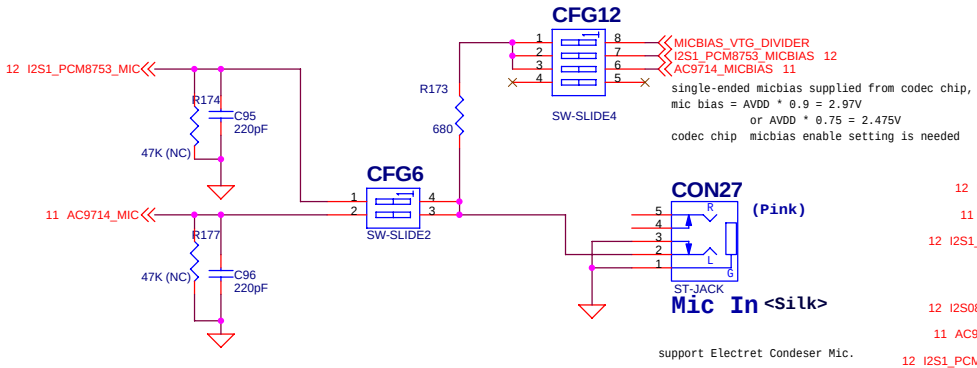


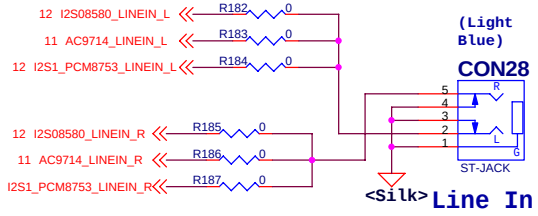
Ext. Clk Sel.	CFG10 To.	CFG11 From
[1]	I2S0	OSC1 36.864MHz
[2]	PCM0	OSC2 16.9344MHz
[3]	I2S1	8580PLL
[4]	PCM1	8753PLL
All Off (Default)		



<mic bias part>







<Silk>

Mic in direction select		
CFG6	[1]	[2]
IIS1_PCM8753	ON	OFF
AC9714(Def.)	OFF	ON

<Silk>

CFG12	Mic bias source
[1]	VTG div. (Def.)
[2]	8753 Codec
[3]	9714 Codec

<Silk> I2S FRONT
Speaker Out -Front L,R -WM8580 OUT1
CON21 PJ-327-2 (Green) ST-JACKc
12 I2S08580_OUT1_L
12 I2S08580_OUT1_R

<Silk> I2S CENTER
Speaker Out -Center, LF -WM8580 OUT2
CON22 PJ-327-2 (Orange) ST-JACKc
12 I2S08580_OUT2_L
12 I2S08580_OUT2_R

<Silk> I2S REAR
Speaker Out -Rear L,R -WM8580 OUT3
CON23 PJ-327-2 (Black) ST-JACKc
12 I2S08580_OUT3_L
12 I2S08580_OUT3_R

<Silk> AC97 OUT
Speaker Out -L,R -WM9714
CON25 PJ-327-2 (Green) ST-JACKc
11 AC9714_OUT_L
11 AC9714_OUT_R

<Silk> I2S1/PCM OUT
Speaker Out -L,R -WM8753
CON26 PJ-327-2 (Green) ST-JACKc
12 I2S1_PCM8753_OUT_L
12 I2S1_PCM8753_OUT_R

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Audio(Ext. Clk & Conn)	Rev: 0.1
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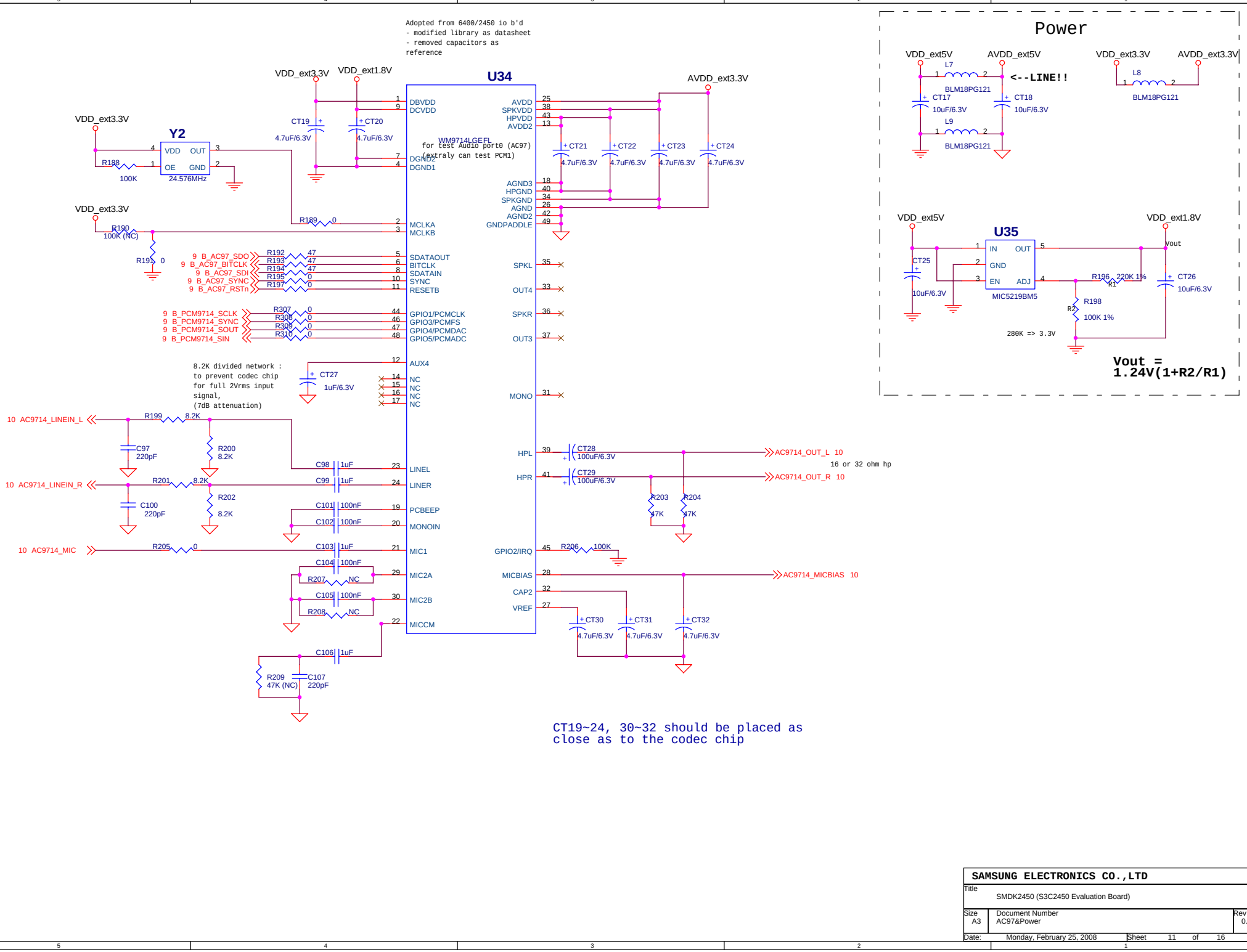
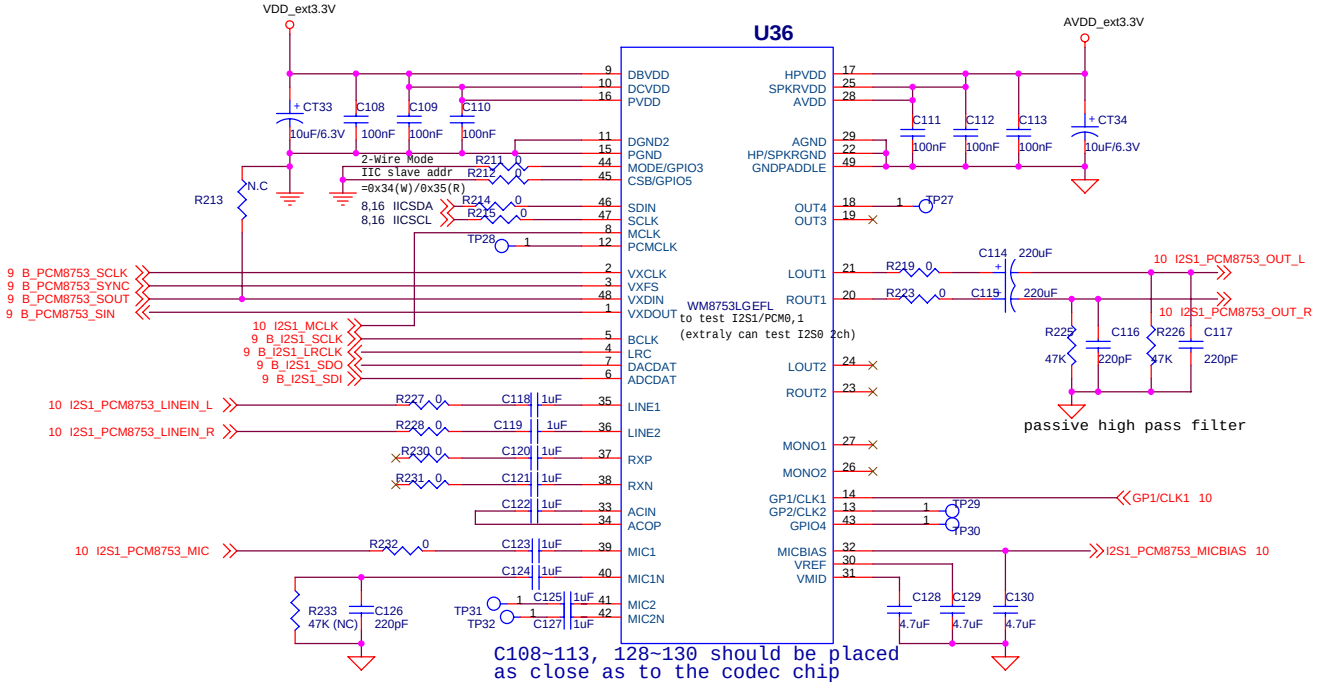
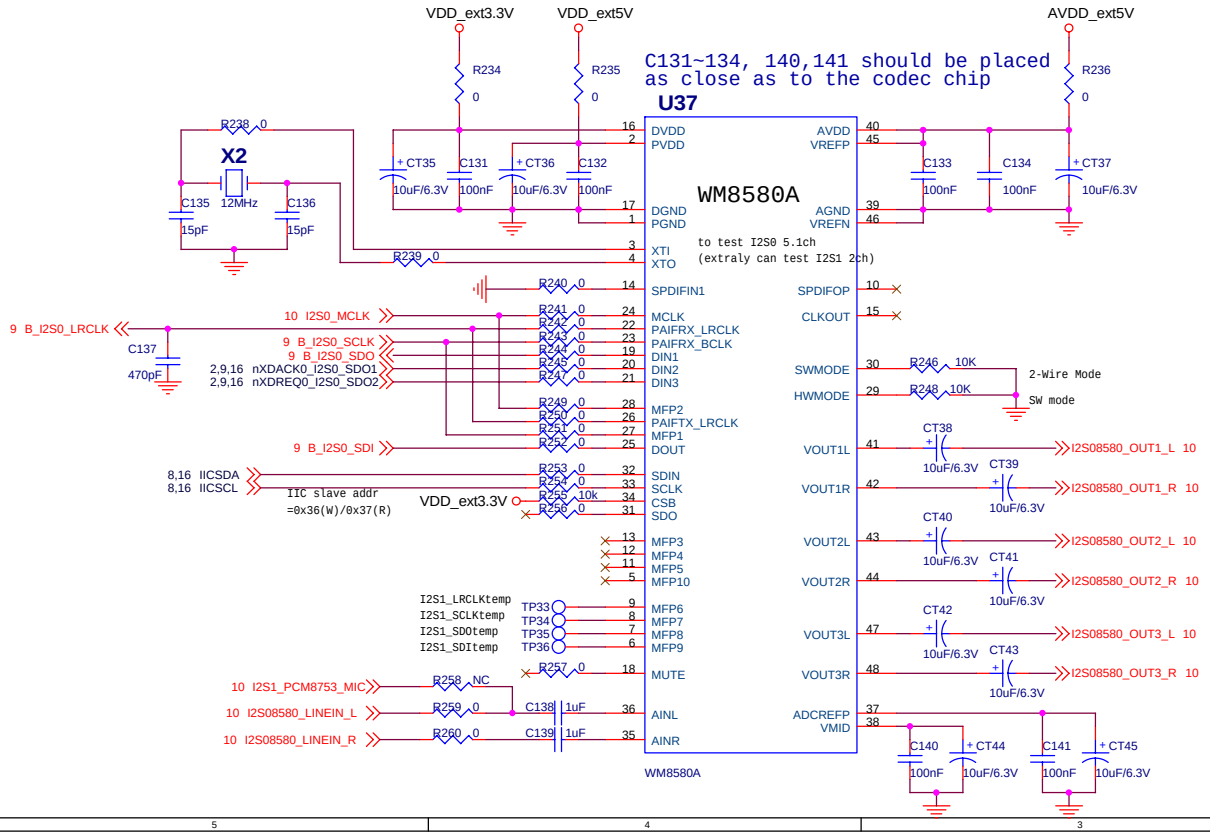

Adopted from 6400/2450 io b'd
- modified library as datasheet
- removed capacitors as reference
U34
WM9714LGEFL
for test Audio port0 (AC97)
(extraly can test PCM1)
DBVDD
DCVDD
DGND2
DGND1
AVDD
SPKVDD
HPVDD
AVDD2
AGND3
HPGND
SPKGND
AGND
AGND2
GNDPADDLE
MCLKA
MCLKB
SDATAOUT
BITCLK
SDATAIN
SYNC
RESETB
GPIO1/PCMCLK
GPIO3/PCMFS
GPIO4/PCMDAC
GPIO5/PCMADC
AUX4
NC
SPKL
OUT4
SPKR
OUT3
MONO
HPL
HPR
LINEL
LINER
PCBEEP
MONOIN
MIC1
MIC2A
MIC2B
MICCM
GPIO2/IRQ
MICBIAS
CAP2
VREF
VDD_ext3.3V
VDD_ext1.8V
AVDD_ext3.3V
Y2
24.576MHz
8.2K divided network :
to prevent codec chip
for full 2Vrms input
signal,
(7dB attenuation)
AC9714_LINEIN_L
AC9714_LINEIN_R
AC9714_MIC
AC9714_OUT_L
AC9714_OUT_R
AC9714_MICBIAS
16 or 32 ohm hp
CT19~24, 30~32 should be placed as close as to the codec chip
Power
VDD_ext5V
AVDD_ext5V
VDD_ext3.3V
AVDD_ext3.3V
<--LINE!!
BLM18PG121
U35
MIC5219BM5
VDD_ext5V
VDD_ext1.8V
Vout
R198
100K 1%
280K => 3.3V
Vout = 1.24V(1+R2/R1)
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
AC97&Power
Rev
0.1
Date:
Monday, February 25, 2008
Sheet
11
of
16





SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2450 (S3C2450 Evaluation Board)			
Size: A3	Document Number: I2S 5.1ch/I2S&PCM		Rev: 0.1
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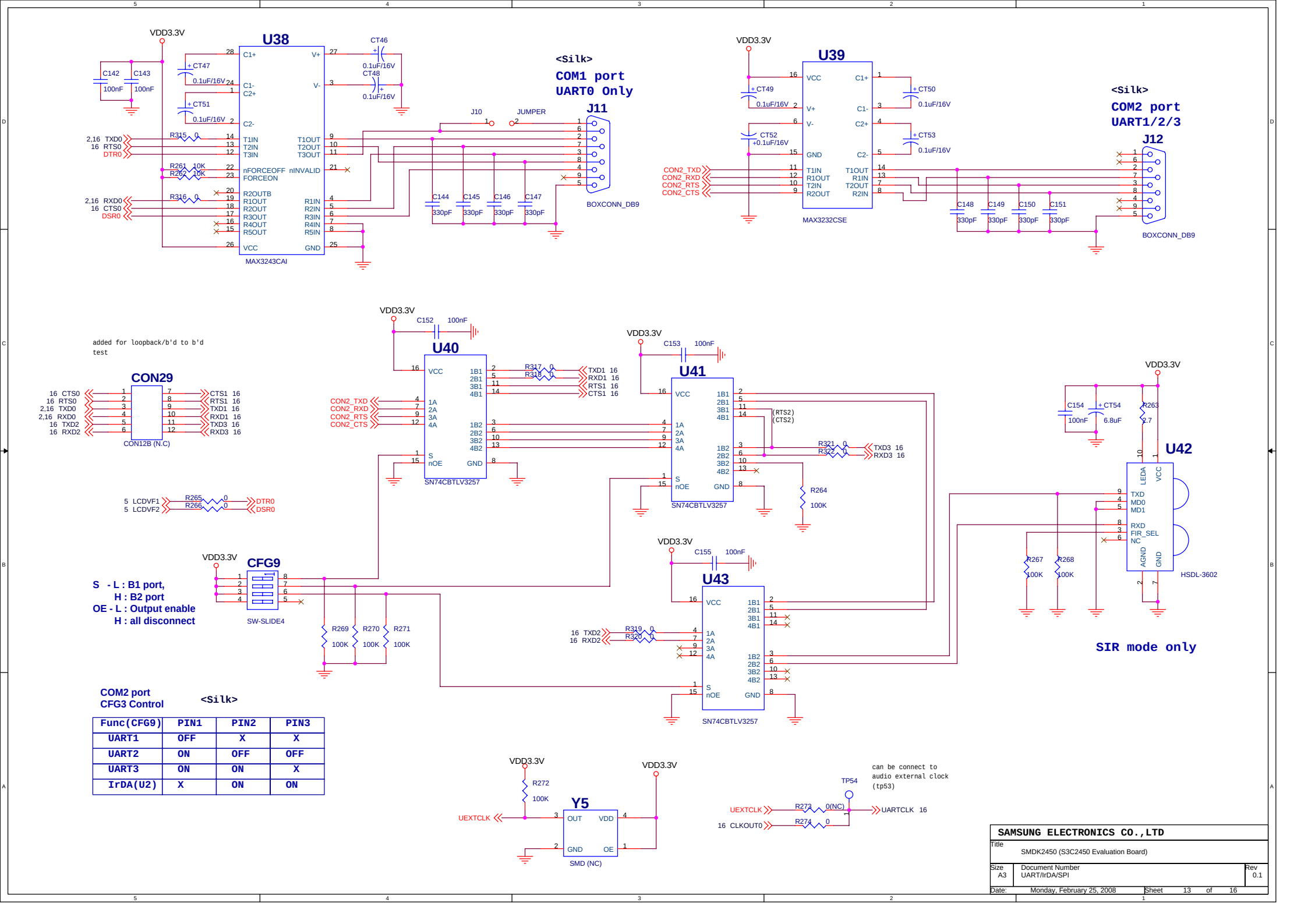
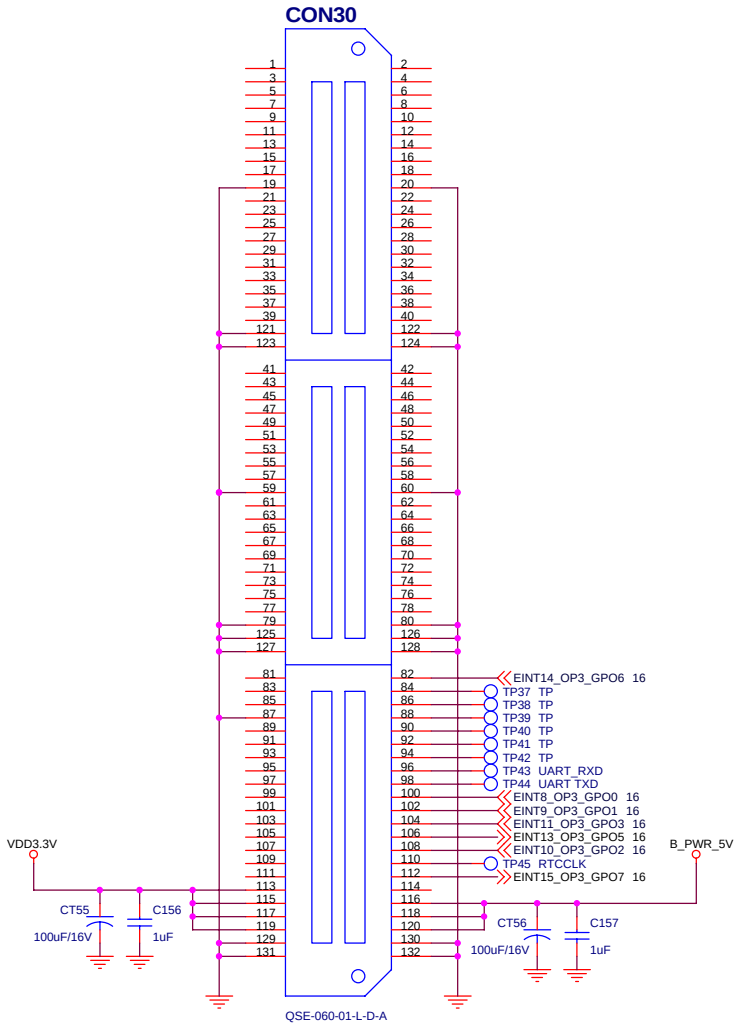


Func(CFG9)	PIN1	PIN2	PIN3
UART1	OFF	X	X
UART2	ON	OFF	OFF
UART3	ON	ON	X
IrDA(U2)	X	ON	ON



External I/O

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: External I/O	Rev: 0.1
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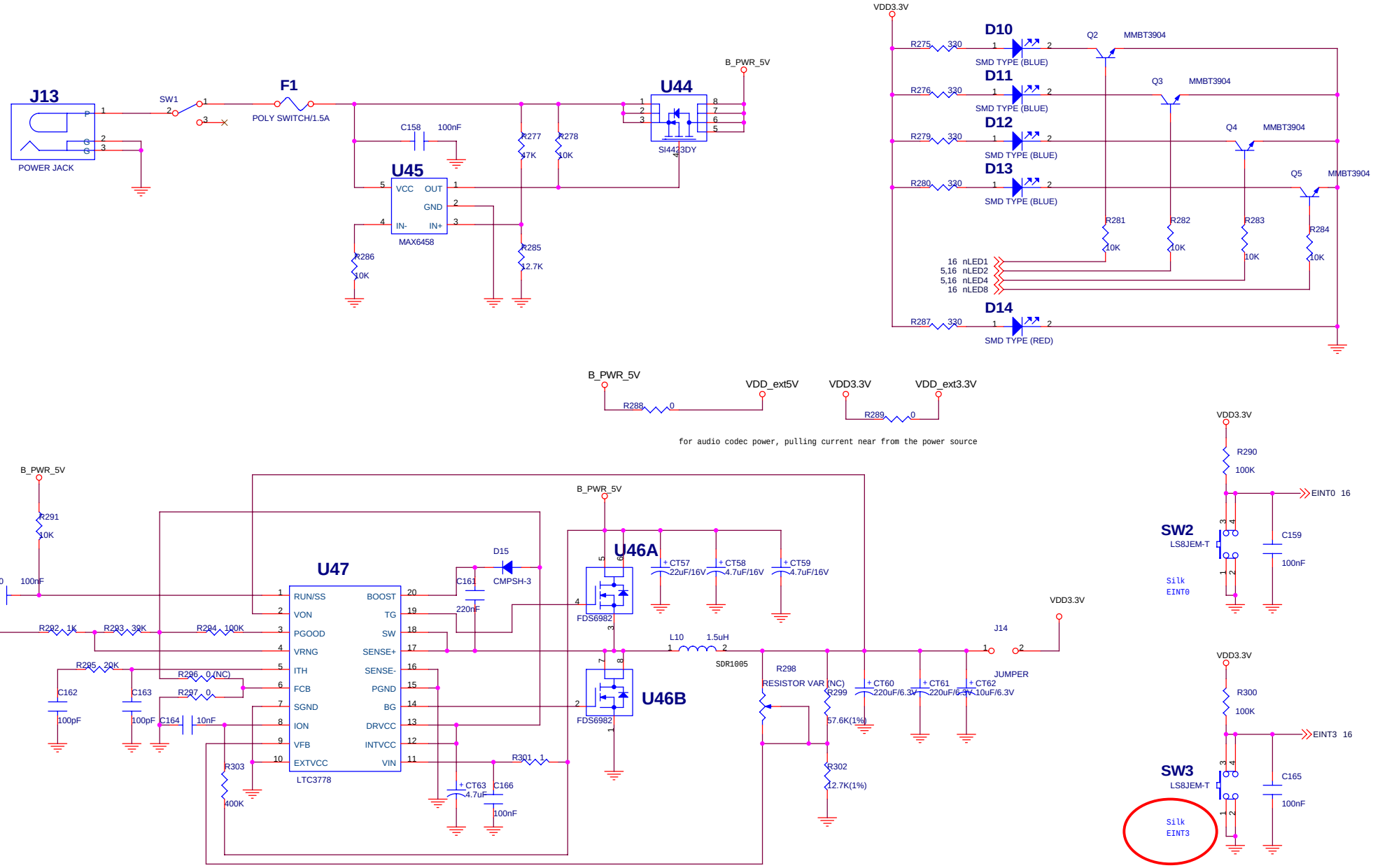
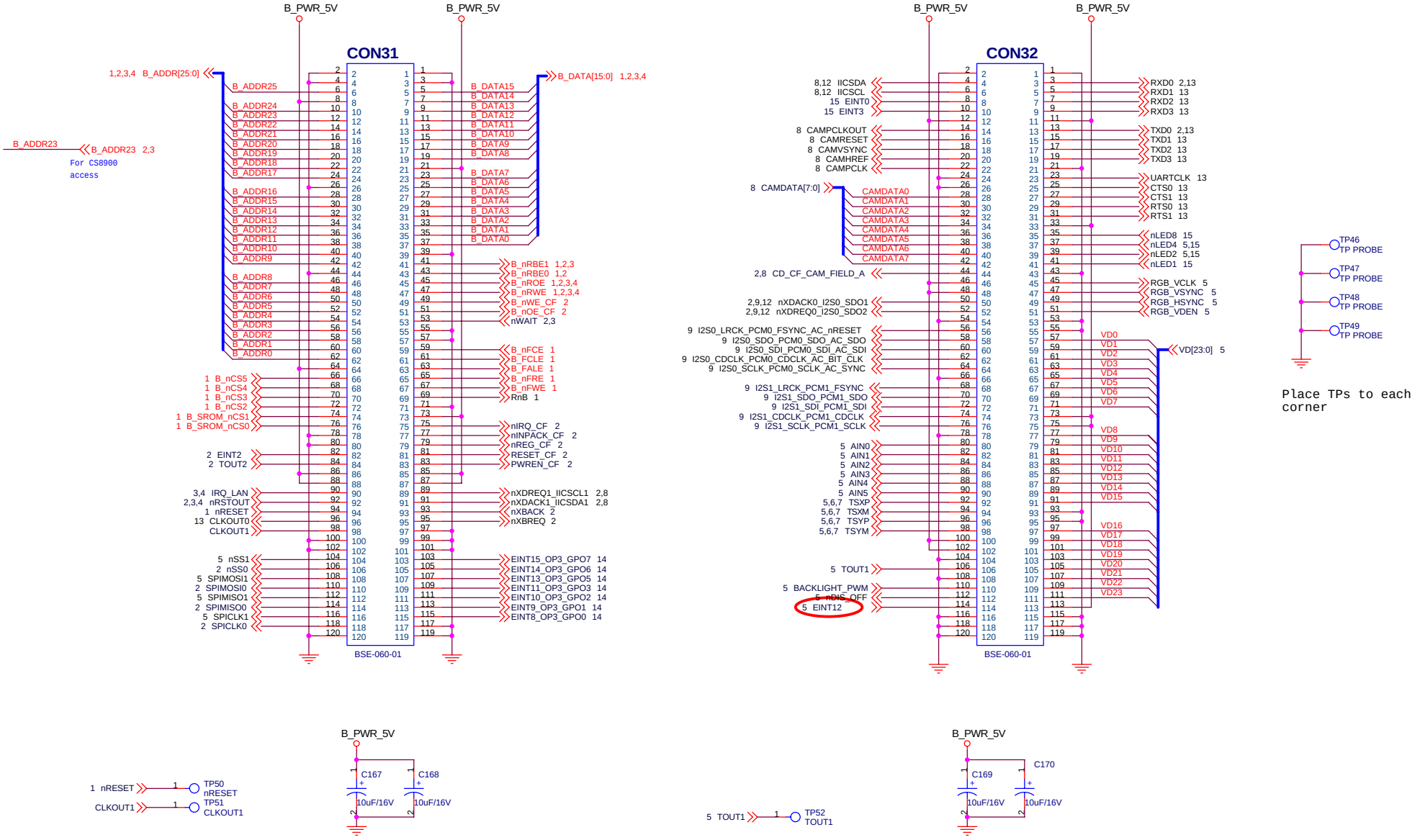


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Base board Power & LED	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 15 of 16	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Board to Board connector	Rev: 0.1
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