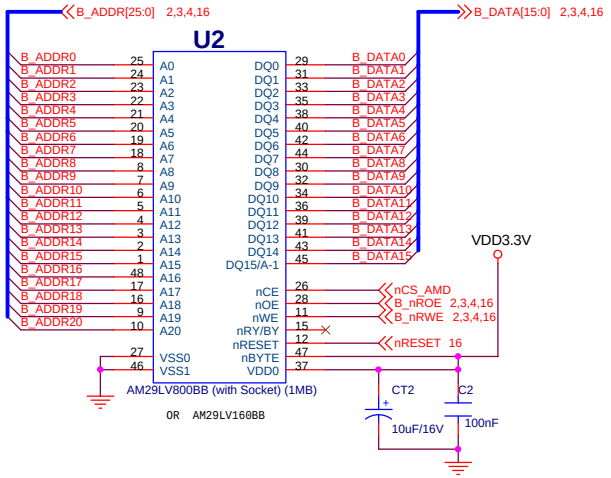
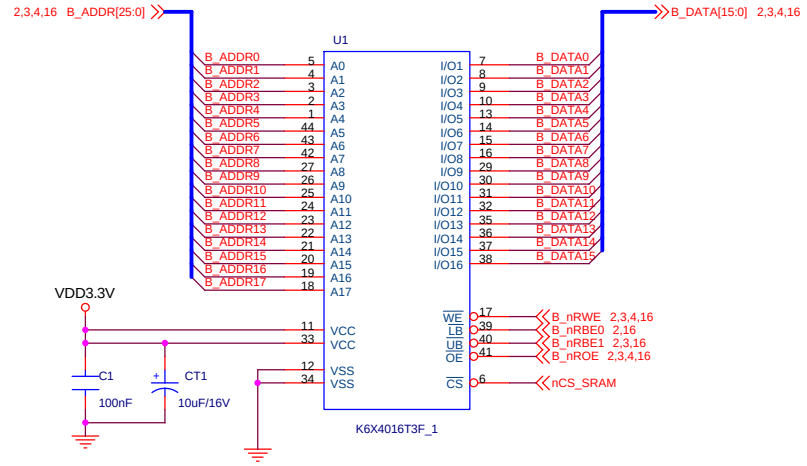
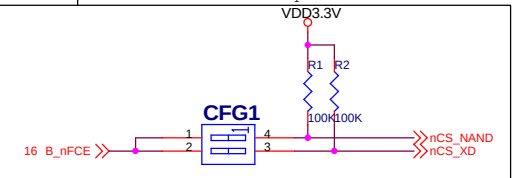
AMD Flash Memory(SOCKET)



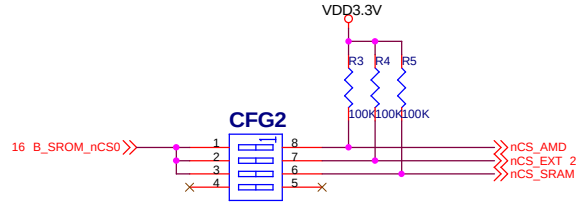
SRAM





<Silk>

CFG1: nFCE	SROM Selector
[2]	XD card
[1]	NAND



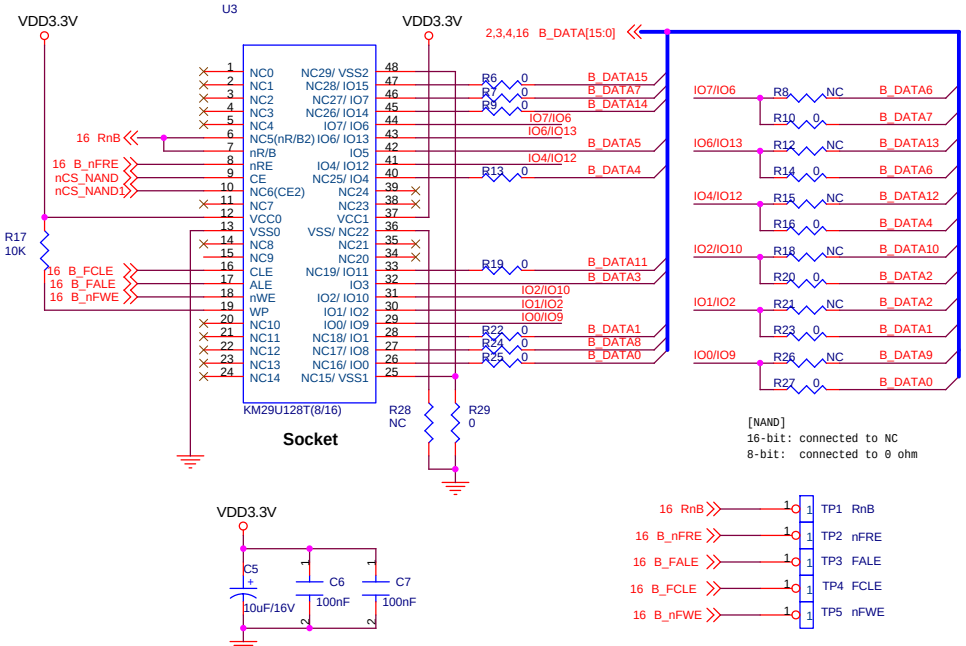
<Silk>

CFG2: nCS0	SROM Selector
[3]	External
[2]	SRAM
[1]	NOR(AMD)

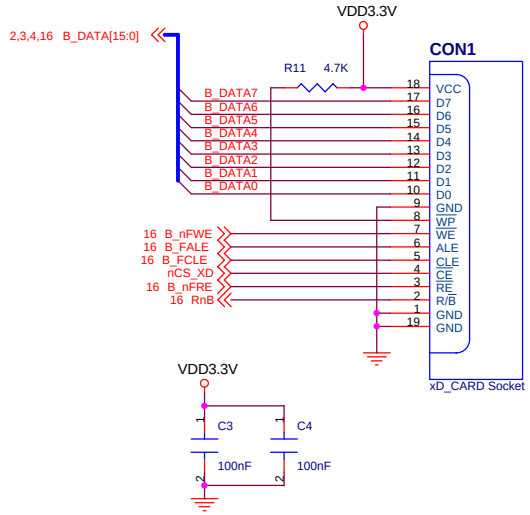
S3C2450
Addition : NAND CS1 & RnB1

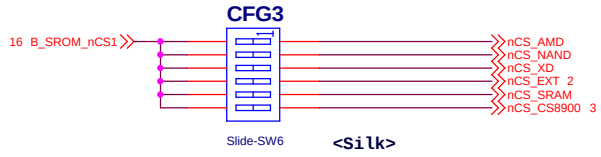
S3C2450
Addition : NAND CS1
SW(To Select Ethernet or Additional Nand CS)

NAND Flash memory (SOCKET)



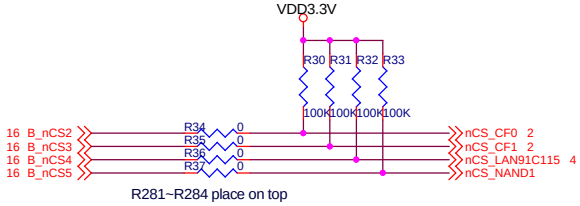
XD PICTURE CARD





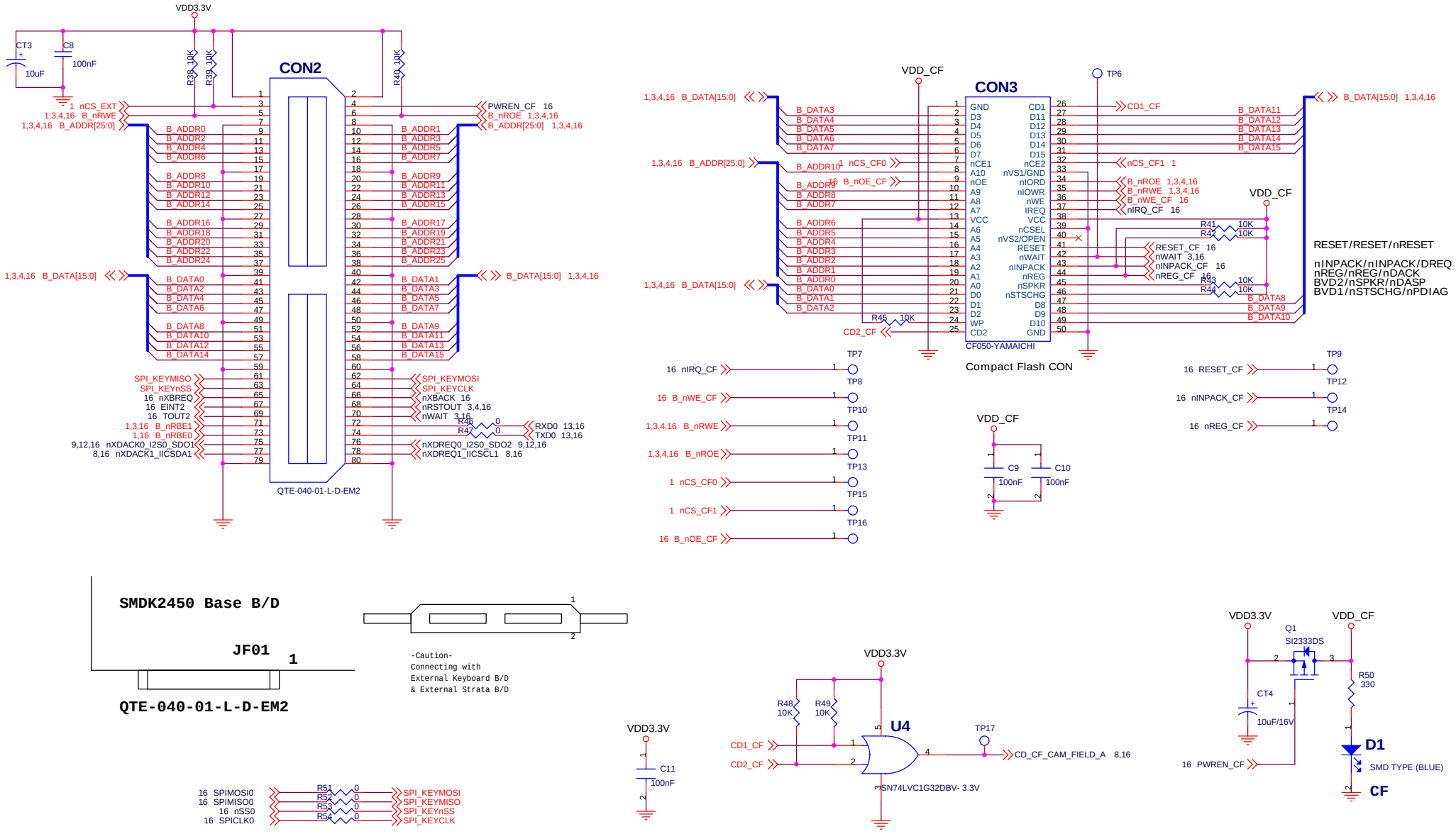
<Silk>

CFG3: nCS1	SROM Selector
[6]	CS8900(CS1)
[5]	SRAM
[4]	External
[3]	XD card
[2]	NAND
[1]	NOR(AMD)

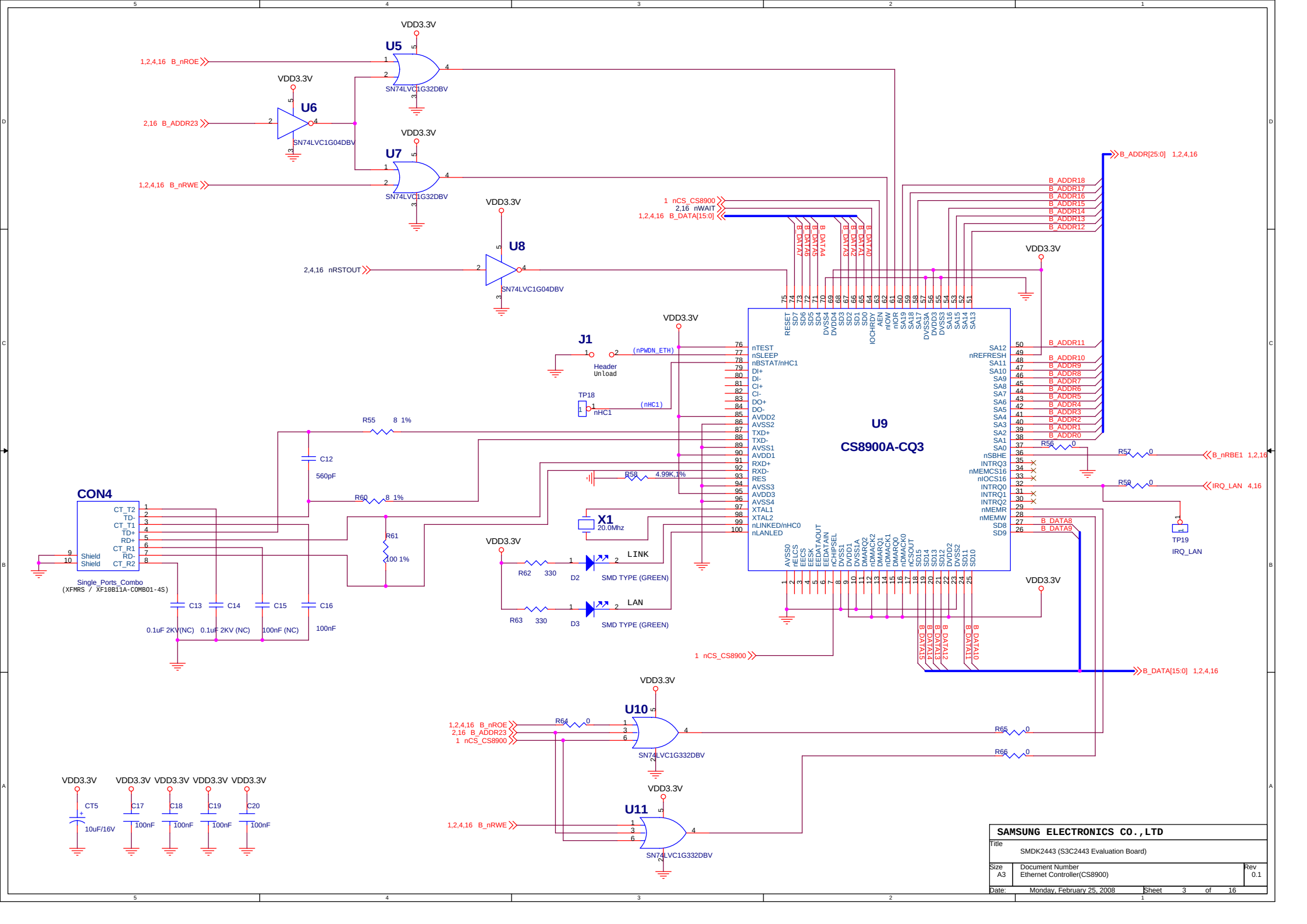


R281~R284 place on top

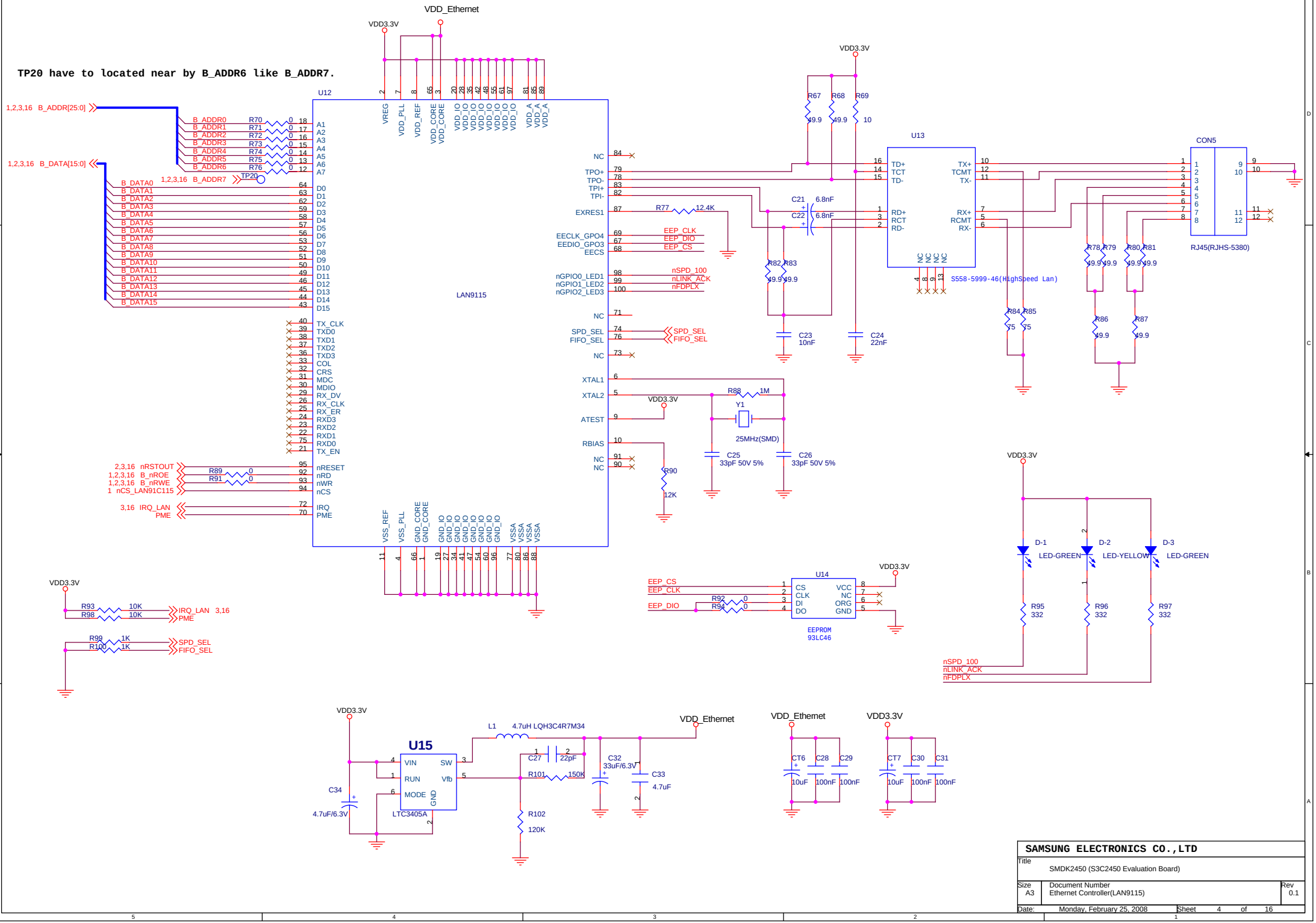
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: NOR/NAND/SRAM/CONFIG	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 1 of 16	



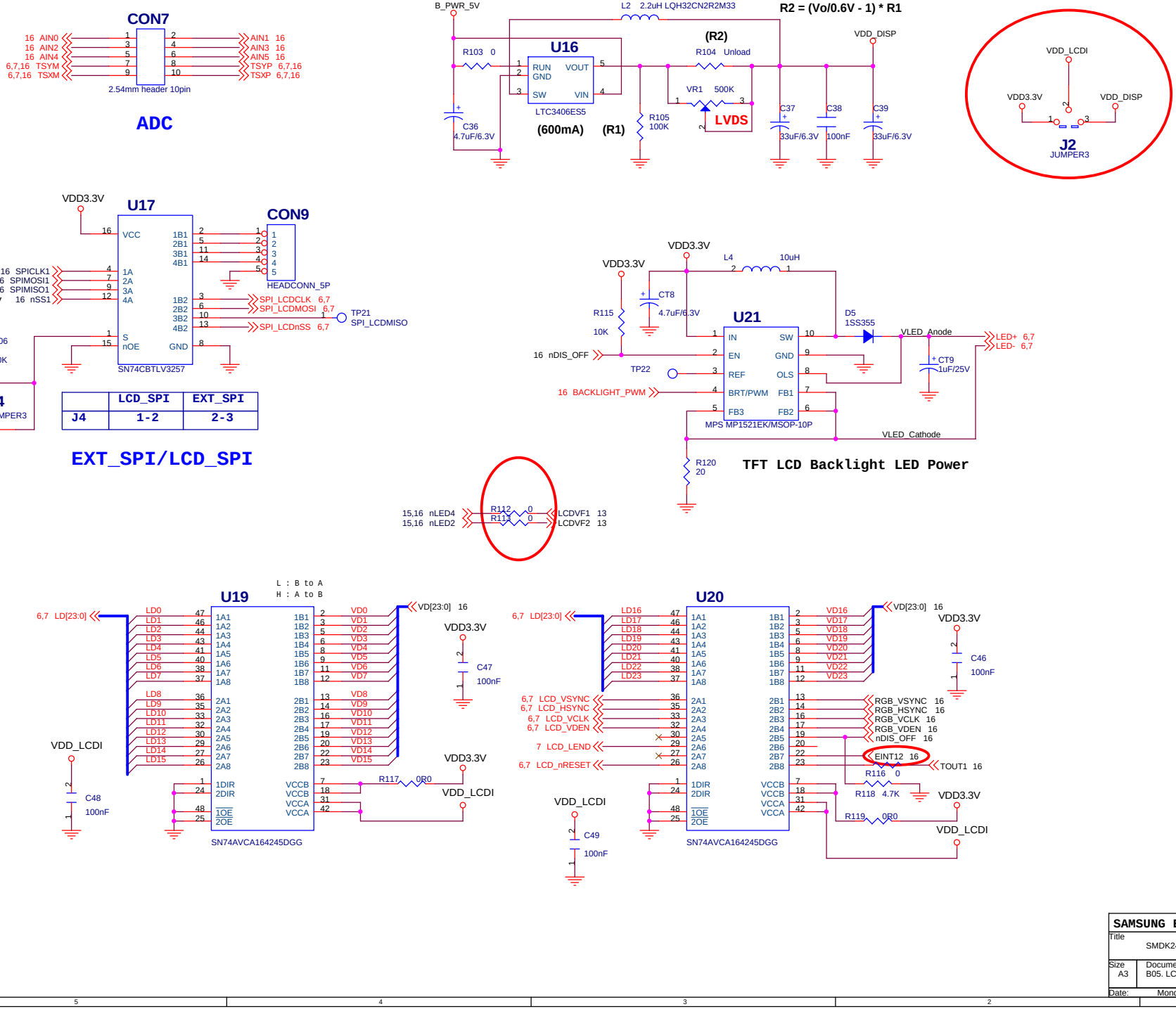
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: External Bus connector & CF interface	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 2 of 16	


U5
SN74LVC1G32DBV
U6
SN74LVC1G04DBV
U7
SN74LVC1G32DBV
U8
SN74LVC1G04DBV
U9
CS8900A-CQ3
U10
SN74LVC1G332DBV
U11
SN74LVC1G332DBV
J1
Header
Unload
TP18
nHC1
TP19
IRQ_LAN
X1
20.0Mhz
CON4
Single_Ports_Combo
(XFMRS / XF10B11A-COMB01-4S)
D2
SMD TYPE (GREEN)
D3
SMD TYPE (GREEN)
LINK
LAN
VDD3.3V
1,2,4,16 B_nROE
2,16 B_ADDR23
1,2,4,16 B_nRWE
2,4,16 nRSTOUT
1 nCS_CS8900
2,16 nWAIT
1,2,4,16 B_DATA[15:0]
B_ADDR[25:0] 1,2,4,16
B_DATA[15:0] 1,2,4,16
B_nRBE1 1,2,16
IRQ_LAN 4,16
(nPWDN_ETH)
(nHC1)
R55 8 1%
R56 0
R57 0
R58 4.99K,1%
R59 0
R60 8 1%
R61 100 1%
R62 330
R63 330
R64 0
R65 0
R66 0
C12 560pF
C13 0.1uF 2KV(NC)
C14 0.1uF 2KV (NC)
C15 100nF (NC)
C16 100nF
CT5 10uF/16V
C17 100nF
C18 100nF
C19 100nF
C20 100nF
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2443 (S3C2443 Evaluation Board)
Size A3
Document Number
Ethernet Controller(CS8900)
Rev 0.1
Date: Monday, February 25, 2008
Sheet 3 of 16

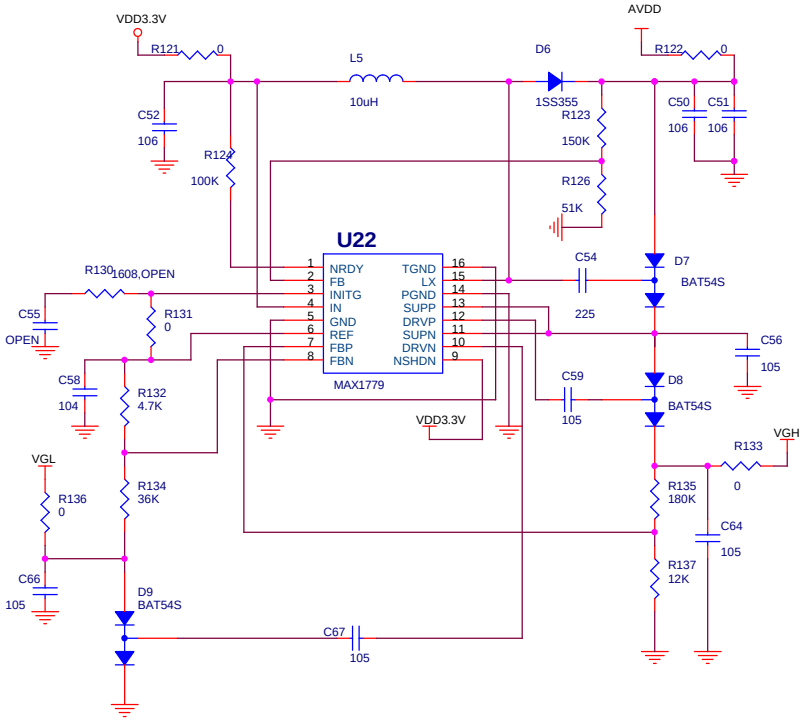
TP20 have to located near by B_ADDR6 like B_ADDR7.

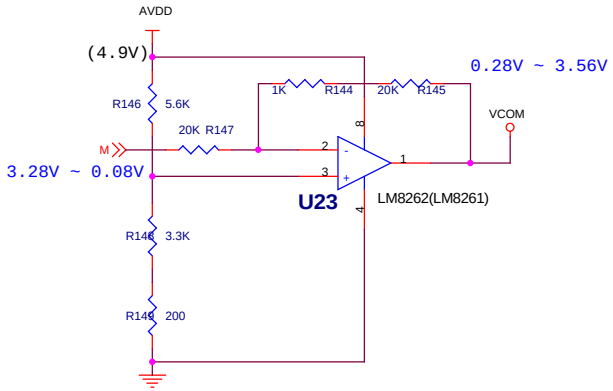


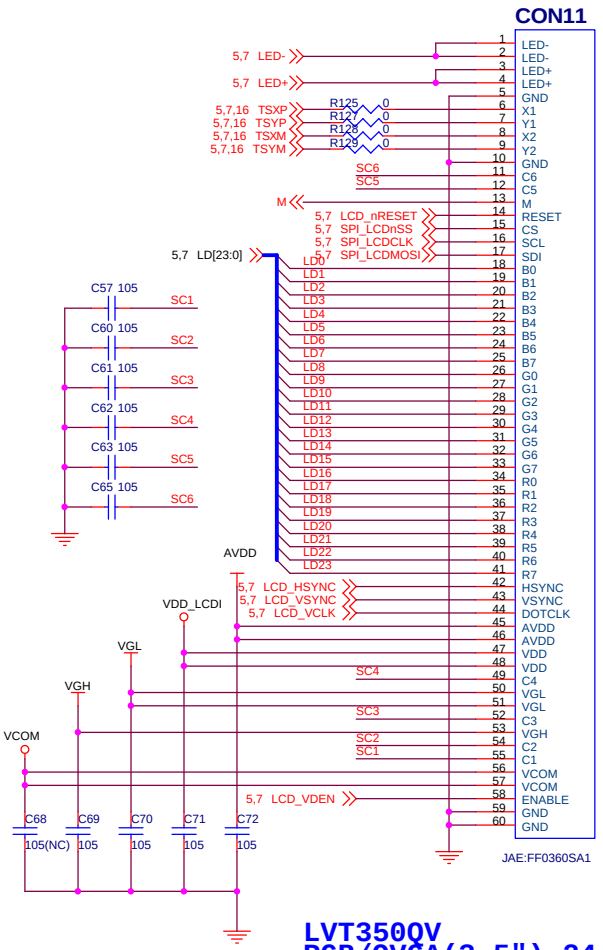
SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2450 (S3C2450 Evaluation Board)			
Size: A3	Document Number: Ethernet Controller(LAN9115)		Rev: 0.1
Date: Monday, February 25, 2008	Sheet 4 of 16		



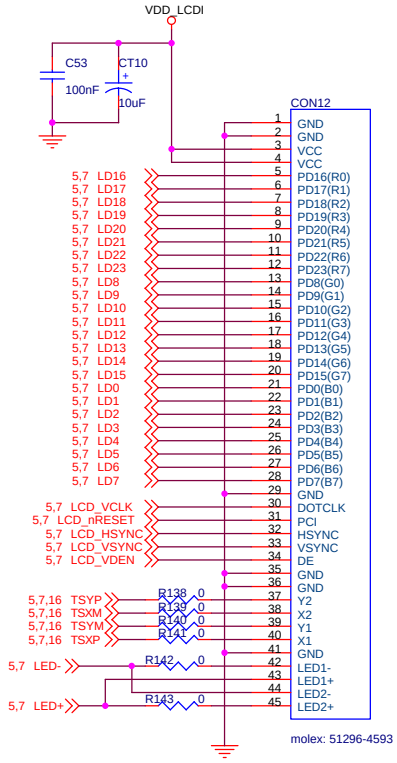
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: B05. LCD General/SPI/ADC	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 5 of 16	





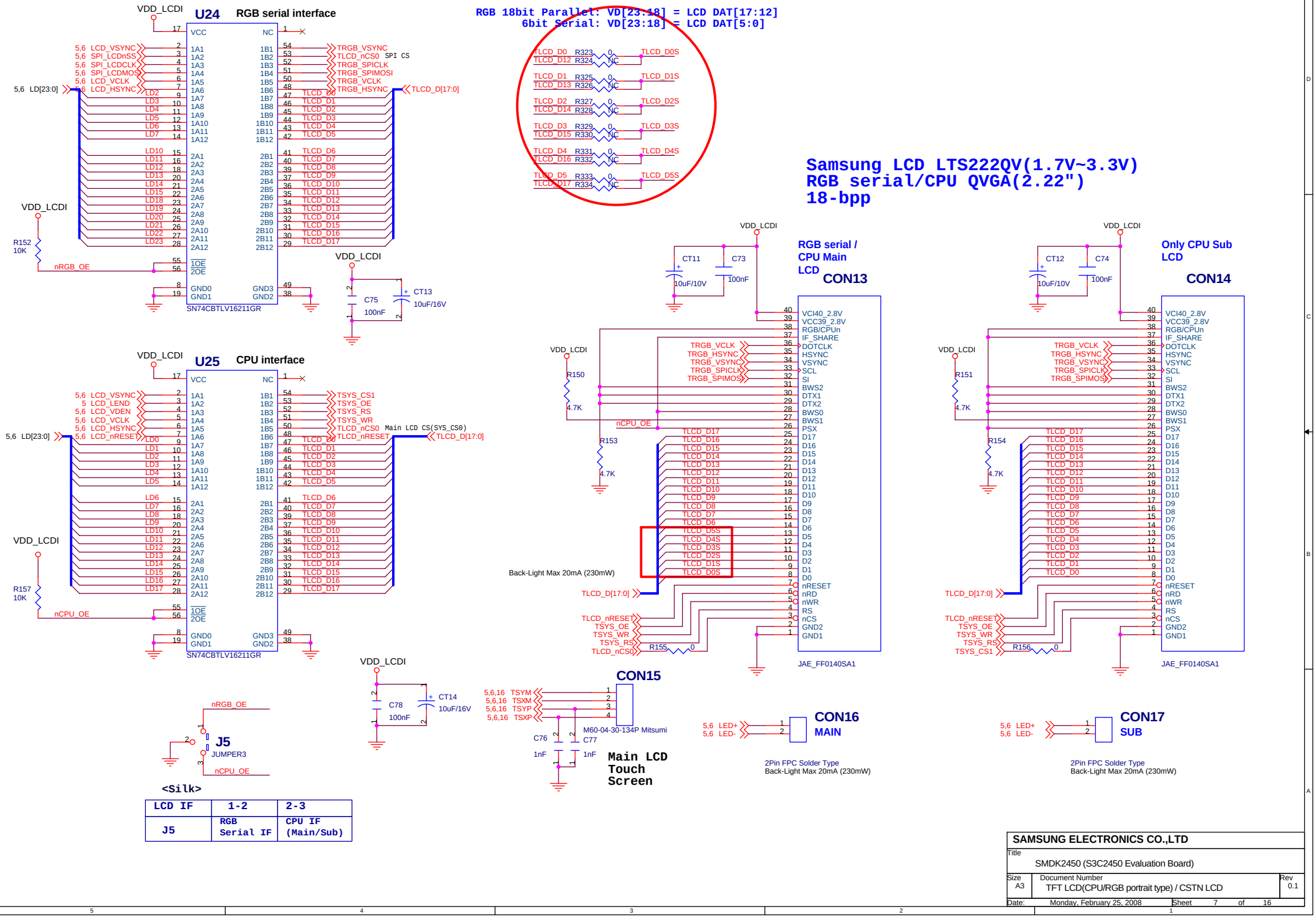


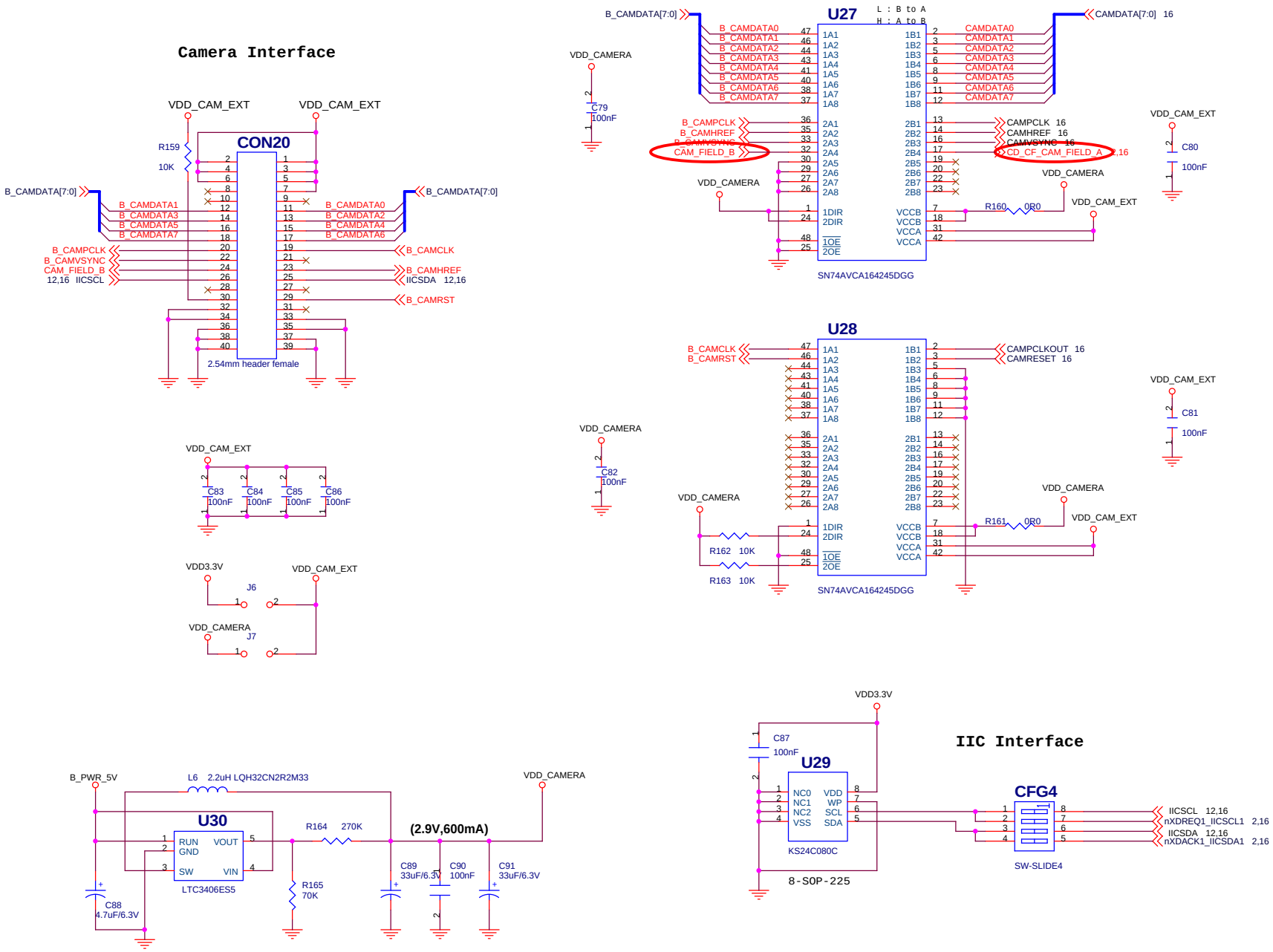
LVT350QV
RGB/QVGA(3.5") 24-bpp



LTE480WE
RGB/WVGA(4.8") 24-bpp
- Default

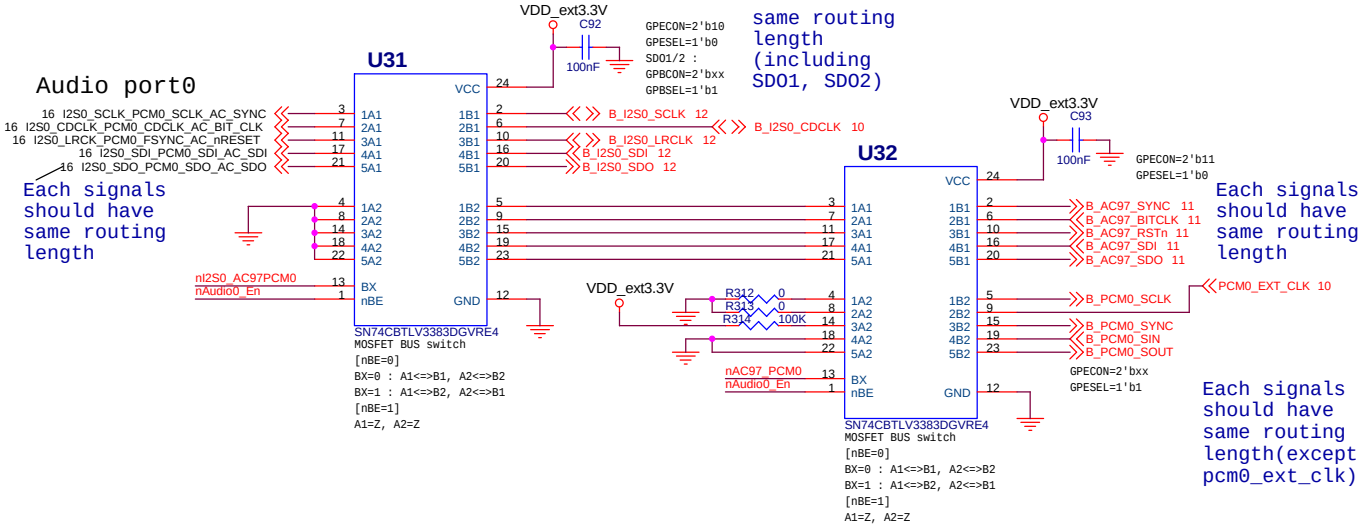
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: LCD interface & TFT LCD(Landscape type)	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 6 of 16	

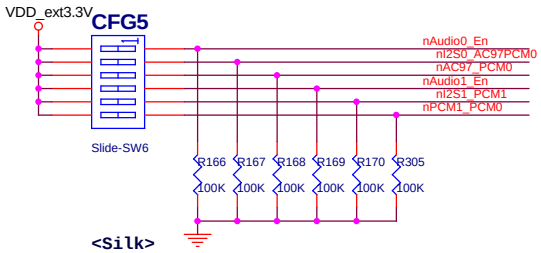

RGB 18bit Parallel: VD[23:18] = LCD DAT[17:12]
6bit Serial: VD[23:18] = LCD DAT[5:0]
Samsung LCD LTS222QV(1.7V~3.3V)
RGB serial/CPU QVGA(2.22")
18-bpp
U24 RGB serial interface
U25 CPU interface
SN74CBTLV16211GR
RGB serial / CPU Main LCD
CON13
Only CPU Sub LCD
CON14
JAE_FF0140SA1
CON15
Main LCD Touch Screen
M60-04-30-134P Mitsumi
CON16
MAIN
CON17
SUB
2Pin FPC Solder Type
Back-Light Max 20mA (230mW)
Back-Light Max 20mA (230mW)
J5
JUMPER3
<Silk>
LCD IF | 1-2 | 2-3
J5 | RGB Serial IF | CPU IF (Main/Sub)
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number
TFT LCD(CPU/RGB portrait type) / CSTN LCD
Rev 0.1
Date: Monday, February 25, 2008
Sheet 7 of 16



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Camera Interface	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 8 of 16	

Audio port0

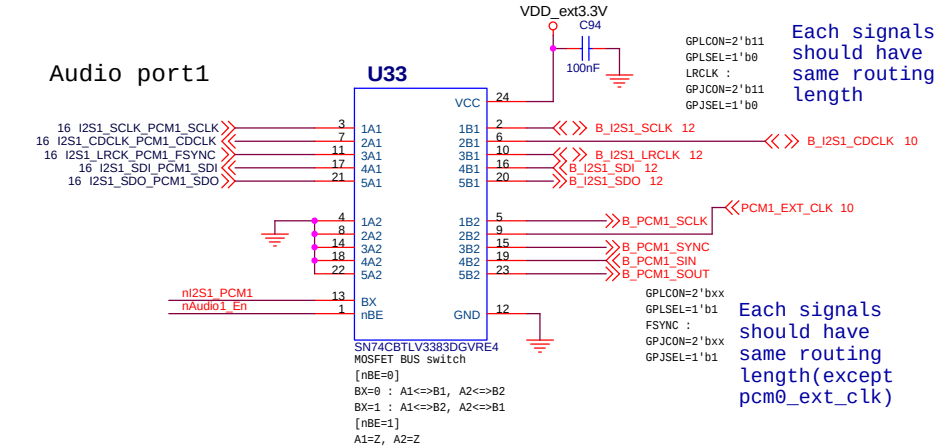


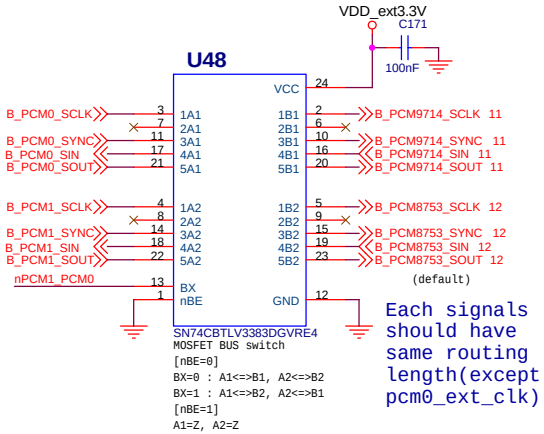


CFG5: Audio port Enable/Demux						
PORT #	Audio0			Audio1		
En/Disable	[1]			[4]		
Enable	OFF(Def.)			OFF(Def.)		
Disable	ON			ON		
Demux	[2]	[3]	[6]	Demux	[5]	[6]
I2S0 (Def)	OFF	X	X	IIS1* (Def)	OFF	X
AC97	ON	OFF	X	PCM1*	ON	OFF (8753)
PCM0	ON	ON	ON (8753)			
*For I2S1,PCM1 set CFG6 switch of CPU b'd						

<Pcm0/1 select>

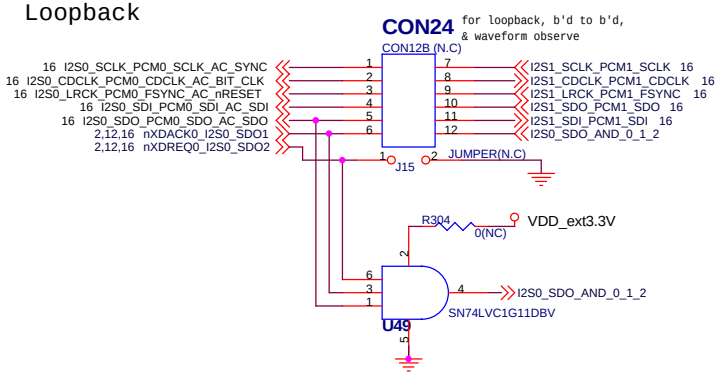
Audio port1





Pcm0/1 are verified by 8753 codec(default)
but can be verified by 9714(sw setting is needed)

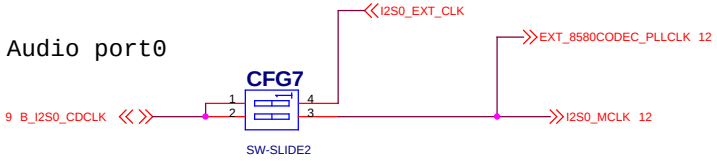
Loopback



SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2450 (S3C2450 Evaluation Board)			
Size: A3	Document Number: Audio(Demux)		Rev: 0.1
Date: Monday, February 25, 2008	Sheet 9 of 16		

<i2s cdclk select/codec operating clk supply>

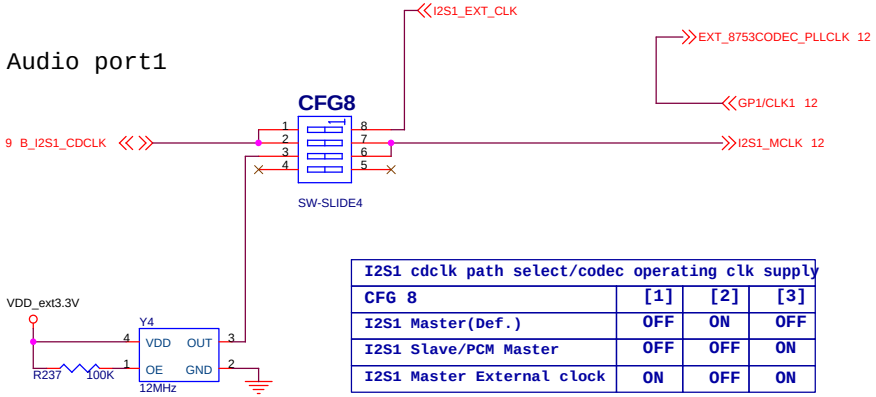
Audio port0



<Silk>

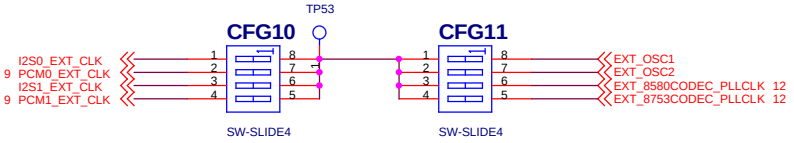
I2S0 cdclk path select		
CFG 7	[1]	[2]
I2S0 Master(Def.)	OFF	ON
I2S0 Slave	OFF	OFF
I2S0 Master External clock	ON	OFF

Audio port1

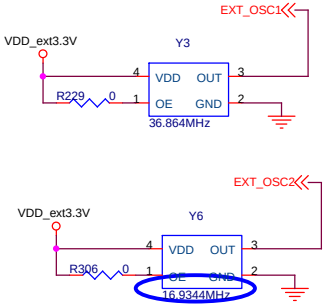


I2S1 cdclk path select/codec operating clk supply			
CFG 8	[1]	[2]	[3]
I2S1 Master(Def.)	OFF	ON	OFF
I2S1 Slave/PCM Master	OFF	OFF	ON
I2S1 Master External clock	ON	OFF	ON

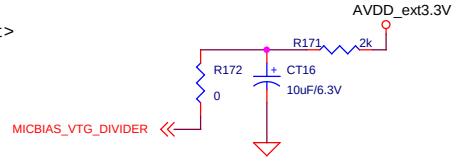
<External Clock select part>

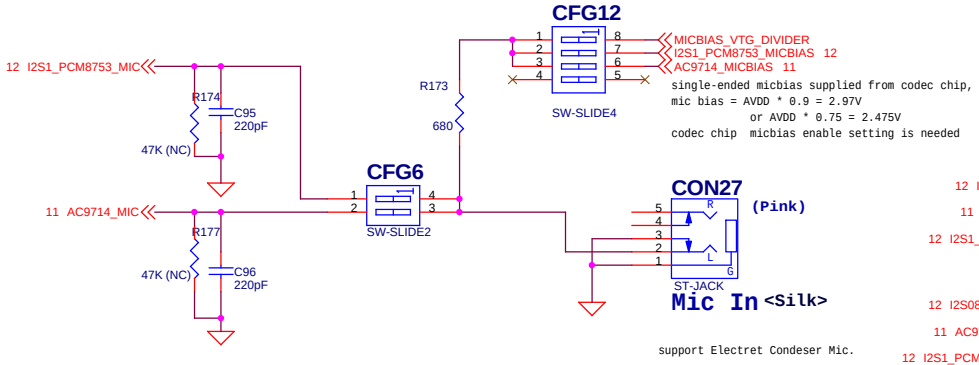


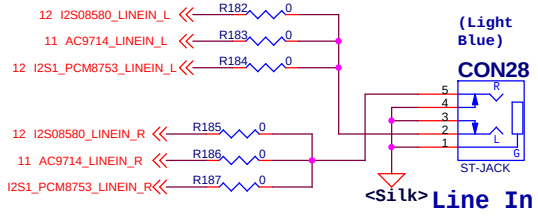
Ext. Clk Sel.	CFG10 To.	CFG11 From
[1]	I2S0	OSC1 36.864MHz
[2]	PCM0	OSC2 16.9344MHz
[3]	I2S1	8580PLL
[4]	PCM1	8753PLL
All Off (Default)		



<mic bias part>







<Silk>

Mic in direction select		
CFG6	[1]	[2]
IIS1_PCM8753	ON	OFF
AC9714(Def.)	OFF	ON

<Silk>

CFG12	Mic bias source
[1]	VTG div. (Def.)
[2]	8753 Codec
[3]	9714 Codec

<Silk> I2S FRONT
Speaker Out -Front L,R -WM8580 OUT1
CON21 PJ-327-2 (Green) ST-JACKc
12 I2S08580_OUT1_L
12 I2S08580_OUT1_R

<Silk> I2S CENTER
Speaker Out -Center, LF -WM8580 OUT2
CON22 PJ-327-2 (Orange) ST-JACKc
12 I2S08580_OUT2_L
12 I2S08580_OUT2_R

<Silk> I2S REAR
Speaker Out -Rear L,R -WM8580 OUT3
CON23 PJ-327-2 (Black) ST-JACKc
12 I2S08580_OUT3_L
12 I2S08580_OUT3_R

<Silk> AC97 OUT
Speaker Out -L,R -WM9714
CON25 PJ-327-2 (Green) ST-JACKc
11 AC9714_OUT_L
11 AC9714_OUT_R

<Silk> I2S1/PCM OUT
Speaker Out -L,R -WM8753
CON26 PJ-327-2 (Green) ST-JACKc
12 I2S1_PCM8753_OUT_L
12 I2S1_PCM8753_OUT_R

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Audio(Ext. Clk & Conn)	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 10 of 16	

Adopted from 6400/2450 io b'd
- modified library as datasheet
- removed capacitors as reference

U34

WM9714LGEFL
for test Audio port0 (AC97)
(extraly can test PCM1)

DBVDD, DCVDD, DGND2, DGND1, AVDD, SPKVDD, HPVDD, AVDD2, AGND3, HPGND, SPKGND, AGND, AGND2, GNDPADDLE, MCLKA, MCLKB, SDATAOUT, BITCLK, SDATAIN, SYNC, RESETB, GPIO1/PCMCLK, GPIO3/PCMFS, GPIO4/PCMDAC, GPIO5/PCMADC, AUX4, NC, NC, NC, NC, SPKL, OUT4, SPKR, OUT3, MONO, HPL, HPR, GPIO2/IRQ, MICBIAS, CAP2, VREF, PCBEEP, MONOIN, MIC1, MIC2A, MIC2B, MICCM

VDD_ext3.3V, VDD_ext1.8V, AVDD_ext3.3V

CT19 4.7uF/6.3V, CT20 4.7uF/6.3V, CT21 4.7uF/6.3V, CT22 4.7uF/6.3V, CT23 4.7uF/6.3V, CT24 4.7uF/6.3V

Y2: VDD, OUT, OE, GND, 24.576MHz, R188 100K

R189 0, R190 100K (NC), R191 0

9 B_AC97_SDO, 9 B_AC97_BITCLK, 9 B_AC97_SDI, 9 B_AC97_SYNC, 9 B_AC97_RSTn
R192 47, R193 47, R194 47, R195 0, R197 0

9 B_PCM9714_SCLK, 9 B_PCM9714_SYNC, 9 B_PCM9714_SOUT, 9 B_PCM9714_SIN
R307 0, R308 0, R309 0, R310 0

8.2K divided network :
to prevent codec chip
for full 2Vrms input
signal,
(7dB attenuation)

CT27 1uF/6.3V

10 AC9714_LINEIN_L, R199 8.2K, C97 220pF, R200 8.2K
10 AC9714_LINEIN_R, R201 8.2K, C100 220pF, R202 8.2K
10 AC9714_MIC, R205 0

C98 1uF, C99 1uF, C101 100nF, C102 100nF, C103 1uF, C104 100nF, R207 NC, C105 100nF, R208 NC, C106 1uF, R209 47K (NC), C107 220pF

CT28 100uF/6.3V, CT29 100uF/6.3V
AC9714_OUT_L 10, AC9714_OUT_R 10
16 or 32 ohm hp
R203 47K, R204 47K

R206 100K
AC9714_MICBIAS 10

CT30 4.7uF/6.3V, CT31 4.7uF/6.3V, CT32 4.7uF/6.3V

CT19~24, 30~32 should be placed as close as to the codec chip

Power

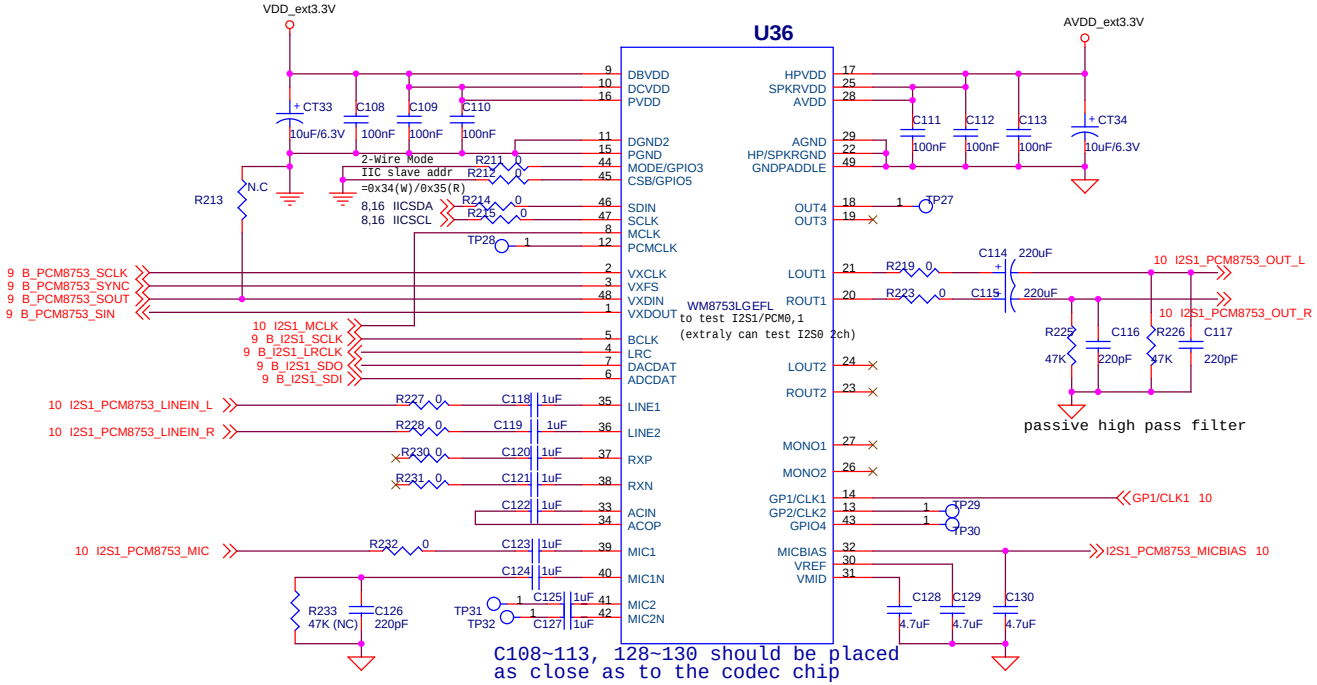
VDD_ext5V, AVDD_ext5V, VDD_ext3.3V, AVDD_ext3.3V
L7 BLM18PG121, L8 BLM18PG121, L9 BLM18PG121
<--LINE!!
CT17 10uF/6.3V, CT18 10uF/6.3V

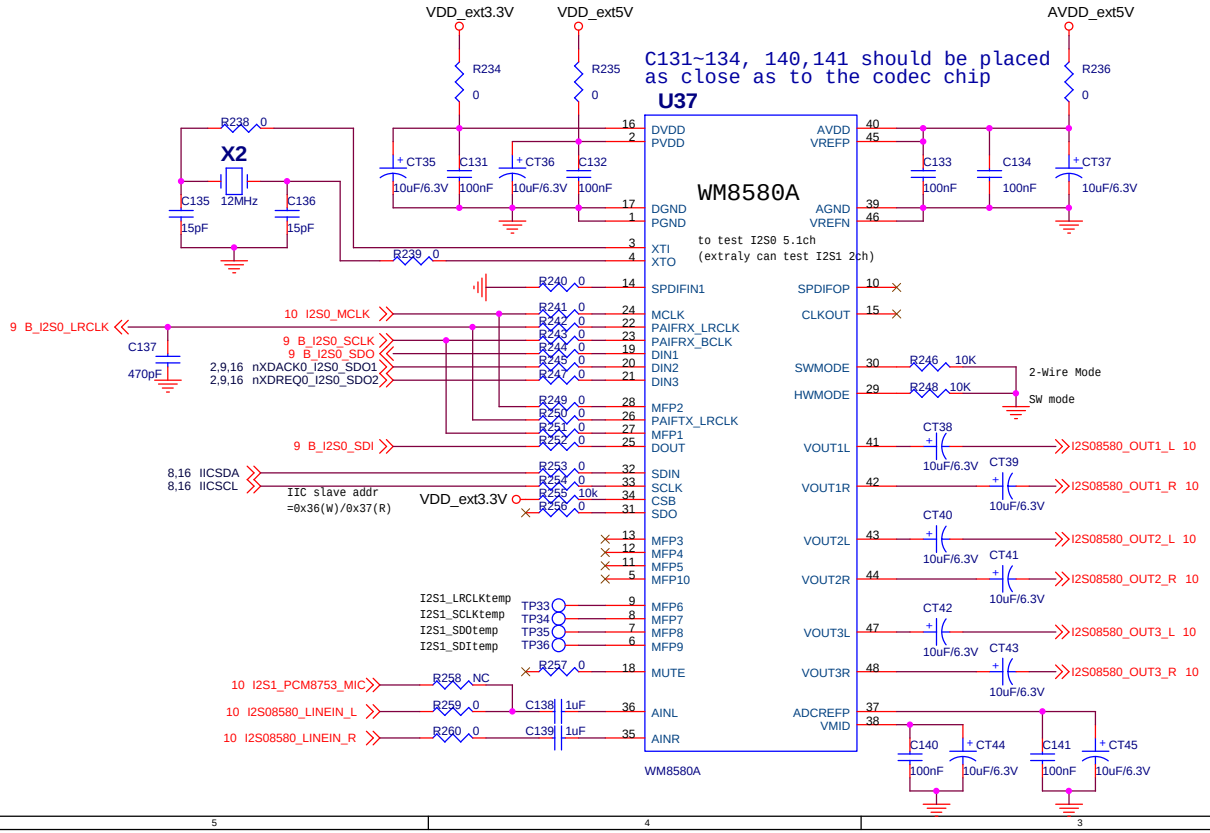
U35

MIC5219BM5: IN, OUT, GND, EN, ADJ
VDD_ext5V, VDD_ext1.8V, Vout
CT25 10uF/6.3V, CT26 10uF/6.3V
R196 220K 1%, R198 100K 1%
280K => 3.3V

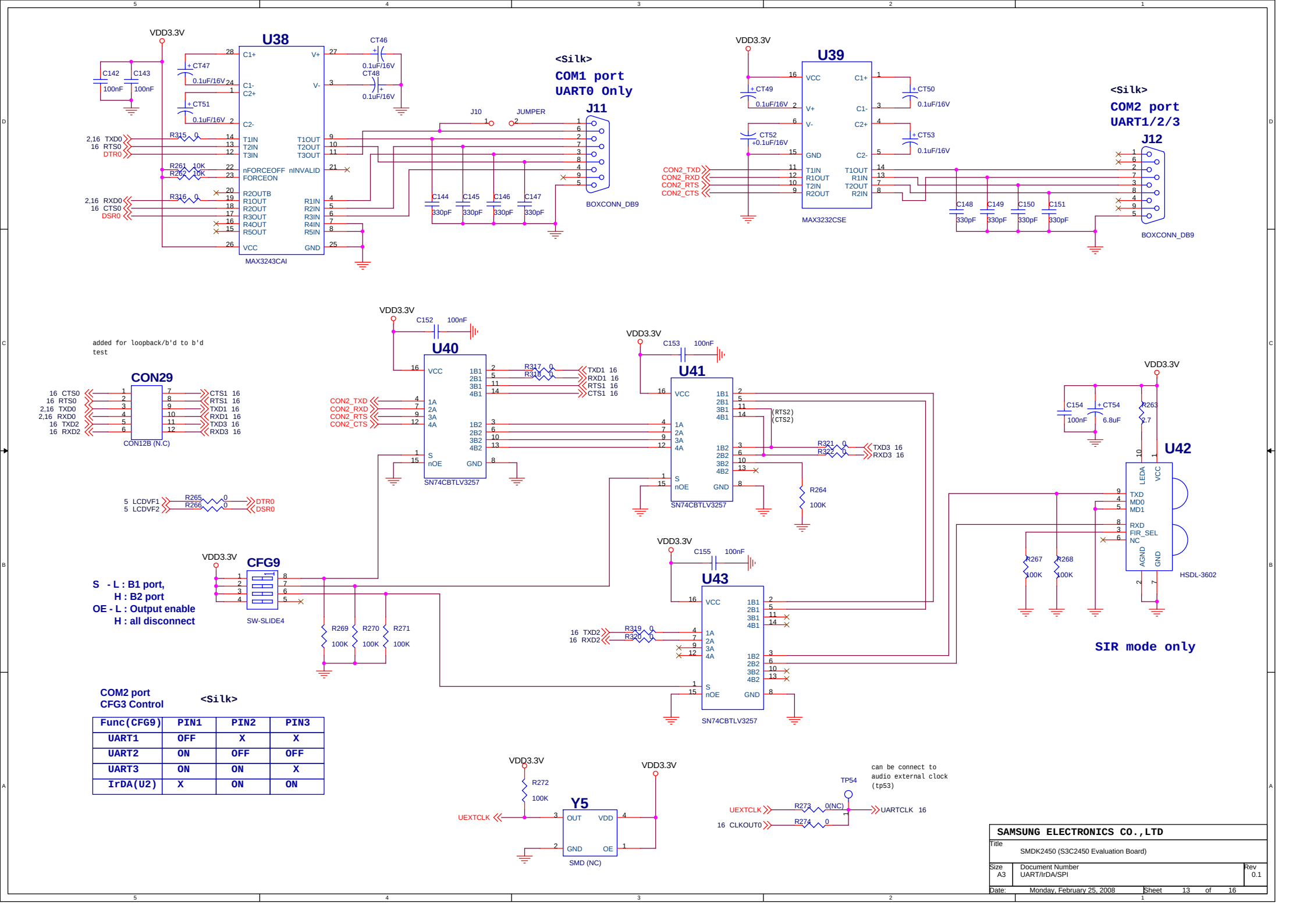
Vout = 1.24V(1+R2/R1)

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: AC97&Power	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 11 of 16	





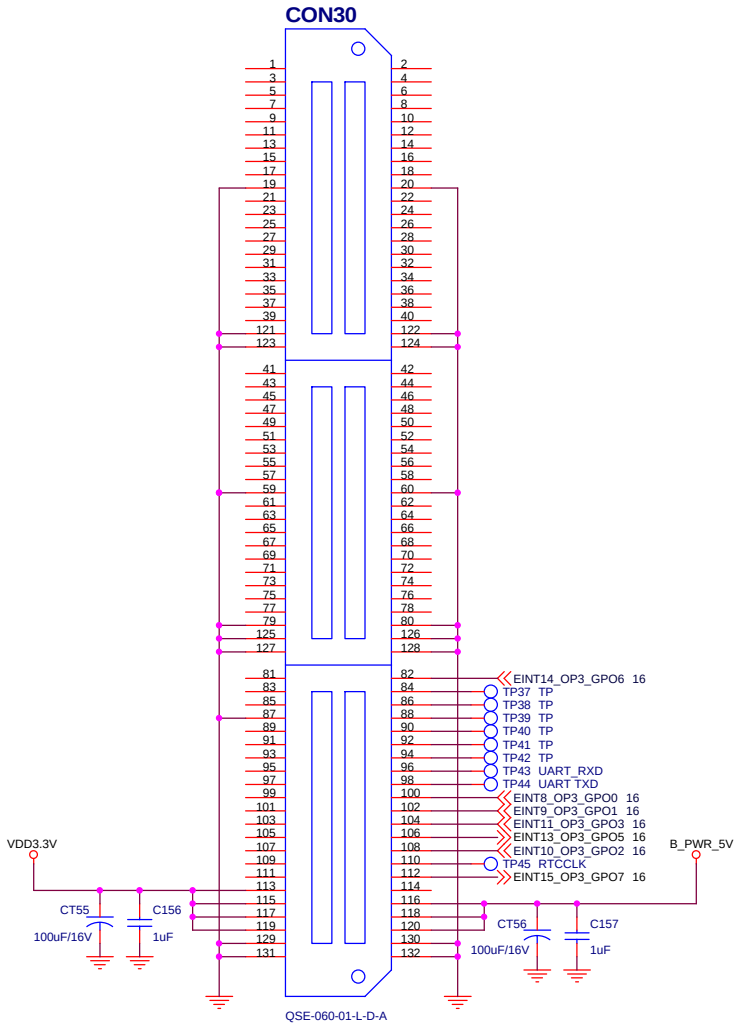
SAMSUNG ELECTRONICS CO.,LTD	
Title	SMDK2450 (S3C2450 Evaluation Board)
Size A3	Document Number I2S 5.1ch/I2S&PCM — Rev 0.1
Date: Monday, February 25, 2008	Sheet 12 of 16



COM2 port CFG3 Control **<Silk>**

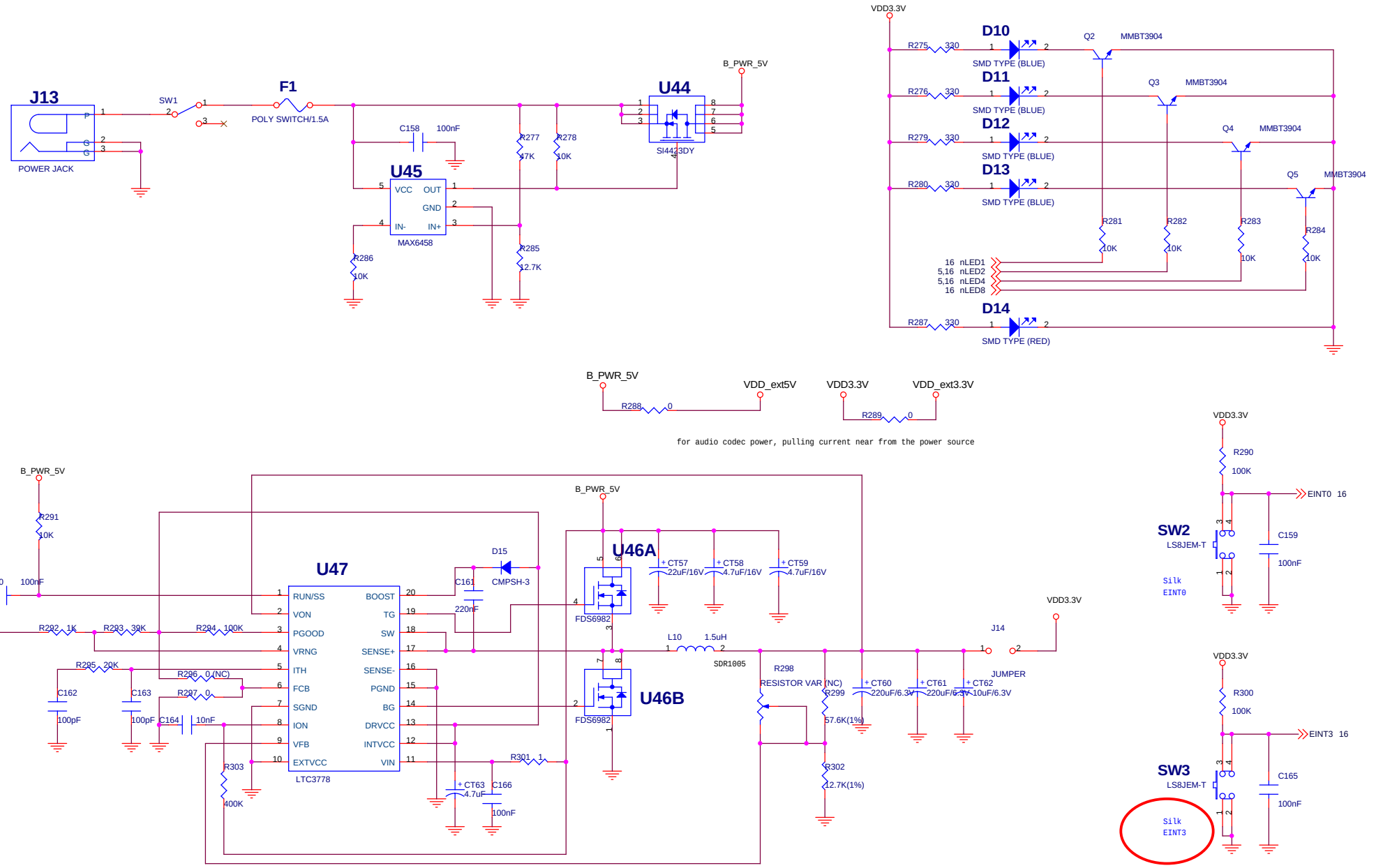
Func(CFG9)	PIN1	PIN2	PIN3
UART1	OFF	X	X
UART2	ON	OFF	OFF
UART3	ON	ON	X
IrDA(U2)	X	ON	ON

SAMSUNG ELECTRONICS CO.,LTD	
Title: SMDK2450 (S3C2450 Evaluation Board)	
Size: A3	Document Number: UART/IrDA/SPI — Rev: 0.1
Date: Monday, February 25, 2008	Sheet 13 of 16

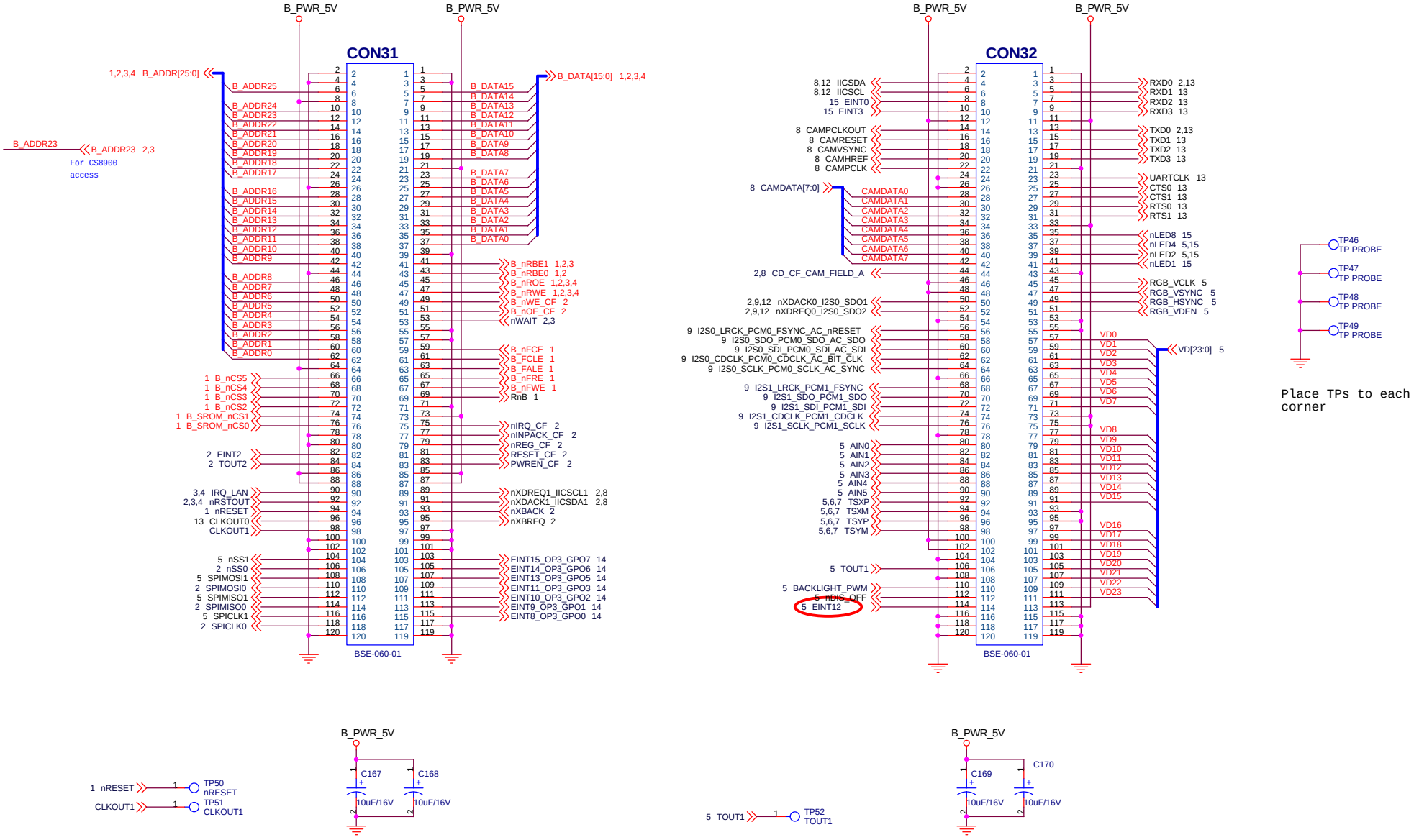


External I/O

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: External I/O	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 14 of 16	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Base board Power & LED	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 15 of 16	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Board to Board connector	Rev: 0.1
Date: Monday, February 25, 2008	Sheet 16 of 16	