FM-1288

High Performance Voice Processor for Automotive Handsfree

User Configuration Manual
(Product Information) version 0.6

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Status Information

The status of this User's Configuration Manual is **Production Information**.

Advance Information

Information for designers concerning Fortemedia product in development. All values specified in the document are the target values of the design. Minimum and maximum values, if specified, are only given as guidance to the final specification limits and must not be considered as the final values.

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Product Information

Final User's Configuration Manual including the guaranteed minimum and maximum limits for the electrical specifications.

Product User's Configuration Manual supersede all previous document versions.

Note

While every case has been taken to ensure the accuracy of the contents in this Data Sheet, Fortemedia cannot accept responsibility for any errors. Fortemedia reserves the right to make technical changes to its products as part of its development program.

TABLES

Document History

Revision	Date	Description
0.1	Feb 20, 2012	Early Draft, original publication date
0.2	March 25, 2012	Editorial updates, 1st draft Advance Information
0.3	June 04, 2012	Yan Tang, First Release Draft
0.4	July 01, 2012	Yan Tang, AiGuo Zhang, Harry Liu, et al. First Release version
0.5	July 03, 2012	AiGuo Zhang, editorial updates
0.6	Sept 20, 2012	Harry Liu, editorial updates

1.0 Overview

This document lists and describes all the control parameters accessible to the user for controlling the FM1288 Voice Processor.

The information contained in this document helps the user to

- Set up the FM-1288 hardware for different operation modes ;
- Debug the system data path during system integration ; and
- Adjust the various parameters to optimize for performance in different acoustic settings

2.0 Glossary and Notation

For a full list of terminology and glossary, please see **References** at the end of this document.

Throughout this document, these terminologies and abbreviations are used freely:

Echo refers to the sound signal coupled from the loudspeaker output back into the microphone input via the acoustic path 回声

Near end (NE) refers to the local conversation end point using the voice terminal equipped with the FM-1288

Far end (FE) refers to the conversation end point opposite to the near end

Double Talk(DT) refers to the situation during which Near end talker and Far end talker are talking at the same time 两端同时说话

Receiving Direction refers to the line-in voice path going towards loudspeaker output line in---

Sending Direction refers to the microphone input voice path going towards line-out mic-->line-out

Para[***address*****,** ***ID*** **]** is the notation used to denote a FM-1288 configurable parameter with name *ID* in alphanumeric and located at the data RAM *address* represented in hexadecimals

3.0 General configuration

The following is a description on how to set the general configuration by the host processor through the Serial Host Interface (SHI) port which is an I^2C-compatible interface.

The default general configuration profile for FM-1288 is 1-microphone input mode, running under 8 kHz sampling rate for microphone in, line in and line out. On this voice processor, the Microphone input ADC and Speaker out DAC sampling rate are always fixed to be 16 KHz. The line in and line out signal pair could be configured to either 16 KHz or 8 KHz depending on the application configuration. The voice processing performed is always in the higher resolution of 16 KHz to ensure the best possible quality, and down-sampling to 8 KHz will be done automatically for proper rate matching when line in/out pair is configured to 8 KHz.

3.1 Default Profile Setup 默认设置

1) Select internal profiles by setting **Para[0x22F8, profile_index]** as following:

Para[0x22F8, profile_index]	Internal profile
0x8000	1mic 8k (VDA setup)

2) Configure the user setting for the appliance.

3) To set **Para[0x22FB, dv_parser_sync_flag]** synchronization flag, the default value of it is 0x8000; writing it to 0 means that configuration has been completed. 默认0X8000 值为0 配置成功

For example, VEC

```
0x22f8      0x0     : choose profile
0x2301      0x12    : user's setting (Optional)
0x2302      0x1     : user's setting (Optional)
0x22fb      0x0     : let IC run after configuration is done
```

3.2 Bandwidth Control Selection

Para[0x2301, sample_rate]	Internal profile
0x0002	16KHz MIC/SPK sample rate, PCM/I2S data rate set to 16KHz. -->16Khz 16Khz-->
0x0012	-->16Khz 8khz--> 16KHz MIC/SPK sample rate, PCM/I2S data rate set to 8KHz

3.3 Single Microphone Hands-free Application Recommended Settings

For the Hands-free single-microphone mode in the most commonly deployed automotive applications, the following key voice processing components can be configured as follows:

Table 1: Single Microphone Hands-Free Application Settings 免提单麦克

Component	1 microphone hands free applicaton Recommended option 推荐设置
Mic-in HPF/ Line-in HPF	On
AEC	On
BF (1-mic mode, no BF)	Off
BVE	On
DRC	On
SPK_ATTN	On
PF	On
FENS	On
Line-in AGC / Mic-in AGC	Off
Mic de-emphasis filter	On
Line-in emphasis filter / de-emphasis filter	Off
Idle noise suppression	On
Adjust noise suppression according to SNR	On
Noise residue stabilizer	On
Mic-in emphasis filter	Off/On
Spk-out HPF	On
BWE	Off

4.0 Microphone Signal Conditions for FM-1288

Before starting any parameter tuning, the microphone mounting in the target system should be checked first to ensure that the system can work properly.

Consideration of Air-tightness for microphones 检查敏感度

Good mechanical design and mounting ensure air-tightness, which is very important to prevent performance degradation. To test airtight for main microphone, play the same NE (or FE) sound, then cover/uncover main microphone, and then record both signals respectively to find out the difference between the two. Then apply the same procedure to the reference microphone. A difference of 15dB or more is considered as a good condition.

Table 2: Air-tight Condition for Microphones

	Mic sensitivity without covered by mud (dB)	Mic sensitivity with covered by mud (dB)	Criterion
NE	Ane	Bne	Ane – Bne > 15db
FE	Afe	Bfe	Afe – Bfe > 15db

To verify if the microphone sensitivities have been properly set, first clear these:

Para[0x3807, MAX_MIC0_readout], and 麦克风敏感度
Para[0x3809, MAX_LIN_readout].

Then play the typical test vectors to watch the 2 parameters which must not be saturated for microphone input and line-in signals.

The microphone signal should not be saturated except under usual conditions, such as wind blow, strong vibration, peak Far End talk volume, etc., especially during Far End talks. If on average the microphone is saturated more than once every several seconds, the performance will be much degraded, and there is something wrong with the acoustics of the system.

Configure the system to play out a loud audio signal from the speaker, the peak digital value should not reach 0x7fff.

Confirm the delay between the echo and line-in signal for proper AEC operation: the delay should be larger than **Para[0x2339, _tdaec_delay_length]** and it ought to be a system-dependent, but time-invariant, constant value. 延迟时间 要大于 0xx2339 的值，时间

5.0 Debugging Support Information

Table 3: Debugging Signals

Index	Address	Signal	Description
1	0x0000	Mic0 signal	Mic0 input signal
2	0x0001	Mic1_signal	Mic1 input signal
3	0x0002	Linein_signal	Linein input signal
4	0x01da	Lineout_dac	Analog lineout signal
5	0x01db	Spkout_dac	Analog spkout signal
6	0x0004	Lineout_digital	I2s/pcm lineout signal
7	0x0007	Fe_vad	The VAD to indicate the far end signals into mic(echo)
8	0x0008	Fe_vad_big	The VAD to indicate the big far end signals into mic(big echo)
9	0x0009	Fe_vad_li	The VAd to indicate the far end signals
10	0x000b	Vad01	subband vad0 for 172Hz ~672Hz
11	0x000c	Vad02	subband vad0 for 672Hz ~1359Hz
12	0x000d	Vad03	subband vad0 for 1297Hz ~2391Hz
13	0x000e	Vad04	subband vad0 for 2328Hz ~4000Hz
14	0x000f	Vad05	subband vad0 for 4000Hz ~6800Hz
15	0x0010	Td_lf_vad	The VAD to indicate the low frequency double talk
16	0x0011	Aec_wrong_vad_cntr	Counter to show AEC wrong or not
17	0x0012	DR_bin_cnt	The VAD to indicate the far end signals, looser than Fe_vad_li.
18	0x0013	Fe_vad_li_fq	The VAD to indicate the far end signals
19	0x0018	Vad0_pop	The modulated near end voice VAD
20	0x0019	Noise_pow_avg	The noise average power
21	0x001a	Idle_noise_pow	The noise power after noise suppression
22	0x23f1	Signal_pass[0]	The sending signal of main channel before AEC 发送主要信息通道 降噪前
23	0x23f3	Signal_pass[2]	The sending signal of main channel before BEAM2 with micgain0 applied
24	0x23f5	Signal_pass[4]	The sending signal of main channel before NS
25	0x23f6	Signal_pass[5]	The sending signal of reference channel before NS 参考信号
27	0x23f7	Signal_pass[6]	The sending signal of main channel after NS
28	0x23f8	Signal_pass[7]	The sending signal of reference channel after NS, the estimated noise
29	0x23f2	Signal_pass[1]	The receiving signal before FENS
30	0x23f4	Signal_pass[3]	The receiving signal after FENS
31	0x23ff	Signal_pass[14]	The reference signal to AEC

If I^2S are not available for some product design, or only the analog signal can be passed out, SAMTuner is suggested to be used for debugging and tuning with vad information.

Para[0x232c, vad_info_bitset] shows VAD info. Each bit of this parameter holds a certain VAD info which is associated with the GUI-based SAMTuner for easy tunings. 显示语音活动检测信息

Para[0x3807 ~ DM0x380a] provides the current max values of all inputs and outputs, the information is refreshed in every sample. You can set **Para[0x3807 ~ DM0x380a]** to zeros to clear this information for a second tuning.所有输入输出信息

Para[0x3813, debug_flag] is a very important debug flag that can be used for tuning. 调试标记

- Turn off the modules on the data path that are of no concern to you so that they will not affect the debug information you need.
- Set **Para[0x230c,mic_volume]** as 0x100 unit gain to see the original signal. 原始信号
- Setting **Para[0x3813,debug_flag]** as one of the above table can pass the corresponding signal multiple mic_volume to line-out.
- Note that if **Para[0x3813,debug_flag]** is set as 0, lineout is **normal lineout signal**. So if you want to get mic0 input signal (address=0), need to set them as the following:

  mic 0(input)-->line out

  - **Para[0x22EE, _mic_revert_mode]** = 1 (and remember to restore it to zero for normal operation). 记得回复至0
  - **Para[0x3813,debug_flag]** =1

22ee
3813

5.1 Bypass modes

Table 4: Signal Paths and Gains of Bypass Modes

mode	Uplink 上行		Downlink	
	path	gain	path	gain
1	mic0-> chi0_tx	0 db	chi0_rx->spk	0 db
2	Mic1-> chi0_tx	0 db	chi0_rx->spk	0 db
3	mic0/mic1-> i2s0_tx	0 db	i2s0_rx->spk	0 db
0x10	Mic0-> spk	0 db	Lin->lineout(PCM)	0 db

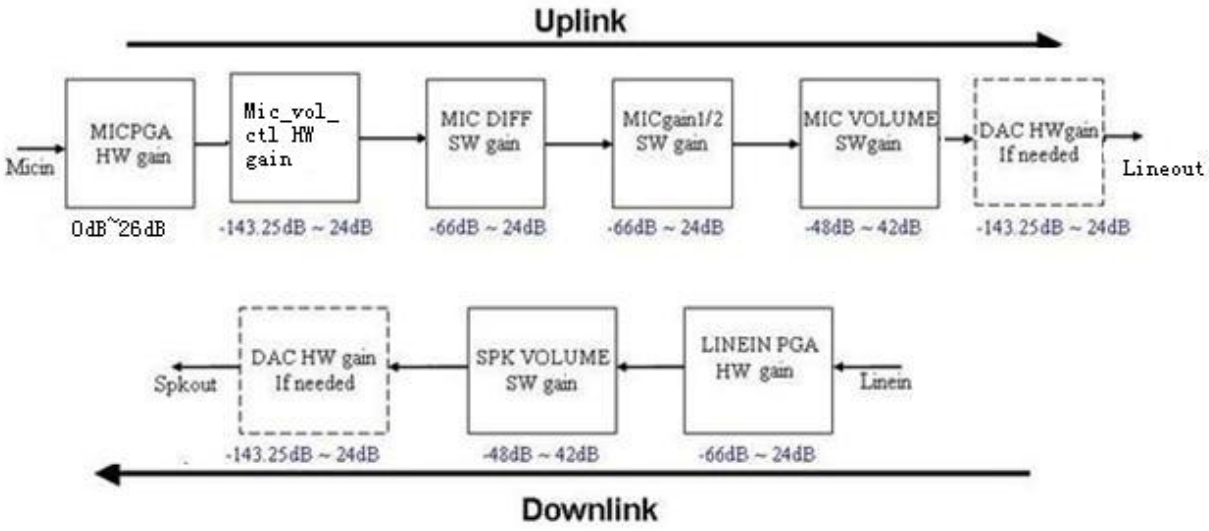
Table 5: Bypass Modes key parameters

Address	Name	Description	Default Value 预设值
0x22FA	_dv_enable_b	Device enable. D0: MIC0 D1: MIC1 D2: MICBIAS D3: Analog spkout D4: Analog Line in D5: Analog Line out D8: PCM/I2S select, =1, PCM enable D11: DPLL track enable/disable, =1, track enable; =0, track disable D15: Reserved	0x003F 0x25
0x2300	_line_pass	=0: normal mode; =1:PCM-mono bypass mode. mic0->chi0_tx without gain,chi0_rx ->spk without gain. =2:PCM-mono bypass mode. mic1->chi0_tx without gain,chi0_rx -> spk without gain. =3:IIS bypass mode. MIC0/1 to I2S L/R Trans channel without gain, I2S L or R Recv data to SPK out without gain. =0x10: MIC0 -> SPK, and LIN->Lout (PCM) without gain.	0x0000
0x2301	_sample_rate	Overall sampling rate. Bit [0:3] : =2: 16KHz normal mode, CODEC and PCM/I2S are both set to 16Kz. =0x12: CODEC 16KHz and PCM/I2S are set to 8KHz	0x0012

6.0 Performance Tuning 性能调节

This section discusses the performance tuning procedure in detail. First the **Gain Flow** and the **VADs** will be introduced. There are different gains and VADs designed at various locations on the signal path, the user must have an overall idea about gain flow and VADs in advance. And then the detailed **Performance Tuning Procedures** will be provided, the tuning sequence is conformant to that designed using with the GUI based SAMTuner.

6.1 Gain FLow



Gain flow for sending and receiving directions

1) **Para[0x22e5, _adc_pga_gain] bit[7:4], mic1, bit[3:0], mic0;** 0x22--10 0010 0010

增益设置

Mic in /line PGA setting

LINE_IN_PGA[11:8], MIC1_IN_PGA[7:4], MIC0_IN_PGA[3:0]	PGA Gain (dB)
[0 0 0 0]	-2
[0 0 0 1]	-1
[0 0 1 0]	0
[0 0 1 1]	2
[0 1 0 0]	4
[0 1 0 1]	6
[0 1 1 0]	8

[0 1 1 1]	10
[1 0 0 0]	12
[1 0 0 1]	14
[1 0 1 0]	16
[1 0 1 1]	18
[1 1 0 0]	20
[1 1 0 1]	22
[1 1 1 0]	24
[1 1 1 1]	26

2) **Para[0x2307, mic_vol_ctl],** it includes two parts: Coarse control and Fine control for hardware digital gain. 0xf8f8

Gain = Coarse Gain + Fine Gain

Coarse control (Bit [7: 4])

Bit [7:4]	E	F	0	1	2	3	4	5	6	7	8	9	A	B
Gain (dB)	+24	+12	0	-12	-24	-36	-48	-60	-72	-84	-96	-108	-120	-132

Fine control (Bit [3: 0])

Bit [3:0]	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Gain (dB)	0	-0.75	-1.5	-2.25	-3	-3.75	-4.5	-5.25	-6	-6.75	-7.5	-8.25	-9	-9.75	-10.5	-11.25

3) **Para[0x2348, micgain0]**, Level boost on main channel, 0x0800 as unit gain; 05A0

4) **Para[0x2349, micgain1]**, Level boost on reference channel, 0x0800 as unit gain; 06A0

5) **Para[0x22e5, _adc_pga_gain] bit[11:8], linein_pga,** setting uses the table above;

6) **Para[0x230D, spk_volume],** 0x100 as unit gain. 0180

7) **Para[0x22e9,_dac_pga_gain],** DAC PGA gain for Lineout and speaker out, setting uses the tables below.

DAC LINE_OUT PGA Table

LINE_OUT_PGA[3:0]	LINE_OUT PGA Gain Control (dB)	Differential Output Signal (Vpp)
[0 0 0 0]	+2	3.00
[0 0 0 1]	0	2.40
[0 0 1 0]	-2	1.91
[0 0 1 1]	-4	1.51
[0 1 0 0]	-6	1.20

[0 1 0 1]	-8	0.95
[0 1 1 0]	-10	0.76
[0 1 1 1]	-12	0.60
[1 0 0 0]	-14	0.48
[1 0 0 1]	-16	0.38
[1 0 1 0]	-18	0.30
[1 0 1 1]	-20	0.24
[1 1 0 0]	-22	0.19
[1 1 0 1]	-24	0.15
[1 1 1 0]	-26	0.12
[1 1 1 1]	-28	0.09

Programmable Gain range: +2dB ~ -28dB & Step : -2dB

DAC SPK_OUT PGA Table

LINE_OUT_PGA[3:0]	LINE_OUT PGA Gain Control (dB)	Differential Output Signal (Vpp)
[0 0 0 0]	+2	3.00
[0 0 0 1]	0	2.40
[0 0 1 0]	-2	1.91
[0 0 1 1]	-4	1.51
[0 1 0 0]	-6	1.20
[0 1 0 1]	-8	0.95
[0 1 1 0]	-10	0.76
[0 1 1 1]	-12	0.60
[1 0 0 0]	-14	0.48
[1 0 0 1]	-16	0.38
[1 0 1 0]	-18	0.30
[1 0 1 1]	-20	0.24
[1 1 0 0]	-22	0.19
[1 1 0 1]	-24	0.15
[1 1 1 0]	-26	0.12
[1 1 1 1]	-28	0.09

Programmable Gain range: +2dB ~ -28dB & Step : -2dB

6.2 Activity Detectors (VAD)

8	0x0008	Fe_vad_big	The VAD to indicate the big far end signals into mic(big echo)
9	0x0009	Fe_vad_li	The VAd to indicate the far end signals
10	0x000b	Vad01	subband vad0 for 172Hz ~672Hz
11	0x000c	Vad02	subband vad0 for 672Hz ~1359Hz
12	0x000d	Vad03	subband vad0 for 1297Hz ~2391Hz
13	0x000e	Vad04	subband vad0 for 2328Hz ~4000Hz
14	0x000f	Vad05	subband vad0 for 4000Hz ~6800Hz
15	0x0010	Td_lf_vad	The VAD to indicate the low frequency double talk
16	0x0011	Aec_wrong_vad_cntr	Cntr to show aec wrong or not
17	0x0012	DR_bin_cnt	The VAD to indicate the far end signals,looser than Fe_vad_li.
18	0x0013	Fe_vad_li_fq	The VAD to indicate the far end signals
19	0x0018	Vad0_pop	The molulated near end voice vad

The indices 8~19 in the above are frequently used VADs that users often need to examine during perform module performance tuning. The following are some detailed description of the VADs.

1) **FE_VAD:** It is judged in linear AEC module and **controls** the latter echo cancellation related modules. When there is FE voice, FE_VAD should be on; must turn on bit8 of **Para[0x2304,_sp_flag]** to observe FE_VAD.

2) **FE_VAD_BIG**: It is judged in linear AEC module and controls the latter echo cancellation related modules. When FE voice is big, FE_VAD_BIG should be on; must turn on bit8 of **Para[0x2304,_sp_flag]** to observe FE_VAD_BIG.

3) **FE_VAD_LI**: It is judged in FENS module and controls AEC and the latter echo cancellation related modules. When FE voice exists, FE_VAD_LI should be on; must turn on bit14 of **Para[0x2303,_kl_config]** to observe FE_VAD_LI.

4) **Td_lf_vad :** It's used to indicate Double Talk and associated with post filter, speaker attenuation, Fq_NS process. Td_lf_vad is judged in time domain. Under no ambient noise case, if there is NE or double talk, td_lf_vad should be on.

5) **VAD01~VAD05** : They are subband vad0 which are judged in frequency domain when FE doesn't exist. When there is only NE (no double talk) under high SNR condition, vad01~vad05 should be on.

6) **Vad0_pop**: the mixture of vad0 and vad01 ~ vad05.

7.0 Performance Tuning Procedure Details

7.1 Linear AEC 线性回声消除

Linear AEC is the first echo cancellation module to cancel linear echo. It can be turned on or off by setting or clearing bit 8 of **Para[0x2304, _sp_flag].**

Table 6: Linear AEC parameters

Index	Address	Parameter name	Description
1	0x2339	tdaec_delay_length	Additional buffer to account for the Codec delay of the AEC path. Maximum: 0x68, **Minimum:0** 延时
2	0x232f	aec_ref_gain	Gain for AEC ref channel. Unit gain: 0x100 回声 参考通道增益
3	0x2337	tdaec_nw_shift	Control convergent speed and convergent stability. Bigger value will make convergence faster and more unstable. **Range:0xFFF0~0** 控制收敛速度
4	0x2333	tdaec_fe_vad_th	Threshold for fe_vad decision. Lower values can cause more active echo cancellation. Range: 0~0x7FFF 回应消除 阀值
5	0x2332	tdaec_fe_vad_th_high	Threshold for fe_vad_big decision. Higher values can increase vad0 decision and decrease frequency domain echo suppression, the effect is less echo suppression and more full duplex maintained. Range: 0~0x7FFF

远端(linein) 近端(Mic)

Criterion: For NE signals, the processed signal should be nearly same as the input of linear AEC; For FE signals, the processed signal should have above 15dB attenuation. Normally good AEC performance can achieve above 18dB echo cancellation.

Please note the following:

1) **Para[0x2339, aec_delay_length] -** it can be used to compensate for long delay between echo (0x23f1, signal Pass[0]) and AEC reference input (0x23ff, signal_pass[14]) signals. By recording the two signals, tone signal is suggested to be played as the linein, the actual delay D1 can be measured. Make sure that **Para**[0x2339, aec_delay_length] is smaller than D1, otherwise linear AEC can't work. 延时时间 要大于两个信号的延时，否则无法工作

2) **Para[0x232f, aec_ref_gain] -** it is used to balance the power difference between echo and AEC reference input signals. Check AEC reference input (0x23ff, signal_pass[13]) signals to make sure it is not saturated.

7.2 Frequency Domain Activity Detectors 频域活动检测

These are the key parameters for VAD01, VAD02, VAD03, VAD04, and VAD05

Table 7: Voice Activity Detectors - VAD01, VAD02, VAD03, VAD04, VAD05

Index	Address	Parameter name	Description
1	0x2382	_fqpara_vad_thrd_low	SNR threshold for vad01. if sub-band SNR smaller than this threshold. Range: 0~0x7FFF
2	0x2383	_fqpara_vad_thrd_high	SNR threshold for vad02~vad05. if sub-band SNR smaller than this threshold. Range: 0~0x7FFF

Criterion :

VAD01, VAD02, VAD03, VAD04, and VAD05 are similar to subband vad0 under high SNR, which won't flash when FE exists and should flash when in-beam NE voice exists for corresponding subband.

7.3 Frequency Domain Noise Suppression

频域：噪声抑制，回音消除，通过0x2303（bit0）来控制是否开启

Frequency domain includes NS and nonlinear echo cancellation functions. It can be turned on or off by setting or clearing bit0 of **Para[0x2303, _kl_config].**

Frequency domain NS supply non-stationary NS and stationary NS for HS mode and only supply stationary NS for 2mic HF and 1mic HF mode. There are some key parameters affecting its performance as listed in the table below:

Table 8: Frequency Domain Noise Suppression (FDNS) parameters

Address	Parameter name	Description	Sub Module
0x236E	**_ss_bounds_high[0]**	Noise suppression level, 0x7fff is unit gain, means 0db noise suppression, smaller value makes heavier noise suppression and less voice pass. Range: 0~0x7FFF	抑制噪声　值越大越弱
0x236F	**_ss_bounds_high[1]**	base gain factor for noise suppression, will be self-doubled if vad01 ≤ 0. A larger value means heavier suppression and less voice passed thru. Range: 0~0x7F7F Bit[15~8]: base gain factor for f < 2350Hz component; Bit[7~0]: extra gain factor on base gain for f ≥ 2350Hz component after left banked; Default value = 0x0B80 but it is improper, please configure it to **0x0B05**. this means 0x0B00 as gain factor for f < 2350Hz, and 0x1000 = (0xB00 + 0x500) as gain factor for f ≥ 2350Hz.	Gain factor initialization 值越大 过滤越多
0x2370	**_ss_bounds_high[2]**	extra gain factor for noise suppression when no big echo, will be applied if voice probability very low, bigger value can reduce watering sound. Range: 0~0x7FFF	额外增益，。没有大的回声，就无语音 值越大　减少回声噪声（）
0x2373	**_fqpara_gndL_div**	Noise tracking factor to adapt to not so stable stationary noise. Larger value when outside noise goes up and down frequently. (180~440Hz). Range: 0~0x7FFF	Noise ground 噪音 参考面 噪音变化越大，值越大

0x2374	**_fqpara_gndM_div**	Noise tracking factor for 440~2300Hz. Range: 0~0x7FFF	
0x2375	**_fqpara_gndH_div**	Noise tracking factor for 2300~7500Hz. Range: 0~0x7FFF	
0x2384	**_fqpara_snr_order**	Threshold for speech SNR, higher value will suppress more noise and keep less voice. Range: 0~0x9 信噪比阀值	SNR_ADJUST, which is controlled by bit 7 of **Para[0x2303, _kl_config]**
0x239C	**_fqpara_inbeam_dec**	Weakens NS when SNR is very high. Higher value improves voice quality in quiet environment, but also raises noise floor. Therefore, it needs to be tuned together with idle noise suppression. Range: 0~0x7FFF	
0x23ED	**_idle_noise_thrd**	idle noise suppression will be applied if noise level lower than this threshold. Bigger value will make idle noise cut more active. Range: 0~0x7FFF	IDLE noise , which is controlled by bit 8 of **Para[0x2303, _kl_config]**
0x23EE	**_idle_ins_attn**	The suppressing level for idle noise, 0x7fff is unit gain. Range: 0~0x7FFF	

Criterion: Pure NS should be stable without obvious watering sound; NS for NE with noise should have no obvious noise up when NE and noise down between NE interval as well as keeping more small NE voice.

Please note the following:

FDNS parameters are user preference settings. If the default can't be accepted, the following steps are recommended:

1) **Step 1:** FDNS level has direct relationship with **Para[0x236E~0x2370],** normally when adjust NS level to smaller (**Para[0x236E, _ss_bounds_high[0])** with heavier suppression, need to adjust gain factor to bigger (**Para[0x236f~0x2370])** to avoid noise up and down at the same time;

2) **Step 2:** **Para[0x2384, _fqpara_snr_order] is** a fine-adjustment compensation parameter, generally used for different chassis related to the talker mouth to phone microphone distance, depending on the phone type. The default is using bartype phone. 微调

3) **Step 3:**Only when the suppressed stationary or non-stationary noise has special high residue for some frequency range, **Para[0x2373~0x2375]** can be considered to raise for related frequency range to get more stable noise suppression;

4) **Step 4: Para[0x239c~0x239e]** allow the user to exercise fine control over non-stationary noise reduction based on observed signal-to-noise ratio(SNR). **Para[0x239c]** is for SNR observed in beam.

5) **Step 5:** Idle noise sub module will generate a suppressed gain which will be applied at the point of mic_volume in the gain flow. So if you use modules turn on/off to see the modules before mic_volume apply, remember to turn off idle noise. It is used to make high SNR cases with more clean noise floor, and can be tuned together with **Para**[0x239C, _fqpara_inbeam_dec] for more favorable voice quality and reasonable noise floor.

7.4 Frequency Domain Echo Cancellation 频域回波消除

Frequency domain includes NS and echo cancellation functions. It can be turned on or off by setting or clearing bit0 of **Para[0x2303, _kl_config]**. Frequency domain echo cancellation can be considered as a kind of non-stationary NS together with PF gain apply in frequency domain. There are some key parameters affecting its performance as listed in the table below:

Table 9: Frequency Domain Echo Control parameters

Address	Parameter name	Description	Sub Module
0x2380	**_fqpara_beta_uv_fe**	Beta2 weight for FE only Range: 0~0x7FFF	UND
0x2381	**_fqpara_beta_mixed_fe**	Beta2 weight for Double-Talk Range: 0~0x7FFF	
0x23EE	**_idle_ins_attn**	The suppressing level for idle noise, 0x7fff is unit gain Range: 0~0x7FFF	
0x23B3	**_tdpf_pf_z_factor_exp_high**	Strength of AEC post-filter at no double talk. A larger value results in stronger echo suppression, but less full duplex. Range: 0~0x20	TDPF , which is controlled by bit 9 of **Para[0x2304, _sp_flag]** 值越大 越消除 但是影响双工通信
0x23B4	**_tdpf_pf_z_factor_exp_low**	Strength of AEC at double talk. Higher values give stronger echo suppression, but less full duplex. Range: 0~0x20	
0x23BC	**_tdpf_pf_z_factor_exp_extreme**	Strength of AEC post-filter when: no DT (td_lf_vad<=0, aec_wrong_vad_cntr>0) Higher values gives stronger echo suppression, but less full duplex	

0x23B5	**_tdpf_pf_coef_gain**	Full duplex enhancement factor when DT detected meanwhile echo doesn't dominate. It's possible to let more echo pass through, too! Range: 0~0x7FFF	
0x23B7	**_pf_wait**	Estimated length for echo tail coverage (frames), each frame means 16ms Range: 0~0x32	预计回声长度（不说话后听到的回声），一帧16MS
0x23B8	**_tdpf_min_attn_NE**	pf gain under the case of DT detected meanwhile small echo.	pf增益下，检测到的回声
0x23B9	**_tdpf_min_attn_no_NE**	pf gain under the case of small echo only(no DT).	PF gain under different cases
0x23BA	**_tdpf_max_attn_no_DT**	pf gain under the case of Big echo only(no DT). PF gives the heaviest echo suppression	pf增益下检测到大回声，回声抑制（在没有两端同时说话的情况下）
0x23A5	**_fqpara_pf_start_bin**	Decide which band will be applied into PF function. At frequency < DM0x23a5 * 31.25Hz, don't apply PF gain. RANGE: 0x0~0x10	决定哪些频率的信号，经过PF滤波器
0x23BE	**_lfvad_noise_thrd**	A threshold for DT detection noise floor. Bigger value makes detection harder. if td_lf_vad false alarm under Echo + noise case, set the value smaller to make td_lf_vad detection harder.	
0x23BF	**_lfvad_addon_thrd**	Also threshold for DT detection. Bigger value makes detection harder. This is used together with lfvad_noise_thrd.	DT侦测阀值

Criterion: Pure echo cancellation should be clean, allow more NE voice pass during DT. When stationary noise exists, need to control the noise up and down to a reasonable level.

Please note the following

To investigate actual target device (e.g. PDA) mockup's spectrum character →NE and FE spectrum difference, follow this procedure below:

1) Play NE and FE voice with **Para[0x2310, _linein_HPF_sel]**=0x80, then record from mic0 (0x23f1,signal_pass[0]), find their cross point on the whole.

2) Select right Line-in HPF by setting **Para[0x2310, _linein_HPF_sel]** by NE/FE spectrum cross point. As an example, if the desired crossing point is 360Hz, then the Bit Bit[0] and Bit[2] of **Para[0x2310, _linein_HPF_sel]** are set to select 360Hz line-in path HPF and 270Hz LPF for td_lf_vad detection.

3) Fine tune modules before FD.

4) Play NE and FE voice, fine tune **Para[0x23BE, _lfvad_noise_thrd]** and **Para[0x23BF _lfvad_addon_thrd]** then check td_lf_vad. It should be on when there is DT or NE, and should keep off when there is only echo.

5) Play NE and FE voice under ambient noise environment, then fine tune **Para[0x23BE, _lf_noise_vad_thrd]** . Td_lf_vad should not flash for only noise or noise+echo case.

6) TDPF tuning: Check to make sure that vad3 is fine tuned, then tune **Para[0x23B3~0x23B5**], **Para[0x23b3].**

- **_tdpf_pf_z_factor_exp_high]** is used for only FE exists.
- **Para[0x23b4, _tdpf_pf_z_factor_exp_low**] and the following 3 parameters **Para[0x23b5, _tdpf_pf_coef_gain], Para[0x23b8,** and **_tdpf_min_attn_NE]** are all used for DT.
- Normally **Para[0x23b4, _tdpf_pf_z_factor_exp_low]** < **Para [0x23b3, _tdpf_pf_z_factor_exp_high]**

7) PF gain applying in FD **Para[0x23A5, _fqpara_pf_start_bin]** decide that PF gain won't be applied at frequency < **Para[0x23A5, _fqpara_pf_start_bin**] * 31.25.Hz . Normally, it is decided by the cross point of NE/FE. Bigger value means less echo cancellation and more DT.

8) Echo tail - If echo still exists with corresponding fe_vad not flash, the echo is called echo tail. For some application cases, such as small vehicle chassis, the echo tail is easily captured. **Para[0x23B7, _pf_wait]** estimates the length for echo tail coverage (frames), each frame means 16ms. Such as the echo tail lasts for 120ms → 48/16=3. If the **Para[0x23B7, _pf_wait]** is set as 3, extra echo cancellation will continue even when no fe_vad inside 48ms, so it also will affect DT and NE.

7.5 Lineout Equalizer 均衡器

Lineout equalizer will apply 23-band equalization in the sending direction. It is commonly used to compensate for the frequency response on the microphone to line-out data path. The control parameters of lineout equalizer are described in the following table, and the SAMTuner supplies easier tuning for this module with a graphical user interface (GUI).

Table 10: Line-out Equalizer parameters

Address	Parameter name	Description
0x2390~0x2395	**_fqpara_equal[0~5]**	23-band Line-out EQ. 0x4444 means 0dB gain on all bands. 0x4444 0增益 **_fqpara_equal** [0] defines the gain on band1~band4: Bit[15~12] (109.375Hz ~ 171.875Hz), Bit[11~8] (171.875Hz ~ 234.375Hz), Bit[7~4] (234.375Hz ~ 296.875Hz), Bit[3~0] (296.875Hz ~ 421.875Hz); **_fqpara_equal** [1] defines the gain on band5~band8: Bit[15~12] (421.875Hz ~ 546.875Hz), Bit[11~8] (546.875Hz ~ 671.875Hz), Bit[7~4] (671.875Hz ~ 859.375Hz), Bit[3~0](859.375Hz ~ 1046.875Hz); **_fqpara_equal** [2] defines the gain on band9~band12: Bit[15~12] (1046.875Hz ~ 1234.375Hz), Bit[11~8] (1234.375Hz ~ 1546.875Hz), Bit[7~4] (1546.875Hz ~ 1859.375Hz), Bit[3~0] (1859.375Hz ~ 2171.875Hz); **_fqpara_equal** [3] defines the gain on band13~band16: Bit[15~12] (2171.875Hz ~ 2484.375Hz), Bit[11~8](2484.375Hz ~ 2984.375Hz), Bit[7~4] (2984.375Hz ~ 3484.375Hz), Bit[3~0] (3484.375Hz ~ 3984.375Hz);

		_fqpara_equal [4] defines the gain on band17~band20: Bit[15~12] (3984.375Hz ~ 4484.375Hz), Bit[11~8] (4484.375Hz ~ 4984.375Hz), Bit[7~4] (4484.375Hz ~ 5484.375Hz), Bit[3~0] (5484.375Hz ~ 5984.375Hz); **_fqpara_equal** [5] defines the gain on band21~band23: Bit[15~12] (5984.375Hz ~ 6484.375Hz), Bit[11~8] (6484.375Hz ~ 6984.375Hz), Bit[7~4] (6984.375Hz ~ 7984.375Hz). The gain on each band represented by a 4-bit Gain index - 0: +6dB, 1: +4dB, 2: +2dB, 3: +1dB, 4: 0dB, 5: -1dB, 6: -2dB, 7: -4dB, 8: -6dB, 9: -8dB, A: -10dB, B: -13dB, C: -16dB, D: -20dB, E: -30dB, F: -50dB.

Criterion: Raise or drop corresponding frequency range as the parameter set.

Please note that if the FDNS is turned off, then lineout equalizer won't work because it is a sub module of FDNS.

7.6 Comfort Noise Fill 背景噪音

During the echo cancellation process, the background noise could be suppressed along with residual echo. A noise fill is needed to eliminate the unpleasant effect of noise-pumping, in which case the Far end listening will hear the background noise level going louder and softer. The function is enabled by setting Bit0 of **Para[0x2305, _ft_flag],** and the level of noise pasted is set by **Para[0x2372, _tdsp_noisegain]** with 0x2000 as unit gain.

Criterion: The lineout noise floor should be reasonable flat for only noise and noise with FE.

7.7 Far End Noise Suppression (FENS)

远端噪声抑制

line-in-->spk

FENS is the noise suppression module in the receiving direction. It can be turned on or off by setting or clearing bit14 of **Para[0x2303,_kl_config].** FENS only performs stationary NS.

Table 11: Far End Noise Suppression (FENS) parameters

Address	Parameter name	Description	Submodule
0x23DB	**_FENS_min_gain**	The smallest suppression level for FENS. Bigger value will suppress less noise. Unit gain is 0x7fff. 值越大 抑制噪音能力越小 Range: 0~0x7fff	FENS
0x23DC	**_FENS_VAD_thrd**	Threshold for FENS VAD, bigger value will make less voice pass and more noise suppression; Range:0~0x7fff 远端静音噪声抑制阀值 值越大，通过的声音越少，噪音抑制越多	
0x23DD	**_FENS_vad_cnt_thrd**	Threshold for FENS noise vad counter, when counter bigger than threshold, judge as noise. Bigger value will keep more voice. Range:0~0x20 值越大，越多声音通过	

FENS included internal equalizer will apply 23-band equalization in the receiving direction. It is commonly used to compensate for the frequency response on the line-in to loudspeaker-out data path. The control parameters of the FENS equalizer are described in the following table, and the SAMTuner supplies easier tuning for this module with a graphical user interface (GUI).

Address	Parameter name	Description
0x23DF~0x23e4	**_FENS_equal[0~5]**	23-band SPK-out EQ. 0x4444 means 0dB gain on all bands. **_FENS_equal** [0] defines the gain on band1~band4: Bit[15~12] (109.375Hz ~ 171.875Hz), Bit[11~8] (171.875Hz ~ 234.375Hz), Bit[7~4] (234.375Hz ~ 296.875Hz), Bit[3~0] (296.875Hz ~ 421.875Hz); **_FENS_equal** [1] defines the gain on band5~band8: Bit[15~12] (421.875Hz ~ 546.875Hz), Bit[11~8] (546.875Hz ~ 671.875Hz), Bit[7~4] (671.875Hz ~ 859.375Hz), Bit[3~0](859.375Hz ~ 1046.875Hz); **_FENS_equal** [2] defines the gain on band9~band12: Bit[15~12] (1046.875Hz ~ 1234.375Hz), Bit[11~8] (1234.375Hz ~ 1546.875Hz), Bit[7~4] (1546.875Hz ~ 1859.375Hz), Bit[3~0] (1859.375Hz ~ 2171.875Hz); **_FENS_equal** [3] defines the gain on band13~band16: Bit[15~12] (2171.875Hz ~ 2484.375Hz), Bit[11~8](2484.375Hz ~ 2984.375Hz), Bit[7~4] (2984.375Hz ~ 3484.375Hz), Bit[3~0] (3484.375Hz ~ 3984.375Hz); **_FENS_equal** [4] defines the gain on band17~band20: Bit[15~12] (3984.375Hz ~ 4484.375Hz), Bit[11~8] (4484.375Hz ~ 4984.375Hz), Bit[7~4] (4484.375Hz ~ 5484.375Hz), Bit[3~0] (5484.375Hz ~ 5984.375Hz);

		_FENS_equal [5] defines the gain on band21~band23: Bit[15~12] (5984.375Hz ~ 6484.375Hz), Bit[11~8] (6484.375Hz ~ 6984.375Hz), Bit[7~4] (6984.375Hz ~ 7984.375Hz). The gain on each band represented by a 4-bit Gain index - 0: +6dB, 1: +4dB, 2: +2dB, 3: +1dB, 4: 0dB, 5: -1dB, 6: -2dB, 7: -4dB, 8: -6dB, 9: -8dB, A: -10dB, B: -13dB, C: -16dB, D: -20dB, E: -30dB, F: -50dB.

Criterion: Pure NS should be stable without obvious watering sound; NS for FE with noise should has no obvious noise up when FE and noise down between NE interval as well as keeping more small FE voice.

Please note that if the FENS is turned off, then lineout equalizer won't work because it is a sub module of FENS. 关闭 FENS，line-out equalizer无法工作

7.8 Bright Voice Enhancement (BVE) 响亮语音增强

接受方向 line-in-->spk

BVE module will control the output gain of the receiving direction by the ambient noise collected by mic, high ambient noise will lead to higher gain to bright the spkout voice.

It can be turned on/off by setting/clearing bit 4 of **Para[0x2305, _ft_flag].** There are some key parameters affecting its performance as listed in the table below:

Table 12: Bright Voice Enhancement (BVE) parameters

Address	Parameter name	Description
0x22D3	**_AVC_SNR_thrd**	Works when Bit[4] of 0x2305 is ON. This sets the SNR threshold to trigger be action, smaller value means it is harder to trigger be 值越小，越难触发
0x22D4	**_AVC_vol_thrd**	Works when Bit[4] of 0x2305 is ON The threshold to trigger frequency adjustment (decrease low and increase high freqency). When avc_gain_out >threshold, it will trigger the frequency adjustment. DM address for avc_gain_out: 0x380F 触发频率阀值

Criterion: Subjective test with noisy environment, turn on BVE can obviously hear the speaker out bigger. Continuous NE voice shouldn't boost speakout by BVE.

7.9 Bandwidth Extension (BWE)

带宽扩展

Band Width Extension (BWE) is designed to enhance narrow bandwidth voice signal from [200, 3400]Hz to [120, 7400] Hz on downlink path. This feature is supported only when DSP is on Slave mode. 只在，从机工作时支持

- When CODEC and PCM/I^2S are both 16kHz (host already duplicated PCM/I^2S input data of 8kHz sampling voice signal to 16kHz by repeating each sample). BWE is supported in both digital and analog interface. Set Bit[11] of **Para[0x2305, _ft_flag]** to turn on BWE. 当 。。。16k。。时，支持模拟与数字接口

- When CODEC is on 16kHz, while PCM/I^2S is on 8kHz, DSP will duplicate PCM/I^2S input each sample to form a 16kHz voice data. In this case, BWE is only supported in DAC analog interface. To turn on BWE feature, set Bit[11] of **Para[0x2305, _ft_flag]** and set Bit[4] of **Para[0x2301, _sample_rate**]. 模拟接口

- The index of EQ gains for BWE 4KHz higher component is designated in parameter DM0x2399 and DM0x239A. Their default values are 0xBBCD and 0xEEFF respectively.

7.10 Far Field Pickup (FFP) 远距离拾音

FFP function is combined by Lout-AGC module and Lout-DRC module, so you can turn on this feature by the following switch: 0x2304 bit [15]=1 and 0x2303 bit [12] =1 at the same time.

Lout-AGC module implement adaptive gain control when talk from different fields, such as for far-field talk, we expect increase lout-gain to get standard output; otherwise, for near-field talk, decrease lout-gain to get output as the similar standard level.

Lout-DRC module implement dynamic range control, in this FFP function, we expect to get the following effect: when talk switches between near field and far field, output remains a fixed range.

Table 13: Far Field Pickup parameters

Index	Address	Parameter name	Description
1	0x2304 bit [15]	**Lout-AGC feature switch**	This bit is set to 1, turn on Lout-AGC
2	0x2303 bit [12]	**Lout-DRC feature switch**	This bit is set to 1, turn on Lout-DRC
3	0x2360	**_fdmicagc_minagc**	Minimum gain, -10dB (0x800 is unit gain) Range:0x100~0x800.
4	0x2361	**_fdmicagc_maxagc**	Maximum gain, +10dB (0x800 is unit gain) Range:0x800~0x2000.
5	0x2362	**_fdmicagc_alpha_up**	Smooth factor of power estimation for AGC control when voice on, the smaller then faster. Range:0x1~0x7E00.
6	0x2363	**_fdmicagc_alpha_down**	Smooth factor of power estimation for AGC control when voice off, the smaller then faster. Range: 0x1~0x7E00.
7	0x2364	**_fdmicagc_ref_low**	Lout-AGC level controller. Big values lift up the adjustable lout power range. (Observe DM0x2366 for current Lout-AGC gain, to match your expected output level with unit gain) Range: 0x1~0x400
8	0x380c	**_mic_agc_gain**	Real-time gain applied, 0x800 is unit gain. NOTE: this is variable for observation, not for tuning.

10	0x23D3	**_lout_drc_level**	Level for Lout-DRC module Range: 0x1~0x4000
11	0x23D4	**_lout_drc_slant**	The control speed for Lout-DRC module, the bigger then faster. Range: 0x1000~0x7F00

Performance optimization recommendations:

For Lout-AGC module,

1. First select your control range by your application; such as talk field from 30cm to 5m, the difference of measured power level between 30cm and 5m is about 18dB, then your control range should bigger 18dB. We suggest select 6dB bigger range (in this case: 24dB)
2. Select minimum and maximum boundary by control range. In this sample, you can select (-12dB, +12dB), or (-18dB, +6dB), or (-6dB, +18dB), or others, but we suggest the best sequence for your choice is as follows:(-18dB, +6dB): this is down side, AGC gain is mostly smaller than unit gain, so mic_volume need more gain in this case.(-12dB, +12dB): this is symmetrical(-6dB, +18dB): this is up side
3. Select reference level for Lout-AGC.
   To make sure the runtime gain varies in our control range, we need reference level. In this sample, we can select talk at 3m at reference level which corresponding AGC gain is unit gain. Procedure:
   - Play normal voice or talk at 3m.
   - Observe DM(0x2366) value.
   - Adjust the DM(0x2364) parameter to make sure DM(0x2366) varies about 0x800.

   In this case, the value of 0x2364 is as our reference level.

To speed up Lout-AGC convergence time, can adjust parameters in 0x2362 and 0x2363

For Lout-DRC module,

1. Select expected output level by parameter 0x23D3.
   Output level range is 0x~ 0X7FFF.
   If you expected output range is PSL (about 0x2000), you can set 0x23D3 = PSL/4 (about 0x800) Certainly you can set some smaller to get more remarkable result.
2. Select control speed of DRC by parameter 0x23D4.
   The bigger value means faster convergence. 越大收敛越快

8.0 FM-1288 Parameter Table

Table 14: FM-1288 Parameter Table

Control	Address	Name	Description	Value
	0x22C0	_i2s0_L_tx_p	Reserved	0x0004
	0x22C1	_i2s0_R_tx_p	Reserved	0x0004
	0x22C2	_i2s1_L_tx_p	Reserved	0x0003
	0x22C3	_i2s1_R_tx_p	Reserved	0x0003
LDO	0x22C4	_LDO_ctl_stat	Refer to definition of HW MMR register:0x3FD2	0x0620
CODEC	0x22C5	_mic_addgain_ctl	Refer to definition of HW MMR register:0x3FC0: bit[14,13,8] bit[14:13], select additional gain (10) bit[8], select if apply additional gain (1: means "not apply")	0x4100
Clock	0x22C6	_CODEC_CLK_div	DIV_1: clock divider for CODEC. Range in 0x5 ~ 0x7F	0x000C
Clock	0x22C7	_CODEC_CLK_mul	MUL_0: clock multiplier for CODEC. Range in 0x5 ~ 0xFF or 0 (0 means 256)	0x000C
Clock	0x22C8	_PLL_div_type	MCLK(main clock dource) description: Bit[5]: 1 means MCLK is multiplier of 2.048MHz,0 means else; Bit[4~0]: DIV_0: PLL input divider. Select DIV_0, DIV_1(para 0x22C6), MUL_0(para 0x22C7) to gurantee: MCLK * MUL_0 /(DIV_1 * DIV_0) = 2.048M if Bit[5]=1,then only need to gurantee MCLK/DIV_0=2.048M	0x002C
	0x22C9	_PLL_xtal_clk	Whether PLL is bypassed:0: DSP clock is from PLL,1: PLL bypassed(DSP clock equals to input MCLK)	0x0000
Clock	0x22CA	_chi_CLK_set	Refer to definition of HW MMR register:0x3FF0 bit[15:8]:FCLK, bit[7:0]:BCLK BCLK setting for PCM in 16K system. FORMULA: BCLK = 4.096Mhz/2*(chi_BCLK_set+1) FCLK setting for PCM in 16K system. FORMULA: FCLK = BCLK/(chi_FCLK_set+1) #FORMULA: FCLK=BCLK/(chi_FCLK_set+1)	0x1F03
	0x22CB	_reserved11		0x0000
	0x22CC	_chi_CLK_set_8k	Refer to definition of HW MMR register:0x3FF0 bit[15:8]:FCLK, bit[7:0]:BCLK BCLK setting for PCM in 8K system. FORMULA:BCLK = 4.096Mhz/2*(chi_BCLK_set_8K+1) FCLK setting for PCM in 8K system. FORMULA: FCLK = BCLK/(chi_FCLK_set_8K+1) #FORMULA:	0x1F07

Control	Address	Name	Description	Value
			FCLK=BCLK/(chi_FCLK_set_8K+1)	
	0x22CD	_reserved12		0x0000
	0x22CE	_i2s_CLK_set	Refer to definition of HW MMR register:0x3FF1 bit[15:8]:LRLK, bit[7:0]:BCLK BCLK setting for I2S in16K system. FORMULA: BCLK = 4.096Mhz/2*(i2s_BCLK_set+1) LRCK setting for I2S in 16K system. FORMULA:LRCK = BCLK/2*(_i2s_LRCK_set + 1) #FORMULA: LRCK=BCLK/2*(_i2s_LRCK_set+1)	0x0F03
	0x22CF	_reserved13		0x0000
	0x22D0	_i2s_CLK_set_8k	Refer to definition of HW MMR register:0x3FF1 bit[15:8]:LRLK, bit[7:0]:BCLK BCLK setting for I2S in 8K system. FORMULA:BCLK = 4.096Mhz/2*(_i2s_BCLK_set_8k+1) LRCK setting for I2S in 8K system. FORMULA:LRCK = BCLK/2*(i2s_LRCK_set_8K + 1) #FORMULA: LRCK=BCLK/2*(i2s_LRCK_set_8K+1)	0x0F07
	0x22D1	_reserved14		0x0000
	0x22D2	_i2s_special_Mode	Reserved	0x0294
	0x22D3	_AVC_SNR_thrd	Works when Bit[4] of 0x2305 is ON SNR threshold to trigger BVE, smaller value means harder to trigger BVE	0x0003
	0x22D4	_AVC_vol_thrd	Works when Bit[4] of 0x2305 is ON The threshold to trigger frequency adjustment(decrease low and increase high freuqency). When avc_gain_out >threshold, it will trigger the frequency adjustment. DM address for avc_gain_out: 0x380F	0x2000
	0x22D5	_SCL_Speed	Control speed of eeprom read operation, default: 0x20 Need change before eeprom read(power-on, time relies on MCLK)	0x0040
	0x22D6	_read_eeprom_times	Control fail-retry times of eeprom read operation, (times= 3 - dm(0x22D6)), range:0~3 Need change before eeprom read(power-on, time relies on MCLK)	0x0004
	0x22D7	_reserve_22D7[0]		0x0000
	0x22D8	_reserve_22D7[1]		0x0000
	0x22D9	_reserve_22D7[2]		0x0000
	0x22DA	_reserve_22D7[3]		0x0000
	0x22DB	_reserve_22D7[4]		0x0000
	0x22DC	_reserve_22D7[5]		0x0000
	0x22DD	_reserve_22D7[6]		0x0000
	0x22DE	_reserve_22D7[7]		0x0000

Control	Address	Name	Description	Value
	0x22DF	_reserve_22D7[8]		0x0000
	0x22E0	_gain_state_thrd	Works when Bit[1] of sp_flag is ON Controls how easy a peak is identified as an "isolated peak", smaller value means easier	0x3200
	0x22E1	_gain_adjust1_dB	Works when Bit[1] of sp_flag is ON If an "isolated peak" is identified, that peak is attenuated by this amount if vad01 is ON	0x4400
	0x22E2	_gain_adjust2_dB	Works when Bit[1] of sp_flag is ON If an "isolated peak" is identified, that peak is attenuated by this amount if vad01 is OFF	0x3000
Volume	0x22E3	_vol_inc_step	Volume step size. Default is 0dB, it means if 0x22e3 is increased by 0x1, the spk volume will be decreased by 0dB.	0x7FFF
	0x22E4	_vol_index	This parameter will be set by the host. The number must be 1-9, 1 means max volume, 9 means min volume. Response time <=8ms. #RANGE: 0x1-0x9	0x0001
ADC	0x22E5	_adc_pga_gain	Refer to definition of HW MMR register:0x3FC2 bit[11:8], lin, bit[7:4], mic1, bit[3:0], mic0	0x0222
	0x22E6	_adc_vol_mute	Refer to definition of HW MMR register:0x3FC3 bit[8] control ADC clock bit[7:1] control mute bit[0] control DAC clock	0x0000
DAC	0x22E7	_dac_vol_ctl	Refer to definition of HW MMR register:0x3FC4 bit[15:8] control SPK vol bit[7:0] control LOUT vol	0x0000
	0x22E8	_dac_vol_mute	Refer to definition of HW MMR register:0x3FC5 bit[7:1] control DAC mute	0x0000
	0x22E9	_dac_pga_gain	Refer to definition of HW MMR register:0x3FC6 bit[7:4], lout, bit[3:0], spk	0x0011
GPIO	0x22EA	_gpio_ctl_set	Refer to definition of HW MMR register:0x3FE6	0x000C
	0x22EB	_Bypass123_rate_config	Reserved	0x07D0
Volume	0x22EC	_vol_inc_step_gpio	the volume step for GPIO control vol up/down	0x0040
	0x22ED	_spk_volume_cap_gpio	the volume cap for GPIO control vol up/down	0x1000
MIC	0x22EE	_mic_revert_mode	D0: = 1,swap mic0/mic1. = 0, no swap	0x0000
	0x22EF	_mu_rx_exc	Exclusive logic for Mu-law or A-law at RX end. Bit value: 0: no NOT, 1: NOT	0x0000
	0x22F0	_mu_tx_exc	Exclusive logic for Mu-law or A-law at TX end. Bit value: 0: no NOT, 1: NOT	0x0000
	0x22F1	_pwrdwn_set	Designate pwrdwn-resume or pwrdwn-reset mode.0xC000(pwrdwn-resume mode, Default),0xD000(pwrdwn-reset mode)	0xC000

Control	Address	Name	Description	Value
MIPS setting	0x22F2	_mips_setting	Default 60MIPS: MIPS = 1.024 * (1 + Bit[6~0] of 0x22f2), 0x40 means 65 MIPS. its value should be multiple of 4.	0x003C
	0x22F3	_ANA_mips_set	MIPS setting when SW bypass mode	0x0028
	0x22F4	_PWD_mips_set	MIPS setting after entering into power-down ISR	0x0032
ByPass	0x22F5	_ana_com_mode	Determine which transition will trigger SW bypass mode and select which type of SW bypass. D15:controls which transition to trigger SW bypass mode. = 0, H-L toggling, = 1, L-H toggling. D7-D0: controls which type of SW bypass is selected. =0:PCM-mono bypass mode. mic0->chi0_tx without gain ,chi0_rx->chi1_tx without gain =1:PCM-mono bypass mode. mic1->chi0_tx without gain ,chi0_rx->chi1_tx without gain =2:IIS bypass mode. mic0/mic1->i2s0 without gain, i2s0_L_rx->i2s1_L_tx,i2s0_R_rx->i2s1_R_tx without gain =3: Analog communication mode	0x0000
	0x22F6	_DAC_mode_select	Reserved	0x0002

Control	Address	Name	Description	Value
	0x22F7	_sidetone_gain	Gain for generated side-tone, unit gain: 0x0800. Range: 0 ~ 0x7FFF.	0x0080
Applica-tion Profile setting	0x22F8	_profile_index	If want to do internal profiles selection, then must set parameter 0x22f8 bit [15] = 1 at 1st host parameter configure, default value of this bit is 0.If internal profiles is selected, 0x22f8 bit [14~0] decides which profile. In 31391 chip there are 4 internal modes. 0: default, 1MIC VDA	0x0000
I2S	0x22F9	_digi_control	PCM/I2S control. related to dm(0x3FF2) D0-D3: serial word length for PCM mode, word length = (CHI_SLEN + 1). The word length is fixed at 32 bits: 16 bits for each channel (left or right) for IIS mode. D4: =1,one cycle delay; =0, zero cycle delay. D5: 1: high state of LRCK is for left channel data.0:low state of LRCK is for left channel. D6: 1: rising edge latch RX data in I2S mode.0: falling edge latch RX data in I2S mode D7: 1: LRCK is generated internally.0: LRCK is generated externally. D8: 1, FRAME is generated internally. 0,FRAME is generated externally. D9: TXDC_TRI. =1: pin TXDC is tri-stated,=0: pin TXDC is driven. D10: TXDP_TRI. =1: pin TXDP is tri-stated,=0: pin TXDP is driven. D11:I2S_left_int. 1,I2S interrupt is triggered when entire word of left channel is received. 0,I2S interrupt is triggered when entire word of right channel is received. D12: Reserved D13: 1,BCLK is generated internally in I2S. 0,BCLK is generated externally in I2S. D14: 1,BCLK is generated internally in PCM. 0, BCLK is generated externally in PCM. D15: 1,rising edge latch data in PCM. 0, falling edge latch data in PCM. For the above 4 bits, 1: internal, 0: external.	0x007F
Hard-ware Device Enable	0x22FA	_dv_enable_b	Device enable. D0: MIC0 D1: MIC1 D2: MICBIAS D3: Analog spk out D4: Analog Line in D5: Analog Line out D8: CHI/I2S select, =1, PCM enable D11: DPLL track enable/disable, =1, track enable; =0, track disable D15: Reserved (TX1/RX1 selection, =1:Pin4/5 are TX1/RX1 of PCM/I2S; =0:Pin4/5 is GPIO[10,9])	0x003F
	0x22FB	_dv_parser_sync_flag	0x8000 (0x8000: before parameter configure, 0x0 means finish configure, 0xA5A5 means DSP running)	0xA5A5
	0x22FC	reserve_22FC	Reserved	0x0000
	0x22FD	_dv_fmmask	Interrupt mask.0x04: chi_i2s interrupt,	0x0034

Control	Address	Name	Description	Value
			0x10: SW bypass interrupt, 0x20: codec interrupt	
VAD	0x22FE	_vad_led_flag	GPIO control VAD OUT, refer to the definition of 0x232C	0x0040
	0x2300	_line_pass	=0: normal mode; =1:PCM-mono bypass mode. mic0->chi0_tx without gain,chi0_rx ->spk without gain. =2:PCM-mono bypass mode. mic1->chi0_tx without gain,chi0_rx -> spk without gain. =3:IIS bypass mode. MIC0/1 to I2S L/R Trans channel without gain, I2S L or R Recv data to SPK out without gain. =0x10: MIC0 -> SPK, and LIN->Lout (PCM) without gain.	0x0000

Control	Address	Name	Description	Value
SAMPLE RATE	0x2301	_sample_rate	Overall sampling rate. Bit [0:3] : =2: 16K normal mode, both CODEC and PCM/I2S are 16K. =0x12: CODEC 16K and PCM/I2S 8K mode	0x0012
MIC	0x2302	_num_of_mics	Bits[1:0]: number of microphones. Bit[4]: uni_omni Bit[8]: PSEUDO-2mic	0x0012
	0x2303	_kl_config	Flags for doing frame processing D0: use frame processing D1: pass NND to 0x23f8 (for tuning only) D2: pass UND to 0x23f8 (for tuning only) D3: use Fq domain ref_ch EQ D4: dynamic range control (DRC) D5: speaker attenuation D6: Reserved D7: adjust noise suppression with SNR D8: idle noise suppression D9: pass out original comfort noise (for tuning only) D10: Reserved D11: noise residue stabilizer (mainly on semi-stationary noise) D12: Lout DRC D13: Reserved D14: line in NS D15: bypass frequency domain process	0x5991
	0x2304	_sp_flag	D0: adjustable Mic in HPF, default is 180HzHPF D1: isolated noise peak reduce D2: mic pre-emphasis filter, D3: mic de-emphasis filter, D4: mic 120hz HPF filter, D5: reserved D6: LINEIN_EMPHFILTER D7: LINEIN_DEEMPHFILTER D8: linear AEC, D9: non-linear AEC, post-filter, D10: Reserved D11: line-in AGC, D12: Reserved D13: reserved D14: FENS_FFTONLY D15: MICIN_AGC	0x03CF
	0x2305	_ft_flag	D0: noise paste back, D1: Reserved D2: Reserved D3: Reserved D4: BVE	0x0031

Control	Address	Name	Description	Value
			D5: beamforming2 D6: Reserved D7: PCM/IIS_B13_PCM_SIGN_EX D8: PCM bus 13-bit LPCM zero padding D9: PCM bus 8-bit PCM A-law D10: PCM bus 8-bit PCM Mu-law D11: BAND_WIDTH_EXTENSION D12: Reserved D13: SIDETONE_GENERATE D14: Reserved D15: Reserved	
	0x2306	_frame_counter	Debug indicator. It shows how many frame has passed	0x3E15
MIC	0x2307	_mic_vol_ctl	D15~8,MIC1 volume setting. D7~0,MIC0 volume setting. It is MIC volume control after digital filter (digital gain) for all microphones. 0xE0, 0xF0, 0xFC, 0x0, 0x10, 0x14. //+24dB, +12dB, +3dB, 0dB, -12dB, -15dB. Range:-143.25db ~24db; Volume setting [7:4]: 0x0 (0 dB) 0x4 (-48 dB) 0x8 (-96 dB) 0xc (Not allowed) 0x1 (-12 dB) 0x5 (-60 dB) 0x9 (-108 dB) 0xd (Not allowed) 0x2 (-24 dB) 0x6 (-72 dB) 0xa (-120 dB) 0xe (+24 dB) 0x3 (-36 dB) 0x7 (-84 dB) 0xb (-132 dB) 0xf (+12 dB) Volume setting [3:0]: 0x0 (0 dB) 0x4 (-3.00 dB) 0x8 (-6.00 dB) 0xc (-9.00 dB) 0x1 (-0.75 dB) 0x5 (-3.75 dB) 0x9 (-6.75 dB) 0xd (-9.75 dB) 0x2 (-1.50 dB) 0x6 (-4.50 dB) 0xa (-7.50 dB) 0xe (-10.50 dB) 0x3 (-2.25 dB) 0x7 (-5.25 dB) 0xb (-8.25 dB) 0xf (-11.25 dB) Real volume = Volume for [7:4] + Volume for [3:0]	0x0000
	0x2308	_mic_diff_gain	Reserved	0x0CB0
	0x2309	_lin_vol_ctl	Line-in digital gain. same as mic_vol_ctl	0x0000
DAC	0x230A	_DAC_pgagain	Reserved	0x1A00
	0x230B	_DAC_ctrl	Reserved	0x001E
MIC	0x230C	_mic_volume	Microphone volume.0x0: minimum,0x7fff: maximum, 0x100: maintain the same volume as input.	0x0300
SPK	0x230D	_spk_volume	Speaker volume.0x0: minimum,0x7fff: maximum, 0x100: maintain the same volume as input	0x0180
	0x230E	_spk_mute	Speaker mute.0: mute, 0xffff: no mute.	0xFFFF
MIC	0x230F	_mic_mute	Microphone mute.0: mute, 0xffff: no mute.	0xFFFF
	0x2310	_linein_HPF_sel	D0: line in 360Hz HPF D1: Reserved	0x1205

Control	Address	Name	Description	Value
			D2: 270Hz LPF for LF_vad D3: 250Hz LPF for LF_vad D4: Reserved D5: Reserved D6: line in 300Hz HPF D7: line in 120Hz HPF D8: adjustable line in HPF D9: USE_IIS0/Chi0_L_AS_LINEIN D10: USE_IIS0/Chi0_R_AS_LINEIN D11: USE_IIS0/Chi0_LR_AS_LINEIN	
	0x2311	_Adj_micHPF_coef[0]	HPF coefficient for mic, mic signal can be 8k/16k sample rate, default is 180Hz,16k	0x3825
	0x2312	_Adj_micHPF_coef[1]		0xC7DD
	0x2313	_Adj_micHPF_coef[2]		0x3825
	0x2314	_Adj_micHPF_coef[3]		0x89E5
	0x2315	_Adj_micHPF_coef[4]		0x6DBE
	0x2316	_Adj_micHPF_coef[5]		0x7FFF
	0x2317	_Adj_micHPF_coef[6]		0x8020
HPF	0x2318	_Adj_micHPF_coef[7]		0x7FFF
	0x2319	_Adj_micHPF_coef[8]		0x8194
	0x231A	_Adj_micHPF_coef[9]		0x7D88
	0x231B	_Adj_linHPF_coef[0]	HPF coefficient for Lin, Lin signal can be 8k/16k sample rate, default is 180Hz,16k	0x5558
	0x231C	_Adj_linHPF_coef[1]		0xAAAA
	0x231D	_Adj_linHPF_coef[2]		0x5558
	0x231E	_Adj_linHPF_coef[3]		0x8A31
	0x231F	_Adj_linHPF_coef[4]		0x6CEF
	0x2320	_Adj_linHPF_coef[5]		0x5558
	0x2321	_Adj_linHPF_coef[6]		0xAAAF
	0x2322	_Adj_linHPF_coef[7]		0x5558
	0x2323	_Adj_linHPF_coef[8]		0x8200
	0x2324	_Adj_linHPF_coef[9]		0x7C9D
SPK	0x2325	_spk_db_drop	The maximum speaker volume attenuation at double talk, (0x7FFF is unit gain)	0x5300
	0x2326	_spk_db_decay	SPK attenuation recovery speed when double talk is over	0x0034
VAD	0x2327	_vad3p_alpha	Decay factor when VAD3 =1 at SPK attenuation feature, 0x7FFF is slowest	0x7EE0
MIC	0x2328	_mic_sat_th	Criterion for setting half duplex mode at main microphone	0x7E00
SPK	0x2329	_spk_db_extension		0x000A
AEC	0x232A	_sat_hd_time	The duration for holding in half-duplex mode if half-duplex is triggered. Unit: 1/16000 second.	0x1000
	0x232B	_chii2s_clock_on	Reserved.	0x0000
VAD	0x232C	_vad_info_bitset	Bit collection of all kinds VAD info. Bit definition:	0x0000

Control	Address	Name	Description	Value
			VAD1_LED 0x0001(Reserved) VAD2_LED 0x0002(Reserved) TD_LF_VAD_LED 0x0004 VAD0_LED 0x0008(Reserved) FEVAD_LED 0x0010 FEVAD_BIG_LED 0x0020 NE_VAD 0x0040 MMIC_SAT 0x0100 RMIC_SAT 0x0200 FEVAD_LI_LED 0x0800	
	0x232D	_reserve_232D[0]		0x0000
	0x232E	_reserve_232D[1]		0x0000
AEC	0x232F	_aec_ref_gain	Gain for AEC ref channel. Unit-gain: 0x100	0x0080
	0x2330	_minmu	Lower limit of AEC MU	0x0300
	0x2331	_maxmu	Upper limit of AEC MU	0x3FFF
	0x2332	_tdaec_fe_vad_th_high	Threshold for fe_vad_big decision. Higher values can increase vad0 decision and decrease frequency domain echo suppression, the effect is less echo suppression and tilts it towards full duplex. Range: 0~0x7FFF	0x0030
	0x2333	_tdaec_fe_vad_th	Threshold for fe_vad decision. Lower values can cause more active echo cancellation. Range: 0~0x7FFF	0x0008
	0x2334	_aec_wrong_vad_spread_fac	The upper threshold of AEC stability control	0x0860
	0x2335	_tdaec_ws_thold	The lower threshold of AEC stability control	0x0580
	0x2336	_tdaec_minmu_nofe	When no FE voice, this minimum mu value is used	0x0008
	0x2337	_tdaec_nw_shift	Control convergent speed and convergent stability. Bigger value will make convergence faster and more unstable. Range:0xFFF0~0	0x0000 0xffff
	0x2338	_tdaec_fe_vad_shift	Control convergent speed when FE VAD	0x0003
	0x2339	_tdaec_delay_length	Additional buffer to account for the Codec delay of the AEC path. Maximum: 0x68, minimum:0 #RANGE: 0x0-0x68	0x0010
	0x233A	_pitch_ex_floor_fac		0x1800
	0x233B	_pitch_ex_hipeak_fac		0x7A1B
	0x233C	_pitch_ex_lowpeak_fac		0x55DD
	0x233D	_reserve_233D[0]		0x0000
	0x233E	_reserve_233D[1]		0x0000
	0x233F	_reserve_233D[2]		0x0000
	0x2340	_reserve_233D[3]		0x0000
	0x2341	_reserve_233D[4]		0x0000
	0x2342	_reserve_233D[5]		0x0000
	0x2343	_reserve_233D[6]		0x0000
	0x2344	_reserve_233D[7]		0x0000
	0x2345	_reserve_233D[8]		0x0000

Control	Address	Name	Description	Value
	0x2346	_reserve_233D[9]		0x0000
MIC	0x2347	_tdsp_micgain1_high	Level boost on reference channels before pushing into BF process. 0x0800: times 1;Range:0~0x7fff	0x1800
	0x2348	_tdsp_micgain0	Level boost on main channels before pushing into BF process. 0x0800: times 1; Range:0~0x7fff	0x1800
	0x2349	_tdsp_micgain1	Level boost on reference channels before pushing into BF process. 0x0800: times 1;Range:0~0x7fff	0x0C00
	0x234A	_tdsp_emph_mmic1	Emphasis filter coefficient for MIC0 path.	0x3000
	0x234B	_tdsp_emph_mmic2	Emphasis filter coefficient for MIC0 path.	0xF1EC
	0x234C	_tdsp_emph_const1	Emphasis filter coefficient for MIC1 path.	0x3000
	0x234D	_tdsp_emph_const2	Emphasis filter coefficient for MIC1 path.	0xF1EC
	0x234E	_tdsp_emph_back_const 1	Emphasis filter coefficients for Line In/ SPK out path.	0x3000
	0x234F	_tdsp_emph_back_const 2	Emphasis filter coefficients for Line In/ SPK out path.	0xF1EC
	0x2350	_reserve_2350[0]		0x0000
	0x2351	_reserve_2350[1]		0x0000
	0x2352	_reserve_2350[2]		0x0000
	0x2353	_reserve_2350[3]		0x0000
	0x2354	_reserve_2350[4]		0x0000
	0x2355	_reserve_2350[5]		0x0000
	0x2356	_reserve_2350[6]		0x0000
	0x2357	_DAC_out_gain		0x0100
	0x2358	_reserve_2358[0]		0x0000
	0x2359	_reserve_2358[1]		0x0000
	0x235A	_reserve_2358[2]		0x0000
	0x235B	_reserve_2358[3]		0x0000
	0x235C	_reserve_2358[4]		0x0000
	0x235D	_reserve_2358[5]		0x0000
	0x235E	_reserve_2358[6]		0x0000
	0x235F	_beam2_shift	Controls the step size for BF2. bigger value gives out higher convergence speed but may cause instability.	0x0020
MIC	0x2360	_fdmicagc_minagc	Minimum gain, -10dB (0x800 is unit gain)	0x0288
	0x2361	_fdmicagc_maxagc	Maximum gain, +10dB (0x800 is unit gain)	0x194C
	0x2362	_fdmicagc_alpha_up	Smooth factor of power estimation for AGC control	0x7333 平滑因子
	0x2363	_fdmicagc_alpha_down	Smooth factor of power estimation for AGC control	0x5999
	0x2364	_fdmicagc_ref_low	MIC-in AGC level controller. Big values lift up the adjustable MIC-in power range. DM address for mic_agc_gain:0x380C	0x0090
	0x2365	_mic0_sw_I2Sgain	Gain applied to mic0 when mic signals come from PCM/I2S(0x800: unity).	0x0800

Control	Address	Name	Description	Value
	0x2366	reserve_2366[0]		0x0000
	0x2367	reserve_2366[1]		0x0000
AGC	0x2368	_tdagc_aalpha	Smooth factor of power estimation for line-in AGC control	0x7E41
	0x2369	_tdagc_inv_pgain	No use	0x5CCD
	0x236A	_tdagc_ref	Line-in AGC level controller. Higher values lift up the adjustable line-in levels. (Check DM 0x380E for current line-in AGC gain, 0x800: unity) DM address for linein_agc_gain:0x380E	0x003E
	0x236B	_tdagc_minagc	Lowest allowed AGC gain, -8dB	0x032F
	0x236C	_tdagc_maxagc	Highest allowed AGC gain, +8dB	0x1418
	0x236D	_reserve_236D		0x0000
Noise Suppression	0x236E	_ss_bounds_high[0]	_ss_bounds_high[0]: Noise suppression level, 0x7fff is unitgain ,means 0db noise suprression , smaller value makes heavier noise suppression and less voice pass.Range: 0~0x7FFF _ss_bounds_high[1]: base gain factor for noise suppression, will be self-doubled if vad01 <= 0. bigger value makes heavier suppression and less voice pass. Range: 0~0x7FFF Bit[15~8]: base gain factor for f < 2350Hz component; Bit[7~0]: base gain factor for f >= 2350Hz component after left banked; Default value is 0x0B05, this means 0x0B00 as gain factor for f < 2350Hz, and 0x1000 = (0xB00 + 0x500) as gain factor for f >= 2350Hz. _ss_bounds_high[2]: extra gain factor for noise suppression when no big echo, will be applied if voice probability very low, bigger value can reduce watering sound. Range: 0~0x7FFF	0x1449
	0x236F	_ss_bounds_high[1]		0x0B05
	0x2370	_ss_bounds_high[2]		0x0C00
	0x2371	_reserve_2371		0x0000
	0x2372	_tdsp_noisegain	Noise paste-back factor.	0x6000
	0x2373	_fqpara_gndL_div	Noise tracking factor to adapt to not so stable stationary noise. Larger value when outside noise goes up and down frequently. (180~440Hz) Range: 0~0x7FFF	0x1200
	0x2374	_fqpara_gndM_div	440~2300Hz, Noise tracking factor.Range: 0~0x7FFF	0x1A00
	0x2375	_fqpara_gndH_div	2300~7500Hz, Noise tracking factor.Range: 0~0x7FFF	0x0B80

Control	Address	Name	Description	Value
	0x2376	_fqpara_min_recursive		0x0F00
	0x2377	_reserve_2377[0]		0x0000
	0x2378	_reserve_2377[1]		0x0040
	0x2379	_reserve_2377[2]		0x0000
	0x237A	_reserve_2377[3]		0x0000
	0x237B	_fqpara_period	Noise estimation period, can be set to any value. Current value enables estimation to converge in about 1 sec	0x0011
	0x237C	_fqpara_beta1	UND = Max(Beta1*Nd, Beta2*NND). (Beta1: 0x237c, Beta2: 0x237d~0x237f when no echo, 0x2380~0x2381 when echo). Beta1 is always used for stationary noise, Beta2 is used for non-stationary noise. Range: 0~0x7FFF	0x7800
	0x237D	_fqpara_beta_v2	Beta2 for NE voice only. Range: 0~0x7FFF	0x0500
	0x237E	_reserve_237E[0]		0x0000
	0x237F	_reserve_237E[1]		0x0000
	0x2380	_fqpara_beta_uv_fe	Beta2 for FE only.Range: 0~0x7FFF	0x0A00
	0x2381	_fqpara_beta_mixed_fe	Beta2 for Double-Talk.Range: 0~0x7FFF	0x0700
	0x2382	_fqpara_vad_thrd_low	Threshold for Low_vad from 187.5Hz~1000Hz. Range: 0~0x7FFF	0x0340
	0x2383	_fqpara_vad_thrd_high	Threshold for High_vad from 672Hz~6800Hz. Range: 0~0x7FFF	0x03C0
	0x2384	_fqpara_snr_order	Threshold for speech SNR, higher value will suppress more noise and keep less voice. Range: 0~0x9	0x0004
	0x2385	_reserve_2385[0]		0x0000
	0x2386	_reserve_2385[1]		0x3C00
	0x2387	_reserve_2385[2]		0x0040
	0x2388	_reserve_2385[3]		0x38CA
	0x2389	_reserve_2385[4]		0x0010
	0x238A	_reserve_2385[5]		0x0144
	0x238B	_reserve_2385[6]		0x0500
	0x238C	_reserve_2385[7]		0x4000
	0x238D	_fqpara_shape_start	The start point of NS shape function	0x0005
	0x238E	_fqpara_shape_slant	The slant of ns shape	0x3800
	0x238F	_fqpara_ns_shex		0x0300
	0x2390	_fqpara_equal[0]	Bit definition identical to FENS_equal[]. Refer to DM23DF~23E4.	0x4444
	0x2391	_fqpara_equal[1]		0x4444
	0x2392	_fqpara_equal[2]		0x4444
	0x2393	_fqpara_equal[3]		0x4444
	0x2394	_fqpara_equal[4]		0x4444

Control	Address	Name	Description	Value
	0x2395	_fqpara_equal[5]		0x4444
	0x2396	_echo_Domin_vad_thrd	Reserved.	0x7000
	0x2397	_echo_Domin_equal_vad_thrd	Reserved.	0x6000
	0x2398	_echo_domin_vad_grd	Reserved.	0x0080
BWE	0x2399	_BWE_FENS_equal_4Khigher[0]	the equalizer on 4K higher band in Receiving direction for BWE. Refer to the definition of "FENS_equal[4~5]"(DM23E3 ~ DM23E4).	0xBBCD
	0x239A	_BWE_FENS_equal_4Khigher[1]		0xEEFF
	0x239B	_reserve_239B		0x6000
	0x239C	_fqpara_inbeam_dec	Reduces NS when SNR is very high. larger value improves voice quality in quiet environment, but also raises noise floor. therefore, it needs to be tuned together with idle noise suppression. The range is 0~0x7FFF	0x4000
	0x239D	_reserve_239D[0]		0x1000
	0x239E	_reserve_239D[1]		0x1000
	0x239F	_reserve_239D[2]		0x1FFF
	0x23A0	_reserve_239D[3]		0x0001
	0x23A1	_alpha_snr_nofe		0x7E00
	0x23A2	_alpha_snr_fe		0x7C00
	0x23A3	_post_stab_min		0x331F
	0x23A4	_tdpf_noise_DT_min_attn	Reserved	0x3400
	0x23A5	_tdpf_start_bin	pf gain under the case of echo does NOT dominate meanwhile DT detected.	0x0009 0x0000
	0x23A6	_reserve_23A6[0]		0x0000
	0x23A7	_reserve_23A6[1]		0x0000
	0x23A8	_deemph_ln[0]	De-emphasis filter coefficients used in frequency domain processing. Have to be set by SAMTuner, no hand tuning allowed.	0x5A44
	0x23A9	_deemph_ln[1]		0x3598
	0x23AA	_deemph_ln[2]		0x2606
	0x23AB	_deemph_ln[3]		0x1DCE
	0x23AC	_deemph_ln[4]		0x171B
	0x23AD	_deemph_ln[5]		0x11F8
	0x23AE	_deemph_ln[6]		0x0F9F
	0x23AF	_deemph_ln[7]		0x0ED3
	0x23B0	_deemph_ln[8]		0x0000
	0x23B1	_deemph_ln[9]		0x0000

Control	Address	Name	Description	Value
	0x23B2	_fqpara_pow_SS_init	Initial value for pow_SS,bigger for handset mode, smaller for hands-free mode	0x0140
	0x23B3	_tdpf_pf_z_factor_exp_high	Strength of AEC post-filter at no double talk. Higher values gives stronger echo suppression, but less full duplex Range: 0~0x20	0x0003 0x0002
	0x23B4	_tdpf_pf_z_factor_exp_low	Strength of AEC at double talk. Higher values give stronger echo suppression, but less full duplex Range: 0~0x20	0x0001
	0x23B5	_tdpf_pf_coef_gain	pf gain under the case of echo does NOT dominate meanwhile DT detected.	0x6000
	0x23B6	_tdpf_extra_gain	It is used to suppress more at noise environment, bigger value means more suppression	0x0009
	0x23B7	_pf_wait	Estimated length for echo tail coverage (frames)each frame means 16ms Range: 0~0x32	0x0003
	0x23B8	_tdpf_min_attn_NE	pf gain under the case of DT detected meanwhile small echo.	0x7800
	0x23B9	_tdpf_min_attn_no_NE	pf gain under the case of small echo only(no DT).	0x4800
	0x23BA	_tdpf_max_attn_no_DT	pf gain under the case of Big echo only(no DT). PF gives the heaviest suppression !	0x1000
	0x23BB	_tdpf_min_attn_echo_domin		0x1800
	0x23BC	_tdpf_pf_z_factor_exp_extreme	Strength of AEC post-filter when: no DT (td_lf_vad<=0, aec_wrong_vad_cntr>0) Higher values gives stronger echo suppression, but less full duplex	0x0009
	0x23BD	_tdpf_flatness_thrd	Reserved.	0x0F00
	0x23BE	_lfvad_noise_thrd	The threshold for DT detection noise floor. Larger value increases the threshold. If td_lf_vad setting experiences false alarms under Echo + noise case, try decreasing to make td_lf_vad detection.	0x0200 0x00E0
	0x23BF	_lfvad_addon_thrd	Another threshold for DT detection. Larger value increases the threshold. Adjust this in conjunction with lfvad_noise_thrd.	0x0140 0x0054
	0x23C0	_reserve_23BE[0]		0x0000
	0x23C1	_reserve_23BE[1]		0x0000
	0x23C2	_reserve_23BE[2]		0x0000
	0x23C3	_reserve_23BE[3]		0x0000
	0x23C4	_reserve_23BE[4]		0x0000
	0x23C5	_reserve_23BE[5]		0x0000
	0x23C6	_reserve_23BE[6]		0x0000
	0x23C7	_reserve_23BE[7]		0x0000
	0x23C8	_reserve_23BE[8]		0x0000
	0x23C9	_reserve_23BE[9]		0x0000
	0x23CA	_reserve_23BE[10]		0x0000
	0x23CB	_reserve_23BE[11]		0x0000

Control	Address	Name	Description	Value
	0x23CC	_reserve_23BE[12]		0x0000
	0x23CD	_reserve_23BE[13]		0x0000
	0x23CE	_DAC_output_select	Reserved	0x8000
	0x23CF	_vad0_rat_thrd_fe	Vad0 detection threshold when fe_vad_big is ON. Higher values make it HARDER to detect vad0. Range: 0~0x7FFF	0x0780 0x0400
	0x23D0	_vad0_rat_thrd_nofe	Vad0 detection threshold when fe_vad_big is OFF. Higher values make it harder to detect vad0. Range: 0~0x7FFF	0x0680 0x0300
	0x23D1	_vad02_thrd		0x0700 0x0200
	0x23D2	_vad03_thrd		0x0500 0x0100
	0x23D3	_lout_drc_level	Range:0~0x7fff	0x1340 0x1400
	0x23D4	_lout_drc_slant	Range:0~0x7fff	0x26E0
	0x23D5	_vad3_rat_thrd	Reserved.	0x6800 0x6000
	0x23D6	_reserve_23D6[0]		0x7F00
	0x23D7	_reserve_23D6[1]		0x0080
	0x23D8	_reserve_23D6[2]		0x1ED2
	0x23D9	_reserve_23D6[3]		0xF472
	0x23DA	_FENS_var_factor	FENS Noise suppression factor.	0x7800
	0x23DB	_FENS_min_gain	The smallest suppression level for FENS . Bigger value will suppress less noise. Range:0~0x7fff. Unity gain = 0x7fff.	0x1200
	0x23DC	_FENS_VAD_thrd	Threshold for FENS vad, bigger value will make less voice pass and more noise suppression; Range:0~0x7fff	0x0320
	0x23DD	_FENS_vad_cnt_thrd	Threshold for FENS noise vad counter, when counter bigger than threshold, judge as noise. Larger value retains more noise. voice.Range:0~0x20	0x0004
	0x23DE	_depop_time_chii2s_clockswitch	Reserved.	0x0800

Control	Address	Name	Description	Value
	0x23DF	_FENS_equal[0]	23-band SPK-out EQ. 0x4444 means 0dB gain on all bands. FENS_equal[0] defines the gain on band1~band4: Bit[15~12] (109.375Hz ~ 171.875Hz), Bit[11~8] (171.875Hz ~ 234.375Hz), Bit[7~4] (234.375Hz ~ 296.875Hz), Bit[3~0] (296.875Hz ~ 421.875Hz); FENS_equal[1] defines the gain on band5~band8: Bit[15~12] (421.875Hz ~ 546.875Hz), Bit[11~8] (546.875Hz ~ 671.875Hz), Bit[7~4] (671.875Hz ~ 859.375Hz), Bit[3~0](859.375Hz ~ 1046.875Hz); FENS_equal[2] defines the gain on band9~band12: Bit[15~12] (1046.875Hz ~ 1234.375Hz), Bit[11~8] (1234.375Hz ~ 1546.875Hz), Bit[7~4] (1546.875Hz ~ 1859.375Hz), Bit[3~0] (1859.375Hz ~ 2171.875Hz); FENS_equal[3] defines the gain on band13~band16: Bit[15~12] (2171.875Hz ~ 2484.375Hz), Bit[11~8](2484.375Hz ~ 2984.375Hz), Bit[7~4] (2984.375Hz ~ 3484.375Hz), Bit[3~0] (3484.375Hz ~ 3984.375Hz); FENS_equal[4] defines the gain on band17~band20: Bit[15~12] (3984.375Hz ~ 4484.375Hz), Bit[11~8] (4484.375Hz ~ 4984.375Hz), Bit[7~4] (4484.375Hz ~ 5484.375Hz), Bit[3~0] (5484.375Hz ~ 5984.375Hz); FENS_equal[5] defines the gain on band21~band23: Bit[15~12] (5984.375Hz ~ 6484.375Hz), Bit[11~8] (6484.375Hz ~ 6984.375Hz), Bit[7~4] (6984.375Hz ~ 7984.375Hz). the gain on each band represented by Gain index(4 bit index): 0: +6dB, 1: +4dB, 2: +2dB, 3: +1dB, 4: 0dB, 5: -1dB, 6: -2dB, 7: -4dB, 8: -6dB, 9: -8dB, A: -10dB, B: -13dB, C: -16dB, D: -20dB, E: -30dB, F: -50dB.	0x4444
	0x23E0	_FENS_equal[1]		0x4444
	0x23E1	_FENS_equal[2]		0x4444
	0x23E2	_FENS_equal[3]		0x4444
	0x23E3	_FENS_equal[4]		0x4444
	0x23E4	_FENS_equal[5]		0x4444
	0x23E5	_drc_alpha_up		0x1000
	0x23E6	_drc_alpha_down		0x7FB0
	0x23E7	_drc_th1	The small-level threshold of DRC	0x1000
	0x23E8	_drc_th2	The big-level threshold of DRC	0x1600
	0x23E9	_drc_slop1	The slant for lower level	0x2E00
	0x23EA	_drc_slop2	The slant for upper level	0x7200
	0x23EB	_drc_quiet_th		0x0000
	0x23EC	_drc_decay_th		0x0000
	0x23ED	_idle_noise_thrd	idle noise suppression will be applied if noise level lower than this threshold. Bigger value will make idle noise cut more active. Range: 0~0x7FFF	0x0A00

Control	Address	Name	Description	Value
	0x23EE	_idle_ins_attn	The suppressing level for idle noise, 0x7fff is unit gain. Range: 0~0x7FFF	0x32F5 0x2000
	0x23EF	_ins_alpha_up	The adaptive factor for idle noise suppression when the input is big, larger value will make the adaption more slower	0x3000
	0x23F0	_ins_alpha_down	The adaptive factor for idle noise suppression when the input is small, larger value will make the adaption more slower	0x7200
	0x23F1	_signal_pass[0]	This is a very important debug flag that can be used for tuning. Putting one of the following values can pass the following signal to line-out: 0xXXXX: Lineout = DM(Probe)*mic_volume 0x0000: normal output Lineout	0x0003
	0x23F2	_signal_pass[1]		0x0000
	0x23F3	_signal_pass[2]		0x0000
	0x23F4	_signal_pass[3]		0x0000
	0x23F5	_signal_pass[4]		0x0000
	0x23F6	_signal_pass[5]		0x0000
	0x23F7	_signal_pass[6]		0x0000
	0x23F8	_signal_pass[7]		0x0000
	0x23F9	_signal_pass[8]		0x0000
	0x23FA	_signal_pass[9]		0x0000
	0x23FB	_signal_pass[10]		0x0000

References

I. Terminology

Table 15: Terminology

Term	Definition
ADC	Analog to Digital
AEC	Acoustic Echo Cancellation 回声消除
BF	Beam-forming
BVE	Bright Voice Enhancement
Codec	Coder-decoder
DAC	Digital to Analog
DM	Data Memory
DSP	Digital Signal Processor
ECHO	Sound signal coupled from loudspeaker to mic via acoustic path
FENS	Far End Noise Noise Suppression
EEPROM	Electrically Erasable Programmable Read-Only Memory
HPF	High Pass Filter 高通滤波器
HFCK	Hands Free Car Kit
IC	Integrated Circuit
IIC	Inter-Integrated Circuit
IIS	Inter-Integrated Circuit Sound
I/O	Input/Output
LQFP	Low Profile Quad Flat Pad
MCU	Micro Controller Unit
MIC	Microphone
MIPS	Million instruction per second
NS	Noise Suppression
NC	Not Connected
PCM	Pulse Code Modulation 脉冲调制
PGA	Programmable Gain Amplification 增益放大
PM	Program Memory
PND	Portable Navigation Device
RAM	Random Access Memory
ROM	Read Only Memory
SHI	Serial Host Interface
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/ Transmitter
VAD	Voice Activity Detection 语音活动检测
Vpp	Voltage, Peak-to-Peak
XTAL	Crystal

II. Related Documents

Table 16: Related Documents

Fortemedia Technology Documents	Document Location
FM1288 Data Sheet	Contact Fortemedia Sales