FNU Pratibha

691 Idlewild Circle, Birmingham, AL 35205 | (321)-389-7174 | https://fnupratibha.github.io/ | pratibha2023@my.fit.edu | LinkedIn

EDUCATION

Florida Institute of Technology, *Melbourne, FL* Jan 2023 - Dec 2024

Master of Science in Computer Engineering (Concentration: FPGA Design and Hardware acceleration): GPA: 3.62/04

- Coursework: Coursework covering fundamentals of computer networks, Embedded Systems, Computer Architecture, Digital Signal Processing, FPGA, digital communication, Modern Data Systems, Quantum Computing, high-performance computing

Dayananda Sagar College of Engineering, *Bangalore, IN* Sep 2018 – Aug 2021

Bachelor of Engineering in Electronics and Communication Engineering, GPA: 3.2/04

- **Coursework**: Analog and Digital Communication, Operating Systems Fundamentals, RTOS, IoT, VLSI
- **Research Project**: COVID-19 Social Distance Monitoring and Contact Tracing- Developed an advanced health monitoring wristband with real-time alerts and social distancing features alongside three team members.

SKILLS & CERTIFICATIONS

- **RTL & FPGA Design**: Advanced RTL (SystemVerilog, VHDL, Verilog), FPGA Implementation, SoC Architecture, High-Level Synthesis, IP Integration, Memory Interface Design (PCIe Gen4, AXI4, DDR4/HBM), Bus Protocols, Timing Closure, Place & Route Design Synthesis
- **Verification & Debug**: UVM, Assertion-Based & Formal Verification, Clock Domain Crossing/Reset Domain Crossing (CDC/RDC) Analysis, Power & Signal Analysis, Protocol Analysis, Hardware Debug (ILA), Functional Coverage, Testbench Development, STA
- **Programming & Scripting**: Python/TCL for HLS & ML/FPGA, C/C++ (Linux/Windows), Build Systems (Make, CMake), Version Control (Git), MATLAB, Perl, Bash, Shell Scripting Hardware-Software Co-Design
- **Tools Expertise**: Vivado, Vitis HLS, ModelSim/QuestaSim, VCS, Synopsys Design Compiler, Cadence Genus, Intel Quartus Prime
- **Optimization & Analysis**: Pipeline Design, Memory Optimization, Resource Utilization, PPA Trade-offs, Latency Reduction, Clock Tree Analysis

EXPERIENCE

Florida Institute of Technology, Melbourne, FL Feb 2025 – Present

Research Associate (Volunteer)

- Developed and implemented FPGA-based architectures for high-performance computing, improving system efficiency by 30% and accelerating computation speed for real-time processing
- Optimized FPGA algorithms, reducing execution time by 40%, contributing to advancements in embedded systems and hardware acceleration
- Authored 3+ technical reports and contributed to research publications, documenting experimental results for researchers, technical reports, and industry presentations

Florida Institute of Technology, Melbourne, FL Jan 2024 – Dec 2024

Graduate Teaching Assistant

- Facilitated hands-on laboratory sessions for 100+ students in microprocessor architecture, demonstrating assembly programming concepts for 8085/8086 and 8051 platforms, resulting in 90% average practical assessment scores
- Mentored students through 15+ signal processing experiments, integrating MATLAB for DSP applications while coaching hands-on microcontroller programming using sensors, accelerometers, and Raspberry Pi 4, fostering practical engineering skills
- Planned and provided comprehensive lab documentation for peripheral interfacing (8259 PIC/8255 PPI), instructing students in interrupt handling and I/O operations, leading to improved student comprehension of hardware-software interaction

DXC Technology, HPE, Bangalore, IN Feb 2021 – Dec 2022

Associate Professional Software Engineer

- Architected and implemented system-level firmware modules for enterprise servers, developing robust error handling mechanisms that reduced critical failures by 45% and maintained 99.9% system uptime
- Spearheaded firmware optimization initiatives through advanced debugging tools and memory structure refinement, resulting in 35% latency reduction and successful deployment of 100+ BIOS/UEFI updates across multiple server platforms
- Designed an automated validation framework using SQL and industry-standard tools, cutting validation cycles by 40% and post-deployment issues by 60%

EmbedKari systems Pvt ltd. Bangalore, IN Sep 2020 – Feb 2021

Hardware Design Intern

- Engineered a mixed-signal embedded system using TI ARM Cortex-M4F, achieving 25% power optimization and 95% detection accuracy
- Developed and validated peripheral interfaces (GPIO, PWM, ADC/DAC, SPI, UART, I2C) with 98% reliability and less than 5ms latency
- Executed real-time firmware with sensor fusion algorithms, achieving 20ms response time for critical event detection for home automation

PROJECTS

Florida Institute of Technology, *Melbourne, FL* Jan 2024 – Dec 2024

Thesis : Accelerating Parameter Optimization for Quantum Machine Learning (QML) using Field Programmable Gate Arrays (FPGA)

- Optimized parameter tuning algorithms on FPGA, reducing computational resource usage by 20% and achieving a 5x speedup in training compared to CPU-based optimization.
- Accelerated quantum circuit simulation by integrating FPGA with a Quantum Processing Unit (QPU) using Xilinx Vitis AI on PYNQ Framework, reducing CPU resource consumption by 60% and achieving 100x speedup.
- Enhanced ML inference efficiency through custom dual-kernel FPGA acceleration, maintaining FPGA resource utilization under 1%, and delivered 95% ML model accuracy while meeting power and timing constraints

Project: Financial Planner/Predictor with Pynq-z2 and Raspberry Pi Design Jan 2023 – May 2023

- Designed custom state machine architecture on using FPGA, optimizing financial computation modules that achieved 85% prediction accuracy
- Engineered high-speed bidirectional communication interface between FPGA and Raspberry Pi, implementing robust GPIO protocols and error handling mechanisms that ensured reliable data transmission with 99.9% integrity across platforms
- Spearheaded development of responsive Python-based analytics dashboard in 3-person team, architecting push-button navigation system and real-time visualization pipeline that distributed financial insights with 50ms refresh rate