Pratibha

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Summary

Computer Engineering graduate with expertise in CPU architectures, FPGA design, and embedded systems. Skilled in RTL development, firmware engineering, and hardware acceleration for high-performance and real-time applications. Experienced in hardware validation, signal processing, and quantum computing, with a focus on scalable, power-efficient solutions across industry and academia.

Education

Florida Institute of Technology, MS in Computer Engineering: GPA: 3.62/4.0 Jan 2023 – Dec 2024

- **Coursework:** Computer networks, Embedded Systems, Computer Architecture, DSP, FPGA, HPC

Experience

Research Associate (Volunteer), Florida Institute of Technology, Melbourne, FL Jan 2025 – Present

- Utilized C/C++ compilation to RTL workflows within the Xilinx VITIS HLS platform on Alveo U200 to design and develop high-throughput FPGA-based architectures, achieving 30% system throughput
- Developed and verified optimized RTL modules for complex matrix multiplication in C++ through comprehensive simulation and verification methodologies, achieving a 100x speedup for machine learning applications
- Integrated RTL modules with applications via AXI, achieving a 25% data processing increase and efficient multi-kernel resource distribution with resource utilization under 2% through software/hardware co-design and debugging
- Performed timing analysis and implemented constraints to meet timing requirements for high-performance applications

Graduate Teaching Assistant, Florida Institute of Technology, Melbourne, FL Jan 2024 – Dec 2024

- Led microprocessor labs for 100+ students, teaching 8085/8086, 8051 assembly programming, with 90% practical scores
- Mentored students through 15+ signal processing experiments, integrating MATLAB for DSP applications while coaching hands-on microcontroller programming using sensors, accelerometers, and Raspberry Pi 4
- Developed lab documentation for peripheral interfacing (8259 PIC/8255 PPI), teaching interrupt handling and I/O operations to enhance hardware-software understanding

Associate Professional Software Engineer, DXC Technology, HPE, Bangalore, IN Feb 2021 – Dec 2022

- Optimized enterprise server firmware through memory structure refinement and advanced debugging techniques, reducing system latency by 35% and critical failures by 45%
- Developed automated BIOS/UEFI validation framework, reducing cycle time by 40% across server platforms

Skills & Certifications

RTL & FPGA Design: Advanced RTL (SystemVerilog, VHDL, Verilog), FPGA Implementation, SoC Architecture, High-Level Synthesis,IP Integration, Memory Interface Design, Bus Protocols, Timing Closure, Place & Route Design Synthesis

Verification & Debug: UVM, Assertion-Based & Formal Verification, Clock Domain Crossing/Reset Domain Crossing Analysis, Power & Signal Analysis, Hardware Debug, Functional Coverage, Testbench Development, static timing analysis

Protocols & Interfaces: Ethernet, PCIe Gen4, AXI4, DDR/HBM, SPI, UART, I2C, USB, CAN, JTAG

Programming: C/C++, Python, Make, CMake, Git, TCL/Perl Scripting, Hardware-Software Co-Design

Tools: Xilinx Vivado, Vitis HLS, ModelSim/QuestaSim, VCS

Optimization: Pipeline Design, Memory Optimization, Resource Utilization, PPA, Latency Reduction, Clock Tree Analysis

Projects

Thesis: Accelerating Parameter Optimization for Quantum Machine Learning (QML) using Field Programmable Gate Arrays (FPGA), **Florida Institute of Technology, Melbourne, FL** Jan 2024 - Dec 2024

- Implemented high-throughput parallel gradient computation architecture, on AMD Alveo U200 FPGA, maintaining computational resource usage under 1% and achieving a 5x speedup in training compared to CPU-based optimization
- Accelerated quantum circuit simulation by integrating FPGA with a Quantum Processing Unit (QPU) using High-Level Synthesis, integrating with Xilinx Vitis AI PYNQ Framework, reducing CPU resource consumption by 60%
- Enhanced ML inference efficiency through custom AXI4-based interface between FPGA and host system for efficient data transfer, maintaining FPGA resource utilization under 1%, and delivered 95% ML model accuracy while meeting power and timing constraints

Publications

High-Level Acceleration of Quantum Simulation Frameworks on Reconfigurable Hardware Mar 2025
Design Automation Conference (DAC), 2025
FNU Pratibha, Vinayak Jha, Ishraq Islam, Anshul Maurya, Manu Chaudhary Alvir Nobel Naveed Mahmud Esam El-Araby

A Reconfigurable Framework for Hybrid Quantum-Classical Computing Apr 2025
MDPI Journal Algorithms, 2025
FNU Pratibha, Naveed Mahmud