Pratibha

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Summary

Computer Engineering graduate with strong expertise in hardware design and IP verification for embedded systems and FPGA-based platforms. Demonstrated proficiency in developing RTL modules, debugging complex simulations, and implementing rigorous test plans to ensure system quality. Experienced in integrating hardware/software co-design and power/performance optimization, with a drive to refine verification methodologies using innovative techniques.

Education

Florida Institute of Technology, MS in Computer Engineering: GPA: 3.62/4.0 Jan 2023 – Dec 2024

- **Coursework:** Computer Architecture, VLSI, Computer networks, Embedded Systems, DSP, FPGA, HPC

Experience

Electrical Engineering Intern/Co-Op, Avidyne Corporation, Melbourne, FL July 2025 – Oct 2025

- Developed and verified RTL modules for high-speed sensor integration on Lattice FPGA platforms, ensuring robust mixed-signal digital processor performance and precise timing closure.
- Validated FPGA firmware through a complete design-to-validation cycle using the Lattice software suite, which included synthesis, timing analysis, hardware-in-loop testing, and debugging to meet stringent flight-critical requirements.
- Engineered single and multi-layer PCB designs with Altium Designer for complex FPGA-based circuits, optimizing layouts to support reliable high-speed data-bus routing in safety-critical applications.
- Conducted certification compliance testing for DO-254 MOPS by rigorously validating and documenting FPGA and VHDL design elements, aligning with FAA standards and verification test protocols.
- Led board-level bring-up and debugging with oscilloscopes, logic analyzers, and protocol analyzers (I2C, SPI, UART), cutting average debug turnaround time by 20% across new builds
- Translated system specifications into VHDL code and formal test procedures to support hardware requirements verification, contribut- ing to comprehensive pre-silicon validation efforts.

Research Associate (Volunteer), Florida Institute of Technology, Melbourne, FL Jan 2025 – Present

- Collaborating with a team of Ph.D. students on an NSF Computer and Information Science and Engineering (CISE) Research Initiation Initiative (CRII) grant. This project, inspired by my thesis, is investigating heterogeneous hardware systems (quantum processors, GPUs, and reconfigurable processors) for hybrid quantum-classical algorithms
- Architected reconfigurable framework for hybrid quantum-classical computing on AMD Alveo U200/U250 FPGAs using Xilinx Vitis HLS, achieving up to 100x speedup for quantum circuit simulation and 8x improvement for variational quantum classifier (Published: MDPI Algorithms 2025, DAC 2025, IEEE QCE 2025)
- Designed and verified custom complex matrix-vector multiplication IP for dual-kernel architecture using C/C++, utilizing multi-bank DDR memory parallelization (DDR0/DDR1/DDR2) and partitioned on-chip BRAM buffers for low-latency intermediate storage, successfully achieving timing closure through pipeline balancing and constraint refinement
- Optimized high-bandwidth AXI4/AXI-Lite interfaces (32-bit/64-bit data widths) implementing burst-mode DMA transactions and concurrent memory access patterns, achieving 25% system throughput improvement for compute-intensive gradient computation and loss calculation workloads while maintaining multi-gigabit data transfer rates
- Integrated FPGA acceleration framework with industry-standard software tools through Python APIs (PYNQ framework), enabling seamless data exchange, host memory allocation, and kernel execution management
- Implemented optimized RTL design employing advanced HLS pragmas (UNROLL, ARRAY_PARTITION, PIPELINE) for parallel processing and aggressive datapath optimization techniques to minimize resource consumption, achieving under 2% FPGA resource utilization (LUT: 1.26%, DSP: 0.23%, BRAM: 1.81%) while maintaining high-throughput computational performance

Graduate Teaching Assistant, Florida Institute of Technology, Melbourne, FL Jan 2024 – Dec 2024

- Led microprocessor labs for 100+ students, teaching 8085/8086, 8051 assembly programming, with 90% practical scores
- Mentored students through 15+ signal processing experiments, integrating MATLAB for DSP applications while coaching hands-on microcontroller programming using sensors, accelerometers, and Raspberry Pi 4

Skills & Certifications

RTL & FPGA Design: VLSI Design, CMOS Device Physics, ASIC Design Flow, Timing Closure/STA, RTL Design, transistor-level circuit analysis, SoC Architecture, IP Integration, Memory Interface, Bus Protocols, Place/Route, Design Synthesis, STA

Verification & Debug: ILA, Formal Verification, Clock Domain Crossing/Reset Domain Crossing Analysis, Power & Signal Analysis, Hardware Debug, Functional Coverage, Testbench Development, IP Verification, Test Plan Development, UVM, SVTB

Protocols & Interfaces: Ethernet, PCIe Gen4, AXI, APB, DDR/HBM, SPI, UART, I3C, USB, CAN, AMBA

Programming: VHDL, Verilog, C/C++, Python, Make, HSPICE, Git, TCL/Perl Scripting, Bash, Hardware/Software Co-Design

Tools: Xilinx Vivado, Vitis HLS, ModelSim,Lattice Diamond, VCS, Logic/Protocol Analyzers, Oscilloscopes, Signal Generators

Optimization: Pipeline Design, Memory/Power Optimization, Resource Utilization, PPA, Latency Reduction, Clock Tree Analysis

Projects

Thesis: Accelerating Parameter Optimization for Quantum Machine Learning (QML) using Field Programmable Gate Arrays (FPGA), **Florida Institute of Technology, Melbourne, FL** Jan 2024 - Dec 2024

- Implemented high-throughput parallel gradient computation architecture, on AMD Alveo U200 FPGA, through advanced optimization techniques and achieving a 5x speedup in training compared to CPU-based optimization
- Accelerated quantum circuit simulation by integrating FPGA with a Quantum Processing Unit (QPU) using High-Level Synthesis, integrating with Xilinx Vitis AI PYNQ Framework, reducing CPU resource consumption by 60%
- Enhanced ML inference efficiency through custom AXI4-based interface between FPGA and host system for efficient data transfer, maintaining FPGA resource utilization under 1%, and delivered 95% ML model accuracy

I3C Communication Bridge (Microcontroller–FPGA PCB Design) *Aug 2025 - Sept 2025*

- Developed the timing-critical I3C protocol controller RTL in Verilog for a multi-master system, achieving a reliable data rate 4x faster than I2C and enabling seamless system-level integration.
- Architected a mixed-signal interface utilizing a Voltage Level Translator to manage power domain partitioning between 3.3V logic and the low-voltage I3C bus (1.8V), ensuring robust I/O buffer configuration for both open-drain and push-pull modes.
- Engineered a multi-layer PCB design with a focus on critical Signal Integrity (SI), applying meticulous layout practices like matched-length routing and impedance control to meet the demands of high-speed pre-silicon validation.
- Performed detailed Post-Layout Verification using IBIS model simulations and SDF (Standard Delay Format) analysis to analyze and mitigate ringing and crosstalk, guaranteeing reliable 12.5 MHz SDR operation.
- Conducted comprehensive pre-synthesis functional verification (99.9% coverage) via ModelSim and validated final signal quality on hardware using a protocol analyzer, ensuring strict MIPI I3C timing compliance.

Publications

Integrating Reconfigurable Accelerators with Quantum Computing Aug 2025
IEEE International Conference on Quantum Computing and Engineering 2025
FNU Pratibha, Parth Ganeriwala, Naveed Mahmud

A Reconfigurable Framework for Hybrid Quantum-Classical Computing Apr 2025
MDPI Journal Algorithms, 2025
FNU Pratibha, Naveed Mahmud

High-Level Acceleration of Quantum Simulation Frameworks on Reconfigurable Hardware Mar 2025
Design Automation Conference (DAC), 2025
FNU Pratibha, Vinayak Jha, Ishraq Islam, Anshul Maurya, Manu Chaudhary Alvir Nobel Naveed Mahmud Esam El-Araby