

1. 打开 xcore 的工程后，添加 tb 文件夹下的仿真文件。
2. 打开 riscv\_config.sv 文件，注释掉 EXTERNAL\_FASH 信号，并取消 RISCVP\_FPGA\_SIM 的注释。
3. 打开仿真文件 xcore\_tb.v,修改读入的仿真程序的位置。

```
initial begin
```

```
$readmemh("C:/Users/PerfxLab-ChenBotao/Desktop/xcore_generated/rv32im/DIV.elf.verilog", `RAM.mem);
```

```
initial begin
```

4. 打开仿真工具，添加 mem 寄存器信号到仿真，运行仿真，如果 mem[3]为 1，说明自测用例程正确。

The screenshot shows a simulation tool interface. On the left is a component hierarchy tree. In the center is a list of signals with their values and types. On the right is a 'Name' window showing a list of variables.

Component	Signal	Value	Type
u_e203_subsys_hclkgen	e203_subsys_hclkgen	0	Logic
u_riscv_soc_top	riscv_soc_top	00	Array
PPI_AXI	AXI_BUS	00000000	Array
MEM_AXI	AXI_BUS	00	Array
PLIC_AXI	AXI_BUS	00000000	Array
CLINT_AXI	AXI_BUS	00	Array
Instr_AXI	AXI_BUS	00000000	Array
Data_AXI	AXI_BUS	00	Array
DEBUG_AXI	AXI_BUS	00000000	Array
U_riscv_cpu_top	riscv_cpu_top	00	Array
axi_debug	AXI_BUS	00000000	Array
riscv_cpu	riscv_cpu	00000000	Array
riscv_core	riscv_core	00000000	Array
core_clock_gate_i	cluster_clock_gating	0	Logic
riscv_if_stage	riscv_if_stage	1e	Array
riscv_id_stage	riscv_id_stage	80001000	Array
registers_i	riscv_register_file	0	Logic
decoder_i	riscv_decoder	0	Logic
controller_i	riscv_controller	00000000	Array
int_controller_i	riscv_int_controller	00000000	Array
u_riscv_ex_stage	riscv_ex_stage_fpga	6	Array
riscv_mem_stage	riscv_mem_stage	32	Array
riscv_cs_registers	riscv_cs_registers	0	Array

5. 如果要了解 pc 状态，可以添加 pc\_id 信号，根据仿真结果分析。

The screenshot shows a simulation tool interface. On the left is a component hierarchy tree. In the center is a list of signals with their values and types.

Component	Signal	Value	Type
PPI_AXI	AXI_BUS	00001f17	Array
MEM_AXI	AXI_BUS	1	Logic
PLIC_AXI	AXI_BUS	0	Logic
CLINT_AXI	AXI_BUS	0	Logic
Instr_AXI	AXI_BUS	80001040	Array
Data_AXI	AXI_BUS	0	Logic
DEBUG_AXI	AXI_BUS	1	Logic
U_riscv_cpu_top	riscv_cpu_top	0	Logic
axi_debug	AXI_BUS	0	Array
riscv_cpu	riscv_cpu	3	Array
riscv_core	riscv_core	0	Array
core_clock_gate_i	cluster_clock_gating	80000044	Array
riscv_if_stage	riscv_if_stage	80000040	Array
riscv_id_stage	riscv_id_stage	0	Logic
registers_i	riscv_register_file	0	Logic
decoder_i	riscv_decoder	0	Logic
controller_i	riscv_controller	1	Logic
int_controller_i	riscv_int_controller	1	Logic
u_riscv_ex_stage	riscv_ex_stage_fpga	1	Logic
riscv_mem_stage	riscv_mem_stage	1	Logic
riscv_cs_registers	riscv_cs_registers	1	Logic