

## ram\_256x16 256X16, Mux 4, Drive 12

### High-Speed Single-Port Synchronous SRAM

#### Features

- Precise Optimization for TSMC's Six-Layer Metal 0.18 $\mu$ m CMOS Process
- Fast Access Time (1.06ns at typical process, 1.80V, 25°C)
- Fast Cycle Time (1.00ns at typical process, 1.80V, 25°C)
- High Density (area is 0.06mm<sup>2</sup>)
- One Read/Write Port
- Completely Static Operation
- Near-Zero Hold Time (Data, Address, and Control Inputs)

#### Memory Description

The 256X16 SRAM is a high-performance, synchronous single-port, 256-word by 16-bit memory designed to take full advantage of TSMC's six-layer metal, 0.18-micron CMOS process.

The SRAM's storage array is composed of six-transistor cells and all memory circuitry is fully static. The SRAM operates at a voltage of 1.8V  $\pm$  10% and a junction temperature range of 0°C to +125°C.

#### Pin Description

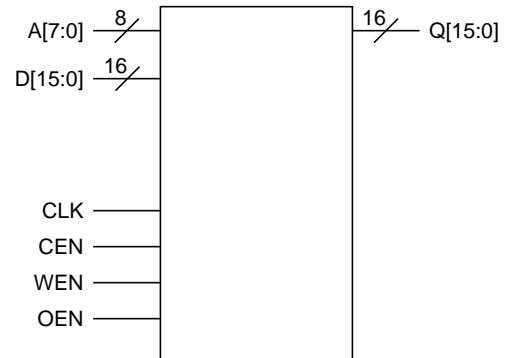
Pin	Description
A[7:0]	Addresses (A[0] = LSB)
D[15:0]	Data Inputs (D[0] = LSB)
CLK	Clock Input
CEN	Chip Enable
OEN	Output Enable
WEN	Write Enable
Q[15:0]	Data Outputs (Q[0] = LSB)

#### Area

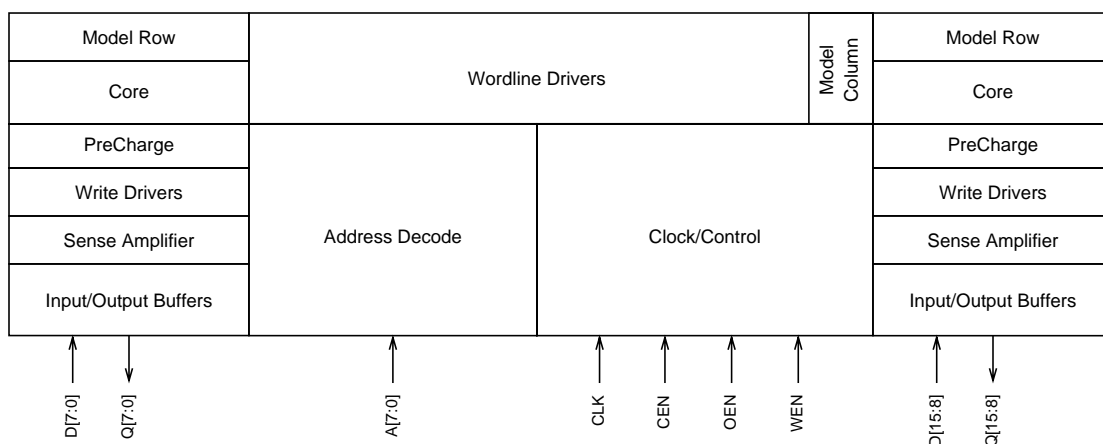
Width ( $\mu$ m)	Height ( $\mu$ m)	Area (mm <sup>2</sup> )
212.94	298.93	0.06

Area parameters do not include ring size of 5.20 $\mu$ m per side.

#### Symbol

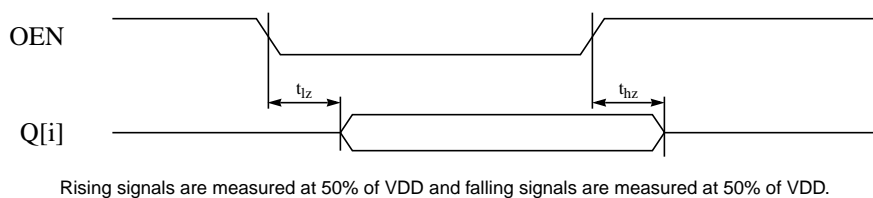


### SRAM Block Diagram

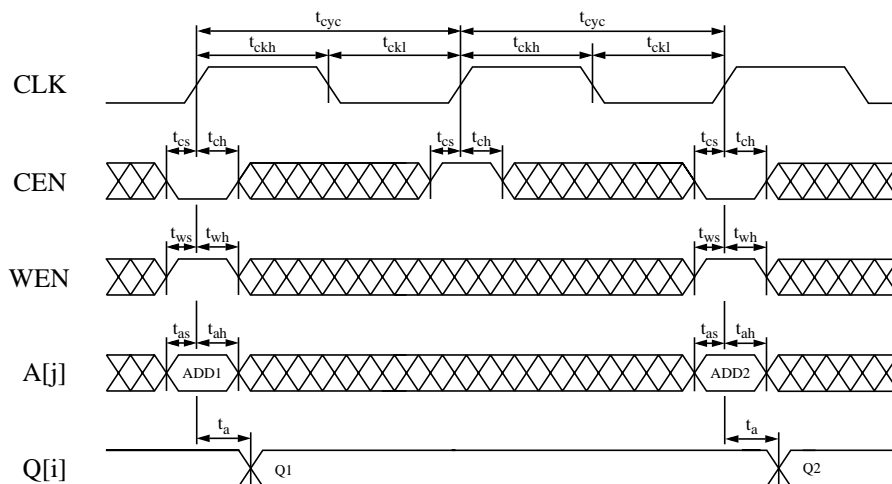


## Mission Mode

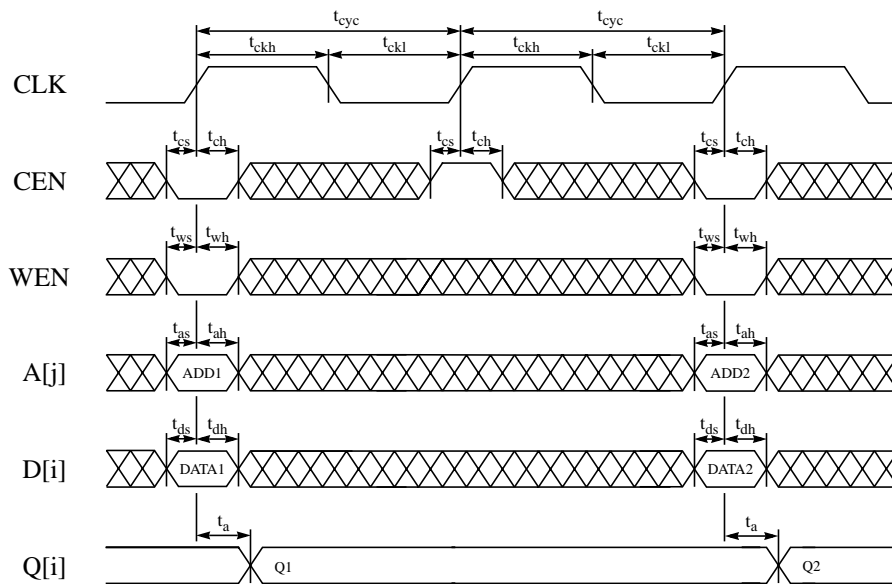
### FIGURE 1. Synchronous Single-Port SRAM Output-Enable Timing



### FIGURE 2. Synchronous Single-Port SRAM Read-Cycle Timing



**FIGURE 3. Synchronous Single-Port SRAM Write-Cycle Timing**



Rising signals are measured at 50% of VDD and falling signals are measured at 50% of VDD.

**SRAM Logic Table**

CEN	WEN	OEN	Data Out	Mode	Function
H	X	L	Last Data	Standby	Address inputs are disabled; data stored in the memory is retained, but the memory cannot be accessed for new reads or writes. Data outputs remain stable.
L	L	L	Data In	Write	Data on the data input bus D[n-1:0] is written to the memory location specified on the address bus A[m-1:0], and driven through to the data output bus Q[n-1:0].
L	H	L	SRAM Data	Read	Data on the data output bus Q[n-1:0] is read from the memory location specified on the address bus A[m-1:0].
X	X	H	Z	High-Z	The data output bus Q[n-1:0] is placed in a high impedance state. Other memory operations are unaffected.

## SRAM Timing: Mission Mode

Parameter	Symbol	Fast Process 1.98V, 0°C		Typical Process 1.80V, 25°C		Slow Process 1.62V, 125°C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Cycle time	$t_{cyc}$	0.69		1.00		1.64	
Access time <sup>1,2</sup>	$t_a$	0.69			1.06		1.74
Address setup	$t_{as}$	0.18		0.28		0.43	
Address hold	$t_{ah}$	0.07		0.09		0.12	
Chip enable setup	$t_{cs}$	0.24		0.32		0.50	
Chip enable hold	$t_{ch}$	0.00		0.00		0.00	
Write enable setup	$t_{ws}$	0.24		0.31		0.50	
Write enable hold	$t_{wh}$	0.00		0.00		0.00	
Data setup	$t_{ds}$	0.11		0.16		0.29	
Data hold	$t_{dh}$	0.00		0.00		0.00	
Output enable to hi-Z	$t_{hz}$		0.42		0.55		0.86
Output enable active <sup>1</sup>	$t_{lz}$		0.37		0.49		0.76
Clock high	$t_{ckh}$	0.08		0.11		0.18	
Clock low	$t_{ckl}$	0.10		0.15		0.26	
Clock rise slew	$t_{ckr}$		4.00		4.00		4.00
Output load factor (ns/pF)	$K_{load}$		0.28		0.38		0.56

<sup>1</sup> Parameters have a load dependence ( $K_{load}$ ), which is used to calculate:  $TotalDelay = FixedDelay + (Kload \times Cload)$ .

<sup>2</sup> Access time is defined as the slowest possible output transition for the typical and slow corners, and the fastest possible output transition for the fast corner.

## Pin Capacitance

Pin	Fast Process 1.98V, 0°C	Typical Process 1.80V, 25°C	Slow Process 1.62V, 125°C
	Value (pF)	Value (pF)	Value (pF)
A[j]	0.053	0.052	0.052
D[i]	0.005	0.005	0.005
CLK	0.181	0.165	0.130
CEN	0.014	0.014	0.014
WEN	0.015	0.015	0.015
OEN	0.010	0.010	0.010
Q[i]	0.021	0.021	0.020

## Power

100.00MHz Operation

Condition	Fast Process 1.98V, 0°C	Typical Process 1.80V, 25°C	Slow Process 1.62V, 125°C
	Value (mA)	Value (mA)	Value (mA)
AC Current <sup>1</sup>	5.888	4.993	4.274
Read AC Current	5.649	4.783	4.088
Write AC Current	6.126	5.203	4.460
Peak Current	179.851	114.483	62.709
Deselected Current <sup>2</sup>	0.000	0.000	0.000
Standby Current <sup>3</sup>	leakage only	leakage only	leakage only

<sup>1</sup> Value assumes 50% read and write operations.

<sup>2</sup> Value assumes SRAM is deselected and only CLK switches.

<sup>3</sup> Value assumes all input and output signals are stable.

## Clock Noise Limit

Signal	Fast Process 1.98V, 0°C		Typical Process 1.80V, 25°C		Slow Process 1.62V, 125°C	
	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)
CLK	10.00	0.82	10.00	0.85	10.00	0.83

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure.

## Power and Ground Noise Limit

Signal	Fast Process 1.98V, 0°C	Typical Process 1.80V, 25°C	Slow Process 1.62V, 125°C
	Voltage (V)	Voltage (V)	Voltage (V)
Power	0.20	0.18	0.16
Ground	0.20	0.18	0.16

The power/ground noise limit is the maximum supply voltage transition allowable without causing a memory failure.