rom_512x16
512X16, Mux 8, Drive 3

High-Speed Single-Port Synchronous ROM

Features

- Precise Optimization for TSMC's Six-Layer Metal 0.18µm CMOS Process
- Fast Access Time (1.22ns at typical process, 1.80V, 25˚C)
- Fast Cycle Time (1.14ns at typical process, 1.80V, 25˚C)
- High Density (area is 0.04mm^2)
- One Read Port
- Completely Static Operation
- Near-Zero Hold Time (Data, Address, and Control Inputs)

Memory Description

The 512X16 SRAM is a high-performance, synchronous single-port, 512-word by 16-bit memory designed to take full advantage of TSMC's six-layer metal, 0.18-micron CMOS process.

The ROM's storage array is a diffusion-programmable one-transistor cell with fully static memory circuitry. The ROM operates at a voltage of 1.8V ± 10% and a junction temperature range of -40˚C to +125˚C.

Pin Description

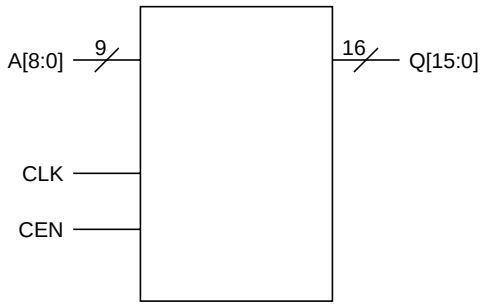
Pin	Description
A[8:0]	Addresses (A[0] = LSB)
CLK	Clock Input
CEN	Chip Enable
Q[15:0]	Data Outputs (Q[0] = LSB)

Area

Width (µm)	Height (µm)	Area (mm^2)
236.81	181.84	0.04

Area parameters do not include ring size of 5.20µm per side.

Symbol



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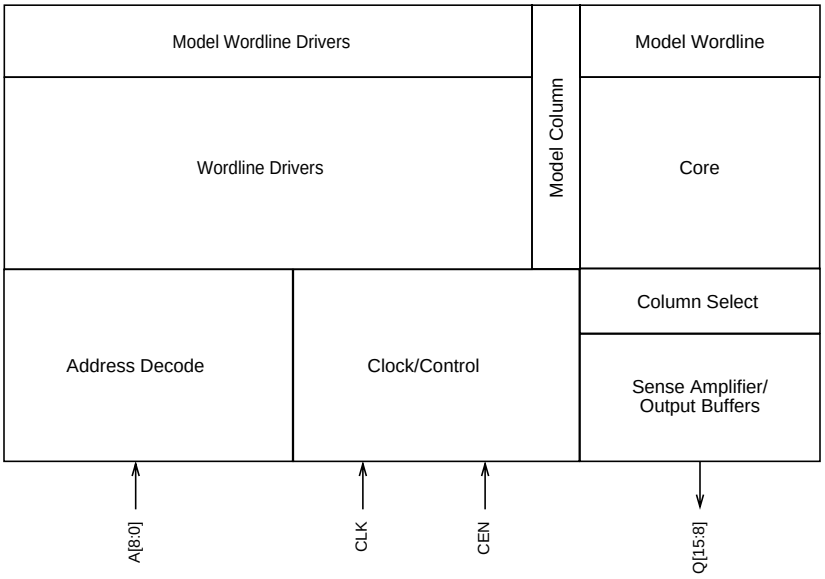
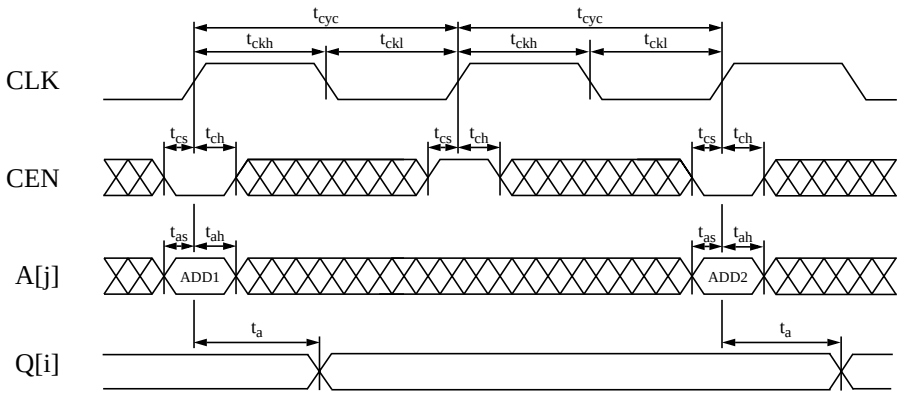
ROM Block Diagram



ROM Timing Diagram

Figure 1. Synchronous ROM Read-Cycle Timing



Rising signals are measured at 50% VDD and falling signals are measured at 50% VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

ROM Logic Table

CEN	Data Out	Mode	Function
H	Last Data	Standby	Address inputs are disabled, and the port cannot be accessed for new reads. Data outputs remain stable.
L	ROM Data	Read	Data on the output bus Q[n-1:0] is read from the memory location specified on the address bus A[m-1:0].

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ROM Timing

Parameter	Symbol	Fast Process 1.98V, 0˚C		Typical Process 1.80V, 25˚C		Slow Process 1.62V, 125˚C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Cycle time	t_{cyc}	0.83		1.14		1.80	
Access time[1,2]	t_a	0.82			1.22		1.96
Address setup	t_{as}	0.21		0.30		0.51	
Address hold	t_{ah}	0.00		0.00		0.00	
Chip enable setup	t_{cs}	0.26		0.34		0.55	
Chip enable hold	t_{ch}	0.00		0.00		0.00	
Clock high	t_{ckh}	0.08		0.11		0.18	
Clock low	t_{ckl}	0.12		0.18		0.30	
Clock rise slew	t_{ckr}		4.00		4.00		4.00
Output load factor (ns/pF)	K_{load}		0.74		0.99		1.45

[1] Parameters have a load dependence (K_{load}), which is used to calculate: $TotalDelay = FixedDelay + (Kload \times Cload)$.

[2] Access time is defined as the slowest possible output transition for the typical and slow corners, and the fastest possible output transition for the fast corner.

Pin Capacitance

Pin	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Value (pF)	Value (pF)	Value (pF)
A[j]	0.051	0.050	0.049
CLK	0.267	0.253	0.210
CEN	0.014	0.014	0.014

Power

1.00MHz Operation

Condition	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Value (mA)	Value (mA)	Value (mA)
AC Current	0.187	0.132	0.097
Peak Current	195.471	134.599	74.361
Deselected Current[1]	0.000	0.000	0.000
Standby Current[2]	leakage only	leakage only	leakage only

[1] Value assumes ROM is deselected and only CLK switches.

[2] Value assumes all input and output signals are stable.

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Clock Noise Limit

Signal	Fast Process 1.98V, 0˚C		Typical Process 1.80V, 25˚C		Slow Process 1.62V, 125˚C	
	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)
CLK	10.00	0.81	10.00	0.84	10.00	0.82

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure.

Power and Ground Noise Limit

Signal	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Voltage (V)	Voltage (V)	Voltage (V)
Power	0.20	0.18	0.16
Ground	0.20	0.18	0.16

The power/ground noise limit is the maximum supply voltage transition allowable without causing a memory failure.

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