SOMMAIRE

UNIT :

Unit ID	Unit Name
0	BRU/CMP or AGU
1	LSU
2	ALU
3	VPU/PDIV

ADD : Addition

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	ADD : 0x000 0000 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 + RS2
Latency : 3 cycles
Example : add.w r0,r1,r2

SUB : Substraction

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	SUB : 0x040 0001 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 - RS2
Latency : 3 cycles
Example : sub.w r0,r1,r2

MULS : Multiplication Signed

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	MULS : 0x080 0010 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 x RS2
Latency : 3/3/4/5 cycles
Example : muls.w r0,r1,r2

MULU : Multiplication Unsigned

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	MULU : 0xC00 0011 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 x RS2
Latency : 3/3/4/5 cycles
Example : mulu.w r0,r1,r2

DIVS : Division Signed

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	DIVS : 0x100 0100 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 / RS2
Latency : 3/3/5/10 cycles
Example : divs.l r0,r1,r2

DIVU : Division Unsigned

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	DIVU : 0x140 0101 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 / RS2
Latency : 3/3/5/10 cycles
Example : divu.b r0,r1,r2

AND : And

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	AND : 0x180 0110 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 & RS2
Latency : 3 cycles
Example : and.b r0,r1,r2

OR : Or

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	OR : 0x1C0 0111 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 | RS2
Latency : 3 cycles
Example : or.l r0,r1,r2

XOR : Exclusive Or

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	XOR : 0x200 1000 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 ~ RS2
Latency : 3 cycles
Example : xor.q r0,r1,r2

ASL : Arithmetic Shift Left

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	AND : 0x240 1001 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 << RS2
Latency : 3 cycles
Example : asl.b r0,r1,r2

LSL : Logical Shift Left

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	OR : 0x280 1010 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 << RS2
Latency : 3 cycles
Example : lsl.l r0,r1,r2

ASR : Arithmetic Shift Right

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10 9 8 7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Register	Size ----	XOR : 0x2C0 1011 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 >> RS2
Latency : 3 cycles
Example : asr.q r0,r1,r2

LSR : Logical Shift Right

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Register	Size ----	XOR : 0x300 1100 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	10 bits	2 bits

Operation : RD.size = RS1 >> RS2
Latency : 3 cycles
Example : lsr.b r0,r1,r2

ADDI : Addition Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	ADDI: 0x001 0000 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 + IMM
Latency : 3 cycles
Example : addi.w r0,r1,100

SUBI : Substraction Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	SUBI: 0x005 0001 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 - IMM
Latency : 3 cycles
Example : addi.w r0,r1,100

MULSI : Multiplication Signed Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	MULSI: 0x009 0010 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 x IMM
Latency : 3/3/4/5 cycles
Example : mulsi.b r0,r1,100

MULUI : Multiplication Unsigned Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	MULUI: 0x00D 0011 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 x IMM
Latency : 3/3/4/5 cycles
Example : mului.w r0,r1,100

DIVSI : Division Signed Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	DIVSI: 0x011 0100 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 / IMM
Latency : 3/3/5/10 cycles
Example : divs.l r0,r1,100

DIVUI : Division Unsigned Immediate

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Immediate	Size ----	DIVUI: 0x015 0101 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 / IMM
Latency : 3/3/5/10 cycles
Example : divs.l r0,r1,100

ANDI : And Immediate

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Immediate	Size ----	ANDI: 0x019 0110 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 & IMM
Latency : 3 cycles
Example : andi.w r0,r1,100

ORI : Or Immediate

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Immediate	Size ----	ORI: 0x01D 0111 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 | IMM
Latency : 3 cycles
Example : ori.l r0,r1,100

XORI : Exclusive Or Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	Source 1 Immediate	Size ----	XORI: 0x021 1000 01	Unit ----
6 bits	6 bits	10 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 ~ IMM
Latency : 3 cycles
Example : xori.q r0,r1,100

ASLI : Arithmetic Shift Left Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	0000 -----	Source 1 Immediate	Size ----	ASLI: 0x025 1001 01	Unit ----
6 bits	6 bits	6 bits	6 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 << IMM
Latency : 3 cycles
Example : asli.w r0,r1,100

LSLI : Logical Shift Left Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	0000 -----	Source 1 Immediate	Size ----	ASLI: 0x029 1010 01	Unit ----
6 bits	6 bits	6 bits	6 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 << IMM
Latency : 3 cycles
Example : lsli.l r0,r1,100

ASRI : Arithmetic Shift Right Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	0000 -----	Source 1 Immediate	Size ----	ASRI: 0x02D 1011 01	Unit ----
6 bits	6 bits	6 bits	6 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 >> IMM
Latency : 3 cycles
Example : asri.w r0,r1,100

LSRI : Logical Shift Right Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 2 Register	0000 -----	Source 1 Immediate	Size ----	LSRI: 0x030 1100 01	Unit ----
6 bits	6 bits	6 bits	6 bits	2 bits	6 bits	2 bits

Operation : RD.size = RS2 >> IMM
Latency : 3 cycles
Example : lsri.w r0,r1,100

ADDQ : Addition Quick immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 1 Immediate	Size ----	ADDQ: 0x002 0000 10	Unit ----
6 bits	16 bits	2 bits	6 bits	2 bits

Operation : RD.size += IMM
Latency : 3 cycles
Example : addi.w r0,r1,100

-------------------etc etc

MOVEI : Move Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 1 Immediate	Size ----	Move 0x3 10	Unit ----
6 bits	20 bits	2 bits	2 bits	2 bits

Operation : RD.size = IMM
Latency : 3 cycles
Example : movei.w r0,100

NOP : No Operation

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0000 0000 0000 0000 0000 --------------------------------	NOP : 0x04 00e1 00	Unit ----
24 bits	6 bits	2 bits

Operation : **...**
Latency : 1/3 cycles
Example : nop /nop.e

SWITCH : Switch

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0000 0000 0000 0000 0000 --------------------------------	Switch : 0x10 010c 00	Unit ----
24 bits	6 bits	2 bits

Operation : RF&0xFE = c
Latency : 1/2 cycles
Example : switch 0

CMP : Compare

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Register	Source 1 Register	-------------------- 0000 0000 0000	Size ----	CMP 0x0 0000	Unit ----
6 bits	6 bits	12 bits	2 bits	4 bits	2 bits

Operation : RF = RS1 ? RS2
Latency : 3 cycles
Example : cmp.b r1,r2

PCMP.H : Posits Half Compare

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Posit Register	Source 1 Posit Register	---------------- 0000 0000 00	Size2 ----	Size1 ----	PCMPH 0x4 0100	Unit ----
6 bits	6 bits	10 bits	2 bits	2 bits	4 bits	2 bits

Operation : RF = PH1 ? PH2
Latency : 3 cycles
Example : pcmp.h vp0x,vp0y

PCMP.S : Posits Single Compare

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Posit Register	Source 1 Posit Register	---------------------- 0000 0000 0000 00	PCMPS 0x8 1000	Unit ----
6 bits	6 bits	14 bits	4 bits	2 bits

Operation : RF = PS1 ? PS2
Latency : 3 cycles
Example : pcmp.s vp0,vp1

CMPI : Compare Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Register	Source 1 Immediate	Size ----	**CMP I** 0x1 01	Unit ----
6 bits	20 bits	2 bits	2 bits	2 bits

Operation : RF = RS1 ? IMM<<3
Latency : 3 cycles
Example : cmpi.b r1,42

PCMPI.H : Posits Half Compare Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Posit Register	Source 1 Immediate	---- 0000	Size ----	**PCHI** 0x2 10	Unit ----
6 bits	16 bits	4 bits	2 bits	2 bits	2 bits

Operation : RF = RS1 ? IMM<<3
Latency : 3 cycles
Example : pcmpi.h vp0x,3.41

PCMPI.S : Posits Single Compare Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Posit Register	Source 1 Immediate	**PCSI** 0x3 11	Unit ----
6 bits	20 bits	2 bits	2 bits

Operation : RF = RS2 ? IMM<<3
Latency : 3 cycles
Example : pcmpi.s vp0,3.41

BNE : Branch Not Equal

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BNE : 0x00C 0000 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if(Z != 0) PC += IMM x 8
Latency : 1/2 cycles
Example : bne label

BEQ : Branch Equal

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BNE : 0x04C 0001 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if(Z != 1) PC += IMM x 8
Latency : 1/2 cycles
Example : beq label

BL : Branch Less

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BL : 0x08C 0010 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bl label

BLE : Branch Less or Equal

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BLE : 0x0CC 0011 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : ble label

BG: Branch Greater or Equal

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BG : 0x10C 0100 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bg label

BGE : Branch Greater or Equal

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BGE : 0x14C 0101 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bge label

BLS : Branch Less Signed

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2	1 0
Source Immediate	-------- 00 0000	BLS : 0x18C 0110 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bls label

BLES : Branch Less or Equal Signed

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2	1 0
Source Immediate	-------- 00 0000	BLES : 0x1CC 0111 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bles label

BGS: Branch Greater or Equal Signed

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2	1 0
Source Immediate	-------- 00 0000	BGS : 0x20C 1000 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bgs label

BGES : Branch Greater or Equal Signed

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	BGES : 0x24C 1001 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : if() PC += IMM x 8
Latency : 1/2 cycles
Example : bges label

B : Branch Unconditional

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	B : 0x28C 1010 0011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : PC += IMM x 8
Latency : 1/2 cycles
Example : bges label

JMP : Jump

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	JMP : 0x02C 0000 1011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : PC = IMM x 8
Latency : 1/2 cycles
Example : jmp label

JMPR : Jump Relative

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	JMPR : 0x06C 0001 1011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : PC = LR + IMM x 8
Latency : 1/2 cycles
Example : jmpr label

CALL : Call

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	CALL : 0x0AC 0010 1011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : PC = IMM x 8
Latency : 1/2 cycles
Example : call label

CALLR : Call Relative

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source Immediate	-------- 00 0000	CALLR : 0x0EC 0011 1011 00	Unit ----
14 bits	6 bits	10 bits	2 bits

Operation : PC = LR + IMM x 8
Latency : 1/2 cycles
Example : callr label

RET : Return

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0000 0000 0000 0000 0000 --------------------------------	RET : 0x2C 1111 00	Unit ----
24 bits	6 bits	2 bits

Operation : **...**
Latency : 1/2 cycles
Example : ret

LDM : Load Memory

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Immediate	Size ----	LDM: 0x0 +0 00	Unit ----
6 bits	6 bits	12 bits	2 bits	4 bits	2 bits

Operation : RD.size = SP_MEMORY(RS2 + IMM)
Latency : 4 cycles
Example : ldm.w r0,42[r1]

STM : Store Memory

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 4 3 2	1 0
Source 3 Register	Source 2 Register	Source 1 Immediate	Size ----	STM: 0x4 +1 00	Unit ----
6 bits	6 bits	12 bits	2 bits	4 bits	2 bits

Operation : SP_MEMORY(RS2 + IMM) = RS3.size
Latency : 4 cycles
Example : stm.w r0,42[r1]

LDC : Load Cache

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 4 3 2	1 0
Destination Register	Source 2 Register	Source 1 Immediate	Size ----	LDC: 0x1 +0 01	Unit ----
6 bits	6 bits	12 bits	2 bits	4 bits	2 bits

Operation : RD.size = SP_MEMORY(RS2 + IMM)
Latency : 4 cycles
Example : ldm.w r0,42[r1]

STC : Store Cache

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 4 3 2	1 0
Source 3 Register	Source 2 Register	Source 1 Immediate	Size ----	STC: 0x5 +1 01	Unit ----
6 bits	6 bits	12 bits	2 bits	4 bits	2 bits

Operation : SP_MEMORY(RS2 + IMM) = RS3.size
Latency : 4 cycles
Example : stm.w r0,42[r1]

IN : In I/O Memory

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source 1 Immediate	--------- 0000 0000	Size ----	IN: 0x001 0000 01	Unit ----
6 bits	8 bits	8 bits	2 bits	6 bits	2 bits

Operation : RD.size = SPIO_MEMORY(IMM)
Latency : 3 cycles
Example : in.w r0,42

OUT : Out I/O Memory

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Register	Source 1 Immediate	--------- 0000 0000	Size ----	OUT: 0x001 1000 01	Unit ----
6 bits	8 bits	8 bits	2 bits	6 bits	2 bits

Operation : SPIO_MEMORY(IMM) = RS2.size
Latency : 3 cycles
Example : out.q r0,42

OUTI : Out I/O Memory Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 2 Immediate	Source 1 Immediate	IN: 0x001 0000 01	Unit ----
8 bits	16 bits	6 bits	2 bits

Operation : SPIO_MEMORY(IMM2) = IMM1
Latency : 3 cycles
Example : outi.b r0,13

LDMV : Load Memory Vector Posits

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source 2 Register	Source 1 Immediate	Size ----	LDMV: 0x03 +000 11	Unit ----
6 bits	3 bits	13 bits	2 bits	6 bits	2 bits

Operation : VPD.size = SP_MEMORY(RS2 + IMM*16)
Latency : 4 cycles
Example : ldmv.xy vp0,42[r1]

STMV : Store Memory Vector Posits

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Source 3 Posit Register	Source 2 Register	Source 1 Immediate	Size ----	STMV: 0x13 +100 11	Unit ----
6 bits	3 bits	13 bits	2 bits	6 bits	2 bits

Operation : SP_MEMORY(RS2 + IMM*16) = VPS.size
Latency : 4 cycles
Example : stmv.xy vp0,42[r1]

LDCV : Load Cache Vector Posits

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23	22 21 20 19 18 17 16 15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Register	Source 1 Immediate	Size ----	LDMV: 0x0B +010 11	Unit ----
6 bits	3 bits	13 bits	2 bits	6 bits	2 bits

Operation : VPD.size = SP_MEMORY(RS2 + IMM*16)
Latency : 4 cycles
Example : ldcv.xy vp0,42[r1]

STCV : Store Cache Vector Posits

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23	22 21 20 19 18 17 16 15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Source 3 Posit Register	Source 2 Register	Source 1 Immediate	Size ----	STMV: 0x1B +110 11	Unit ----
6 bits	3 bits	13 bits	2 bits	6 bits	2 bits

Operation : SP_MEMORY(RS2 + IMM*16) = VPS.size
Latency : 4 cycles
Example : stcv.xy vp0,42[r1]

PADD.H : Posits Half Addition

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PADD.H : 0x00 00 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPH = PS1 + PS2
Latency : 4 cycles
Example : padd.h vp0,vp0y, vp0z

PSUB.H : Posits Half Substraction

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PSUB.H : 0x20 00 1000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPH = PS1 - PS2
Latency : 4 cycles
Example : psub.h vp0,vp0y, vp0z

PMUL.H : Posits Half Multiplication

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PMUL.H : 0x40 01 0000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPH = PS1 x PS2
Latency : 4 cycles
Example : pmul.h vp0,vp0y, vp0z

PMULADD.H : Posits Half Multiplication Addition

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PMADD.H : 0x60 01 1000 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPH = PS1 + (PS1 x PS2)
Latency : 4 cycles
Example : pmuladd.h vp0,vp0y, vp0z

PADD.S : Posits Single Addition

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12 11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 0000	PADD.S : 0x80 10 0000 00	Unit ----
6 bits	6 bits	6 bits	4 bits	8 bits	2 bits

Operation : PD = PS1 + PS2
Latency : 5 cycles
Example : padd.s vp0,vp0, vp0

PSUB.S : Posits Single Substraction

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12 11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 0000	PSUB.S : 0xA0 10 1000 00	Unit ----
6 bits	6 bits	6 bits	4 bits	8 bits	2 bits

Operation : PD = PS1 - PS2
Latency : 5 cycles
Example : psub.s vp30,vp10, vp20

PMUL.S : Posits Single Multiplication

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 0000	PMUL.S : 0xC0 11 0000 00	Unit ----
6 bits	6 bits	6 bits	4 bits	8 bits	2 bits

Operation : PD = PS1 x PS2
Latency : 5 cycles
Example : pmul.s vp1,vp2, vp3

PMADD.S : Posits Single Multiplication Addition

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 0000	PMADD.S : 0xE0 11 1000 00	Unit ----
6 bits	6 bits	6 bits	4 bits	8 bits	2 bits

Operation : PD = PS1 + (PS1 x PS2)
Latency : 5 cycles
Example : pmuladd.s vp0,vp8, vp7

PADD.XYZW : Vector Posits Half Addition

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 00	Size ----	PADD : 0x04 00 0001 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPD.size = VPS1.size + VPS2.size
Latency : 4 cycles
Example : padd.xyzw vp0,vp1, vp2

PSUB.XYZW : Vector Posits Half Substraction

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 00	Size ----	PSUB : 0x24 00 1001 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPD.size = VPS1.size - VPS2.size
Latency : 4 cycles
Example : psub.xyzw vp0,vp1, vp2

PADDS : Vector Posits Half Addition with Single

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PADDS: 0x08 00 0010 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPD.size = VPS1.size + PS2
Latency : 4 cycles
Example : padds.xyzw vp0,vp1, vp2x

PSUBS : Vector Posits Half Addition with Single

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PSUBS: 0x28 00 1010 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPD.size = VPS1.size - PS2
Latency : 4 cycles
Example : psubs.xyzw vp0,vp1, vp2x

PIPR : Posits Half Inner Product

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PIPR : 0x6C 01 1011 00	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : PD = VPS1.size . VPS2.size
Latency : 4 cycles
Example : pipr.xyz vp0,vp0y, vp0z

PMOVE : Posits Move

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source Posit Register	--------- 0000 00	Size2 ----	Size1 ----	PMOVE: 0x01 00 0000 01	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : VPDst.select2 = VPSrc.select1
Latency : 3 cycles
Example : pmove vp0y, vp0z

VPMOVE : Vector Posits Move

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source Posit Register	------ 0000 0000	Size1 ----	VPMOVE: 0x05 00 0001 01	Unit ----
6 bits	6 bits	8 bits	2 bits	8 bits	2 bits

Operation : VPDst.size = VPSrc.size
Latency : 3 cycles
Example : **v**pmove vp0, vp1

PMOVEI.H : Posits Half Move Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source Immediate	Size ----	PMOVEIH: 0x11 0100 01	Unit ----
6 bits	16 bits	2 bits	6 bits	2 bits

Operation : PDst.select = IMM
Latency : 3 cycles
Example : pmovei.h vp0y, 42.7

PMOVEI.S : Posits Single Move Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source Immediate	PMOVEIS: 0x15 0101 01	Unit ----
6 bits	20 bits	6 bits	2 bits

Operation : PDst = IMM
Latency : 3 cycles
Example : pmovei.h vp0, 42.3

VPMOVEI.H : Vector Posits Half Move Immediate

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source Immediate	Size ----	VPMOVEI: 0x19 0110 01	Unit ----
6 bits	16 bits	2 bits	6 bits	2 bits

Operation : VPDst.size = IMM
Latency : 3 cycles
Example : **v**pmovei.xyz vp0y, 42.7

PMOVERO : Posits Move Register Out

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Source Posit Register	------ 0000 0000	Size1 ----	PMOVERO: 0x08 00 0010 01	Unit ----
6 bits	6 bits	8 bits	2 bits	8 bits	2 bits

Operation : RDst = VPSrc.size
Latency : 3 cycles
Example : pmovero r0,vp1

PMOVERI : Posits Move Register In

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Register	Destination Posit Register	------ 0000 0000	Size1 ----	PMOVERI: 0x0D 00 0011 01	Unit ----
6 bits	6 bits	8 bits	2 bits	8 bits	2 bits

Operation : VPSrc.size = RDst
Latency : 3 cycles
Example : pmoveri vp1,r0

PDIV.H : Posits Half Division

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12	11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	Size2 ----	Size1 ----	PDIV.H : 0x02 00 0000 10	Unit ----
6 bits	6 bits	6 bits	2 bits	2 bits	8 bits	2 bits

Operation : PDst = Psrc1.select1 / PSrc2.select1
Latency : 6 cycles
Example : pdiv.h vp0,vp0y, vp0z

PDIV.S : Posits Single Division

description...
description...

Operation Code :

31 30 29 28 27 26	25 24 23 22 21 20	19 18 17 16 15 14	13 12 11 10	9 8 7 6 5 4 3 2	1 0
Destination Posit Register	Source 2 Posit Register	Source 1 Posit Register	---- 0000	PDIV.H : 0x02 00 0000 10	Unit ----
6 bits	6 bits	6 bits	4 bits	8 bits	2 bits

Operation : PDst = PSrc1 / PSrc2
Latency : 8 cycles
Example : pdiv.s vp0,vp1, vp2

PSQRT.H : Posits Half Square Root

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source Posit Register	------ 0000 0000	Size ----	Size ----	PSQRT.H: 0x08 00 0010 01	Unit ----
6 bits	6 bits	8 bits	2 bits	2 bits	8 bits	2 bits

Operation : PDst = SQRT (VPSrc.select)
Latency : 10 cycles
Example : psqr.h vp1y,vp1x

PSQRT.S : Posits Half Square Root

description...
description...

Operation Code :

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Destination Posit Register	Source Posit Register	------ 0000 0000	Size ----	PSQRT.H: 0x08 00 0010 01	Unit ----
6 bits	6 bits	8 bits	2 bits	8 bits	2 bits

Operation : PDst = SQRT(VPSrc)
Latency : 14 cycles
Example : psqrt.s vp0,vp1