

- **Everything so far has had a fixed set of bits for Exponent and Significand.**
 - What if the field widths were variable?
 - Also, add a “**u-bit**” to tell whether number is exact or in-between unums.
 - “Promises to be to floating point what floating point is to fixed point.”
- **Claims to save power!**
- **Posits : hardware-friendly version of unums**

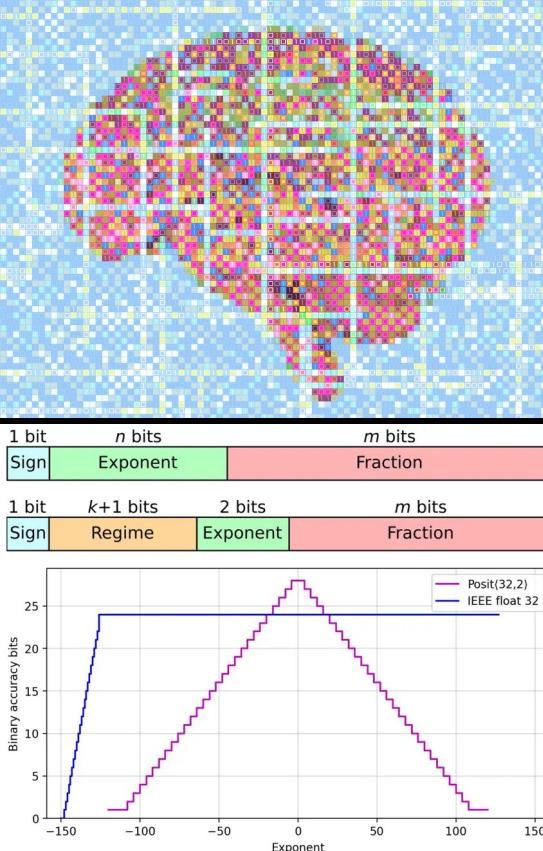


[https://en.wikipedia.org/wiki/Unum_\(number_format\)](https://en.wikipedia.org/wiki/Unum_(number_format))

Dr. John Gustafson

Garcia, Yan

Posits, a New Kind of Number, Improves the Math of AI



Scientists at Spain's Complutense University of Madrid have developed a processor core that can deploy the posit standard, a numerical representation that improves over standard floating-point arithmetic processors, in hardware. Complutense researchers synthesized the hardware in a field-programmable gate array to compare computations performed using 32-bit floats alongside 32-bit posits. Posits exhibited a four-order-of-magnitude improvement in matrix multiplication accuracy without losing computation time. "It's possible that posits will speed up [artificial intelligence] training because you're not losing as much information on the way," said Complutense's David Mallasén Quintana.

spectrum.ieee.org/floating-point-numbers-posit-processor

← This graph shows components of floating-point-number representation [top] and posit representation [middle]. The accuracy comparison shows posits' advantage when the exponent is close to 0.



UC Berkeley
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CS61C

Great Ideas in Computer Architecture (a.k.a. Machine Structures)



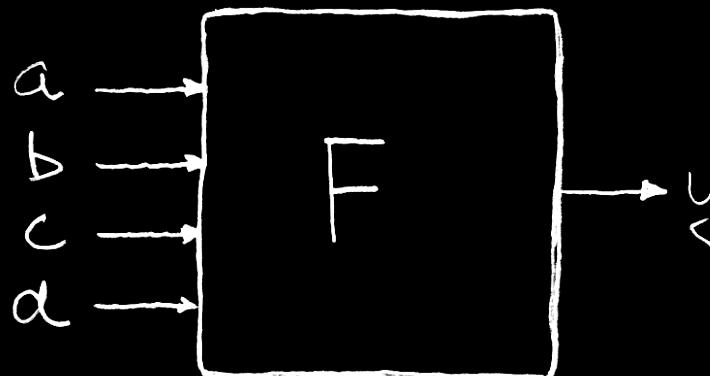
UC Berkeley
Teaching Professor
Lisa Yan

Combinational Logic

Truth Tables

真值表

Truth Tables



How many Fs
(4-input devices)
@ Fry's?

a	b	c	d	y
0	0	0	0	$F(0,0,0,0)$
0	0	0	1	$F(0,0,0,1)$
0	0	1	0	$F(0,0,1,0)$
0	0	1	1	$F(0,0,1,1)$
0	1	0	0	$F(0,1,0,0)$
0	1	0	1	$F(0,1,0,1)$
0	1	1	0	$F(0,1,1,0)$
0	1	1	1	$F(0,1,1,1)$
1	0	0	0	$F(1,0,0,0)$
1	0	0	1	$F(1,0,0,1)$
1	0	1	0	$F(1,0,1,0)$
1	0	1	1	$F(1,0,1,1)$
1	1	0	0	$F(1,1,0,0)$
1	1	0	1	$F(1,1,0,1)$
1	1	1	0	$F(1,1,1,0)$
1	1	1	1	$F(1,1,1,1)$

TT Example #1: 1 iff one (not both) a,b=1

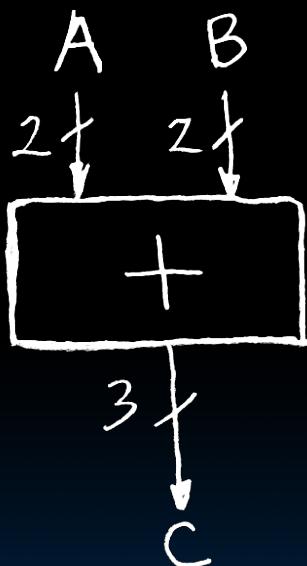
a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

$$\bar{a}b + a\bar{b}$$



a	y
0	b
1	\bar{b}

TT Example #2: 2-bit adder



A a_1a_0	B b_1b_0	C $c_2c_1c_0$
00	00	000
00	01	001
00	10	010
00	11	011
01	00	001
01	01	010
01	10	011
01	11	100
10	00	010
10	01	011
10	10	100
10	11	101
11	00	011
11	01	100
11	10	101
11	11	110

How
Many
Rows?

TT Example #3: 32-bit unsigned adder

A	B	C
000 ... 0	000 ... 0	000 ... 00
000 ... 0	000 ... 1	000 ... 01
.	.	.
.	.	.
.	.	.
111 ... 1	111 ... 1	111 ... 10

How
Many
Rows?

TT Example #4: 3-input majority circuit

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

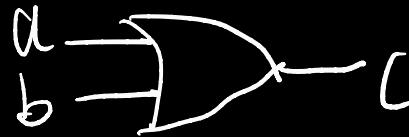


Logic Gates

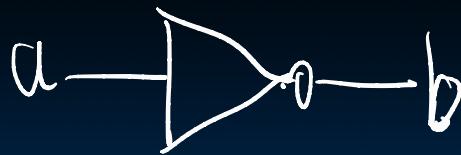
Logic Gates (1/2)



\wedge AND A standard logic gate symbol for AND. It consists of two inputs labeled 'a' and 'b' entering a single output terminal labeled 'c'. The symbol is a rectangle with a diagonal line from the top-left corner to the bottom-right corner.



\vee OR A standard logic gate symbol for OR. It consists of two inputs labeled 'a' and 'b' entering a single output terminal labeled 'c'. The symbol is a rectangle with a diagonal line from the top-left corner to the bottom-right corner.



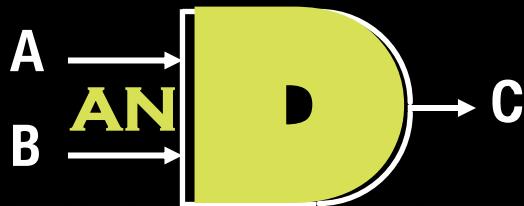
\neg NOT A standard logic gate symbol for NOT. It consists of a single input terminal labeled 'a' entering a single output terminal labeled 'b'. The symbol is a triangle pointing downwards.

ab	c
00	0
01	0
10	0
11	1

a	b
0	1
1	0

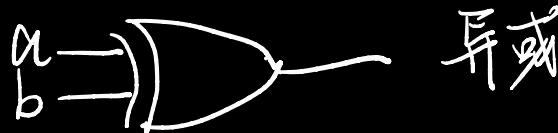
and vs. or ... how to recall which is which

and gate symbol



a	b	y
0	0	0
0	1	0
1	0	0
1	1	1

Logic Gates (2/2)



XOR



NAND



NOR



ab	c
00	0
01	1
10	1
11	0

ab c

00 1

01 1

10 1

11 0

ab c

00 1

01 0

10 0

11 0



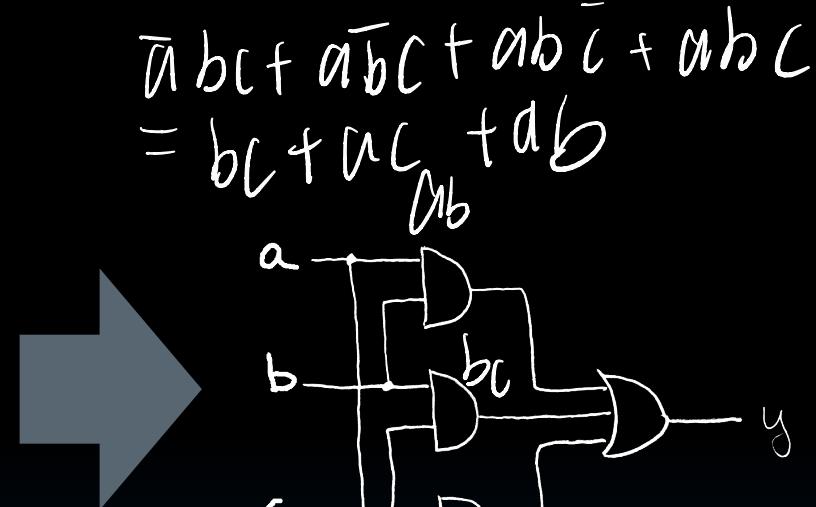
2-input gates extend to n-inputs

- N-input XOR is the only one which isn't so obvious
- It's actually simple...
 - XOR is a 1 iff the # of 1s at its input is odd

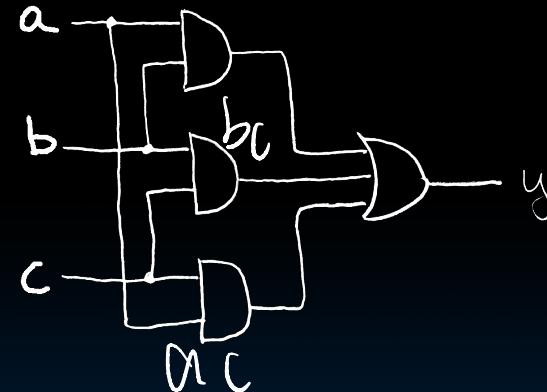
a	b	c	y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table → Gates (e.g., majority circ.)

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



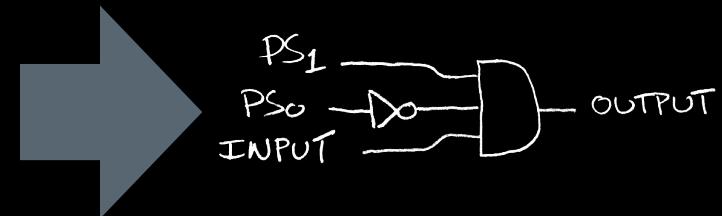
$$\begin{aligned} & \bar{a}bc + \bar{a}\bar{b}c + ab\bar{c} + abc \\ &= bc + ac + ab \end{aligned}$$



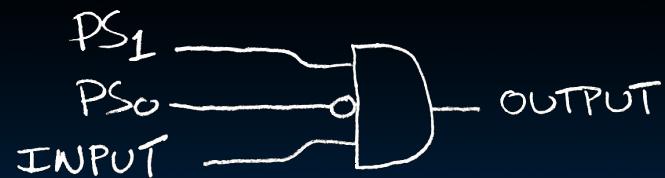
$$ab + bc + ac$$

Truth Table → Gates (e.g., FSM circuit)

PS	Input	NS	Output
00	0	00	0
00	1	01	0
01	0	00	0
01	1	10	0
10	0	00	0
10	1	00	1



or equivalently...

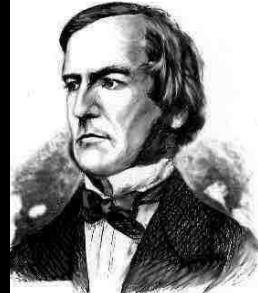


Boolean Algebra

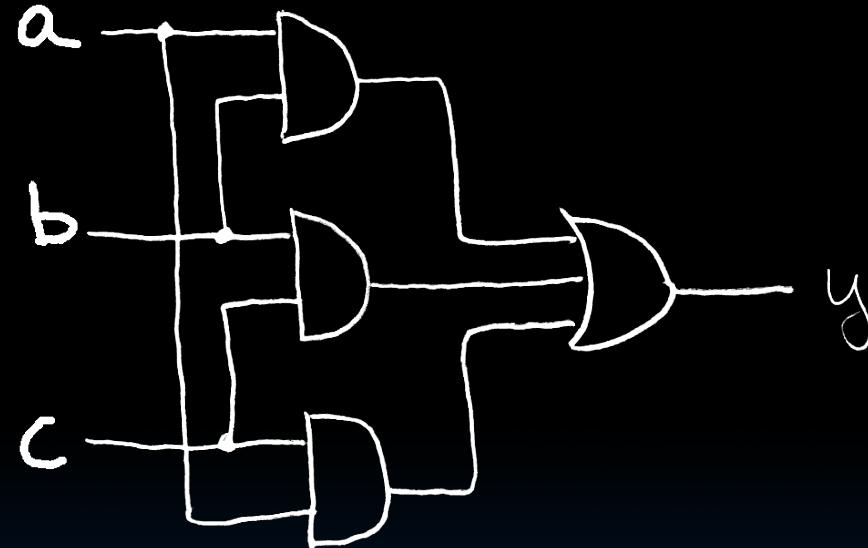
布尔代数

Boolean Algebra

- George Boole, 19th Century mathematician
- Developed a mathematical system (algebra) involving logic
 - later known as “Boolean Algebra”
- Primitive functions: AND, OR and NOT
- Power of Boolean Algebra
 - there's a one-to-one correspondence between circuits made up of AND, OR and NOT gates and equations in BA
- + means OR, • means AND, \bar{x} means NOT



Boolean Algebra (e.g., for majority fun.)

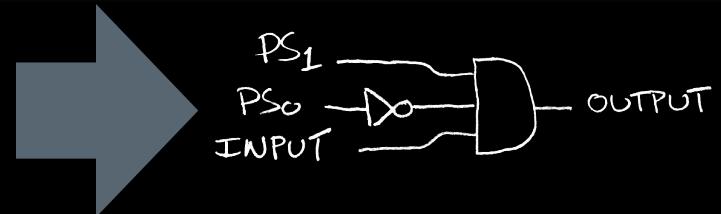


$$y = a \cdot b + a \cdot c + b \cdot c$$

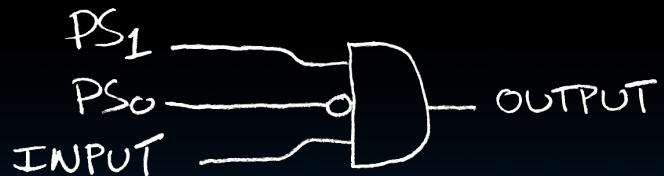
$$y = ab + ac + bc$$

Boolean Algebra (e.g., for FSM)

PS	INPUT	NS	OUTPUT
00	0	00	0
00	1	01	0
01	0	00	0
01	1	10	0
10	0	00	0
10	1	00	1



or equivalently...



$$OUTPUT = PS_1 \cdot \overline{PS_0} \cdot INPUT$$

BA: Circuit & Algebraic Simplification



$$\begin{aligned} y &= ab + a + c \\ &\downarrow \end{aligned}$$

equation derived from original circuit

$$\begin{aligned} ab + a + c & \\ &= a(b + 1) + c \\ &= a(1) + c \\ &= a + c \\ &\downarrow \end{aligned}$$

algebraic simplification

BA also great for circuit verification
Circ X = Circ Y? Use BA to prove!



simplified circuit



Laws of Boolean Algebra

Laws of Boolean Algebra

$$x + y \cdot z = (x + y) \cdot (x + z)$$

$$x \cdot \bar{x} = 0$$

$$x + \bar{x} = 1$$

complementarity

$$x \cdot 0 = 0$$

$$x + 1 = 1$$

laws of 0's and 1's

$$x \cdot 1 = x$$

$$x + 0 = x$$

identities

$$x \cdot x = x$$

$$x + x = x$$

idempotent law 

$$x \cdot y = y \cdot x$$

$$x + y = y + x$$

commutative law

$$(xy)z = x(yz)$$

$$(x + y) + z = x + (y + z)$$

associativity

$$x(y + z) = xy + xz$$

$$x + yz = (x + y)(x + z)$$

distribution

$$xy + x = x$$

$$\frac{(x + y)x}{(x + y)} = x$$

uniting theorem

$$x \cdot \bar{y} = \bar{x} + \bar{y}$$

$$\frac{(x + y)\bar{x}}{(x + y)} = \bar{x} \cdot \bar{y}$$

DeMorgan's Law



Boolean Algebraic Simplification Example

$$\begin{aligned}y &= ab + a + c \\&= a(b + 1) + c \quad \textit{distribution, identity} \\&= a(1) + c \quad \textit{law of 1's} \\&= a + c \quad \textit{identity}\end{aligned}$$



Canonical Forms

Canonical forms (1/2)

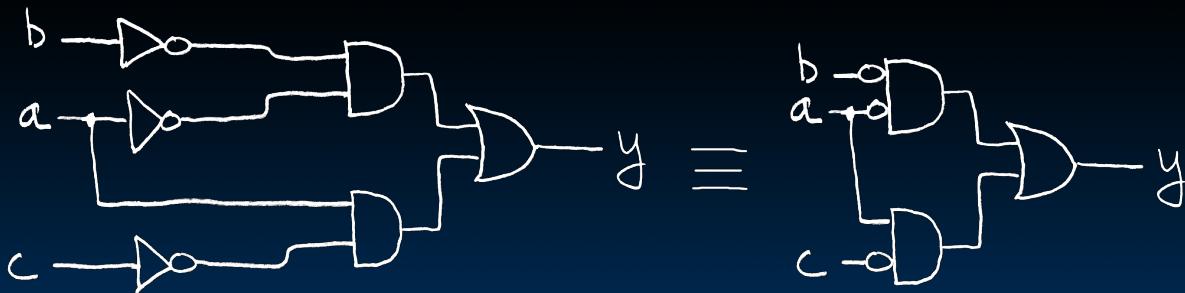
	abc	y
$\bar{a} \cdot \bar{b} \cdot \bar{c}$	000	1
$\bar{a} \cdot \bar{b} \cdot c$	001	1
	010	0
	011	0
$a \cdot \bar{b} \cdot \bar{c}$	100	1
	101	0
$a \cdot b \cdot \bar{c}$	110	1
	111	0

**Sum-of-products
(ORs of ANDs)**

$$y = \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + a\bar{b}\bar{c} + ab\bar{c}$$

Canonical forms (2/2)

$$\begin{aligned}y &= \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + a\bar{b}\bar{c} + ab\bar{c} \\&= \bar{a}\bar{b}(\bar{c} + c) + a\bar{c}(\bar{b} + b) \quad \textit{distribution} \\&= \bar{a}\bar{b}(1) + a\bar{c}(1) \quad \textit{complementarity} \\&= \bar{a}\bar{b} + a\bar{c} \quad \textit{identity}\end{aligned}$$



L16 Three questions

1) $(a+b) \cdot (\bar{a}+b) = b$

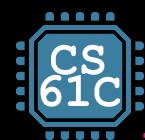
2) N-input gates can be thought of cascaded 2-input gates. i.e.,

$$(a \Delta b \Delta c \Delta d \Delta e) = a \Delta (b \Delta (c \Delta (d \Delta e)))$$

where Δ is one of AND, OR, XOR, NAND

3) You can use NOR(s) with clever wiring to simulate AND, OR, & NOT

F F F
F F T
F T F
F T T
T F F
T F T
T T F
T T T



Answer

1) $(a+b) \cdot (\bar{a}+b) = a\bar{a} + ab + b\bar{a} + bb = 0 + b(a+\bar{a}) + b = b+b = b$ TRUE

2) (next slide)

3) You can use NOR(s) with clever wiring to simulate AND, OR, & NOT.

$$\text{NOR}(a,a) = \overline{a+a} = \overline{a} \cdot \overline{a} = \overline{a}$$

Using this NOT, can we make a NOR an OR? An And? TRUE

1) $(a+b) \cdot (\bar{a}+b) = b$

2) N-input gates can be thought of cascaded 2-input gates. I.e.,

$$(a \Delta b \Delta c \Delta d \Delta e) = a \Delta (b \Delta (c \Delta (d \Delta e)))$$

where Δ is one of AND, OR, XOR, NAND

3) You can use NOR(s) with clever wiring to simulate AND, OR, & NOT

1	2	3
F	F	F
F	T	F
F	F	T
T	T	F
T	F	F
T	F	T
T	T	F
T	T	T

Garcia, Yan

Answer (for question 2)

- 1)
 - 2) N-input gates can be thought of cascaded 2-input gates. I.e.,
 $(a \Delta bc \Delta d \Delta e) = a \Delta (bc \Delta (d \Delta e))$
where Δ is one of AND, OR, XOR, NAND... **FALSE**
- Let's confirm!

		CORRECT 3-input			
xyz		AND	OR	XOR	NAND
000	0	0	0	0	1
001	0	1	1	1	1
010	0	1	1	1	1
011	0	1	0	1	1
100	0	1	1	1	1
101	0	1	0	1	1
110	0	1	0	1	1
111	1	1	1	1	0

		CORRECT 2-input			
yz		AND	OR	XOR	NAND
00	0	0	0	0	1
01	0	1	1	1	1
10	0	1	1	1	1
11	1	1	1	0	0

“And In conclusion...”

- Pipeline big-delay CL for faster clock
- Finite State Machines extremely useful
 - You'll see them again in (at least) 151A, 152 & 164
- Use this table and techniques we learned to transform from 1 to another

