

# **VIEW FROM THE TOP**

*Conversations with Global Leaders*

## **Driving Moore's Law:**

A Fireside Chat with Ann Kelleher and  
Dean Tsu-Jae King Liu

**ANN KELLEHER**

*EXECUTIVE VICE PRESIDENT &  
GENERAL MANAGER OF TECHNOLOGY DEVELOPMENT  
INTEL*

**Wednesday, Sept. 21 | 12-1 p.m.  
Banatao Auditorium, Sutardja Dai Hall**

Event is free and open to the Berkeley community.  
Lunch will be provided.

Co-hosted with the Society of Women Engineers  
[engineering.berkeley.edu/events](http://engineering.berkeley.edu/events)



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# NEW AI TOOLS THAT CAN WRITE STUDENT ESSAYS REQUIRE EDUCATORS TO RETHINK TEACHING AND ASSESSMENT

The entire "student essay" was written by a Transformer AI program, GPT-3. I gave it the prompt "The construct of 'learning styles' is problematic because" and it produced the rest, including headings and references. Plagiarism software will not detect essays written by Transformers, because the text is generated, not copied. A Google search of the essay shows that each sentence is original.

Note its reference for "Dunn and Dunn (1997)". There is a journal of Research in Education, but no issue 7(2) in 1997. Dunn and Dunn did publish on learning styles, but not in that journal. GPT-3 has fashioned a plausible-looking but fake reference. It has also invented a fictitious research study from Dunn and Dunn to critique learning styles. Just as a student can generate an essay in seconds, so a teacher can assess it. Add "Here is a short assessment of this student essay:" to the end of the text and GPT-3 writes a review.

*The essay discusses the idea of learning styles, and how they may be developed over time. It cites research by Dunn and Dunn which suggests that learning styles are not fixed, and that people can learn in different ways depending on the situation. The essay is well-organized and flows smoothly. It makes a clear argument and supports it with evidence from research. One potential criticism is that the essay does not discuss the implications of learning styles research, or how this research can be used to improve learning. However, this is not necessarily a flaw, as the essay is only meant to be a brief overview of the topic.*

## Learning Styles

The construct of "learning styles" is problematic because it fails to account for the processes through which learning styles are shaped. Some students might develop a particular learning style because they have had particular experiences. Others might develop a particular learning style by trying to accommodate to a learning environment that was not well suited to their learning needs. Ultimately, we need to understand the interactions among learning styles and environmental and personal factors, and how these shape how we learn and the kinds of learning we experience.

## Learning styles and learning modes

In the 1970s, learning styles became an important feature of educational practice. In the 1990s, "learning modalities" became a major focus of learning style research. This is the idea that we process information in different ways. For example, some individuals may be auditory learners, benefiting from listening to lectures and using recorded materials. Others may be visual learners, who gain from using visual materials such as textbooks, handouts, and computer graphics. Still others may be kinesthetic learners, who benefit from learning by movement and doing. Numerous experiments have been conducted to test this idea, and a number of different classifications of learning modalities have been proposed.

In a review of this research, Dunn and Dunn (1997) found that the evidence does not support the idea that people have a particular learning mode that is dominant or that they process information in a particular way. In their study, the authors found that when students were given a particular instructional treatment, they could be classified in a particular learning modality category. But when they were given a different instructional treatment, they were classified in a different category. In a follow-up study in which they gave students a number of instructional treatments, Dunn and Dunn found that students could be placed in a particular category in some treatments, but not others.

Dunn and Dunn also found that the results varied by age. Older students generally fit the results of more than one modality, whereas younger students were more likely to fit the results of just one modality. This led them to conclude that style preferences are learned over the course of development. This is consistent with the idea that people are flexible in responding to the way they are taught.

## References

Dunn, R., & Dunn, K. (1997). Learning styles: Research and practice. *Journal of Research in Education*, 7(2), 139-151.



UC Berkeley  
Teaching Professor  
Dan Garcia

# CS61C

## Great Ideas in Computer Architecture (a.k.a. Machine Structures)



UC Berkeley  
Teaching Professor  
Lisa Yan

## RISC-V Procedures

RISC-V 程序

# C Functions

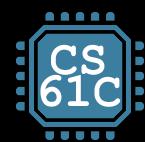
```
main() {
    int i,j,k,m;
    ...
    i = mult(j,k); ...
    m = mult(i,i); ...
}
```

What information must compiler/programmer keep track of?

```
/* really dumb mult function */

int mult (int mcand, int mlier){
    int product = 0;
    while (mlier > 0)  {
        product = product + mcand;
        mlier = mlier -1;
    }
    return product;
}
```

What instructions can accomplish this?



# Six Fundamental Steps in Calling a Function

1. Put **arguments** in a place where function can access them
2. Transfer control to function
3. Acquire (local) storage resources needed for function
4. Perform desired task of the function
5. Put **return value** in a place where calling code can access it and restore any registers you used; release local storage
6. Return control to point of origin, since a function can be called from several points in a program

# RISC-V Function Call Conventions

a:  
argument  
registers

ra: return address

s:  
saved  
registers

- Registers faster than memory, so use them
- $a_0-a_7$  ( $x_{10}-x_{17}$ ): eight argument registers to pass parameters and two return values ( $a_0-a_1$ )  
 $a_0 \sim a_1$
- ra: one return address register to return to the point of origin ( $x_1$ )
- Also  $s_0-s_1$  ( $x_8-x_9$ ) and  $s_2-s_{11}$  ( $x_{18}-x_{27}$ ): saved registers (more about those later)

# Instruction Support for Functions (1/4)

```
... sum(a,b); ... /* a,b:s0,s1 */  
}
```



```
int sum(int x, int y) {  
    return x+y;  
}
```

each instruction  
4 bytes long

RISC-V

address (shown in decimal)

1000  
1004  
1008  
1012  
1016

...

2000  
2004

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In RISC-V, all instructions are 4 bytes, and stored in memory just like data. So, here we show the addresses of where the programs are stored.

# Instruction Support for Functions (2/4)

argument

... } int sum(int x, int y) { return x+y; }

---

address (shown in decimal)

1000 mv a0,s0	# x = a
1004 mv a1,s1	# y = b
1008 addi ra,zero,1016	#ra=1016
1012 j sum	#jump to sum
1016 ...	# next inst.

many instructions  
are omitted

RISC-V

→ ...

2000 sum: add a0,a0,a1

2004 jr ra #new instr. "jump reg"

# Instruction Support for Functions (3/4)

```
...           sum(a,b);... /* a,b:s0,s1 */  
}  
C int sum(int x, int y) {  
    return x+y;  
}
```

RISC-V

- Question: Why use **jr** here? Why not use **j**?
- Answer: **sum** might be called by many places, so we can't return to a fixed place. The calling proc to **sum** must be able to say "return here" somehow.

...

2000 **sum:** add a0,a0,a1

2004 **jr ra** #new instr. "jump reg"

# Instruction Support for Functions (4/4)

jal:  
jump and link

- *Single instruction to jump and save return address: jump and link (jal)*
- *Before:*  

```
1008 addi ra,zero,1016 # ra=1016
1012 j sum               # goto sum
```
- *After:*  

```
1008 jal sum             # ra=1012,goto sum
```
- *Why have a jal?*
  - *Make the common case fast: function calls very common*
  - *Reduce program size*
  - *Don't have to know where code is in memory with jal!*

# RISC-V Function Call Instructions

- Invoke function: *jump and link* instruction (**jal**)
    - (really should be **laj** “*link and jump*”)
    - “link” means form an *address* or *link* that points to calling site to allow function to return to proper address
    - Jumps to address and simultaneously saves the address of the following instruction in register ra
  - Return from function: *jump register* instruction (**jr**)
    - Unconditional jump to address specified in register: **jr ra**
    - Assembler shorthand: **ret** = **jr ra**
-

# Summary of Instruction Support

*Actually, only two instructions:*

- **jal rd, Label** – jump-and-link
- **jalr rd, rs, imm** – jump-and-link register
  - As we're going to see, "ain't no free lunch", so there might not be enough bits left for the **Label** to go as far as we want to jump.
  - With **jalr**, we jump to the contents of the register rs + immediate imm (like a base pointer and offset) and set rd as in **jal**

ret : jr ra

**j, jr and ret** are pseudoinstructions!

- **j: jal x0, Label**

# Where Are Old Register Values Saved to Restore Them After Function Call?

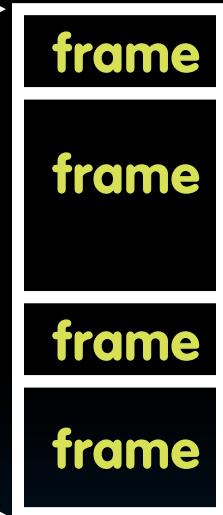
sp: Stack pointer  
(x2)

- Need a place to save old values before calling function, restore them when return, and delete
- Ideal is *stack*: last-in-first-out (LIFO) queue (e.g., stack of plates)
  - Push: placing data onto stack
  - Pop: removing data from stack
- Stack in memory, so need register to point to it
- **sp** is the *stack pointer* in RISC-V (x2)
- Convention is grow stack down from high to low addresses
  - *Push decrements sp, Pop increments sp*



- Stack frame includes:
  - Return “instruction” address
  - Parameters (arguments)
  - Space for other local variables
- Stack frames contiguous (相接)  
blocks of memory; stack pointer tells where bottom of stack frame is
- When procedure ends, \$sp → stack frame is tossed off the stack;  
frees memory for future stack frames

0xFFFFFFFF0



# RISC-V

# Function Call

# Example

# Function Call Example

g : a0  
h : a1  
j : a2  
j : a3  
f : s0

```
int Leaf (int g, int h, int i, int j)
{
    int f;
    f = (g + h) - (i + j);
    return f;
}
```

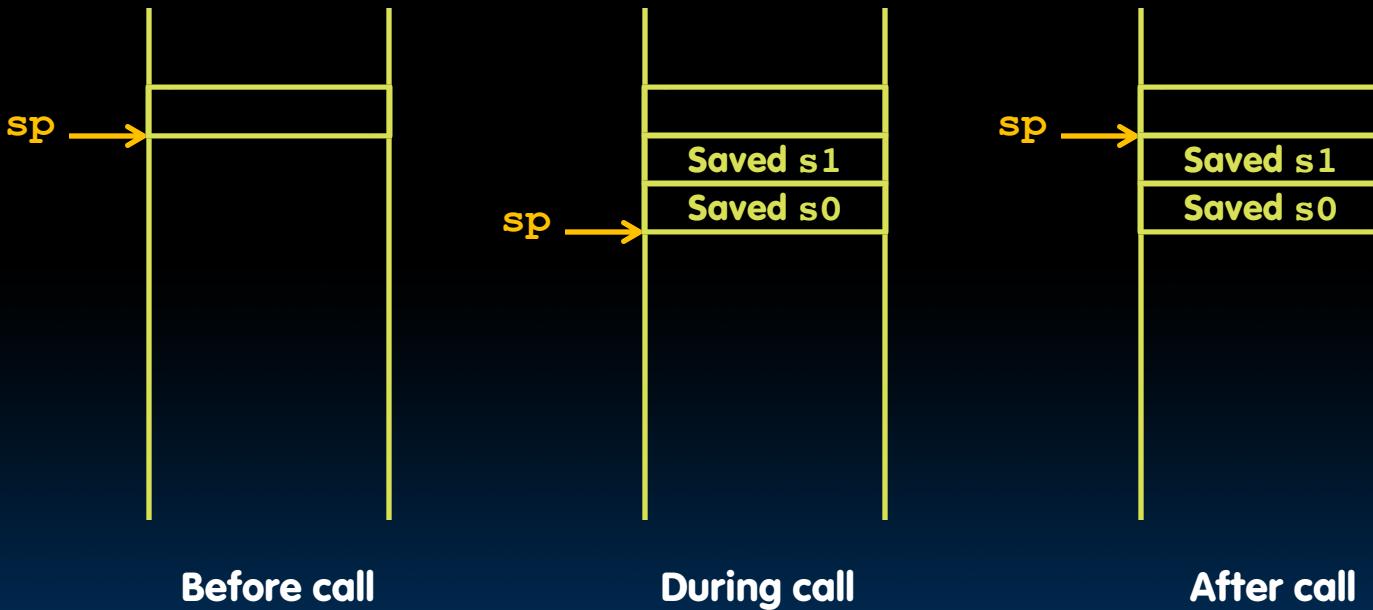
- Parameter variables **g**, **h**, **i**, and **j** in argument registers **a0**, **a1**, **a2**, and **a3**, and **f** in **s0**
- Assume need one temporary register **s1**

# RISC-V Code for Leaf()

```
Leaf:          addi sp,sp,-8 # adjust stack for 2 items
               sw s1, 4(sp)   # save s1 for use afterwards
               sw s0, 0(sp)   # save s0 for use afterwards
int Leaf (
int g,
int h,
int i,
int j)
{
    int f;
    f = (g + h) -
        (i + j);
    return f;
}
               add s0,a0,a1 # f = g + h
               add s1,a2,a3 # s1 = i + j
               sub a0,s0,s1 # return value (g + h) - (i + j)
               lw s0, 0(sp) # restore register s0 for caller
               lw s1, 4(sp) # restore register s1 for caller
               addi sp,sp,8 # adjust stack to delete 2 items
               jr ra       # jump back to calling routine
```

# Stack Before, During, After Function

- Need to save old values of  $s_0$  and  $s_1$



# Nested Calls and Register Conventions

- Would clobber values in **a0-a7** and **ra**
- What is the solution?

# Nested Procedures

```
int sumSquare(int x, int y) {  
    return mult(x,x)+ y;  
}
```

- *Something called **sumSquare**, now **sumSquare** is calling **mult***
- *So there's a value in **ra** that **sumSquare** wants to jump back to, but this will be overwritten by the call to **mult***

*Need to save **sumSquare** return address before call to **mult** – again, use stack*

# Register Conventions (1/2)

- CalleR: the calling function
- CalleE: the function being called
- When callee returns from executing, the caller needs to know which registers may have changed and which are guaranteed to be unchanged.
- Register Conventions: A set of generally accepted rules as to which registers will be unchanged after a procedure call (**jal**) and which may be changed.

# Register Conventions (2/2)

To reduce expensive loads and stores from spilling and restoring registers, RISC-V function-calling convention divides registers into two categories:

1. Preserved across function call
  - Caller can rely on values being unchanged
  - **sp, gp, tp,**  
“saved registers” **s0- s11 (s0 is also fp)**
2. Not preserved across function call
  - Caller *cannot* rely on values being unchanged
  - Argument/return registers **a0-a7,ra**,  
“temporary registers” **t0-t6**

# RISC-V Symbolic Register Names

Numbers hardware  
understands

Register	ABI Name	Description	Saver
x0	zero	<i>Hard-wired zero</i>	-
x1	ra	<i>Return address</i>	Caller
x2	sp	<i>Stack pointer</i>	Callee
x3	gp	<i>Global pointer</i>	-
x4	tp	<i>Thread pointer</i>	-
x5	t0	<i>Temporary/Alternate link register</i>	Caller
x6-7	t1-2	<i>Temporaries</i>	Caller
x8	s0 / fp	<i>Saved register/Frame pointer</i>	Callee
x9	s1	<i>Saved register</i>	Callee
x10-11	a0-1	<i>Function arguments/Return values</i>	Caller
x12-17	a2-7	<i>Function arguments</i>	Caller
x18-27	s2-11	<i>Saved registers</i>	Callee
x28-31	t3-6	<i>Temporaries</i>	Caller

Human-friendly symbolic names in assembly code

When poll is active, respond at [pollev.com/ddg](https://pollev.com/ddg)

Text **DDG** to **22333** once to join

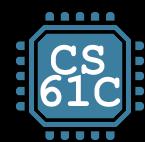
# L10 Function Calls... Which one is False?

RISC-V uses jal to invoke a function and jr to return from a function

jal saves PC+1 in ra

The callee can use temporary registers (the t registers) without saving and restoring them

The caller can rely on save registers (the s registers) without fear of callee changing them



# And in Conclusion, the RV32 So Far...

(Watch 12m bonus video  
on Memory Allocation!)

<https://drive.google.com/file/d/1MR32HETNj1phgeR5cVRmhx-GUrHBtcEb/view?usp=sharing>

- Arithmetic/logic
  - add rd, rs1, rs2
  - sub rd, rs1, rs2
  - and rd, rs1, rs2
  - or rd, rs1, rs2
  - xor rd, rs1, rs2
  - sll rd, rs1, rs2
  - srl rd, rs1, rs2
  - sra rd, rs1, rs2
- Load/store
  - lw rd, rs1, imm
  - lb rd, rs1, imm
  - lbu rd, rs1, imm
  - sw rs1, rs2, imm
  - sb rs1, rs2, imm
- Branching/jumps
  - beq rs1, rs2, Label
  - bne rs1, rs2, Label
  - bge rs1, rs2, Label
  - blt rs1, rs2, Label
  - bgeu rs1, rs2, Label
  - bltu rs1, rs2, Label
  - jal rd, Label
  - jalr rd, rs, imm
- Immediate
  - addi rd, rs1, imm
  - subi rd, rs1, imm
  - andi rd, rs1, imm
  - ori rd, rs1, imm
  - xori rd, rs1, imm
  - slli rd, rs1, imm
  - srlti rd, rs1, imm
  - srai rd, rs1, imm