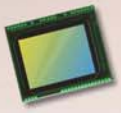

datasheet

PRELIMINARY SPECIFICATION

1/3.06" color CMOS 13 megapixel (4224 x 3136)
PureCel®Plus image sensor

OV13855

color CMOS 13 megapixel (4224 x 3136) PureCel®Plus image sensor

datasheet (COB)
PRELIMINARY SPECIFICATION

version 1.21
june 2016

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- smartphones and feature phones
- PC multimedia
- tablets
- wearables

ordering information

- **OV13855-GA5A-Z** (color, chip probing, 150 µm backgrinding, reconstructed wafer)

features

- 1.12 µm x 1.12 µm pixel
- optical size of 1/3.06"
- 33.15° CRA
- support for PDAF
- 13MP at 30 fps
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- supports images sizes: 13Mp (4224 x 3136), 10Mp (4224 x 2376), 3Mp (2112 x 1568), and more
- 3.3k bits of embedded one-time programmable (OTP) memory for customer use
- support for output formats: 10-bit RGB RAW
- interlaced row HDR output
- two-wire serial bus control (SCCB)
- MIPI serial output interface (1-, 2-lane, or 4-lane)
- two on-chip phase lock loops (PLLs)
- 2x binning support
- image quality controls: defect pixel correction, automatic black level calibration, and lens shading correction
- built-in temperature sensor
- suitable for module size of 8.5 mm x 8.5 mm x <5mm

key specifications (typical)

- **active array size:** 4256 x 3168
- **power supply:**
  - analog: 2.7 to 3.0V (2.8V nominal)
  - core: 1.14 to 1.26V (1.2V nominal)
  - I/O: 1.7 to 1.9V (1.8V nominal)
- **power requirements:**
  - active: 233mW (based on ISP ON)
  - standby: 1mW
  - XSHUTDN: <10µA
- **temperature range:**
  - operating: -30°C to +85°C junction temperature (see **table 7-2**)
  - stable image: 0°C to +60°C junction temperature (see **table 7-2**)
- **output interface:** 4-lane MIPI serial output
- **output formats:** 10-bit RGB RAW
- **lens size:** 1/3.06"
- **input clock frequency:** 6~27 MHz
- **lens chief ray angle:** 33.15° non-linear (see **figure 9-2**)
- **maximum image transfer rate:**
  - 13MP (4224 x 3136): 30 fps
  - 10MP (4224 x 2376): 30 fps
  - 3MP (2112 x 1568): 60 fps
- **sensitivity:** TBD
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **minimum exposure:** 4-row
- **maximum exposure:** VTS-8
- **pixel size:** 1.12 µm x 1.12 µm
- **dark current:** TBD
- **image area:** 4749.696 µm x 3535.488 µm
- **die dimensions:** 5868 µm x 4950 µm (COB), 5918 µm x 5000 µm (RW) (see **section 8** for details)

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV13855 image sensor. The die information is shown in **section 8**.

table 1-1 signal descriptions (sheet 1 of 2)

pad number	signal name	pad type	description
1	DVDD	power	power for digital circuit
2	DOGND	ground	ground for I/O
3	AGND	ground	ground for analog circuit
4	AVDD	power	power for analog circuit
5	**SID**	input	SCCB address selection 0: SCCB address is 0x6C 1: SCCB address is 0x20
6	**FSIN**	I/O	frame sync input
7	**SDA**	I/O	SCCB data
8	**SCL**	input	SCCB input clock
9	**XSHUTDN**	input	reset and power down (active low)
10	**TM**	input	test mode (active high with internal pull down resistor)
11	DOVDD	power	power for I/O circuit
12	**EXTCLK**	input	system input clock / scan clock input
13	DOGND	ground	ground for I/O circuit
14	DVDD	power	power for digital circuit
15	**VSYNC**	I/O	video output vertical signal
16	DOGND	ground	ground for I/O circuit
17	DVDD	power	power for digital circuit
18	DVDD	power	power for digital circuit
19	DOGND	ground	ground for I/O circuit
20	AVDD	power	power for analog circuit
21	AGND	ground	ground for analog circuit
22	ATEST	analog I/O	analog test I/O
23	AVDD	power	analog power
24	AGND	ground	analog ground

table 1-1 signal descriptions (sheet 2 of 2)

pad number	signal name	pad type	description
25	VH	input	reference
26	VN1	input	reference
27	VN2	input	reference
28	DVDD	power	power for digital circuit
29	DOGND	ground	ground for I/O circuit
30	**MDP2**	I/O	MIPI TX data lane 2 positive output
31	**MDN2**	I/O	MIPI TX data lane 2 negative output
32	**MDP0**	I/O	MIPI TX data lane 0 positive output
33	**MDN0**	I/O	MIPI TX data lane 0 negative output
34	EGND	ground	ground for MIPI TX circuit
35	PVDD	power	PLL analog power
36	EVDD	power	power for MIPI TX circuit
37	**MCP**	I/O	MIPI TX clock lane positive output
38	**MCN**	I/O	MIPI TX clock lane negative output
39	EGND	ground	ground for MIPI TX circuit
40	**MDP1**	I/O	MIPI TX data lane 1 positive output
41	**MDN1**	I/O	MIPI TX data lane 1 negative output
42	EVDD	power	power for MIPI TX circuit
43	**MDP3**	I/O	MIPI TX data lane 3 positive output
44	**MDN3**	I/O	MIPI TX data lane 3 negative output
45	DOVDD	power	power for I/O circuit
46	DVDD	power	power for digital circuit
47	DVDD	power	power for digital circuit
48	DOGND	ground	ground for I/O circuit
49	DOGND	ground	ground for I/O circuit

table 1-2 configuration under various conditions

pad	signal name	XSHUTDN[a]	after XSHUTDN release[b]	software standby
5	SID	input	input	input
6	FSIN	high-z	high-z	high-z (configurable)
7	SDA	open drain	I/O	I/O
8	SCL	input	input	input
9	XSHUTDN	input	input	input
10	TM	input	input	input
12	EXTCLK	input	input	input
15	VSYNC	high-z	high-z	high-z (configurable)
30	MDP2	high-z	high	high by default (configurable)
31	MDN2	high-z	high	high by default (configurable)
32	MDP0	high-z	high	high by default (configurable)
33	MDN0	high-z	high	high by default (configurable)
37	MCP	high-z	high	high by default (configurable)
38	MCN	high-z	high	high by default (configurable)
40	MDP1	high-z	high	high by default (configurable)
41	MDN1	high-z	high	high by default (configurable)
43	MDP3	high-z	high	high by default (configurable)
44	MDN3	high-z	high	high by default (configurable)

a. XSHUTDN = 0

b. XSHUTDN from 0 to 1

figure 1-1 pad diagram

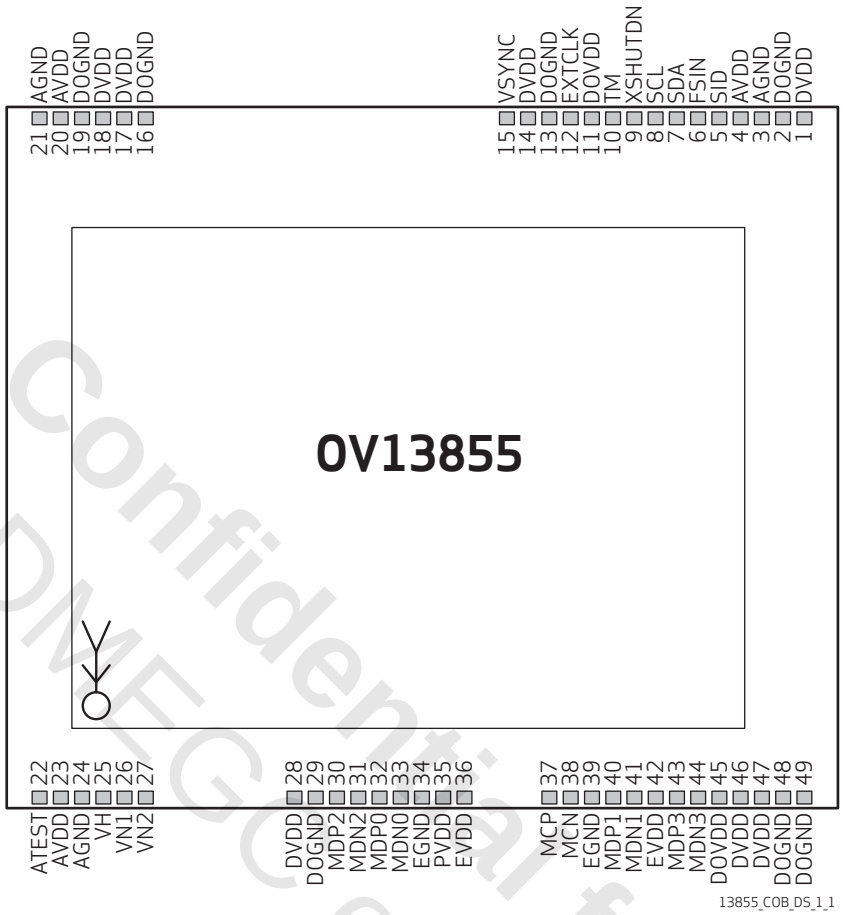


table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

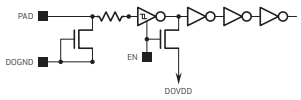
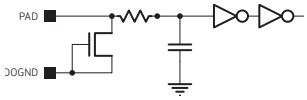
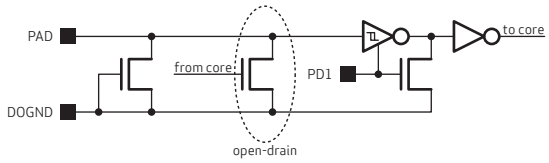
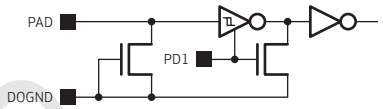
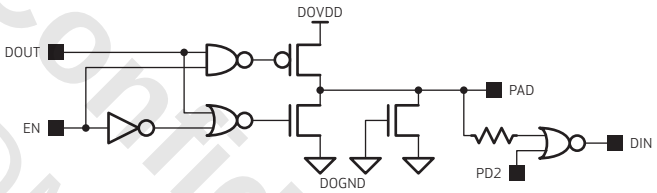
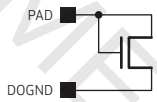
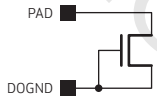
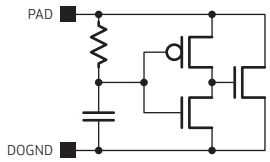
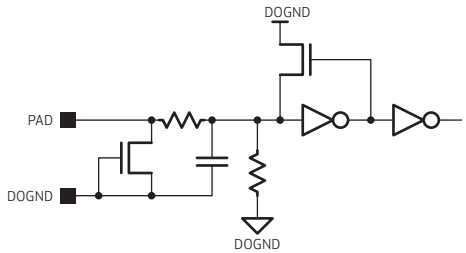
symbol	equivalent circuit
EXTCLK	
SID	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
SDA	
SCL	
FSIN/VSYNC	
VN, VN1, VN2	
MDP3, MDP2, MDP1, MDP0, MDN3, MDN2, MDN1, MDN0, MCP, MCN, EGND, AGND, DOGND, VH	
AVDD, EVDD, DVDD, DOVDD, PVDD	
XSHUTDN, TM	

2 system level description

2.1 overview

The OV13855 RAW RGB PureCel®Plus image sensor is a high performance, 1/3.06-inch, 13 megapixel CMOS image sensor that delivers 4224x3136 at 30 fps. It provides full-frame, sub-sampled, and windowed 10-bit MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV13855 has a 13 megapixel image array capable of operating at up to 30 frames per second (fps) in 10-bit resolution with complete user control over image quality, formatting and output data transfer. Some image processing functions, such as defective pixel canceling, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV13855 includes 8k bits (1024 bytes) of one-time programmable (OTP) memory (252 bytes are reserved for OmniVision and 772 bytes are reserved for customers). The OV13855 has a MIPI interface of up to four lanes.

2.2 architecture

The OV13855 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV13855 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OV13855 block diagram

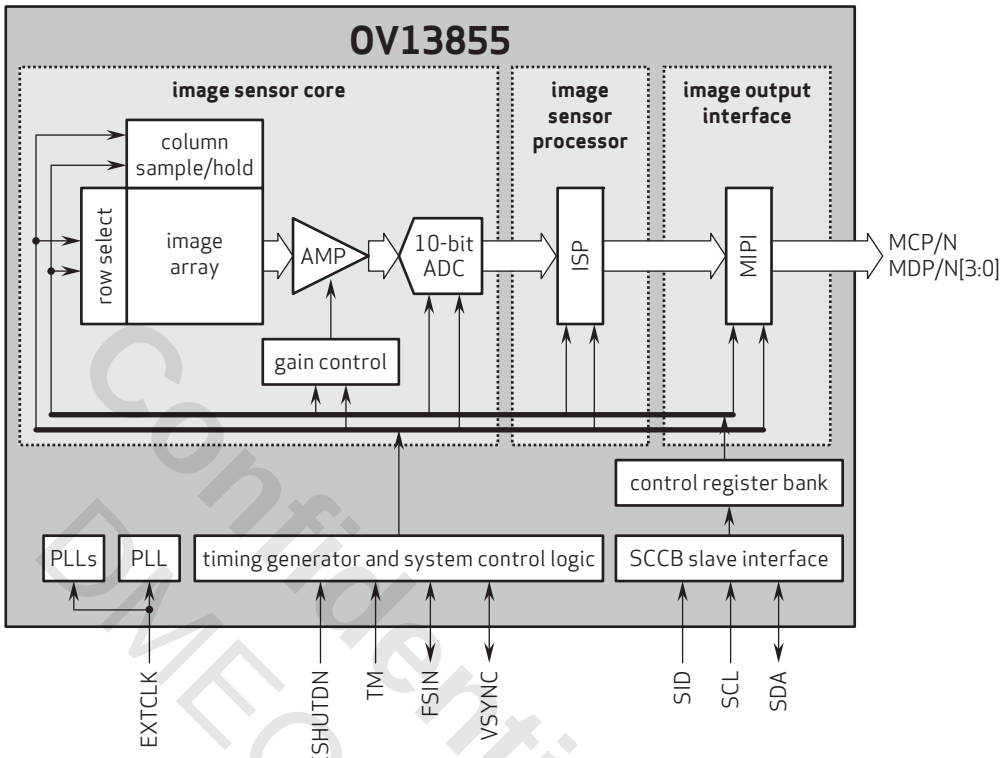
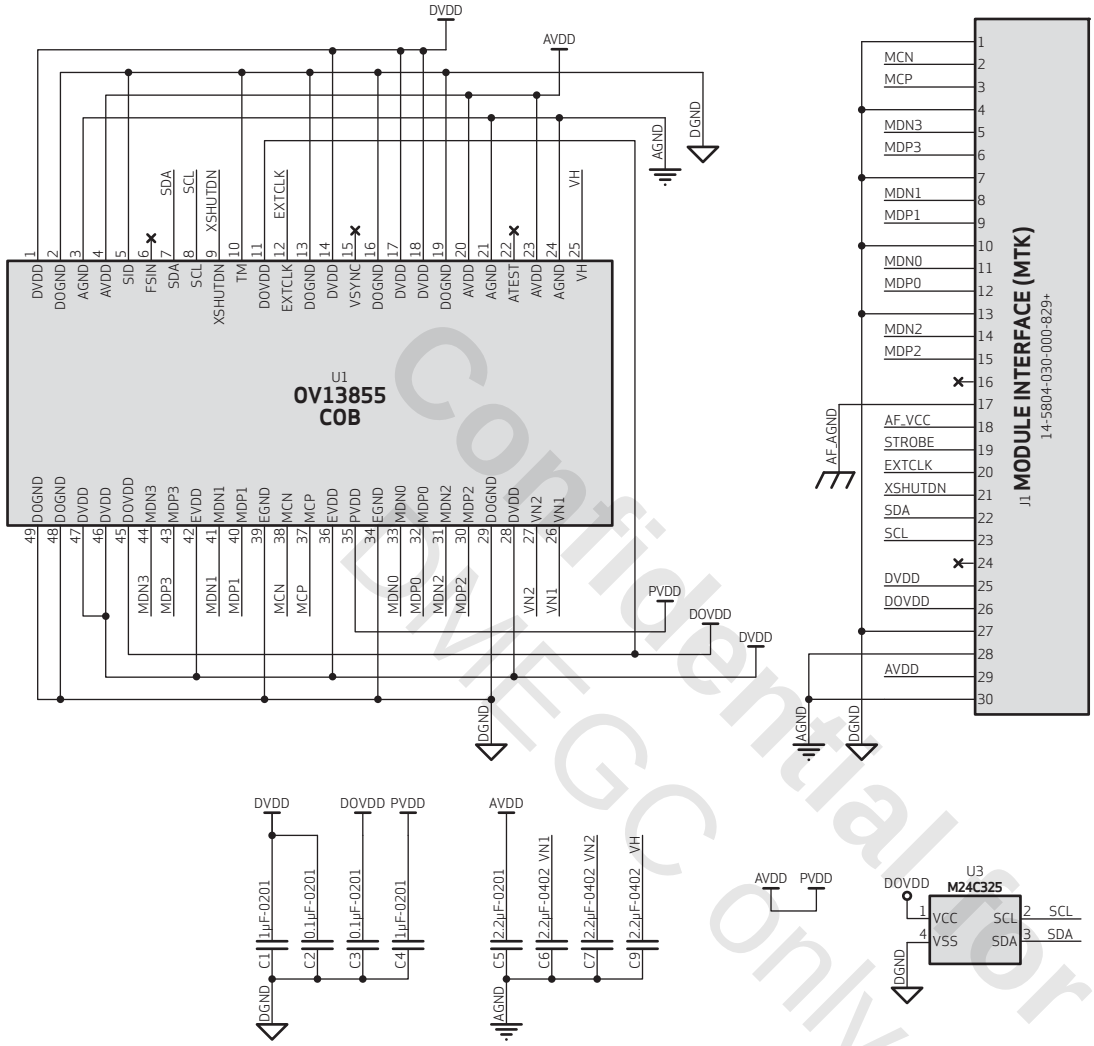


figure 2-2 OV13855 reference schematic



note 1 XSHUTDOWN(XSHUTDN) should be connected to DOVDD outside of module if unused.

note 2 for other pins, such as VSYNC, FSIN, if unused, can be left floating

note 3 AVDD is 2.7-3.0V for sensor analog power (clean).

note 4 DOVDD is 1.62-1.98V for sensor digital IO power (clean).

note 5 DVDD is 1.14-1.26V for sensor digital core power (clear).

note 6 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).

note 7 capacitors should be close to the related sensor pins.

note 8 MCP and MCN are MIPI clock lane positive and negative output. MDPx and MDNx are MIPI data lane positive and negative output.

note 9 traces of MCP, MCN, MDPx, and MDNx should have the same or similar length. differential impedance of the clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 10 AF_VCC and AF_AGND is the power supply for auto focus related circuitary. AF_VCC can be 2.8-3.3V

13855_COB_DS_2_2

2.3 format and frame

The OV13855 supports RAW RGB output with 1/2/4-lane MIPI interface.

table 2-1 format and frame rate

format	resolution	frame rate	methodology	10-bit output MIPI data rate
13.2 Mpixel	4224 x 3136	30 fps	full resolution (4:3)	4-lane @ 1080 Mbps/lane
10 Mpixel	4224 x 2376	30 fps	crop (16:9)	4-lane @ 1080 Mbps/lane
3.3 Mpixel	2112 x 1568	60 fps	Bin2/Skip2	4-lane @ 540 Mbps/lane

2.4 I/O control

The OV13855 can configure its I/O pads as an input or output. For the output signal, it follows one of two paths: either from the data path or from register control.

table 2-2 I/O control registers

function	register	description
output drive capability control	0x3663	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
FSIN I/O control	0x3002	Bit[7]: FSIN output enable 0: input 1: output
VSYNC I/O control	0x3002	Bit[6]: VSYNC output enable 0: input 1: output
FSIN output select	0x3010	Bit[7]: enable FSIN as GPIO controlled by register
VSYNC output select	0x3010	Bit[6]: enable VSYNC as GPIO controlled by register
FSIN output value	0x3008	Bit[7]: register control FSIN output
VSYNC output value	0x3008	Bit[6]: register control VSYNC output

2.5 MIPI interface

The OV13855 supports a MIPI interface of up to 4-lanes. The MIPI interface can be configured for 1/2/4-lane and each lane is capable of a data transfer rate of up to 1.2 Gbps.

2.6 power management

Based on the system power configuration (XSHUTDN), the power up sequence will be different. OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.6.1 power up sequence

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDN by GPIO.

Whether or not XSHUTDN is controlled by GPIO, XSHUTDN rising cannot occur before AVDD, DVDD and DOVDD.

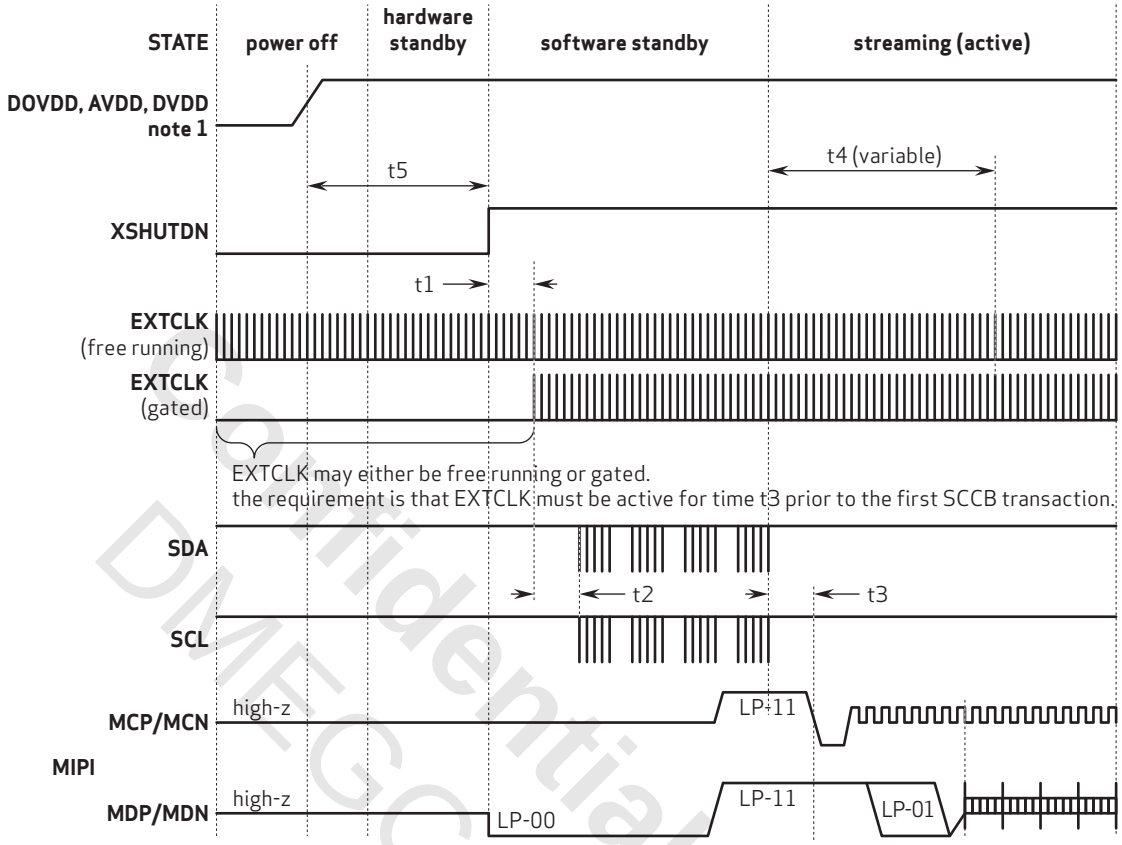
table 2-3 power up sequence

XSHUTDN	power up sequence requirement
GPIO	Refer to **figure 2-3** 1. DOVDD, AVDD, and DVDD can rise in any order 2. XSHUTDN rising must occur after AVDD, DOVDD and DVDD are stable

table 2-4 power up sequence timing constraints

constraint	label	min	max	unit
XSHUTDN rising – system ready	t1	5		ms
minimum number of EXTCLK cycles prior to the first SCCB transaction	t2	8192		EXTCLK cycles
PLL start up/lock time	t3		0.2	ms
entering streaming mode – first frame start sequence (variable)	t4	delay related to output frame rate and line timing		lines
AVDD, DOVDD or DVDD, whichever is last – XSHUTDN rising	t5	0	∞	ns

figure 2-3 power up sequence



note 1 DOVDD, AVDD and DVDD may rise in any order

13855_13355_13858_DS_2_3

2.6.2 power down sequence

Pull XSHUTDN low to set the sensor into power down mode. The digital and analog supply voltages can be cut off in any order (e.g., DOVDD, DVDD, then AVDD or AVDD, DVDD, then DOVDD). Similar to the power up sequence, the EXTCLK input clock may be either gated or continuous. To avoid bad frames from MIPI, OmniVision recommends setting the sensor into sleep mode in inter frame first before sending the sensor into power down mode by setting register 0x3021[6:5]=2'b00 and register 0x0100 = 0x00.

table 2-5 power down sequence

XSHUTDN	power down sequence requirement
GPIO	Refer to **figure 2-5** 1. software standby recommended 2. pull XSHUTDN low for minimum power consumption 3. pull AVDD, DVDD, and DOVDD low in any order

table 2-6 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of EXTCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDN falling	t2	512		EXTCLK cycles
XSHUTDN falling – AVDD, DVDD or DOVDD falling whichever is first	t3	0.0		ns

figure 2-4 software standby sequence

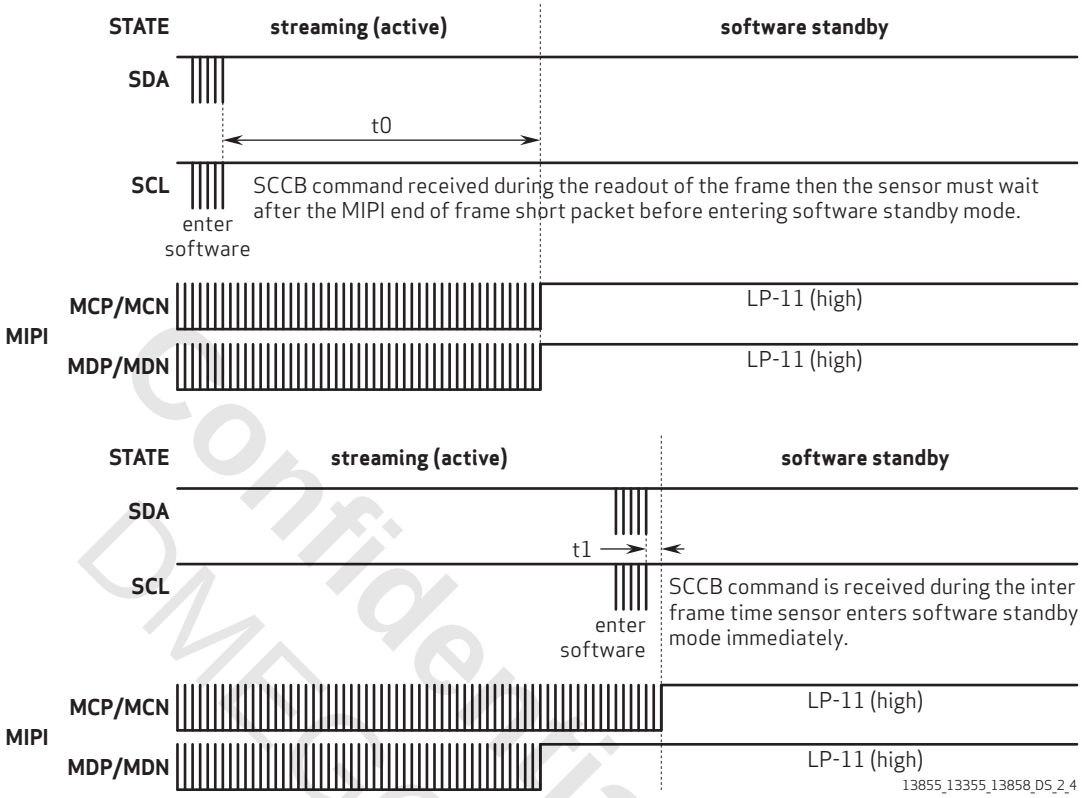
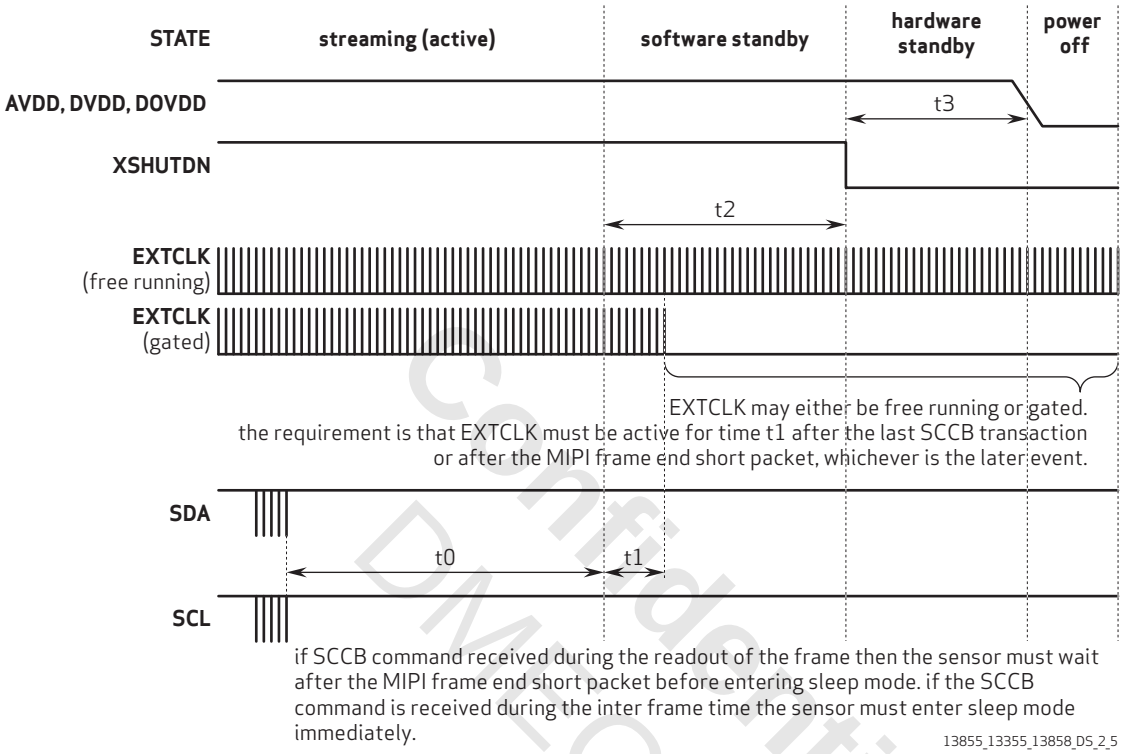


figure 2-5 power down sequence



2.7 reset

The whole chip will be reset during power up. Manually applying a hardware reset (XSHUTDN=0) upon power up is recommended even though the on-chip power up reset is included. The hardware reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 2 ms.

2.7.1 power ON reset

The power on reset can be controlled from an external pin. Additionally, in this sensor, a power on reset is generated after the core power becomes stable.

2.7.2 software reset

When register 0x0103[0] is configured as 1, all registers are reset to default value.

2.8 standby mode

Two suspend modes are available for the OV13855:

- hardware standby
- software standby

2.8.1 hardware standby

If XSHUTDN is tied to low, it will initiate hardware standby mode. In this mode, the total power consumption will be less than 100 µW.

2.8.2 software standby

Executing a software power down (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During the resume state, all the registers are restored to their original values.

table 2-7 hardware and standby description

mode	description
hardware standby with XSHUTDN	1. enabled by pulling XSHUTDN low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

The OV13855 has two on-chip PLLs which generate the system clock from a 6~27MHz input clock. A programmable clock divider is provided to generate different frequencies for the system. PLL settings can only be changed during sensor software standby mode (0x0100 = 0).

2.9.1 PLL1

The PLL1 generates a default 135 MHz pixel clock and 1080 MHz MIPI serial clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz.

2.9.2 PLL2

The PLL2 generates a default 108 MHz system clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. PLL2 is only used for sensor timing and should not be adjusted by the customer.

figure 2-6 clock scheme

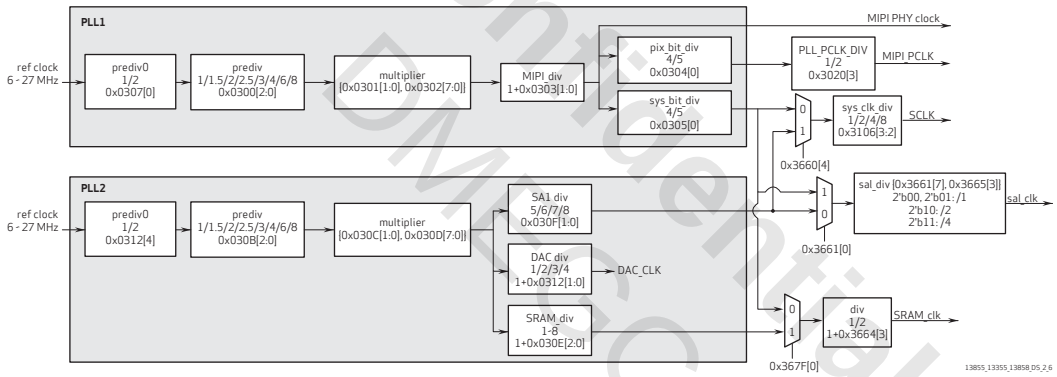


table 2-8 PLL control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x02	RW	Bit[2:0]: pll1_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL_CTRL_1	0x00	RW	Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x5A	RW	Bit[7:0]: pll1_multiplier[7:0]

table 2-8 PLL control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x0303	PLL_CTRL_3	0x00	RW	Bit[1:0]: pll1_divpx 00: /1 01: /2 10: /3 11: /4
0x0304	PLL_CTRL_4	0x00	RW	Bit[0]: pll1_pix_bitdiv 0: /4 1: /5
0x0305	PLL_CTRL_5	0x01	RW	Bit[0]: pll1_sys_bitdiv 0: /4 1: /5
0x0307	PLL_CTRL_7	0x00	RW	Bit[0]: pll1_predivp 0: /1 1: /2
0x030B	PLL_CTRL_B	0x00	RW	Bit[2:0]: pll2_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x030C	PLL_CTRL_C	0x00	RW	Bit[1:0]: pll2_r_divp[9:8]
0x030D	PLL_CTRL_D	0x36	RW	Bit[7:0]: pll2_r_divp[7:0]
0x030E	PLL_CTRL_E	0x05	RW	Bit[2:0]: pll2_sramdiv Control bit value = bit[2:0] + 1
0x030F	PLL_CTRL_F	0x01	RW	Bit[1:0]: pll2_sa1_div 00: /5 01: /6 10: /7 11: /8
0x0312	PLL_CTRL_12	0x01	RW	Bit[4]: pll2_predivp 0: /1 1: /2 Bit[1:0]: pll2_r_divdac 00: /1 01: /2 10: /3 11: /4
0x3020	CLOCK SEL	0x9B	RW	Bit[3]: pclk_sel 0: /1 1: /2

table 2-8 PLL control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3106	SRB HOST INPUT DIS	0x15	RW	Bit[3:2]: sys_clk_div 00: /1 01: /2 10: /4 11: /8

table 2-9 sample PLL configuration

control name	address	input clock (EXTCLK)	
		24 MHz	6 MHz
PLL1_PREDIVP	0x0307[0]	0x0	0x0
PLL1_PREDIV	0x0300[2:0]	0x2	0x0
PLL1_MULTIPLIER	{0x0301[1:0], 0x0302[7:0]}	0x5A	0xB4
PLL1_DIV_MIPI	0x0303[1:0]	0x0	0x0
PLL1_PIX_BITDIV	0x0304[0]	0x0	0x0
PLL1_SYS_BITDIV	0x0305[0]	0x1	0x1
PLL2_PREDIVP	0x3012[4]	0x0	0x0
PLL2_PREDIV	0x030B[2:0]	0x0	0x0
PLL2_MULTIPLIER	{0x030C[1:0], 0x030D[7:0]}	0x36	0x36
PLL2_SA1_DIV	0x030F[1:0]	0x1	0x1
PLL2_SRAMDIV	0x030E[2:0]	0x5	0x5
PLL_PCLK_DIV	0x3020[3]	–	–
SYS_CLK_DIV	0x3106[3:2]	–	–
SCLK	–	108 MHz	108 MHz
PHY_SCLK	–	1080 MHz	1080 MHz
MIPI_PCLK	–	135 MHz	135 MHz

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV13855, the SCCB ID is controlled by the SID pin and can be programmed. If SID is low, the sensor's SCCB address comes from register 0x3003 which has a default value of 0x6C for write (0x6D for read). If SID is high, the sensor's SCCB address comes from register 0x3004 which has a default value of 0x20 for write (0x21 for read). There is an alternative ID in register 0x3005, which has a default value of 0x42 The alternative ID works on both SID high or low.

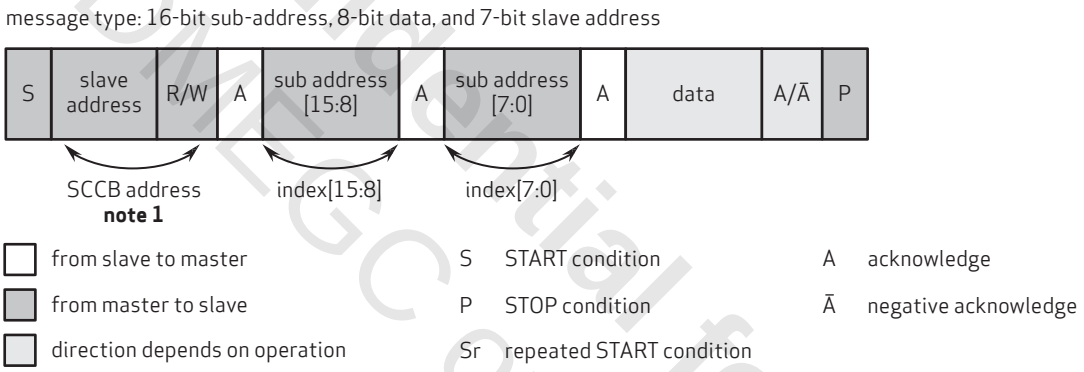
2.10.1 data transfer protocol

The data transfer of the OV13855 follows the SCCB protocol.

2.10.2 message format

The OV13855 supports the message format shown in **figure 2-7**. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-10**.

figure 2-7 message type



note 1 slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

13855_13355_13858_DS_2_7

2.10.3 read / write operation

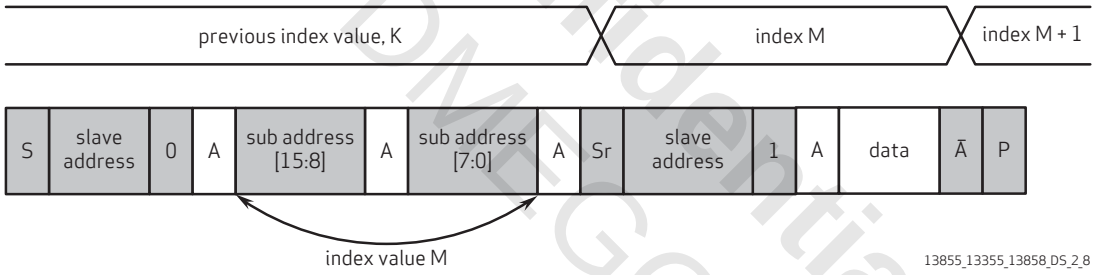
The OV13855 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

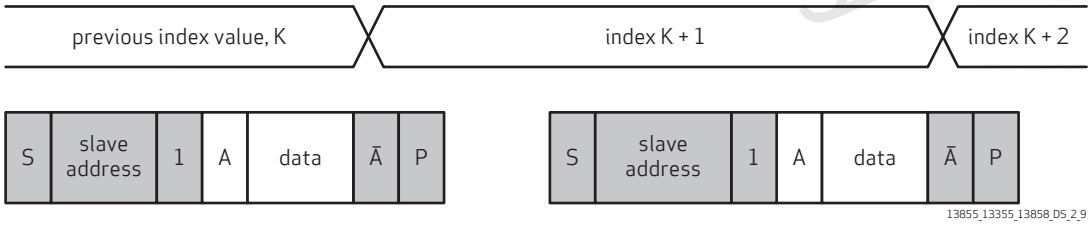
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB single read from random location



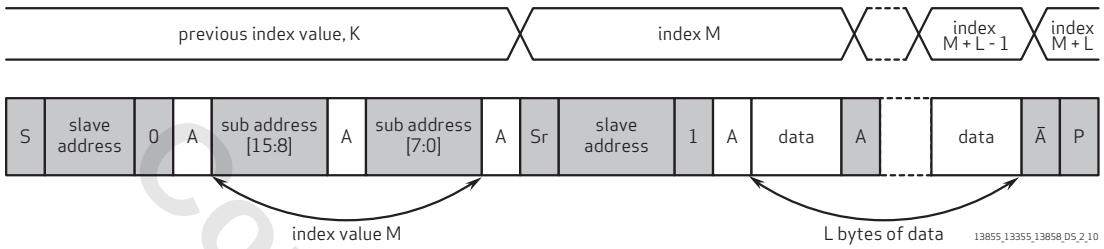
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from current location



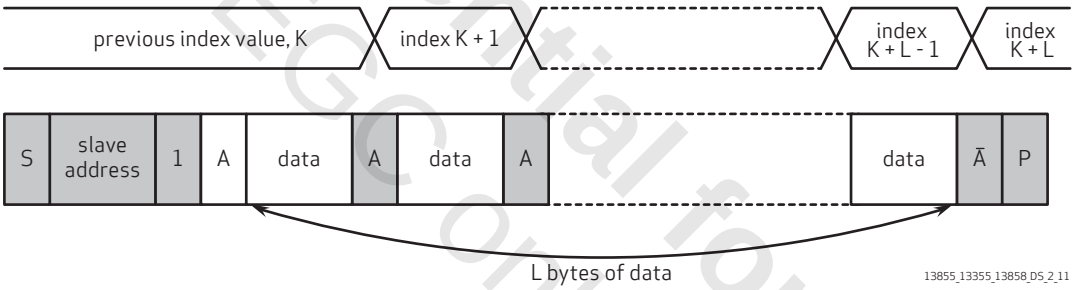
The sequential read from a random location is illustrated in **figure 2-10**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-10 SCCB sequential read from random location



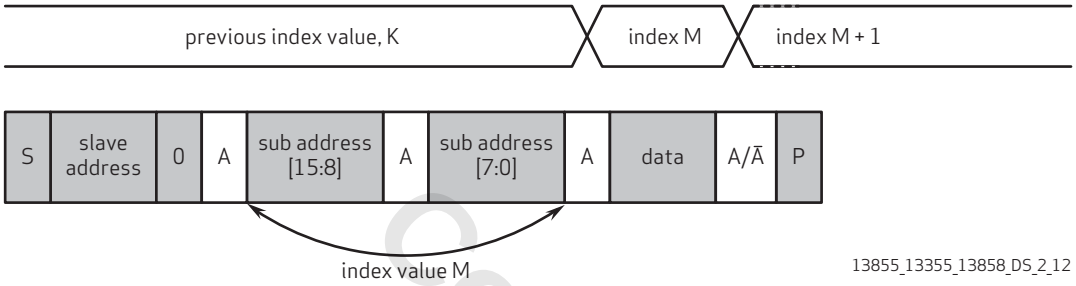
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation, as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from current location



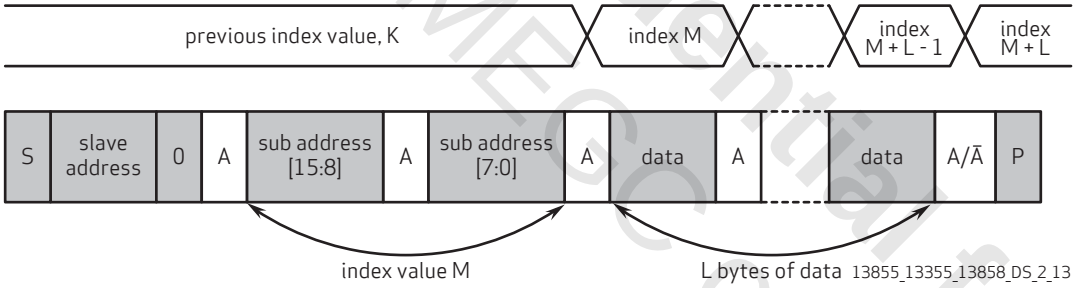
The write operation to a random location is illustrated in **figure 2-12**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-12 SCCB single write to random location



The sequential write is illustrated in **figure 2-13**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-13 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-14 SCCB interface timing

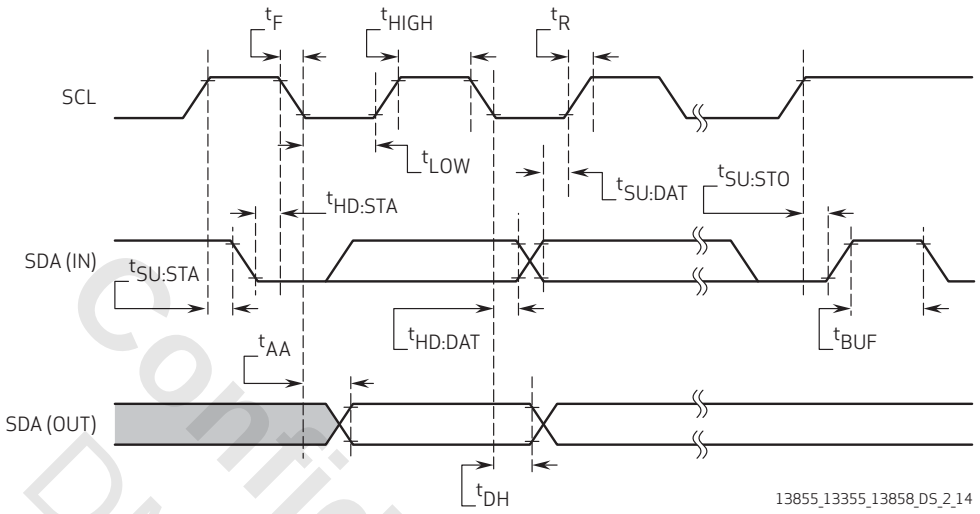


table 2-10 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

2.11 group write

Group write is supported in order to update a group of registers (except 0x31xx) in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary. If more than one group is going to be launched, the second group cannot be recorded or launched before the first group has effectively been launched.

The OV13855 supports up to four groups. These groups share 512 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-11 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	When 0x320B[7] = 1 Bit[6:5]: Group number that group will switch back to after launch group 0 in auto switch mode Bit[4:0]: grp0_frms Number of frames stay in group 0 before auto switch to group defined by 0x3209[6:5] When 0x320B[2] = 1 Bit[7:0]: Number of frames stay in group 0 before auto switch to group defined by 0x320B[1:0]
0x320A	GRP1_PERIOD	0x00	RW	Bit[7:0]: Number of frames stay in second group in context switch mode defined by 0x320B[1:0] (works only when 0x320B[2] = 1)

table 2-11 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320B	GRP_SWCTRL	0x11	RW	Bit[7]: auto_sw Auto launch mode enable Bit[6:5]: Not used Bit[4]: frame_cnt_trig 0: EOF as frame count trigger 1: Group write as frame count trigger Bit[3]: group_switch_repeat Bit[2]: context_en Contact switch mode enable Bit[1:0]: Second group selection

2.11.1 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with the control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.11.2 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM, and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described in sections **section 2.11.2.1** to **section 2.11.2.5**.

2.11.2.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting the register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is a setting example.

```
6C  3208  E0    quick launch group 0
```

2.11.2.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to the register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking, thus delayed. Below is a setting example.

```
6C  3208  A1    delay launch group 1
```

2.11.2.3 launch mode 3: quick auto launch

Quick auto launch works like mode 1, the difference is it will return to a specified group automatically. This is controlled by register 0x3209. Bit[6:5] controls which group to return and Bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is bit[7] of register 0x320B. The operation can be better understood with an example setting:

```
20 3209 44 ;Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
20 320B 80 ; auto launch on
20 3208 E0 ;quick launch group 0.
```

In this example, sensor will quick launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.11.2.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 during the delay launch operation and like mode 3 during the return operation.

The operation can be better understood with an example setting:

```
20 3209 44 ;bit[6:5]: 2, return to group 2, Bit [4:0]: 4: stay 4 frames
20 320B 80 ; auto launch on
20 3208 A0 ;delay launch group 0.
```

In this example, sensor will delay launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.11.2.5 launch mode 5: repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (could be either one of group 1-3, which is specified by register 0x320B[1:0]). The register 0x3209 defines how many frames to stay at group 0 and register 0x320A defines how many frames to stay at the second group.

The operation can be better understood with an example setting:

```
20 3209 02 ; bit[7:0]: 2, stay 2 frames in group 0
20 320A 03 ; bit[7]: 3, stay 3 frames in the second group
20 320B 0E ; bit[3:2]: 3, repeat launch on, Bit[1:0]: 2,
second group select: group 2
20 3208 A0 ; always use a0 for repeat launch
```

In this example, sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, group 2 for 3 frames and repeating.

3 block level description

3.1 pixel array structure

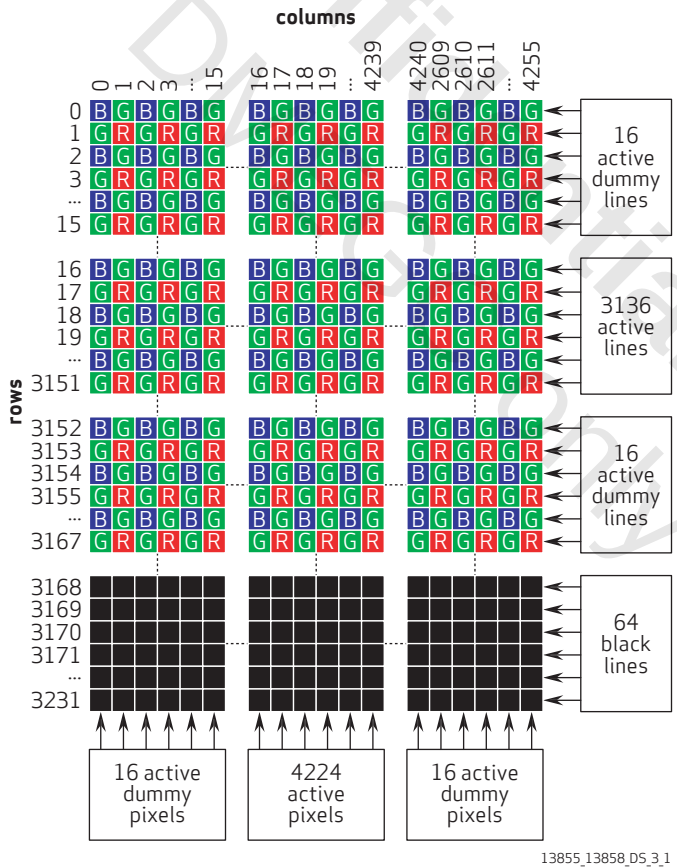
The OV13855 sensor has an image array of 4256 columns by 3232 rows (13,755,392 pixels including 64 black lines). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 13,755,392 pixels, 13,246,464 (4224x3136) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

Exposure time is controlled by registers {0x3500, 0x3501, 0x3502}. Maximum exposure time is VTS-8 and minimum exposure time is 4-row.

figure 3-1 sensor array region color filter layout



3.2 subsampling

The OV13855 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV13855 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of four adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

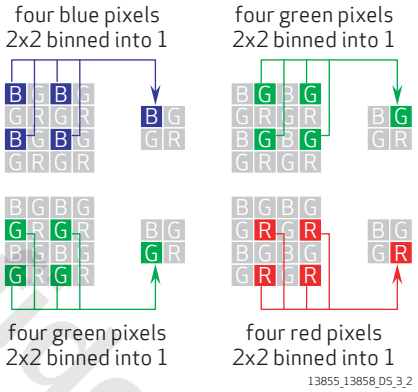


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0x80	RW	Bit[1]: hbin2_o Bit[0]: vbinf_o
0x3814	X_ODD_INC	0x01	RW	Bit[4:0]: Horizontal increase number at odd pixel
0x3815	X_EVEN_INC	0x01	RW	Bit[4:0]: Horizontal increase number at even pixel
0x382A	Y_ODD_INC	0x01	RW	Bit[4:0]: Vertical increase number at odd row
0x382B	Y_EVEN_INC	0x01	RW	Bit[4:0]: Vertical increase number at even row
0x4501	HBIN_CTRL	0x40	RW	Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Debug mode 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Debug mode 10: Select the first pixel 11: Select the last pixel

3.3 alternate row HDR

The OV13855 sensor supports 2-exposure HDR mode. The HDR control bits are 0x3821[1].

0x3821[1]: HDR enable

0: non-HDR mode

1: alternate row HDR mode

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into "long exposure" and "short exposure" in every two rows, as shown in **figure 3-3**. Long exposure time is controlled by registers 0x3500, 0x3501, and 0x3502. Long gain is controlled by registers 0x3508 and 0x3509. Short exposure time is controlled by registers 0x3510, 0x3511, and 0x3512. Short gain is controlled by registers 0x350C and 0x350D. Sequence of MIPI output in HDR mode is similar to normal mode. Output timing of long and short exposure lines are shown in **figure 3-4**.

figure 3-3 alternate row HDR

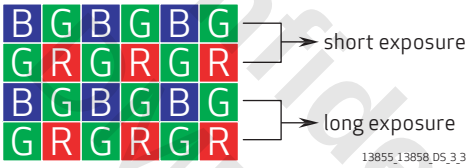


figure 3-4 HDR output timing

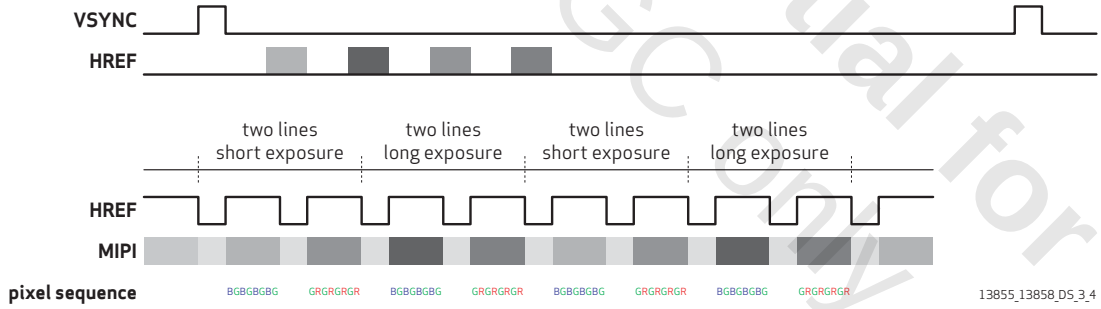


table 3-2 HDR control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3821	FORMAT2	0x00	RW	Bit[1]: HDR enable 0: Disable 1: Enable
0x3500	LONG EXPO	0x00	RW	Long Exposure Bit[3:0]: Long exposure[19:16]

table 3-2 HDR control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3501	LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.
0x3503	AEC MANUAL	0x08	RW	Bit[7]: Reserved Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect in next frame immediately Bit[5]: gain_change_delay option 0: Sensor/real gain change has 1 frame delay latch for BLC control, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain change has no delay on BLC control, takes effect in next frame immediately Bit[4]: gain_delay option 0: Sensor/real gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain has no delay on gain control, takes effect in next frame immediately Bit[3]: Back up (1/16 precision) gain enable When enabled, 0x3503[2] must be 0. For OV13855, this bit must be set to "1". Bit[2]: gain_man_as_gain_snr 0: Manual gain is real gain format, sensor gain will automatically generate by real gain 1: Manual gain is sensor gain format; real gain will automatically generate by sensor gain. Does not work when 0x3503[3]=1 Bit[1]: expo_delay_option 0: Exposure signal for ISP use has 1 frame delay latch, takes effect in the second occurring frame and will sync with new exposure data 1: Exposure signal for ISP has no delay on expo control, takes effect in next frame immediately Bit[0]: expo_change_delay_option 0: Expo change signal for BLC control has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Expo change signal for BLC control has no delay, takes effect in next frame immediately
0x3508	LONG GAIN	0x00	RW	Bit[4:0]: Long_gain[12:8]

table 3-2 HDR control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Gain[7:0] If 0x3503[2]=0, then Gain[12:0] is real gain format, where low 7 bits are fraction bits. Contact local FAE for gain look up table. If 0x3503[2]=1, then Gain[12:0] is sensor gain format, where: Gain[12:8]: Coarse gain 00000: 1x 00001: 2x 00011: 4x 00111: 8x Gain[7]: 1'b1 Gain[6:3]: Fine gain Gain[2:0]: Always 0 For example, 0x080 is 1x gain, 0x180 is 2x gain, and 0x380 is 4x gain. Sensor_gain = coarse_gain * fine_gain = 2^(gain[10]+gain[9]+gain[8]) * (1+(gain[6:0]/128)
0x350A	LONG DIGITAL GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:2]: Long digital gain 00: 1x 01: 2x 10: Not used 11: 4x Bit[1:0]: Debug mode
0x350B	LONG DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x350C	SHORT GAIN	0x00	RW	Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGITAL GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:2]: Short digital gain 00: 1x 01: 2x 10: Not used 11: 4x Bit[1:0]: Debug mode
0x350F	SHORT DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x3510	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]
0x3511	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]

table 3-2 HDR control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3512	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.
0x401A	BLC CTRL1A	0x40	RW	Bit[0]: hdr_en BLC for HDR enable

3.4 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.5 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

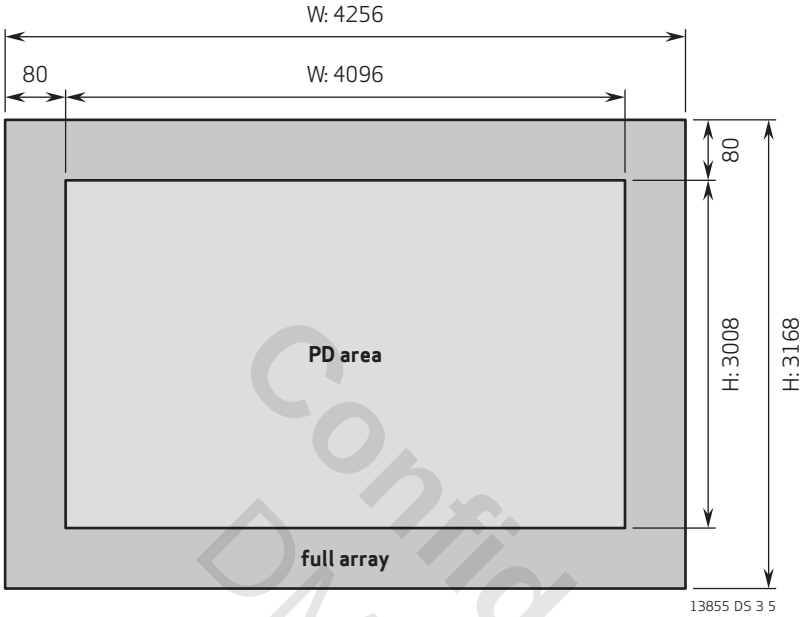
3.6 PD pixel output control

The OV13855 has PD pixels and the PD data will output along with image data.

3.6.1 PD pixel array location

PD pixels are evenly arranged in the PD area. All PD pixels are on the B pixel location using a clear color filter. Total PD pixel amount is 192,512, which is about 92.9% PD coverage for full resolution (4224x3136).

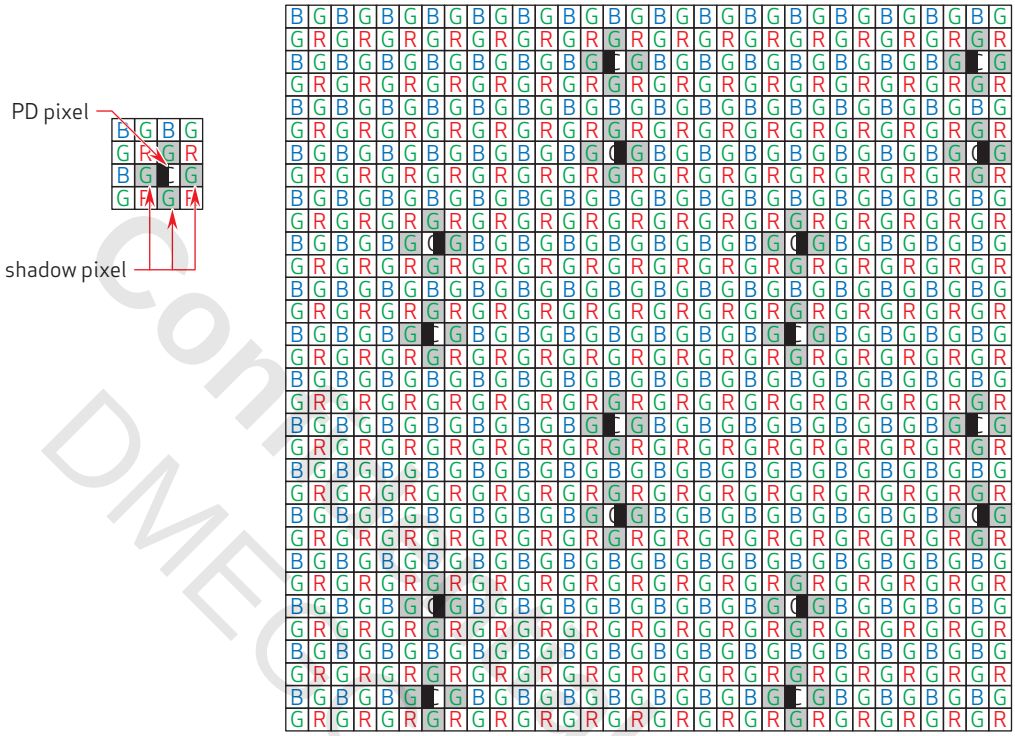
figure 3-5 PD pixel array location diagram



3.6.2 PD pixel pattern

The full size PD pattern is evenly placed in a 32x32 PD area.

figure 3-6 PD pixel pattern



note 1 first 32x32 pattern location is (64, 64) for 4224x3136

note 2 PD pixel is on B location, but is a C (clear) pixel

note 3 output image is non-mirrored, non-flipped

13855_DS_3.6

4 Image sensor core digital functions

4.1 mirror and flip

The OV13855 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

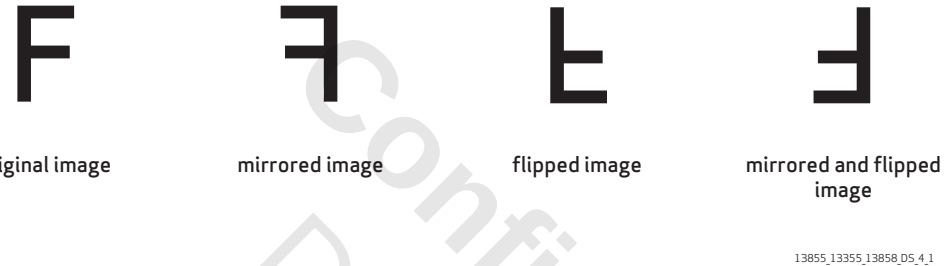


table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0xA0	RW	Timing Control Register Bit[5]: Black line vertical flip enable 0: Normal 1: Vertical flip Bit[4]: Image vertical flip enable 0: Normal 1: Vertical flip Bit[3]: Image horizontal mirror disable 0: Image horizontal mirror enable 1: Normal

4.2 image cropping and windowing

An image cropping area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. A smaller cropping size may achieve higher frame rate. Windowing is achieved by masking off the pixels outside of the window, defined by H_win_off and V_win_off control; thus, the original timing is not affected.

figure 4-2 image cropping and windowing

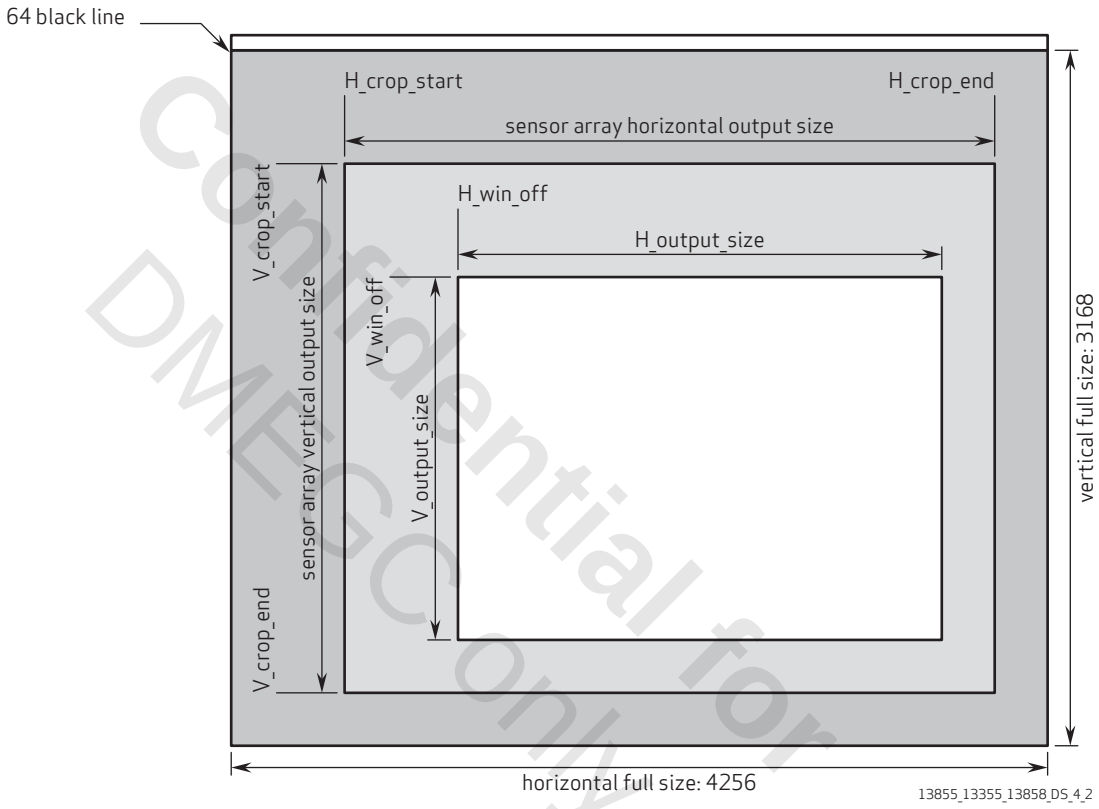


table 4-2 image cropping and windowing control functions

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[3:0]: Manual horizontal crop start address[11:8]
0x3801	H_CROP_START	0x00	RW	Bit[7:0]: Manual horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[3:0]: Manual vertical crop start address[11:8]
0x3803	V_CROP_START	0x08	RW	Bit[7:0]: Manual vertical crop start address[7:0]
0x3804	H_CROP_END	0x10	RW	Bit[3:0]: Manual horizontal crop end address[11:8]
0x3805	H_CROP_END	0x9F	RW	Bit[7:0]: Manual horizontal crop end address[7:0]
0x3806	V_CROP_END	0x0C	RW	Bit[3:0]: Manual vertical crop end address[11:8]
0x3807	V_CROP_END	0x57	RW	Bit[7:0]: Manual vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x10	RW	Bit[3:0]: Horizontal output size[11:8]
0x3809	H_OUTPUT_SIZE	0x70	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OUTPUT_SIZE	0x0C	RW	Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0x30	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x04	RW	Bit[7:0]: Horizontal total size[15:8] HTS must be multiple of 6
0x380D	TIMING_HTS	0x60	RW	Bit[7:0]: Horizontal total size[7:0] HTS must be multiple of 6
0x380E	TIMING_VTS	0x0C	RW	Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0x8E	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[3:0]: Manual horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x18	RW	Bit[7:0]: Manual horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[3:0]: Manual vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x10	RW	Bit[7:0]: Manual vertical windowing offset[7:0]
0x3814	H_INC_ODD	0x01	RW	Bit[3:0]: Horizontal sub-sample odd increase number
0x3815	H_INC_EVEN	0x01	RW	Bit[3:0]: Horizontal sub-sample even increase number
0x3816	V_INC_ODD	0x01	RW	Bit[3:0]: Vertical sub-sample odd increase number
0x3817	V_INC_EVEN	0x01	RW	Bit[3:0]: Vertical sub-sample even increase number

4.3 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These black lines are used as reference for black level calibration

There are two main functions of the BLC:

- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all the pixel values based on digital gain

Registers 0x4004~0x4007 are defined reference windows for black level calibration, these registers can be adjusted manually through an output window.

Black level adjustments can be made with registers 0x4002 and 0x4003.

table 4-3 BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4002	BLK LVL TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blk_lvl_target[9:8] BLC target
0x4003	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0] BLC target
0x400F	BLC CTRL0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Exposure BLC trigger enable
0x4010	BLC CTRL10	0xF0	RW	Bit[7]: off_trig_en Offset BLC trigger enable Bit[6]: gain_chg_trig_en Gain change BLC trigger enable Bit[5]: fmt_chg_trig_en Format change BLC trigger enable Bit[4]: rst_trig_en Reset BLC trigger enable Bit[3]: man_avg_en BLC average in V BLC manual trigger (works only when 0x4010[2] = 1) Bit[2]: man_trig Manual BLC trigger enable Bit[1]: off_frz_en BLC freeze enable Bit[0]: off_always_up BLC always update enable
0x4012	BLC CTRL12	0x08	RW	Bit[7:0]: rst_trig_fn Number of BLC update frames with reset trigger
0x4013	BLC CTRL13	0x02	RW	Bit[7:0]: fmt_trig_fn Number of BLC update frames with format change trigger

table 4-3 BLC registers (sheet 2 of 2)

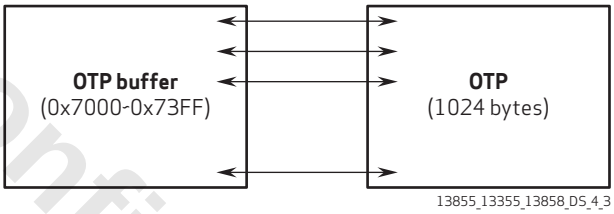
address	register name	default value	R/W	description
0x4014	BLC CTRL14	0x02	RW	Bit[7:0]: gain_trig_fn Number of BLC update frames with gain change trigger
0x4015	BLC CTRL15	0x02	RW	Bit[7:0]: off_trig_fn Number of BLC update frames with offset trigger
0x4016	OFF TRIG TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_trig_th[9:8] Threshold of offset trigger
0x4017	OFF TRIG TH	0x04	RW	Bit[7:0]: off_trig_th[7:0] Threshold of offset trigger
0x401A	BLC CTRL1A	0x40	RW	Bit[0]: hdr_en BLC for HDR enable
0x4052	KCOEF B MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_man[9:8] K for B in manual mode (works only when 0x4001[5] = 1)
0x4053	KCOEF B MAN	0x00	RW	Bit[7:0]: kcoef_b_man[7:0] K for B in manual mode low (works only when 0x4001[5] = 1)
0x4054	KCOEF GB MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gb_man[9:8] K for Gb in manual mode (works only when 0x4001[5] = 1)
0x4055	KCOEF GB MAN	0x00	RW	Bit[7:0]: kcoef_gb_man[7:0] K for Gb in manual mode (works only when 0x4001[5] = 1)
0x4056	KCOEF GR MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gr_man[9:8] K for Gr in manual mode (works only when 0x4001[5] = 1)
0x4057	KCOEF GR MAN	0x00	RW	Bit[7:0]: kcoef_gr_man[7:0] K for Gr in manual mode (works only when 0x4001[5] = 1)
0x4058	KCOEF R MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_r_man[9:8] K for R in manual mode (works only when 0x4001[5] = 1)
0x4059	KCOEF R MAN	0x00	RW	Bit[7:0]: kcoef_r_man[7:0] K for R in manual mode (works only when 0x4001[5] = 1)

4.4 one time programmable (OTP) memory

The OV13855 supports a maximum of 1024 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-5**). Out of 1024 bytes, 608 bytes are reserved for OmniVision and 416 bits are reserved for customers.

There is a dedicated 1024 byte buffer, which is used to temporarily store data to be programmed (written) into OTP or loaded (read) from OTP. The address for this OTP buffer ranges from 0x7000 to 0x73FF.

figure 4-3 OTP buffer



OTP loading data can be triggered when power up or writing 0x01 to register 0x3D81. Power up loading data is enabled by register 0x3D85[3], by default it is off. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer; while in manual mode, part of the data which is defined by the start address ({0x3D88,0x3D89}) and the end address ({0x3D8A,0x3D8B}) of the OTP will be loaded to the OTP buffer.

OTP data can be loaded from 0x7000 to 0x73FF through SCCB interface using a total of 1024 bytes. 0x7000 ~ 0x721F and 0x73C0 ~ 0x73FF are reserved for OmniVision, while 0x7220 ~ 0x73BF (416 bytes) are reserved for customer use. The OTP allocation is shown below.

table 4-4 OTP allocation

start address	end address	bytes usage	assignment
0x7000	0x700F	16	production ID (reserved by OmniVision)
0x7010	0x721F	528	reserved by OmniVision
0x7220	0x73BF	416	reserved for customer
0x73C0	0x73FF	64	reserved by OmniVision

The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.7~3.0V AVDD, 1.2V DVDD and 108MHz system clock.

4.4.1 OTP write

This procedure is used to write specific bytes into the OTP. It is recommended to use this procedure to write to the OTP.

1. Set register 0x3D84[6] = 1 to enable manual mode for partial OTP access.
2. Set address range of OTP to be programmed:
   start address: {0x3D88, 0x3D89}
   end address: {0x3D8A, 0x3D8B}
3. Write data to buffer with address specified in step 2.
4. Set register 0x3D80[0] = 1 to program data stored in buffer into specified OTP bytes.

Example of partial OTP write:

```
6C 3D84 40; [6] partial mode enable

6C 3D85 00

6C 3D88 72; manual OTP start address for access, 0x7220 in this example

6C 3D89 20

6C 3D8A 72; manual OTP end address for access, 0x722F in this example

6C 3D8B 2F

6C 0100 01; stream mode enable

6C 7220 DD; Data[0]

6C 7221 A3; Data[1]

6C 7222 30; Data[2]

6C 7223 00; Data[3]

6C 7224 11; Data[4]

……..

6C 722C 88; Data[12]

6C 722D 99; Data[13]

6C 722E AA; Data[14]

6C 722F BB; Data[15]


6C 3D80 01;[0] program enable

;delay 200ms
```

4.4.2 OTP read

This procedure is used to read specific bytes from OTP to buffer.

1. Set register 0x3D84[6] = 1 to enable manual mode for partial OTP access.
2. Set address range of OTP to be programmed:
   start address: {0x3D88, 0x3D89}
   end address: {0x3D8A, 0x3D8B}
3. Set register 0x3D81[0] = 1 to load data from specific OTP bytes to corresponding buffer.
4. User can read registers within range form start address to end address to check OTP data.

Example of OTP read (partial mode):

```
6C 3D84 40; [6] partial mode enable

6C 3D88 71; manual OTP start address for access

6C 3D89 00

6C 3D8A 71; manual OTP end address for access

6C 3D8B 0C

6C 3D81 01; OTP read enable

;only load data from OTP address 0x7100~0x710C

To use OTP memory under different operating conditions, please contact your local
OmniVision FAE.
```


table 4-5 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x7000~ 0x73FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: OTP_wr_busy (read only) Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	–	RW	Bit[7]: OTP_rd_busy (read only) Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[0]: OTP_load_enable (read and write)
0x3D84	OTP_MODE_CTRL	0x80	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode

table 4-5 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x37	RW	Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start Low Address For Load Setting
0x3D8E	OTP_BIST_ERR_ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIST_ERR_ADDRESS	–	R	OTP Check Error Address Low

4.5 test pattern

table 4-6 test pattern register

address	register name	default value	R/W	description
0x4503	SYNC_REG3	0x00	RW	Bit[7]: r_bar_en Bit[1:0]: bar_style

figure 4-4 color bar

13855_13858_DS_4_4

4.6 temperature sensor

The OV13855 supports an on-chip temperature sensor that covers -64°C ~ +192°C with an error up to 5°C. It can be controlled through the SCCB interface (see **table 4-7**).

If {0x4D13, 0x4D14} ≤ 0xC000, then temperature is positive, Tj (°C) = {(0x4D13, 0x4D14)}/256. If {(0x4D13, 0x4D14)} > 0xC000, the temperature is negative, Tj (°C) = 192 - {(0x4D13[5:0], 0x4D14)}/256

Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register 0x4D12[0].

table 4-7 temperature sensor functions

address	register name	default value	R/W	description
0x4D12	TPM CTRL12	–	W	Bit[0]: Temperature sensor trigger
0x4D13	TPM CTRL13	–	R	Latched Temperature Value, Integer Part
0x4D14	TPM CTRL14	–	R	Latched Temperature Value, Decimal Part

5 image sensor processor digital functions

5.1 DSP general description

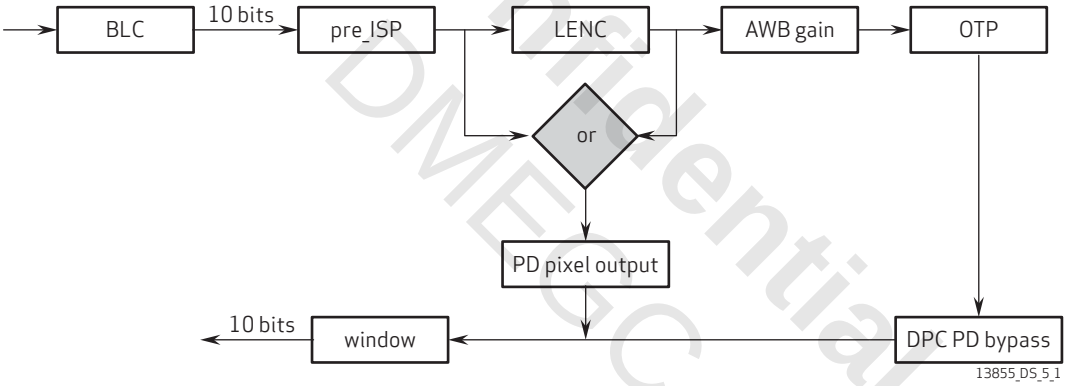
The OV13855 ISP supports two work modes:

- normal mode (1-exposure)
- HDR lite mode (2-exposure)

5.2 ISP block diagram

A simple ISP block diagram is shown in **figure 5-1** which includes some essential modules for RAW image process, such as LENC, DPC, AWB, etc.

figure 5-1 control points of luminance and color channels



The main purposes of the ISP top includes:

- integrate all sub-modules
- create necessary control signals

table 5-1 ISP top registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xED	RW	Bit[7]: WIN enable Bit[5]: DPC enable Bit[4]: OTP enable Bit[3]: WB_gain enable Bit[2]: LENC enable Bit[1]: PD BYP enable Bit[0]: ISP enable

table 5-1 ISP top registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5001	ISP_CTRL_1	0x07	RW	Bit[7:4]: Reserved Bit[3]: Control signal latch mode 0: Enable will be valid immediately 1: Enable will be valid at next frame Bit[2]: Before LENC PD enable 0: PD erase after LENC 1: PD erase before LENC Bit[1]: PD pix check enable for DPC Bit[0]: Rst_protect enable 0: ISP will input href_i in real time 1: After reset, ISP will not input href_i to internal sub-modules before next image

5.3 defective pixel cancellation (DPC)

The main purpose of the DPC function is to remove white/black defect pixels. If the pixel is defective, DPC will use a value calculated from the neighboring normal pixels to replace it.

For DPC control, different type of clusters and correction criteria with gain change can be programmed by registers 0x5200~0x5210 for long exposure and 0x5280~0x5290 for short exposure.

table 5-2 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xED	RW	Bit[5]: dpc_en
0x5200	DPC_CTRL_0	0x1B	RW	Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5201	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5202	ISP_CTRL_2	0x2E	RW	Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list[3]

table 5-2 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5203	ISP_CTRL_3	0x24	RW	Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
0x5204	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]
0x5205	ISP_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
0x5206	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5207	ISP_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5208	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5209	ISP_CTRL_9	0x00	RW	Bit[3:0]: Saturate pixel threshold for clusters
0x520A	ISP_CTRL_10	0x03	RW	Bit[4:0]: Gain threshold list[0]
0x520B	ISP_CTRL_11	0x0F	RW	Bit[4:0]: Gain threshold list[1]
0x520C	ISP_CTRL_12	0x1F	RW	Bit[4:0]: Gain threshold list[2]
0x520D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
0x520E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
0x520F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
0x5210	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]

table 5-3 short DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5280	DPC_CTRL_0	0x1B	RW	Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5281	ISP_CTRL_1	0x94	RW	Bit[7:2]: Vertical number list Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5282	ISP_CTRL_2	0x2E	RW	Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list
0x5283	ISP_CTRL_3	0x24	RW	Bit[6:3]: White pixel threshold list Bit[2:0]: Maximum vertical number

table 5-3 short DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5284	ISP_CTRL_4	0x12	RW	Bit[7:0]: White pixel threshold list
0x5285	ISP_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list
0x5286	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5287	ISP_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5288	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5289	ISP_CTRL_9	0x00	RW	Bit[3:0]: Saturate pixel threshold for clusters
0x528A	ISP_CTRL_10	0x03	RW	Bit[4:0]: White pixel threshold list
0x528B	ISP_CTRL_11	0x0F	RW	Bit[4:0]: White pixel threshold list
0x528C	ISP_CTRL_12	0x1F	RW	Bit[4:0]: White pixel threshold list
0x528D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list
0x528E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list
0x528F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list
0x5290	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list

5.4 window cut (WINC)

The main purpose of the WINC module is to make the image size to be real size by removing offset.

table 5-4 WINC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00	WINC CTRL00	0x00	RW	Bit[3:0]: X_start offset[11:8]
0x5A01	WINC CTRL01	0x00	RW	Bit[7:0]: X_start offset[7:0]
0x5A02	WINC CTRL02	0x00	RW	Bit[3:0]: Y_start offset[11:8]
0x5A03	WINC CTRL03	0x00	RW	Bit[7:0]: Y_start offset[7:0]
0x5A04	WINC CTRL04	0x0C	RW	Bit[3:0]: Window width[11:8]
0x5A05	WINC CTRL05	0xE0	RW	Bit[7:0]: Window width[7:0]
0x5A06	WINC CTRL06	0x09	RW	Bit[3:0]: Window height[11:8]

table 5-4 WINC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A07	WINC CTRL07	0xB0	RW	Bit[7:0]: Window height[7:0]
0x5A08	WINC CTRL08	0x06	RW	Bit[1]: Window enable option 0: Disable window after last valid line 1: Get enable from register Bit[0]: Manual window enable

5.5 manual exposure compensation/ manual gain compensation (MEC/MGC)

Manual exposure provides exposure time settings and sensor gain. The exposure value in registers 0x3500~0x3502 and 0x3510~0x3512 are in units of 1/16 line. Manual gain provides analog gain settings. The OV13855 has a maximum 15.5x analog gain.

note For optimal performance, maximum exposure should be 200ms and minimum exposure line should be 0x3502 = 0x20. For more details, contact your local OmniVision FAE.

table 5-5 AEC_pk registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[3:0]: Long exposure[19:16]
0x3501	LONG EXPO	0x02	RW	Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.
0x3503	AEC MANUAL	0x08	RW	Bit[7]: Reserved Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect in next frame immediately Bit[5]: gain_change_delay option 0: Sensor/real gain change has 1 frame delay latch for BLC control, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain change has no delay on BLC control, takes effect in next frame immediately

table 5-5 AEC_pk registers (sheet 2 of 4)

address	register name	default value	R/W	description
				Bit[4]: gain_delay option 0: Sensor/real gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain has no delay on gain control, takes effect in next frame immediately Bit[3]: Backup (1/16 precision) gain enable When enabled, 0x3503[2] must be 0. For OV13855, this bit must be set to "1". Bit[2]: gain_man_as_gain_snr 0: Manual gain is real gain format, sensor gain will automatically generate by real gain 1: Manual gain is sensor gain format; real gain will automatically generate by sensor gain. Does not work when 0x3503[3]=1 Bit[1]: expo_delay_option 0: Exposure signal for ISP use has 1 frame delay latch, takes effect in second occurring frame and will sync with new exposure data 1: Exposure signal for ISP has no delay on expo control, takes effect in next frame immediately Bit[0]: expo_change_delay_option 0: Expo change signal for BLC control has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Expo change signal for BLC control has no delay, takes effect in next frame immediately
0x3505	GCVT OPTION	0x80	RW	Gain Conversation Option Bit[7]: DAC fixed gain bit Bit[6]: switch_snr_gain_en Bit[5:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set it to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format

table 5-5 AEC_pk registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3507	GAIN SHIFT	0x00	RW	Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits
0x3508	LONG GAIN	0x00	RW	Bit[4:0]: Long gain[12:8]
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] If 0x3503[2]=0, then Gain[12:0] is real gain format, where low 7 bits are fraction bits. Please contact local FAE for the gain look up table. if 0x3503[2]=1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0. For example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain Sensor_gain = coarse_gain * fine_gain = 2^(gain[10]+gain[9]+gain[8]) * (1+(gain[6:0]/128)
0x350A	LONG DIGITAL GAIN	0x04	RW	Bit[3:2]: Long digital gain 00: 1x 01: 2x 11: 4x Bit[1:0]: Debug mode
0x350B	LONG DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x350C	SHORT GAIN	0x00	RW	Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGITAL GAIN	0x04	RW	Bit[3:2]: Short digital gain 00: 1x 01: 2x 11: 4x Bit[1:0]: Debug mode
0x350F	SHORT DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x3510	SHORT EXPO	0x00	RW	Bit[3:0]: Short exposure[19:16]
0x3511	SHORT EXPO	0x02	RW	Bit[7:0]: Short exposure[15:8]

table 5-5 AEC_pk registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3512	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.

5.6 lens correction (LENC)

Lens correction (LENC) corrects the lens shading due to light fall off in the corner area. It computes a gain pixel by pixel according to G/B/R's control points matrix (control registers), then applies the gain to each pixel in the image. The G, B, and R control point matrix size are all 12x10.

Control point selection is according to the absolute coordinate of the input pixel in the sensor array.

A parameter m_nQ is used to adjust the gain for the pixel. It can also be auto calibrated from the real gain or manually set.

figure 5-2 control points of luminance and color channels

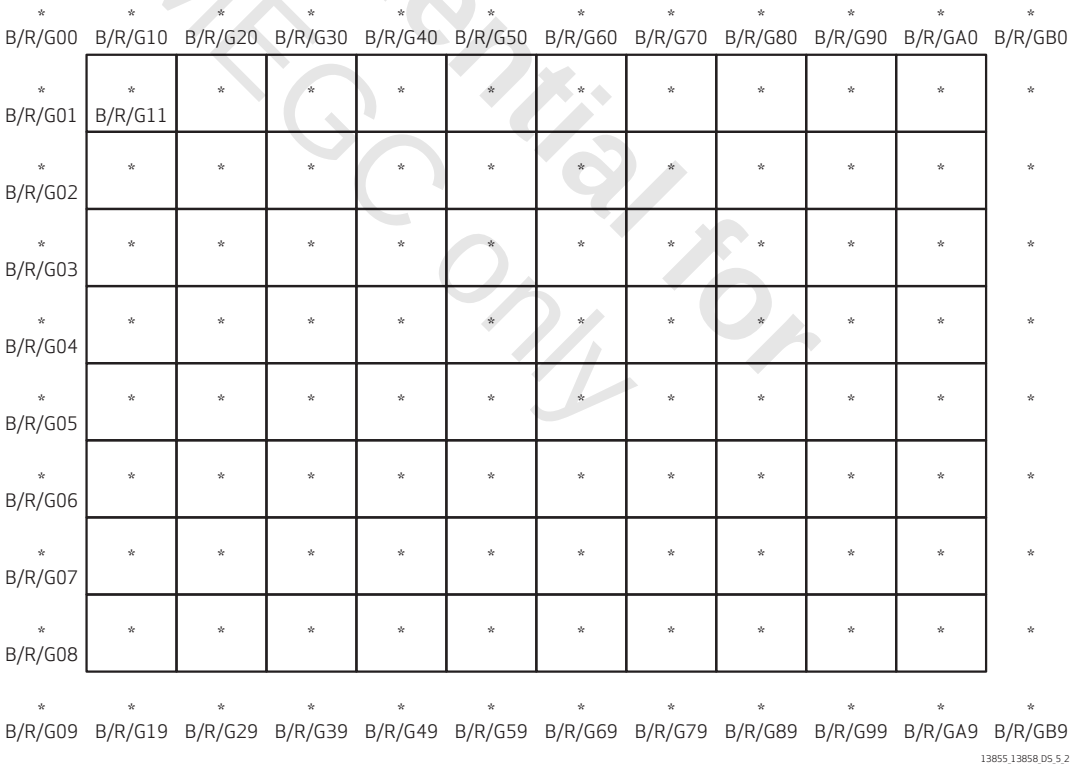


figure 5-3 luminance compensation level calculation

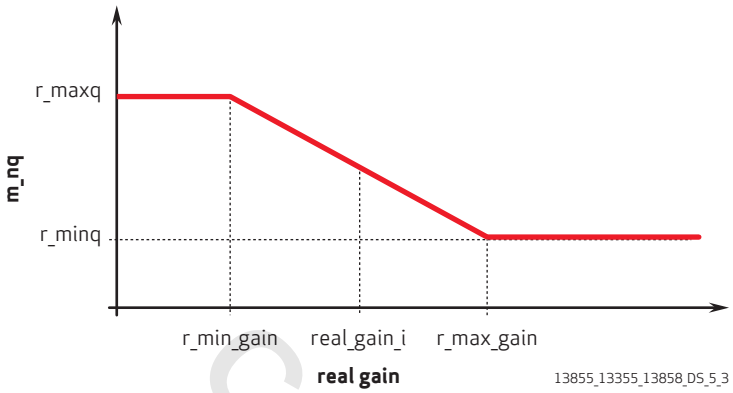


table 5-6 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xED	RW	Bit[2]: Lens correction (LENC) function enable 0: Disable 1: Enable
0x5400	LENC_CTRL_0	0x60	RW	Bit[7:0]: Maxgain threshold
0x5401	LENC_CTRL_1	0x40	RW	Bit[7:0]: Mingain threshold
0x5402	LENC_CTRL_2	0x40	RW	Bit[6:0]: Maxq Apply maximum amplitude
0x5403	LENC_CTRL_3	0x18	RW	Bit[6:0]: Minq Apply minimum amplitude
0x5404	LENC_CTRL_4	0x36	RW	Bit[5]: BLC add enable Must be set to 1 Bit[4]: BLC enable Must be set to 1 Bit[3]: Enable 2x blue/red gain Must be set to 0 Bit[2]: m_nQ auto calculate enable Must be set to 1 Bit[1]: Enable dithering function to avoid lost bit Bit[0]: Enable 2x green gain
0x5405	LENC_CTRL_5	0x01	RW	Bit[4:0]: Horizontal scale[12:8]
0x5406	LENC_CTRL_6	0xE1	RW	Bit[7:0]: Horizontal scale[7:0]
0x5407	LENC_CTRL_7	0x01	RW	Bit[3:0]: Vertical scale[11:8]

table 5-6 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5408	LENC_CTRL_8	0x41	RW	Bit[7:0]: Vertical scale[7:0]
0x5500~ 0x5577	LENC_MT_CTRL_000~ 077	0x80	RW	Bit[7:0]: Coefficient for G channel
0x5578~ 0x55EF	LENC_MT_CTRL_078~0EF	0x80	RW	Bit[7:0]: Coefficient for B channel
0x55F0~ 0x5667	LENC_MT_CTRL_0F0~167	0x80	RW	Bit[7:0]: Coefficient for R channel

5.7 manual white balance

The RAW R/G/B values of a gray object vary with the spectrum of the illumination and the sensor spectral response. The illumination spectrum, is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is around 2850K, while the color temperature of an overcast day is around 6500K.

To make sure that a gray image is truly gray, the sensor needs to adjust the gain for each color channel according to the color temperature. The process is called white balance (WB).

White balanced gain is enabled by default and can be disabled by register 0x5000[3]. The manual white balance (MWB), controlled by register 0x5100~0x5105, provides gain for R, G, and B channels. Each channel gain is 15-bit. 0x400 is 1x gain. Maximum 16x gain is 0x4000.

White balance gain does not have internal latch function. Once it is set, it will take effect immediately.

table 5-7 MWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5100	MWB GAIN00	0x04	RW	Bit[6:0]: wb_gain_B[14:8] MWB gain in blue channel
0x5101	MWB GAIN01	0x00	RW	Bit[7:0]: wb_gain_B[7:0] MWB gain in blue channel
0x5102	MWB GAIN02	0x04	RW	Bit[6:0]: wb_gain_G[14:8] MWB gain in green channel
0x5103	MWB GAIN03	0x00	RW	Bit[7:0]: wb_gain_G[7:0] MWB gain in green channel
0x5104	MWB GAIN04	0x04	RW	Bit[6:0]: wb_gain_R[14:8] MWB gain in red channel

table 5-7 MWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5105	MWB GAIN05	0x00	RW	Bit[7:0]: wb_gain_R[7:0] MWB gain in red channel
0x5106	MWB GAIN06	0x00	RW	Bit[0]: wb_gain_sel 0: MWB control selection 1: Debug mode

table 5-8 MWB control registers for short exposure mode

address	register name	default value	R/W	description
0x5140	MWB GAIN00	0x04	RW	Bit[6:0]: wb_gain_B[14:8] MWB gain in blue channel
0x5141	MWB GAIN01	0x00	RW	Bit[7:0]: wb_gain_B[7:0] MWB gain in blue channel
0x5142	MWB GAIN02	0x04	RW	Bit[6:0]: wb_gain_G[14:8] MWB gain in green channel
0x5143	MWB GAIN03	0x00	RW	Bit[7:0]: wb_gain_G[7:0] MWB gain in green channel
0x5144	MWB GAIN04	0x04	RW	Bit[6:0]: wb_gain_R[14:8] MWB gain in red channel
0x5145	MWB GAIN05	0x00	RW	Bit[7:0]: wb_gain_R[7:0] MWB gain in red channel
0x5146	MWB GAIN06	0x00	RW	Bit[0]: wb_gain_sel 0: MWB control selection 1: Debug mode

5.8 digital gain

Manual digital gain provides the same gain for R, G, and B channels. The OV13855 supports 1x, 2x and 4x digital gain.

table 5-9 digital gain registers

address	register name	default value	R/W	description
0x3503	GAIN CONTROL	0x80	RW	Bit[6]: Digital gain delay option 0: Digital gain (ISP use) has 1 frame delay latch, so it will take effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, so it will take effect in next frame immediately
0x350A	LONG DIGITAL GAIN	0x04	RW	Bit[3:2]: Digital gain for long exposure 00: 1x 01: 2x 11: 4x
0x350E	SHORT DIGITAL GAIN	0x04	RW	Bit[3:2]: Digital gain for short expo 00: 1x 01: 2x 11: 4x
0x5040	DIGITAL GAIN CONTROL	0x19	RW	Bit[5]: blc_dig_gain_option 0: Debug mode 1: Use 0x350A and 0x350E for digital gain control

6 register tables

The following tables provide descriptions of the device control registers contained in the OV13855. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read (when SID=1, 0x20 for write and 0x21 for read).

6.1 PLL [0x0300 - 0x0313, 0x031B - 0x031C]

table 6-1 PLL registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x02	RW	Bit[7:3]: Not used Bit[2:0]: pll1_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL_CTRL_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x5A	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0303	PLL_CTRL_3	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll1_divpx 00: /1 01: /2 10: /3 11: /4
0x0304	PLL_CTRL_4	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_pix_bitdiv 0: /4 1: /5
0x0305	PLL_CTRL_5	0x01	RW	Bit[7:1]: Not used Bit[0]: pll1_sys_bitdiv 0: /4 1: /5
0x0307	PLL_CTRL_7	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_predivp 0: /1 1: /2
0x0308	PLL_CTRL_8	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_bypass

table 6-1 PLL registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x0309	PLL_CTRL_9	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll1_cp
0x030A	PLL_CTRL_A	0x50	RW	Bit[7:0]: pll1_reserve
0x030B	PLL_CTRL_B	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll2_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x030C	PLL_CTRL_C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll2_r_divp[9:8]
0x030D	PLL_CTRL_D	0x36	RW	Bit[7:0]: pll2_r_divp[7:0]
0x030E	PLL_CTRL_E	0x05	RW	Bit[7:3]: Not used Bit[2:0]: pll2_sramdiv Control bit value = bit[2:0] + 1
0x030F	PLL_CTRL_F	0x01	RW	Bit[7:2: Not used Bit[1:0]: pll2_sa1_div 00: /5 01: /6 10: /7 11: /8
0x0310	PLL_CTRL_10	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll2_r_cp
0x0311	PLL_CTRL_11	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_bypass
0x0312	PLL_CTRL_12	0x01	RW	Bit[7:6]: pll2_reserve Bit[5]: pll2_div_rst_sync Bit[4]: pll2_predivp 0: /1 1: /2 Bit[3:2]: Not used Bit[1:0]: pll2_r_divdac 00: /1 01: /2 10: /3 11: /4
0x0313	PLL_CTRL_13	0x00	RW	Bit[7:0]: pll2_reserve

table 6-1 PLL registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x031B	PLL_CTRL_1B	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_rst
0x031C	PLL_CTRL_1C	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_rst

6.2 system [0x0100 - 0x0103, 0x3002 - 0x3008, 0x300A - 0x3022, 0x302A]

table 6-2 system registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x0100	MODEL_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Mode select 0: software_standby 1: Streaming
0x0101~ 0x0102	NOT USED	–	–	Not Used
0x0103	SOFTWARE_RST	–	W	Bit[7:1]: Not used Bit[0]: software_reset
0x3002	PAD OEN2	0x21	RW	Bit[7]: io_fsin_oen Bit[6]: io_vsync_oen Bit[5:0]: Reserved
0x3003	SCCB_ID	0x6C	RW	Bit[7:0]: SCCB programmable ID
0x3004	SCCB ID	0x20	RW	Bit[7:0]: sccb_id SCCB backup programed ID
0x3005	SCCB_ID_2	0x42	RW	Bit[7:0]: sccb_id2
0x3006~ 0x3007	NOT USED	–	–	Not Used
0x3008	PAD_OUT2	0x00	RW	Bit[7]: io_fsin_o Bit[6]: io_vsync_o Bit[5:3]: Reserved Bit[2]: io_sda_o Bit[1:0]: Reserved
0x300A	CHIP ID	0x00	R	Bit[7:0]: chip_id[23:16]
0x300B	CHIP ID	0xD8	R	Bit[7:0]: chip_id[15:8]
0x300C	CHIP ID	0x55	R	Bit[7:0]: chip_id[7:0]

table 6-2 system registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x300D~ 0x300F	NOT USED	–	–	Not Used
0x3010	PAD SEL2	0x00	RW	Bit[7]: io_fsin_sel Bit[6]: io_vsync_sel Bit[5:3]: Reserved Bit[2]: io_sda_sel Bit[1:0]: Reserved
0x3011	WAKE_UP_DELAY	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Stream on delay 000: Delay 2^9 pad clock cycle after stream 001: Delay 2^10 pad clock cycle after stream 010: Delay 2^11 pad clock cycle after stream 011: Delay 2^12 pad clock cycle after stream 100: Delay 2^13 pad clock cycle after stream 101: Delay 2^14 pad clock cycle after stream 110: Delay 2^15 pad clock cycle after stream 111: Delay 2^16 pad clock cycle after stream
0x3012	CLK_GATE_MASK	0x00	RW	Bit[7]: Not used Bit[6]: pclk_mipi_clk_gate_mask Bit[5:0]: Not used
0x3013	CLK_GATE_MASK	0x00	RW	Bit[7]: sclk_dpcm_clk_gate_mask Bit[6]: sclk_mipi_clk_gate_mask Bit[5]: sclk_tpm, sclk_clip_clk_gate_mask Bit[4]: Not used Bit[3]: sclk_isp, sclk_isp_fc_clk_gate_mask Bit[2]: sclk_blc_clk_gate_mask Bit[1]: sclk_sync_fifo, srmclk_sync_fifo_clk_gate_mask Bit[0]: srmclk_psram_clk_gate_mask
0x3014	NOT USED	–	–	Not Used

table 6-2 system registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3015	PUMP CLK DIV	0x10	RW	Bit[7]: Not used Bit[6:4]: Npump clock div 000: /2 001: /4 010: /8 011: /16 100: /32 Others: Disable pump_clk Bit[3]: pd_mipi_auto mode 0: Use original reset as pd_mipi_auto 1: Use synchronous reset as pd_mipi_auto Bit[2:0]: Ppump clock div 000: /2 001: /4 010: /8 011: /16 100: /32 Others: Disable pump_clk
0x3016	MIPI SC CTRL	0x72	RW	Bit[7:5]: mipi_lane_mode N+1 lane Bit[4]: mipi_en 0: MIPI disable 1: MIPI enable Bit[3:2]: r_phy_pd_mipi Bit[1]: phy_rst option 0: rst_sync cannot reset PHY 1: Reset PHY when rst_sync Bit[0]: lane_dis option 0: Not used 1: Disable lanes when pd_mipi
0x3017	MIPI SC CTRL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: MIPI lane disable
0x3018	CLK_CTRL	0xF0	RW	Bit[7]: tclk_tc enable Bit[6]: tclk_snr_ctrl enable Bit[5]: srmclk_psram enable Bit[4]: srmclk_syncfifo enable Bit[3]: rst_tc Bit[2]: rst_snr_ctrl and psram_ctrl Bit[1]: Not used Bit[0]: rst_syncfifo

table 6-2 system registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3019	CTRL_R19	0xF0	RW	Bit[7:6]: Not used Bit[5]: tclk_psv_ctrl Bit[4]: Reserved Bit[3:2]: Not used Bit[1]: rst_psv Bit[0]: Reserved
0x301A	CLKRST0	0xF0	RW	Bit[7:4]: Reserved Bit[3]: mipi_phy_rst_o Bit[2:0]: Reserved
0x301B	CLKRST1	0xD0	RW	Bit[7]: sclk_blc enable Bit[6]: sclk_isp enable Bit[5]: sclk_tpm enable Bit[4]: Reserved Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_tpm Bit[0]: Reserved
0x301C	CLKRST2	0xF0	RW	Bit[7]: Reserved Bit[6]: sclk_mipi_en Bit[5]: Reserved Bit[4]: sclk_efuse_en Bit[3]: Reserved Bit[2]: rst_mipi Bit[1]: Reserved Bit[0]: rst_efuse
0x301D	CLKRST3	0xD8	RW	Bit[7]: sclk_asram_tst_en Bit[6]: sclk_grp_en Bit[5]: sclk_bist_en Bit[4]: sclk_aec_en Bit[3]: rst_asram_tst Bit[2]: rst_grp Bit[1]: rst_bist Bit[0]: rst_aec
0x301E	CLKRST4	0xF0	RW	Bit[7:5]: Reserved Bit[4]: pclk_mipi_en Bit[3:0]: Reserved
0x301F	CLKRST5	0xD0	RW	Bit[7]: Reserved Bit[6]: sclk_isp_fc_en Bit[5]: sclk_dpcm_en Bit[4]: sclk_clip_en Bit[3]: Reserved Bit[2]: rst_isp_fc Bit[1]: rst_dpcm Bit[0]: rst_clip

table 6-2 system registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x3020	CLOCK SEL	0x9B	RW	Bit[7:5]: Not used Bit[4]: sccb_id2_nack 0: SCCB slave returns normal ACK 1: SCCB slave does not return ACK Bit[3]: PCLK_div 0: /1, choose pll_pclk_i 1: /2, choose pll_pclk_d2 Bit[2]: Not used Bit[1]: pclk_inv Reverse PCLK Bit[0]: sclk2x_sel 0: Choose pll_sclk_i 1: Choose_pll_sclk_d2
0x3021	MISC CTRL	0x23	RW	Bit[7]: Not used Bit[6]: Sleep no latch option 0: Sensor enters into sleep mode in blanking period defined by bit[5] 1: Sensor enters into sleep mode immediately Bit[5]: fst_stby_ctr Works only when bit[6] = 0) 0: Software standby enters at vertical blanking 1: Software standby enters at line blanking Bit[4]: mipi_ctr_en 0: Disable function 1: Enable MIPI remote reset and suspend control SC Bit[3]: mipi_rst_sel 0: MIPI remote resets all registers 1: MIPI remote resets all digital modules Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3022	MIPI SC CTRL	0x01	RW	Bit[7:4]: mipi_bit_sel 0100: 8-bit mode 0101: 10-bit mode 0110: 12-bit mode 1000: 16-bit mode Others: 10-bit mode Bit[3]: Reserved Bit[2]: Clock lane disable 1 Bit[1]: Clock lane disable 0 Bit[0]: pd_mipi_by software reset enable

table 6-2 system registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x302A	SUB ID	–	R	Bit[7:4]: Process Bit[3:0]: Version

6.3 SCCB [0x3100 - 0x3108]

table 6-3 SCCB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SCCB OPT	0x32	RW	Bit[7:6]: Not used Bit[5]: Enable register address translating table Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SCCB FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x3103	SCCB SYSREG	0x00	RW	Bit[7]: Not used Bit[6]: ctrl_rst_mipisc Bit[5]: ctrl_rst_srb Bit[4]: ctrl_rst_sccb_s Bit[3]: ctrl_rst_pon_sccb_s Bit[2]: ctrl_rst_clkmod Bit[1]: ctrl_mipi_phy_rst_o Bit[0]: ctrl_pll_rst_o
0x3104	PWUP DIS	0x01	RW	Bit[7:5]: Not used Bit[4]: r_srb_clk_syn_en Bit[3]: pwup_dis2 Bit[2]: pwup_dis1 Bit[1]: pll_clk_sel Bit[0]: pwup_dis0

table 6-3 SCCB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3105	PADCLK DIV	0x11	RW	Bit[7:6]: Not used Bit[5:0]: padclk_div
0x3106	SRB HOST INPUT DIS	0x15	RW	Bit[7]: sramclk_cutoff_byp Bit[6]: sa1clk_cutoff_byp Bit[5:4]: Not used Bit[3:2]: sys_clk_div 00: /1 01: /2 10: /4 11: /8 Bit[1]: rst_arb Bit[0]: bypass_arb
0x3107	SRB_CTRL	0x01	RW	Bit[7]: npump_clk_ausw_dis Bit[6]: npump_clk_sw Bit[5]: auto_sleep_en Bit[4]: pd_mipi_dis_aslp Bit[3]: pumpclk_cutoff_byp Bit[2]: pclk_cutoff_byp Bit[1]: sclk_cutoff_byp Bit[0]: sclk_inv
0x3108	SRB_CTRL	0x01	RW	Bit[7:2]: Not used Bit[1]: pll_sclk_selection 0: pll_sclk_i 1: p_clk_i Bit[0]: Sleep control

6.4 group hold [0x3200 - 0x320F]

table 6-4 group hold registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual Address Is {0x3200[5:0], 4'h0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM Actual Address Is {0x3201[5:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM Actual Address Is {0x3202[5:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM Actual Address Is {0x3203[5:0], 4'h0}

table 6-4 group hold registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	When register 0x320B[7] = 1 Bit[7]: Not used Bit[6:5]: Group number that group will switch back to after launch group 0 in auto switch mode Bit[4:0]: grp0_frms Number of frames stay in group 0 before auto switch to group defined by 0x3209[6:5] When register 0x320B[2] = 1 Bit[7:0]: Number of frames stay in group 0 before auto switch to group defined by 0x320B[1:0]
0x320A	GRP1_PERIOD	0x00	RW	Bit[7:0]: Number of frames stay in second group in context switch mode defined by 0x320B[1:0] (works only when 0x320B[2] = 1)

table 6-4 group hold registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x320B	GRP_SWCTRL	0x11	RW	Bit[7]: auto_sw Auto launch mode enable Bit[6:5]: Not used Bit[4]: frame_cnt_trig 0: EOF as frame count trigger 1: Group write as frame count trigger Bit[3]: group_switch_repeat Bit[2]: context_en Contact switch mode enable Bit[1:0]: Second group selection
0x320C	NOT USED	–	–	Not Used
0x320D	GRP_ACT	–	R	Bit[7:4]: Not used Bit[3:0]: grp_act Indicates which group is active
0x320E	FRAME_CNT_GRP0	–	R	Bit[7:0]: frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	Bit[7:0]: frame_cnt_grp1

6.5 AEC_pk [0x3500 - 0x3518]

table 6-5 AEC_pk registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	LONG EXPO	0x02	RW	Bit[7:0]: Long Exposure[15:8]
0x3502	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.

table 6-5 AEC_pk registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x08	RW	Bit[7]: Reserved Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect in next frame immediately Bit[5]: gain_change_delay option 0: Sensor/real gain change has 1 frame delay latch for BLC control, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain change has no delay on BLC control, takes effect in next frame immediately Bit[4]: gain_delay option 0: Sensor/real gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/real gain has no delay on gain control, takes effect in next frame immediately Bit[3]: Backup (1/16 precision) gain enable When enabled, 0x3503[2] must be 0. For OV13855, this bit must be set to "1". Bit[2]: gain_man_as_gain_snr 0: Manual gain is real gain format, sensor gain will automatically generate by real gain 1: Manual gain is sensor gain format; real gain will automatically generate by sensor gain. Does not work when 0x3503[3]=1 Bit[1]: expo_delay_option 0: Exposure signal for ISP use has 1 frame delay latch, takes effect in second occurring frame and will sync with new exposure data 1: Exposure signal for ISP has no delay on expo control, takes effect in next frame immediately

table 6-5 AEC_pk registers (sheet 3 of 4)

address	register name	default value	R/W	description
				Bit[0]: expo_change_delay_option 0: Expo change signal for BLC control has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Expo change signal for BLC control has no delay, takes effect in next frame immediately
0x3504	RSVD	–	–	Reserved
0x3505	GCVT OPTION	0x80	RW	Gain Conversation Option Bit[7]: DAC fixed gain bit Bit[6]: switch_snr_gain_en Bit[5:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set it to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format
0x3506	RSVD	–	–	Reserved
0x3507	GAIN SHIFT	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits
0x3508	LONG GAIN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Long gain[12:8]
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] If 0x3503[2]=0, then Gain[12:0] is real gain format, where low 7 bits are fraction bits. Contact local FAE for gain look up table. If 0x3503[2]=1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0. For example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain. Sensor_gain = coarse_gain * fine_gain = 2^(gain[10]+gain[9]+gain[8]) * (1+(gain[6:0]/128)

table 6-5 AEC_pk registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x350A	LONG DIGITAL GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:2]: Long digital gain 00: 1x 01: 2x 10: Not used 11: 4x Bit[1:0]: Debug mode
0x350B	LONG DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x350C	SHORT GAIN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGITAL GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:2]: Short digital gain 00: 1x 01: 2x 10: Not used 11: 4x Bit[1:0]: Debug mode
0x350F	SHORT DIGITAL GAIN	0x00	RW	Bit[7:0]: Debug mode
0x3510	SHORT EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3511	SHORT EXPO	0x02	RW	Bit[7:0]: Short exposure[15:8]
0x3512	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits This sensor does not support fraction exposure, so low 4 bits cannot be used and must be set to 0.
0x3513	SNR_GAIN_L	–	R	Bit[7:6]: Not used Bit[5:0]: Long sensor gain[13:8]
0x3514	SNR_GAIN_L	–	R	Bit[7:0]: Long sensor gain[7:0]
0x3515	FINE_SNR_ GAIN_L	–	R	Bit[7:6]: Not used Bit[5:0]: Long fine sensor gain
0x3516	SNR_GAIN_S	–	R	Bit[7:6]: Not used Bit[5:0]: Short sensor gain[13:8]
0x3517	SNR_GAIN_S	–	R	Bit[7:0]: Short sensor gain[7:0]
0x3518	FINE_SNR_ GAIN_S	–	R	Bit[7:6]: Not used Bit[5:0]: Short fine sensor gain

6.6 ANA [0x3600 - 0x3629, 0x3660 - 0x3684, 0x36F0 - 0x36F2]

table 6-6 ANA registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3600~ 0x3629	ANALOG CONTROL	–	–	Analog Control
0x3660	CORE TOP REG00	0x00	RW	Bit[7]: Debug mode Bit[6]: r_rst_otp_sleep_dis 0: Allow software reset to reset OTP 1: Disable software reset to reset OTP Bit[5]: r_rst_ana_sleep_dis 0: Allow software reset to reset analog circuit 1: Disable software reset to reset analog circuit Bit[4]: pll1_sysclk_sel 0: SCLK comes from PLL1 1: SCLK comes from PLL2 Bit[3]: r_fmt_eof_sel 0: Format EOF input comes from ISPFC EOF 1: Format EOF input comes from mipi_eof Bit[2]: rip_sof_en 0: MIPI SOF input comes from timing control SOF (original SOF) 1: MIPI SOF input comes from ISPFC SOF (after ripple delay) Bit[1]: pll_sysclk_sel PLL2 SCLK is used as TCLK after a series of mux 0: pll2_sclk_real comes from pll2_mux_sclk 1: pll2_sclk_real comes from pll2_daclk Bit[0]: mipi_sel_aslp_dis 0: Allow MIPI clock to enter into low power mode 1: Disable MIPI clock to enter into low power mode

table 6-6 ANA registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3661	CORE TOP REG01	0x80	RW	Bit[7]: r_sa1clk_sel 0: pll_sa1_clk comes from sa1_clk_d24 (divided pll1_sclk) 1: pll_sa1_clk comes from pll1_sclk Bit[6:4]: r_bit_shift_mode Shift left ISP output data certain bits 000: No shift 001: Shift left1 bit 010: Shift left 2 bits 011: Shift left 3 bits Others: Left shift 4 bits Bit[3]: byp_isp 0: No bypass, normal data path 1: Bypass ISP data, HREF, valid, all three of these components comes from sync FIFO Bit[2]: r_bit_shift_clip_en 0: No clip, add zero at low bits 1: Clip all to one when one is shift out Bit[1]: r_pump_clk_sel 0: pll_pump_clk comes from pll2_sclk 1: pll_pump_clk comes from pll1_sclk Bit[0]: pll2_sysclk_sel 0: pll2_mux_sclk comes from pll2_sclk 1: pll2_mux_sclk comes from pll1_sclk
0x3662	CORE TOP REG02	0x12	RW	Bit[7:5]: Not used Bit[4:0]: r_blc_black_num BLC black line number used for BLC

table 6-6 ANA registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3663	CORE TOP REG03	0x26	RW	Bit[7]: Reserved Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x Bit[4:3]: Not used Bit[2]: FSIN selection 0: FSIN input enable 1: Fix at 0 Bit[1]: VSYNC selection 0: VSYNC input enable 1: Fix at 0 Bit[0]: Not used
0x3664	CORE TOP REG04	0x70	RW	Bit[7]: otp_rst 0: No effect on OTP reset 1: Force to reset OTP (no matter other reset) Bit[6]: cen_grp_hold 0: Group hold SRAM chip select disable 1: Group hold SRAM chip select enable Bit[5]: cen_otp 0: OTP_fifo SRAM chip select disable 1: OTP SRAM chip select enable Bit[4]: cen_syncfifo 0: sync_fifo SRAM chip select disable 1: sync_fifo SRAM chip select enable Bit[3]: sramclk_sel 0: pll2_sram_clk_real comes from pll2_sram_clk2x 1: pll2_sram_clk_real comes from pll1_sram_clk1x Bit[2]: tc_sof_sel 0: SOF in SCLK domain sync from sync FIFO SOF (after delay) 1: SOF in SCLK domain sync from timing control SOF (original SOF) Bit[1:0]: Analog debug register

table 6-6 ANA registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3665	CORE TOP REG05	0x07	RW	Bit[7:4]: Analog timing control Bit[3]: sa1clk_d24_sel 0: sa1_clk_d24 as sa1_clk_d2 1: sa1_clk_d24 as sa1_clk_d4 Bit[2:0]: Reserved
0x3666~ 0x3673	ANALOG VOLTAGE CONTROL	–	–	Analog Voltage Control
0x3674	CORE_TOP_REG14	0x00	RW	Bit[7:3]: Reserved Bit[2]: r_dpcm_raw12 No 12-bit, fixed at 0 Bit[1]: r_dpcm_bypass_in2 0: Normal DPCM compression 1: If (data_i[1:0] ≥ 2) data_o[9:2] = data_o[9:2] + 1 Bit[0]: r_dpcm_en 0: Bypass DPCM 1: Enable DPCM
0x3675~ 0x367E	ANALOG VOLTAGE CONTROL	–	–	Analog Voltage Control
0x367F	CORE_TOP_REG1F	0x00	RW	Bit[7:1]: Not used Bit[0]: pll_sram_clk_sel 0: pll_sram_clk2x comes from pll1_sclk 1: pll_sram_clk2x comes from pll2_sram_clk2x
0x3680~ 0x3684	ANALOG VOLTAGE CONTROL	–	–	Analog Voltage Control
0x36F0	CORE TOP READ0	–	R	Debug Mode
0x36F1	CORE TOP READ1	–	R	Input Bit[7]: Not used Bit[6]: p_vsync_i_buf Bit[5]: d_tpm_db_i_buf Bit[4]: p_pwdn_buf Bit[3]: p_tm_buf Bit[2]: p_rst_n_buf Bit[1]: p_fsin_i_buf Bit[0]: p_sid_buf
0x36F2	NOT USED	–	–	Not Used

6.7 sensor top [0x3700 - 0x37FF]

table 6-7 sensor top control registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	SENSOR TOP CONTROL	–	–	Sensor Top Control

6.8 timing control [0x3800 - 0x381E, 0x3820 - 0x3829, 0x3832]

table 6-8 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point
0x3803	Y ADDR START	0x08	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	X ADDR END	0x10	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	X ADDR END	0x9F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x0C	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	Y ADDR END	0x57	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0x10	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x70	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x0C	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0x30	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height

table 6-8 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x380C	HTS	0x04	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size HTS must be multiple of 6
0x380D	HTS	0x60	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size HTS must be multiple of 6
0x380E	VTS	0x0C	RW	Bit[7:0]: VTS[15:8] Total vertical timing size
0x380F	VTS	0x8E	RW	Bit[7:0]: VTS[7:0] Total vertical timing size
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal window offset
0x3811	ISP X WIN	0x18	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal window offset
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x10	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	X INC ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[7:5]: Not used Bit[4:0]: x_even_inc
0x3816	Y_INC_ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_odd_inc
0x3817	Y_INC_EVEN	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_even_inc
0x3818	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[15:8] VSYNC start point
0x3819	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[7:0] VSYNC start point
0x381A	VSYNC END	0x00	RW	Bit[7:0]: vsync_end[15:8] VSYNC end point
0x381B	VSYNC END	0x01	RW	Bit[7:0]: vsync_end[7:0] VSYNC end point
0x381C	BLC_NUM_OPTION	0x18	RW	Bit[7:5]: ablc_adj Bit[4:0]: ablc_use_num
0x381D~ 0x381E	NOT USED	–	–	Not Used

table 6-8 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3820	FORMAT1	0xA0	RW	Bit[7:6]: Not used Bit[5]: Black line vertical flip enable 0: Normal 1: Vertical flip Bit[4]: Image vertical flip enable 0: Normal 1: Vertical flip Bit[3]: Image horizontal mirror disable 0: Image horizontal mirror enable 1: Normal Bit[2]: Not used Bit[1]: hbin2_o Bit[0]: vbinf_o
0x3821	FORMAT2	0x00	RW	Bit[7:2]: Reserved Bit[1]: hdr_en_o Bit[0]: vsub48_blc
0x3822	REG22	0xC8	RW	Bit[7:6]: Reserved Bit[5]: r_fix_cnt_en Bit[4]: vts_add_dis Bit[3:0]: r_grp_adj
0x3823	REG23	0x08	RW	Bit[7]: ext_vs_re Bit[6]: ext_vs_en Bit[5]: vts_no_latch Bit[4]: init_man Bit[3:0]: r_grp_adj
0x3824	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value at vs_ext
0x3825	CS RST FSIN	0x20	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value at vs_ext
0x3826	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value at vs_ext
0x3827	R RST FSIN	0x08	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value at vs_ext
0x3828	REG28	0x40	RW	Bit[7]: Not used Bit[6:0]: r_ablc_num_o
0x3829	MIRROR_FLIP_CUT	0x03	RW	Bit[7:3]: Not used Bit[2]: r_flip_cut_opt Bit[1]: r_flip_cut Bit[0]: r_mirr_cut
0x3832	REG32	0x08	RW	Bit[7:4]: vsync_width Bit[3:0]: r_init_offset

6.9 OTP control [0x3D80 - 0x3D8D, 0x3D90 - 0x3D95]

table 6-9 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: otp_pgenb_o 0: Not used 1: Program ongoing (read only) Bit[6:1]: Not used Bit[0]: OTP_program_enable Write 0 to 1 to start programing (write only)
0x3D81	OTP_LOA_CTRL	–	RW	Bit[7]: OTP_rd_busy 0: Not used 1: OTP load ongoing (read only) Bit[6]: Not used Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[3:1]: Not used Bit[0]: OTP_load_enable
0x3D82	OTP_PGM_PULSE	0x88	RW	Program Strobe Pulse Width Unit: 8 × System Clock Period
0x3D83	OTP_LOAD_PULSE	0x08	RW	Load Strobe Pulse Width Unit: System Clock Period
0x3D84	OTP_MODE_CTRL	0x80	RW	Bit[7]: Program disable 0: Not used 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:1]: Reserved Bit[0]: bank_sram_switch
0x3D85	OTP_REG85	0x1B	RW	Bit[7]: Reserved Bit[6]: r_otp_bist_comp_val Bit[5]: otp_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: OTP power up load data enable Bit[2]: Reserved Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D86	SRAM_TEST_SIGNALS	0x02	RW	Bit[7:6]: Reserved Bit[5]: r_test Bit[4]: r_rme Bit[3:0]: r_rm

table 6-9 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D87	OTP_PS2CS	0x0A	RW	OTP PS to CSB Delay Unit: System Clock Period
0x3D88	OTP_START_ ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_EN_ADDRESS	0x00	RW	OTP End High Address for Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address for Manual Mode
0x3D8C	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start High Address for Load Setting
0x3D8D	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start Low Address for Load Setting
0x3D90	R_BASE_ADR_H	0x00	RW	OTP Base High Address
0x3D91	R_BASE_ADR_L	0x00	RW	OTP Base Low Address
0x3D92	PGENB_TIMING	0xE2	RW	Bit[7:4]: t_pgenb_end Bit[3:0]: t_pgenb_start
0x3D93	VDDQ_TIMING	0x46	RW	Bit[7:4]: t_vddq_end Bit[3:0]: t_vddq_start
0x3D94	OTP_CTRL	0x12	RW	Bit[7:0]: Gap between strobe pulse when programmed
0x3D95	OTP_CTRL	0x06	RW	Bit[7:0]: Gap between strobe pulse when loaded

6.10 BLC [0x4000 - 0x401A, 0x4020 - 0x40BF]

table 6-10 BLC registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x13	RW	Bit[7]: r_img_gfirst_rvs (debug mode) Bit[6]: r_blk_rblue_rvs Option for black row red/blue reverse Bit[5]: r_img_rblue_rvs Option for image row red/blue reverse Bit[4]: r_dc_man Set 1-channel BLC DC offset manually Bit[3]: target_adj_dis Disable adjust final applied target Bit[2]: cmp_en Compensation enable by adding color channel difference when using 1-channel BLC Bit[1]: dither_en Dithering enable Bit[0]: mf_en Median filter enable
0x4001	BLC CTRL01	0x60	RW	Bit[7:6]: Reserved Bit[5]: kcoef_man_en Set dark current coefficient manually Bit[4]: off_man_en Set BLC offset manually Bit[3]: zero_ln_out_en Zero line output enable Bit[2]: blk_ln_out_en Black line output enable Bit[1:0]: byp_mode No black offset will be applied on image
0x4002	BLK LVL TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blk_lvl_target[9:8] BLC target
0x4003	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0] BLC target
0x4004	HWIN OFF	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_off[11:8] Left boundary of BLC window
0x4005	HWIN OFF	0x04	RW	Bit[7:0]: hwin_off[7:0] Left boundary of BLC window

table 6-10 BLC registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x4006	HWIN PAD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_pad[11:8] Right boundary of BLC window
0x4007	HWIN PAD	0x04	RW	Bit[7:0]: hwin_pad[7:0] Right boundary of BLC window
0x4008	BLC CTRL08	0x00	RW	Bit[7:0]: bl_start Black line start position
0x4009	BLC CTRL09	0x0F	RW	Bit[7:0]: bl_end Black line end position
0x400A	OFF LIM TH	0x02	RW	Bit[7:0]: off_lim_th[15:8] Threshold for difference between difference channels in same frame (works only when register 0x4000[3] = 0)
0x400B	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0] Threshold for difference between difference channels in same frame (works only when register 0x4000[3] = 0)
0x400C~ 0x400D	NOT USED	–	–	Not Used
0x400E	BLC CTRL0E	0x00	RW	Bit[7:0]: mf_th Median filter threshold in black line
0x400F	BLC CTRL0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Exposure BLC trigger enable Bit[6]: Debug mode Bit[5:4]: Not used Bit[3]: r_v15_one_channel Pure 1-channel BLC enable Bit[2]: r_en_adp_k Enable adaptive K by average Bit[1]: r_dc_offset_mode Add offset in zero line in 1-channel BLC Bit[0]: r_compute_offset_v15 1-channel BLC enable (black line from whole frame, zero line by channel)

table 6-10 BLC registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x4010	BLC CTRL10	0xF0	RW	Bit[7]: off_trig_en Offset BLC trigger enable Bit[6]: gain_chg_trig_en Gain change BLC trigger enable Bit[5]: fmt_chg_trig_en Format change BLC trigger enable Bit[4]: rst_trig_en Reset BLC trigger enable Bit[3]: man_avg_en BLC average in V BLC manual trigger (works only when 0x4010[2] = 1) Bit[2]: man_trig Manual BLC trigger enable Bit[1]: off_frz_en BLC freeze enable Bit[0]: off_always_up BLC always update enable
0x4011	BLC CTRL11	0xFF	RW	Bit[7]: r_off_cmp_man_en Offset compensation manual enable (works only when 0x4000[2] = 1) Bit[6]: off_chg_multi-frame_en Offset BLC multi-frame trigger enable Bit[5]: fmt_chg_multi-frame_en Format change BLC multi-frame trigger enable Bit[4]: gain_chg_multi-frame_en Gain change BLC multi-frame trigger enable Bit[3]: rst_multi-frame_mode Reset BLC multi-frame trigger enable Bit[2]: off_chg_multi-frame_mode Offset change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value Bit[1]: fmt_chg_multi-frame_mode Format change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value Bit[0]: gain_chg_multi-frame_mode Gain change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value
0x4012	BLC CTRL12	0x08	RW	Bit[7:0]: rst_trig_fn Number of BLC update frames with reset trigger

table 6-10 BLC registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x4013	BLC CTRL13	0x02	RW	Bit[7:0]: fmt_trig_fn Number of BLC update frames with format change trigger
0x4014	BLC CTRL14	0x02	RW	Bit[7:0]: gain_trig_fn Number of BLC update frames with gain change trigger
0x4015	BLC CTRL15	0x02	RW	Bit[7:0]: off_trig_fn Number of BLC update frames with offset trigger
0x4016	OFF TRIG TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_trig_th[9:8] Threshold of offset trigger
0x4017	OFF TRIG TH	0x04	RW	Bit[7:0]: off_trig_th[7:0] Threshold of offset trigger
0x4018	BLC CTRL18	0x00	RW	Bit[7]: r_blk_col_auto Enable mini-row auto on/off mode (works only when 0x4018[3]=1) Bit[6]: r_col_one_ch_o Enable mini-row in 1-channel BLC (works only when 0x4018[3]=1) Bit[5]: r_blk_col_out_en Enable mini-row output (works only when 0x4018[3]=1) Bit[4]: r_blk_col_4ch_en Enable mini-row in normal BLC mode (works only when 0x4018[3]=1) Bit[3]: r_blk_col_en Mini-row enable Bit[2]: fix_BLC_always_update Bit[1]: r_cmp_mirror_man_en Bit[0]: r_cmp_mirror_man
0x4019	BLC CTRL19	0x04	RW	Bit[7:0]: r_blk_ln_num Black input line number (works only when 0x401A[2] = 1)

table 6-10 BLC registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x401A	BLC CTRL1A	0x40	RW	Bit[7]: r_h_size_man_en Bit[6]: r_kcoef_mirror Auto K adjustment with mirror on/off Bit[5]: r_adp_dc_switch_en Enable 1-channel BLC to 4-channel BLC auto switch if DC is high Bit[4]: Debug mode Bit[3]: r_vfpn_en Enable BLC to VFPN cancellation Bit[2]: r_ln_man Black input line manual mode Bit[1]: hdr_nsft BLC for 4-exposure HDR Bit[0]: hdr_en BLC for HDR enable
0x4020	BLC CTRL20	0x00	RW	Bit[7:0]: off_cmp_th0000 Works only when 0x4011[7] = 1
0x4021	BLC CTRL21	0x00	RW	Bit[7:0]: off_cmp_th0001 Works only when 0x4011[7] = 1
0x4022	BLC CTRL22	0x00	RW	Bit[7:0]: off_cmp_th0010 Works only when 0x4011[7] = 1
0x4023	BLC CTRL23	0x00	RW	Bit[7:0]: off_cmp_th0011 Works only when 0x4011[7] = 1
0x4024	BLC CTRL24	0x00	RW	Bit[7:0]: off_cmp_th0100 Works only when 0x4011[7] = 1
0x4025	BLC CTRL25	0x00	RW	Bit[7:0]: off_cmp_th0101 Works only when 0x4011[7] = 1
0x4026	BLC CTRL26	0x00	RW	Bit[7:0]: off_cmp_th0110 Works only when 0x4011[7] = 1
0x4027	BLC CTRL27	0x00	RW	Bit[7:0]: off_cmp_th0111 Works only when 0x4011[7] = 1
0x4028	BLC CTRL28	0x00	RW	Bit[7:0]: off_cmp_th1000 Works only when 0x4011[7] = 1
0x4029	BLC CTRL29	0x00	RW	Bit[7:0]: off_cmp_th1001 Works only when 0x4011[7] = 1
0x402A	BLC CTRL2A	0x00	RW	Bit[7:0]: off_cmp_th1010 Works only when 0x4011[7] = 1
0x402B	BLC CTRL2B	0x00	RW	Bit[7:0]: off_cmp_th1011 Works only when 0x4011[7] = 1
0x402C	BLC CTRL2C	0x00	RW	Bit[7:0]: off_cmp_th1100 Works only when 0x4011[7] = 1

table 6-10 BLC registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x402D	BLC CTRL2D	0x00	RW	Bit[7:0]: off_cmp_th1101 Works only when 0x4011[7] = 1
0x402E	BLC CTRL2E	0x00	RW	Bit[7:0]: off_cmp_th1110 Works only when 0x4011[7] = 1
0x402F	BLC CTRL2F	0x00	RW	Bit[7:0]: off_cmp_th1111 Works only when 0x4011[7] = 1
0x4030~ 0x403F	RSVD	–	–	Reserved
0x4040	OFF MAN0000	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0000[9:8] Works only when 0x4001[4] = 1
0x4041	OFF MAN0000	0x00	RW	Bit[7:0]: off_man0000[7:0] Works only when 0x4001[4] = 1
0x4042	OFF MAN0001	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0001[9:8] Works only when 0x4001[4] = 1
0x4043	OFF MAN0001	0x00	RW	Bit[7:0]: off_man0001[7:0] Works only when 0x4001[4] = 1
0x4044	OFF MAN0010	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0010[9:8] Works only when 0x4001[4] = 1
0x4045	OFF MAN0010	0x00	RW	Bit[7:0]: off_man0010[7:0] Works only when 0x4001[4] = 1
0x4046	OFF MAN0011	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0011[9:8] Works only when 0x4001[4] = 1
0x4047	OFF MAN0011	0x00	RW	Bit[7:0]: off_man0011[7:0] Works only when 0x4001[4] = 1
0x4048	OFF MAN0100	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0100[9:8] Works only when 0x4001[4] = 1
0x4049	OFF MAN0100	0x00	RW	Bit[7:0]: off_man0100[7:0] Works only when 0x4001[4] = 1
0x404A	OFF MAN0101	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0101[9:8] Works only when 0x4001[4] = 1
0x404B	OFF MAN0101	0x00	RW	Bit[7:0]: off_man0101[7:0] Works only when 0x4001[4] = 1

table 6-10 BLC registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x404C	OFF MAN0110	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0110[9:8] Works only when 0x4001[4] = 1
0x404D	OFF MAN0110	0x00	RW	Bit[7:0]: off_man0110[7:0] Works only when 0x4001[4] = 1
0x404E	OFF MAN0111	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0111[9:8] Works only when 0x4001[4] = 1
0x404F	OFF MAN0111	0x00	RW	Bit[7:0]: off_man0111[7:0] Works only when 0x4001[4] = 1
0x4050	BLC CTRL50	0x04	RW	Bit[7:0]: zl_start Zero line start position
0x4051	BLC CTRL51	0x0B	RW	Bit[7:0]: zl_end Zero line end position
0x4052	KCOEF B MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_man[9:8] K for B in manual mode (works only when 0x4001[5] = 1)
0x4053	KCOEF B MAN	0x00	RW	Bit[7:0]: kcoef_b_man[7:0] K for B in manual mode low (works only when 0x4001[5] = 1)
0x4054	KCOEF GB MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gb_man[9:8] K for Gb in manual mode (works only when 0x4001[5] = 1)
0x4055	KCOEF GB MAN	0x00	RW	Bit[7:0]: kcoef_gb_man[7:0] K for Gb in manual mode (works only when 0x4001[5] = 1)
0x4056	KCOEF GR MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gr_man[9:8] K for Gr in manual mode (works only when 0x4001[5] = 1)
0x4057	KCOEF GR MAN	0x00	RW	Bit[7:0]: kcoef_gr_man[7:0] K for Gr in manual mode (works only when 0x4001[5] = 1)
0x4058	KCOEF R MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_r_man[9:8] K for R in manual mode (works only when 0x4001[5] = 1)

table 6-10 BLC registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x4059	KCOEF R MAN	0x00	RW	Bit[7:0]: kcoef_r_man[7:0] K for R in manual mode (works only when 0x4001[5] = 1)
0x405A	BLC CTRL5A	0x30	RW	Bit[7:0]: r_dc_th_1_0 Dark current threshold (works only when 0x401A[5] = 1)
0x405B	BLC CTRL5B	0x18	RW	Bit[7:0]: r_dc_th_2_0 Dark current threshold (works only when 0x401A[5] = 1)
0x405C	BLC CTRL5C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: avg_weight for current frame Weight for multi-frame BLC
0x405D	RND GAIN TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rnd_gain_th[9:8] Gain threshold for dithering (works only when 0x4000[1] = 1)
0x405E	RND GAIN TH	0x00	RW	Bit[7:0]: rnd_gain_th[7:0] Gain threshold for dithering (works only when 0x4000[1] = 1)
0x405F	BLC CTRL5F	0x00	RW	Bit[7:0]: r_dc_th_1_1 Dark current threshold (works only when 0x401A[5] = 1)
0x4060	BLC CTRL60	0x00	RW	Bit[7:0]: r_dc_th_2_1 Dark current threshold (works only when 0x401A[5] = 1)
0x4061	BLC CTRL61	0x00	RW	Bit[7:0]: r_dc_th_1_2 Dark current threshold (works only when 0x401A[5] = 1)
0x4062	BLC CTRL62	0x00	RW	Bit[7:0]: r_dc_th_2_2 Dark current threshold (works only when 0x401A[5] = 1)
0x4063	BLC CTRL63	0x00	RW	Bit[7:0]: r_dc_th_1_3 Dark current threshold (works only when 0x401A[5] = 1)
0x4064	BLC CTRL64	0x00	RW	Bit[7:0]: r_dc_th_2_3 Dark current threshold (works only when 0x401A[5] = 1)
0x4065	ZERO LN NUM	0x00	RW	Bit[7:2]: Not used Bit[1:0]: zero_ln_num[9:8] Zero line number

table 6-10 BLC registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x4066	ZERO LN NUM	0x02	RW	Bit[7:0]: zero_ln_num[7:0] Zero line number
0x4067	COL WIN	0x18	RW	Bit[7:0]: col_win Right boundary for mini-row
0x4068	R COL LOW GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_col_low_gain[9:8] Low gain in mini-row threshold (works only when 0x4018[7]=1)
0x4069	R COL LOW GAIN	0x20	RW	Bit[7:0]: r_col_low_gain[7:0] Low gain in mini-row threshold (works only when 0x4018[7]=1)
0x406A	R COL HIGH GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_col_high_gain[9:8] High gain in mini-row threshold (works only when 0x4018[7]=1)
0x406B	R COL HIGH GAIN	0x40	RW	Bit[7:0]: r_col_high_gain[7:0] High gain in mini-row threshold (works only when 0x4018[7]=1)
0x406C	BLC CTRL6C	0x02	RW	Bit[7:6]: Not used Bit[5]: hdr_llss_option Bit[4]: r_cali_no_mirror_sel Bit[3]: r_col_real_gain_sel Bit[2:0]: Debug mode
0x406D	BLC CTRL6D	0x00	RW	Bit[7:0]: mf_col_th Median filter threshold in mini-row
0x406E	BLC CTRL6E	0x00	RW	Bit[7:0]: h_size_man[15:8]
0x406F	BLC CTRL6F	0x00	RW	Bit[7:0]: h_size_man[7:0]
0x4070~ 0x40AF	DEBUG MODE	–	R	Debug Mode
0x40B0	OFF MAN1000	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1000[9:8] Works only when 0x4001[4] = 1
0x40B1	OFF MAN1000	0x00	RW	Bit[7:0]: off_man1000[7:0] Works only when 0x4001[4] = 1
0x40B2	OFF MAN1001	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1001[9:8] Works only when 0x4001[4] = 1
0x40B3	OFF MAN1001	0x00	RW	Bit[7:0]: off_man1001[7:0] Works only when 0x4001[4] = 1

table 6-10 BLC registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x40B4	OFF MAN1010	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1010[9:8] Works only when 0x4001[4] = 1
0x40B5	OFF MAN1010	0x00	RW	Bit[7:0]: off_man1010[7:0] Works only when 0x4001[4] = 1
0x40B6	OFF MAN1011	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1011[9:8] Works only when 0x4001[4] = 1
0x40B7	OFF MAN1011	0x00	RW	Bit[7:0]: off_man1011[7:0] Works only when 0x4001[4] = 1
0x40B8	OFF MAN1100	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1100[9:8] Works only when 0x4001[4] = 1
0x40B9	OFF MAN1100	0x00	RW	Bit[7:0]: off_man1100[7:0] Works only when 0x4001[4] = 1
0x40BA	OFF MAN1101	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1101[9:8] Works only when 0x4001[4] = 1
0x40BB	OFF MAN1101	0x00	RW	Bit[7:0]: off_man1101[7:0] Works only when 0x4001[4] = 1
0x40BC	OFF MAN1110	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1110[9:8] Works only when 0x4001[4] = 1
0x40BD	OFF MAN1110	0x00	RW	Bit[7:0]: off_man1110[7:0] Works only when 0x4001[4] = 1
0x40BE	OFF MAN1111	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1111[9:8] Works only when 0x4001[4] = 1
0x40BF	OFF MAN1111	0x00	RW	Bit[7:0]: off_man1111[7:0] Works only when 0x4001[4] = 1

6.11 format [0x4300 - 0x4302]

table 6-11 format registers

address	register name	default value	R/W	description
0x4300	CLIP MAX HI	0xFF	RW	Bit[7:0]: clip_max[11:4]
0x4301	CLIP MIN HI	0x00	RW	Bit[7:0]: clip_min[11:4]
0x4302	CLIP LO	0x0F	RW	Bit[7:4]: clip_min[3:0] Bit[3:0]: clip_max[3:0]

6.12 column ADC sync and SYNC_FIFO [0x4500 - 0x450B]

table 6-12 format registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4500	FIFO CTRL	0x05	RW	Bit[7:6]: rblue_option Bit[5]: Not used Bit[4:0]: r_fifo_rdly
0x4501	R1	0x00	RW	Bit[7]: r_skip_man_c Bit[6]: read_mem_alw Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Debug mode 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Debug mode 10: Select first pixel 11: Select last pixel Bit[1]: r_dat_swap Bit[0]: r_srclk_inv
0x4502	R2	0x10	RW	Bit[7:0]: r_data_offset

table 6-12 format registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4503	R3	0x00	RW	Bit[7]: r_bar_en Bit[6]: blk_data_opt 0: Use register value 1: Use px_cnt Bit[5]: zline_data_opt 0: Use register value 1: Use px_cnt Bit[4]: 1st_ramp_data_opt 0: Use register value 1: Use px_cnt Bit[1:0]: bar_style 00: Standard bar 01: Normal to gray by line 10: Normal to gray by pixel 11: Same as line cnt
0x4504	R4	0x00	RW	Bit[7:0]: r_blk_data
0x4505	R5	0x00	RW	Bit[7:0]: r_zline_data
0x4506	R6	0x00	RW	Bit[7:0]: r_1st_ramp_data
0x4507	R7	0x0A	RW	Bit[7:6]: Not used Bit[5]: r_sram_RME Bit[4]: r_sram_test Bit[3:0]: r_sram_RM
0x4508	R8	0x00	RW	Bit[7:3]: Not used Bit[2:0]: sync_fifo_rd_start_point[10:8]
0x4509	R9	0x06	RW	Bit[7:0]: sync_fifo_rd_start_point[7:0]
0x450A	RA	0x04	RW	Bit[7:3]: Not used Bit[2]: sync_fifo_one_line_mode Bit[1]: r_mir_man_en Bit[0]: r_mir_man
0x450B	RB	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Choose VREF input of column ADC 00: vref_i 01: vref_i 10: zline_i 11: VREF

6.13 MIPI [0x4800, 0x4802 - 0x480C, 0x4810 - 0x4814, 0x4818 - 0x484F]

table 6-13 MIPI registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x00	RW	Bit[7:6]: Reserved Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Not used Bit[2]: pclk_inv_o 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[1]: first_bit Change clk_lane first bit 0: Output 0x55 1: Output 0xAA Bit[0]: LPX_select for PCLK domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0]

table 6-13 MIPI registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2] hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL03	0x00	RW	Bit[7:5]: Not used Bit[4]: fifo_rd_spd_o Bit[3]: manu_ofset_o t_perio manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1:0]: Reserved
0x4804	NOT USED	–	–	Not Used

table 6-13 MIPI registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 0: Not used 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 0: Not used 1: Manual
0x4806	MIPI CTRL06	0x00	RW	Bit[7:5]: Not used Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx ul_tx T_lpx
0x4808	MIPI CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4809	MIPI CTRL09	0x04	RW	Bit[7]: hcnt_end_man_en 0: Not used 1: Use r_hcnt_end_man Bit[6]: cs_cnt_end_man 0: Not used 1: cs_cnt rolls over as it reaches r_hcnt_end_man Bit[5:0]: pkt_start_offset
0x480A	MIPI CTRL0A	0x00	RW	Bit[7:0]: r_hcnt_end_man[15:8]
0x480B	MIPI CTRL0B	0x00	RW	Bit[7:0]: r_hcnt_end_man[7:0]
0x480C	MIPI CTRL0B	0x12	RW	Bit[7]: mipi_pkt_start_man Use pkt_start_offset aspacket start offset Bit[6:4]: r_mask_ln_num Real masked line number is 2 × r_mask_ln_num Bit[3:0]: fifo_start_size
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Maximum frame counter of frame sync short packet

table 6-13 MIPI registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Maximum frame counter of frame sync short packet
0x4812	NOT USED	–	–	Not Used
0x4813	MIPI CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2]: vc_sel Bit[1:0] VC ID
0x4814	MIPI CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data type Bit[5:0]: dt_man Manual data type
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] Minimum value of hs_zero, unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Minimum value of hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] Minimum value of hs_trail, unit ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Minimum value of hs_trail, unit ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] Minimum value of clk_zero, unit ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Minimum value of clk_zero, unit ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o

table 6-13 MIPI registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare, unit ns clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] Minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] Minimum value of clk_trail, unit ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Minimum value of clk_trail, unit ns clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] Minimum value of lpx_p, unit ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Minimum value of lpx_p, unit ns lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns

table 6-13 MIPI registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare, unit ns hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] Minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Minimum value of hs_exit, unit ns hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI

table 6-13 MIPI registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI PKT STAR SIZE	0x10	RW	Bit[7:6]: Not used Bit[5:0]: mipi_pkt_star_size[5:0]
0x4834~ 0x4836	NOT USED	–	–	Not Used
0x4837	PCLK PERIOD	0x0E	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div = 1 and 1-bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 6-13 MIPI registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A~ 0x483B	NOT USED	–	–	Not Used
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre Unit pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o
0x483E~ 0x4847	NOT USED	–	–	Not Used

table 6-13 MIPI registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x4848	SEL_MIPI_CTRL48	–	R	Bit[7:0]: mipi_fcnt[15:8]
0x4849	SEL_MIPI_CTRL_49	–	R	Bit[7:0]: mipi_fcnt[7:0]
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA OPTION	0x07	RW	Bit[7:2]: Not used Bit[1]: clk_start_sel_o 0: Clock starts after start of frame 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF occurs 1: Frame starts after start of frame
0x484C	SEL MIPI CTRL4C	0x00	RW	Bit[7:4]: Not used Bit[3]: smia_fcnt_i select Bit[2]: prbs_enable Bit[1]: hs_test_only MIPI high speed only test mode enable Bit[0]: set_frame_cnt_0 Set frame count to inactive mode (set to 0)
0x484D	TEST PATTERN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern
0x484E	FE DLY	0x10	RW	Bit[7:0]: fe_dly Last packet to frame end delay/2
0x484F	TEST PATTERN CK DATA	0x55	RW	Bit[7:2]: Not used Bit[1:0]: clk_test_patten_reg

6.14 ISPFC [0x4900 - 0x4903]

table 6-14 ISPFC registers

address	register name	default value	R/W	description
0x4900	R0	0x00	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4901	R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4902	R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4903	R3	0x00	RW	Bit[7]: zero_line_mask_dis Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.15 temperature sensor [0x4D00 - 0x4D14]

table 6-15 temperature sensor registers

address	register name	default value	R/W	description
0x4D00~ 0x4D0F	TPM_CTRL_REG	–	–	Temperature Sensor Control Registers
0x4D10	TPM_CTRL_10	0x00	RW	Bit[7:0]: r_tpm_min
0x4D11	TPM_CTRL_11	0xFF	RW	Bit[7:0]: r_tpm_max
0x4D12	TPM CTRL12	–	W	Writing 0x4D12[0] to '1' Will Trigger Temperature Calculating, Then registers 0x4D12 and 0x4D13 Will Be Latched Temperature Value
0x4D13	TPM CTRL13	–	R	Latched Temperature Value, Integer Part
0x4D14	TPM CTRL14	–	R	Latched Temperature Value, Decimal Part

6.16 DSP [0x5000 - 0x502C, 0x502E - 0x5038, 0x5040 - 0x5049]

table 6-16 DSP registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xED	RW	Bit[7]: WIN enable Bit[6]: Reserved Bit[5]: DPC enable Bit[4]: OTP enable Bit[3]: WB_gain enable Bit[2]: LENC enable Bit[1]: PD BYP enable Bit[0]: ISP enable
0x5001	ISP_CTRL_1	0x07	RW	Bit[7:4]: Reserved Bit[3]: Control signal latch mode 0: Enable will be valid immediately 1: Enable will be valid at next frame Bit[2]: Before LENC PD enable 0: PD erase after LENC 1: PD erase before LENC Bit[1]: PD pix check enable for DPC Bit[0]: Rst_protect enable 0: ISP will input href_i in real time 1: After reset, ISP will not input href_i to internal sub-modules before next image
0x5002	ISP_CTRL_2	0x00	RW	Bit[7]: Manual flip Bit[6]: Manual mirror Bit[5]: Manual HDR pattern Bit[4]: Manual work mode Bit[3]: Flip manual mode Bit[2]: Mirror manual mode Bit[1]: HDR pattern manual mode Bit[0]: Work mode manual mode

table 6-16 DSP registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x5003	ISP_CTRL_3	0x00	RW	Bit[7]: SOF select 0: Pre-ISP output SOF 1: ISP input first pixel Bit[6]: EOF select 0: Last input pixel that ISP process except window 1: Window output EOF Bit[5:4]: Manual CFA pattern Bit[3]: Exposure manual mode Bit[2]: Real gain manual mode Bit[1]: BLC manual mode Bit[0]: CFA pattern manual mode
0x5004	ISP_CTRL_4	0x00	RW	Bit[7:5]: Reserved Bit[4]: PD pix check manual enable for L exposure Bit[3]: PD pix check manual enable for S exposure Bit[2]: PD location manual mode Bit[1]: Image size manual mode Bit[0]: ISP module work manual mode
0x5005	ISP_CTRL_5	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: m_nMF option for PDBypass
0x5006	ISP_CTRL_6	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual real gain0[11:8] for long exposure
0x5007	ISP_CTRL_7	0x10	RW	Bit[7:0]: Manual real gain0[7:0] for long exposure
0x5008	ISP_CTRL_8	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual real gain1[11:8] for short exposure
0x5009	ISP_CTRL_9	0x10	RW	Bit[7:0]: Manual real gain1[7:0] for short exposure
0x500A	ISP_CTRL_10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC0[9:8] for long exposure
0x500B	ISP_CTRL_11	0x10	RW	Bit[7:0]: Manual BLC0[7:0] for long exposure
0x500C	ISP_CTRL_12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC1[9:8] for short exposure
0x500D	ISP_CTRL_13	0x10	RW	Bit[7:0]: Manual BLC1[7:0] for short exposure

table 6-16 DSP registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x500E	ISP_CTRL_14	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual long expo[19:16]
0x500F	ISP_CTRL_15	0x00	RW	Bit[7:0]: Manual long expo[15:8]
0x5010	ISP_CTRL_16	0x10	RW	Bit[7:0]: Manual long expo[7:0]
0x5011	RSVD	–	–	Reserved
0x5012	ISP_CTRL_18	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Manual Hsize[12:8]
0x5013	ISP_CTRL_19	0x80	RW	Bit[7:0]: Manual Hsize[7:0]
0x5014	ISP_CTRL_20	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Manual Vsize[11:8]
0x5015	ISP_CTRL_21	0x40	RW	Bit[7:0]: Manual Hsize[7:0]
0x5016	ISP_CTRL_22	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual L m_nPDCycleX for normal mode and HDR mode long exposure
0x5017	ISP_CTRL_23	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual L m_nPDCycleY for normal mode and HDR mode long exposure
0x5018	ISP_CTRL_24	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDY for normal mode and HDR mode long exposure
0x5019	ISP_CTRL_25	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX1 for normal mode and HDR mode long exposure
0x501A	ISP_CTRL_26	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX2 for normal mode and HDR mode long exposure
0x501B	ISP_CTRL_27	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX3 for normal mode and HDR mode long exposure
0x501C	ISP_CTRL_28	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX4 for normal mode and HDR mode long exposure

table 6-16 DSP registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x501E	ISP_CTRL_30	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinXStart[11:8] for normal mode and HDR mode long exposure
0x501F	ISP_CTRL_31	0x40	RW	Bit[7:0]: Manual L m_nWinXStart[7:0] for normal mode and HDR mode long exposure
0x5020	ISP_CTRL_32	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinYStart[11:8] for normal mode and HDR mode long exposure
0x5021	ISP_CTRL_33	0x40	RW	Bit[7:0]: Manual L m_nWinYStart[7:0] for normal mode and HDR mode long exposure
0x5022	ISP_CTRL_34	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nWinWidth[12:8] for normal mode and HDR mode long exposure
0x5023	ISP_CTRL_35	0x80	RW	Bit[7:0]: Manual L m_nWinWidth[7:0] for normal mode and HDR mode long exposure
0x5024	ISP_CTRL_36	0x0B	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinHeight[11:8] for normal mode and HDR mode long exposure
0x5025	ISP_CTRL_37	0x40	RW	Bit[7:0]: Manual L m_nWinHeight[7:0] for normal mode and HDR mode long exposure
0x5026	ISP_CTRL_38	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual S m_nPDCycleX for HDR mode short exposure
0x5027	ISP_CTRL_39	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual S m_nPDCycleY for HDR mode short exposure
0x5028	ISP_CTRL_40	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDY for HDR mode short exposure
0x5029	ISP_CTRL_41	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX1 for HDR mode short exposure

table 6-16 DSP registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x502A	ISP_CTRL_42	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX2 for HDR mode short exposure
0x502B	ISP_CTRL_43	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX3 for HDR mode short exposure
0x502C	ISP_CTRL_44	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX4 for HDR mode short exposure
0x502E	ISP_CTRL_46	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinXStart[11:8] for HDR mode short exposure
0x502F	ISP_CTRL_47	0x40	RW	Bit[7:0]: Manual S m_nWinXStart[7:0] for HDR mode short exposure
0x5030	ISP_CTRL_48	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinYStart[11:8] for HDR mode short exposure
0x5031	ISP_CTRL_49	0x40	RW	Bit[7:0]: Manual S m_nWinYStart[7:0] for HDR mode short exposure
0x5032	ISP_CTRL_50	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nWinWidth[12:8] for HDR mode short exposure
0x5033	ISP_CTRL_51	0x80	RW	Bit[7:0]: Manual S m_nWinWidth[7:0] for HDR mode short exposure
0x5034	ISP_CTRL_52	0x0B	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinHeight[11:8] for HDR mode short exposure
0x5035	ISP_CTRL_53	0x40	RW	Bit[7:0]: Manual S m_nWinHeight[7:0] for HDR mode short exposure

table 6-16 DSP registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5036	ISP_CTRL_54	0x00	RW	Bit[7]: Disable module window gate clock operation Bit[6]: Debug mode Bit[5]: Disable module DPC gate clock operation Bit[4]: Disable module PDByass gate clock operation Bit[3]: Disable module OTP gate clock operation Bit[2]: Disable module WB_gain gate clock operation Bit[1]: Disable module LENC gate clock operation Bit[0]: Disable Module ISP_top gate clock operation 0: Enable 1: Disable
0x5037	ISP_CTRL_55	0x00	RW	Bit[7:3]: Reserved Bit[2]: Disable gate clock operation during Vblank time Bit[1]: Disable gate clock operation during Hblank time Bit[0]: Disable all gate clock operation in ISP
0x5038	ISP_CTRL_56	0x00	RW	Bit[7:6]: Reserved Bit[5:2]: DPC SRAM RM (read margin) Bit[1]: DPC SRAM RME (read margin enable) Bit[0]: DPC SRAM test1
0x5040	ISP_CTRL_64	0x19	RW	Bit[7:6]: Not used Bit[5]: blc_dig_gain_option 0: Debug mode 1: Use 0x350A, 0x350E for digital gain control Bit[4]: blc_vsync_sel_option Bit[3]: dcblc_en Bit[2:1]: Debug mode Bit[0]: blc_en
0x5041	ISP_CTRL_65	0x50	RW	Bit[7:0]: PD window x offset for auto calculation mode
0x5042	NOT USED	–	–	Not Used
0x5043	ISP_CTRL_67	0x80	RW	Bit[7:0]: PD window width div 32 for auto calculation mode
0x5044	ISP_CTRL_68	0x5E	RW	Bit[7:0]: PD window height div 32 for auto calculation mode

table 6-16 DSP registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x5045	ISP_CTRL_69	0x20	RW	Bit[7:6]: Not used Bit[5:4]: PD map y offset for auto calculation mode Bit[3:1]: Not used Bit[0]: PD map y offset in sub2 format for auto
0x5046	ISP_CTRL_70	0x20	RW	Bit[7:4]: PD map x1 offset for auto calculation mode Bit[3]: Not used Bit[2:0]: PD map x1 offset in sub2 format for auto calculation mode
0x5047	ISP_CTRL_71	0xA4	RW	Bit[7:4]: PD map x2 offset for auto calculation mode Bit[3]: Not used Bit[2:0]: PD map x2 offset in sub2 format for auto calculation mode
0x5048	ISP_CTRL_72	0x20	RW	Bit[7:4]: PD map x3 offset for auto calculation mode Bit[3]: Not used Bit[2:0]: PD map x3 offset in sub2 format for auto calculation mode
0x5049	ISP_CTRL_73	0xA4	RW	Bit[7:4]: PD map x4 offset for auto calculation mode Bit[3]: Not used Bit[2:0]: PD map x4 offset in sub2 format for auto calculation mode

6.17 pre_ISP [0x5080 - 0x5091, 0x50A0 - 0x50AF, 0x050B2 - 0x50B5]

table 6-17 pre_ISP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5080	ISP_CTRL_0	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling enable (rolling bar in test mode) Bit[5]: Transparent effect enable Bit[4]: Black/white or color square selection 0: Color 1: black/white Bit[3:2]: Color bar style Bit[1:0]: Test mode select
0x5081	ISP_CTRL_1	0x01	RW	Bit[7]: Reserved Bit[6]: Window cut enable Bit[5]: ISP test enable Low bits to 0 Bit[4]: Random mode frame-fixed seed enable Bit[3:0]: Random seed
0x5082	ISP_CTRL_2	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Line number interrupt[12:8]
0x5083	ISP_CTRL_3	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x5084~ 0x5087	RSVD	–	–	Reserved
0x5088	ISP_CTRL_8	0x00	RW	Bit[7:5]: Not used Bit[4:0]: X manual offset[12:8]
0x5089	ISP_CTRL_9	0x00	RW	Bit[7:0]: X manual offset[7:0]
0x508A	ISP_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y manual offset[11:8]
0x508B	ISP_CTRL_11	0x00	RW	Bit[7:0]: Y manual offset[7:0]
0x508C	ISP_CTRL_12	0x30	RW	Bit[7:6]: Reserved Bit[5]: Mirror option for x offset Bit[4]: Flip option for y offset Bit[3:2]: Reserved Bit[1]: Offset manual enable 0: Disable 1: Enable Bit[0]: Reserved
0x508D	ISP_CTRL_13	0x00	RW	Bit[7:0]: Reserved
0x508E	ISP_CTRL_14	0x01	RW	Bit[7:0]: Long/short ratio integer ratio part (short based mode) All 0 in HDR2 long based mode

table 6-17 pre_ISP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x508F	ISP_CTRL_15	0x80	RW	Bit[7:0]: Long/short ratio fraction part Short/long ratio in HDR2 long based mode
0x5090~ 0x5091	RSVD	–	–	Reserved
0x50A0	ISP_CTRL_32	–	R	Bit[7:4]: X odd inc[3:0] Bit[3:0]: Y odd inc[3:0]
0x50A1	ISP_CTRL_33	–	R	Bit[7:5]: Not used Bit[4:0]: X offset[12:8]
0x50A2	ISP_CTRL_34	–	R	Bit[7:0]: X offset[7:0]
0x50A3	ISP_CTRL_35	–	R	Bit[7:4]: Not used Bit[3:0]: Y offset[11:8]
0x50A4	ISP_CTRL_36	–	R	Bit[7:0]: Y offset[7:0]
0x50A5	ISP_CTRL_37	–	R	Bit[7:5]: Not used Bit[4:0]: Win x offset[12:8]
0x50A6	ISP_CTRL_38	–	R	Bit[7:0]: Win x offset[7:0]
0x50A7	ISP_CTRL_39	–	R	Bit[7:4]: Not used Bit[3:0]: Win y offset[11:8]
0x50A8	ISP_CTRL_40	–	R	Bit[7:0]: Win y offset[7:0]
0x50A9	ISP_CTRL_41	–	R	Bit[7:5]: Not used Bit[4:0]: Win x output size[12:8]
0x50AA	ISP_CTRL_42	–	R	Bit[7:0]: Win x output size, bit[7:0]
0x50AB	ISP_CTRL_43	–	R	Bit[7:4]: Not used Bit[3:0]: Win x output size[11:8]
0x50AC	ISP_CTRL_44	–	R	Bit[7:0]: Win x output size[7:0]
0x50AD	ISP_CTRL_45	–	R	Bit[7:6]: Reserved Bit[5:4]: X skip Horizontal skip Bit[3:2]: Reserved Bit[1:0]: Y skip Vertical skip
0x50AE	ISP_CTRL_46	–	R	Bit[7:4]: X even inc[3:0] Bit[3:0]: Y even inc[3:0]
0x50AF	ISP_CTRL_47	–	R	Bit[7:4]: Reserved Bit[3]: X odd inc[4] Bit[2]: Y odd inc[4] Bit[1]: X even inc[4] Bit[0]: Y even inc[4]

table 6-17 pre_ISP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x50B2	ISP_CTRL_50	–	R	Bit[7:5]: Not used Bit[4:0]: Pixel number[12:8]
0x50B3	ISP_CTRL_51	–	R	Bit[7:0]: Pixel number[7:0]
0x50B4	ISP_CTRL_52	–	R	Bit[7:4]: Not used Bit[3:0]: Line number[11:8]
0x50B5	ISP_CTRL_53	–	R	Bit[7:0]: Line number[7:0]

6.18 WB_gain for long exposure [0x5100 - 0x5107]

table 6-18 WB_gain for long exposure registers

address	register name	default value	R/W	description
0x5100	MWB GAIN00	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_B[14:8] MWB gain in blue channel
0x5101	MWB GAIN01	0x00	RW	Bit[7:0]: wb_gain_B[7:0] MWB gain in blue channel
0x5102	MWB GAIN02	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_G[14:8] MWB gain in green channel
0x5103	MWB GAIN03	0x00	RW	Bit[7:0]: wb_gain_G[7:0] MWB gain in green channel
0x5104	MWB GAIN04	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_R[14:8] MWB gain in red channel
0x5105	MWB GAIN05	0x00	RW	Bit[7:0]: wb_gain_R[7:0] MWB gain in red channel
0x5106	MWB GAIN06	0x00	RW	Bit[7:1]: Not used Bit[0]: wb_gain_sel 0: MWB control selection 1: Debug mode
0x5107	ISP_CTRL_7	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Manual CFA pattern Bit[3:1]: Not used Bit[0]: Manual CFA pattern enable

6.19 WB_gain for short exposure [0x5140 - 0x5147]

table 6-19 WB_gain for short exposure registers

address	register name	default value	R/W	description
0x5140	ISP_CTRL_0	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_B[14:8] MWB gain in blue channel
0x5141	ISP_CTRL_1	0x00	RW	Bit[7:0]: wb_gain_B[7:0] MWB gain in blue channel
0x5142	ISP_CTRL_2	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_G[14:8] MWB gain in green channel
0x5143	ISP_CTRL_3	0x00	RW	Bit[7:0]: wb_gain_G[7:0] MWB gain in green channel
0x5144	ISP_CTRL_4	0x04	RW	Bit[7]: Not used Bit[6:0]: wb_gain_R[14:8] MWB gain in red channel
0x5145	ISP_CTRL_5	0x00	RW	Bit[7:0]: wb_gain_R[7:0] MWB gain in red channel
0x5146	ISP_CTRL_6	0x00	RW	Bit[7:1]: Not used Bit[0]: wb_gain_sel 0: MWB control selection 1: Debug mode
0x5147	ISP_CTRL_7	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Manual CFA pattern Bit[3:1]: Not used Bit[0]: Manual CFA pattern enable

6.20 DPC [0x5180 - 0x51A6, 0x5200 - 0x5214, 0x5218 - 0x521F, 0x5280 - 0x529F]

table 6-20 is for long exposure. 0x0080 is added to the long exposure register addresses for the short exposure register addresses. Registers 0x5280~0x529F are for short exposure registers (definitions are same as long exposure).

table 6-20 DPC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5180~ 0x51A6	OTP CTRL	–	–	OTP Control
0x5200	ISP_CTRL_0	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5201	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5202	ISP_CTRL_2	0x2E	RW	Bit[7:6]: Not used Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list[3]
0x5203	ISP_CTRL_3	0x24	RW	Bit[7]: Not used Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
0x5204	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]
0x5205	ISP_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
0x5206	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5207	ISP_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5208	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold

table 6-20 DPC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5209	ISP_CTRL_9	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate pixel threshold for clusters
0x520A	ISP_CTRL_10	0x03	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[0]
0x520B	ISP_CTRL_11	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[1]
0x520C	ISP_CTRL_12	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[2]
0x520D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
0x520E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
0x520F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
0x5210	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]
0x5211~ 0x5213	RSVD	–	–	Reserved
0x5214	ISP_CTRL_20	0x00	RW	Bit[7]: Recover clock gate disable Bit[6]: Recover clock gate disable Bit[5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
0x5218	ISP_CTRL_24	–	R	Bit[7]: Not used Bit[6:0]: Bthre
0x5219	ISP_CTRL_25	–	R	Bit[7:5]: Not used Bit[4:0]: Wthre
0x521A	ISP_CTRL_26	–	R	Bit[7:5]: Not used Bit[4:0]: Thre1
0x521B	ISP_CTRL_27	–	R	Bit[7:0]: Thre2
0x521C	ISP_CTRL_28	–	R	Bit[7]: Not used Bit[6:0]: Thre3
0x521D	ISP_CTRL_29	–	R	Bit[7]: Not used Bit[6:0]: Thre4
0x521E	ISP_CTRL_30	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected

table 6-20 DPC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x521F	ISP_CTRL_31	–	R	Bit[7:3]: Not used Bit[2:0]: Vnum
0x5280~ 0x529F	DPC CONTROL FOR SHORT EXPOSURE	–	–	DPC Control for Short Exposure

6.21 LENC [0x5400 - 0x540F, 0x5500 - 0x5667]

table 6-21 LENC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5400	LENC_CTRL_0	0x60	RW	Bit[7:0]: Maxgain threshold
0x5401	LENC_CTRL_1	0x40	RW	Bit[7:0]: Mingain threshold
0x5402	LENC_CTRL_2	0x40	RW	Bit[7]: Not used Bit[6:0]: Maxq Apply maximum amplitude
0x5403	LENC_CTRL_3	0x18	RW	Bit[7]: Not used Bit[6:0]: Minq Apply minimum amplitude
0x5404	LENC_CTRL_4	0x36	RW	Bit[7:6]: Not used Bit[5]: BLC add enable Must be set to 1 Bit[4]: BLC enable Must be set to 1 Bit[3]: Enable 2x blue/red gain Must be set to 0 Bit[2]: m_nQ auto calculate enable Must be set to 1 Bit[1]: Enable dithering function to avoid lost bit Bit[0]: Enable 2x green gain
0x5405	LENC_CTRL_5	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Horizontal scale[12:8]
0x5406	LENC_CTRL_6	0xE1	RW	Bit[7:0]: Horizontal scale[7:0]
0x5407	LENC_CTRL_7	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Vertical scale[11:8]
0x5408	LENC_CTRL_8	0x41	RW	Bit[7:0]: Vertical scale[7:0]

table 6-21 LENC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5409	LENC_CTRL_9	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x540A	LENC_CTRL_A	–	R	Bit[7:0]: x_offset[[7:0]
0x540B	LENC_CTRL_B	–	R	Bit[7:4]: Not used Bit[3:0]: y_offset[11:8]
0x540C	LENC_CTRL_C	–	R	Bit[7:0]: y_offset[7:0]
0x540D	LENC_CTRL_D	–	R	Bit[7:6]: Not used Bit[5]: Flip Bit[4]: Mirror Bit[3:2]: y_skip Bit[1:0]: x_skip
0x540E	LENC_CTRL_E	–	R	Bit[7:2]: Not used Bit[1]: overflow_v Bit[0]: overflow_h
0x540F	LENC_CTRL_F	–	R	Bit[7]: Not used Bit[6:0]: m_nq
0x5500	LENC_MT_CTRL_000	0x80	RW	Bit[7:0]: LENC matrix, G channel, G00
0x5501	LENC_MT_CTRL_001	0x80	RW	Bit[7:0]: LENC matrix, G channel, G01
0x5502	LENC_MT_CTRL_002	0x80	RW	Bit[7:0]: LENC matrix, G channel, G02
0x5503	LENC_MT_CTRL_003	0x80	RW	Bit[7:0]: LENC matrix, G channel, G03
0x5504	LENC_MT_CTRL_004	0x80	RW	Bit[7:0]: LENC matrix, G channel, G04
0x5505	LENC_MT_CTRL_005	0x80	RW	Bit[7:0]: LENC matrix, G channel, G05
0x5506	LENC_MT_CTRL_006	0x80	RW	Bit[7:0]: LENC matrix, G channel, G06
0x5507	LENC_MT_CTRL_007	0x80	RW	Bit[7:0]: LENC matrix, G channel, G07
0x5508	LENC_MT_CTRL_008	0x80	RW	Bit[7:0]: LENC matrix, G channel, G08
0x5509	LENC_MT_CTRL_009	0x80	RW	Bit[7:0]: LENC matrix, G channel, G09
0x550A~ 0x5513	LENC_MT_CTRL_00A~ LENC_MT_CTRL_013	0x80	RW	Bit[7:0]: LENC matrix, G channel, G10~G19
0x5514~ 0x551D	LENC_MT_CTRL_014~ LENC_MT_CTRL_01D	0x80	RW	Bit[7:0]: LENC matrix, G channel, G20~G29
0x551E~ 0x5527	LENC_MT_CTRL_01E~ LENC_MT_CTRL_027	0x80	RW	Bit[7:0]: LENC matrix, G channel, G30~G39
0x5528~ 0x5531	LENC_MT_CTRL_028~ LENC_MT_CTRL_031	0x80	RW	Bit[7:0]: LENC matrix, G channel, G40~G49

table 6-21 LENC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5532~ 0x553B	LENC_MT_CTRL_032~ LENC_MT_CTRL_03B	0x80	RW	Bit[7:0]: LENC matrix, G channel, G50~G59
0x553C~ 0x5545	LENC_MT_CTRL_03C~ LENC_MT_CTRL_045	0x80	RW	Bit[7:0]: LENC matrix, G channel, G60~G69
0x5546~ 0x554F	LENC_MT_CTRL_046~ LENC_MT_CTRL_04F	0x80	RW	Bit[7:0]: LENC matrix, G channel, G70~G79
0x5550~ 0x5559	LENC_MT_CTRL_050~ LENC_MT_CTRL_059	0x80	RW	Bit[7:0]: LENC matrix, G channel, G80~G89
0x555A~ 0x5563	LENC_MT_CTRL_05A~ LENC_MT_CTRL_063	0x80	RW	Bit[7:0]: LENC matrix, G channel, G90~G99
0x5564~ 0x556D	LENC_MT_CTRL_064~ LENC_MT_CTRL_06D	0x80	RW	Bit[7:0]: LENC matrix, G channel, GA0~GA9
0x556E~ 0x5577	LENC_MT_CTRL_06E~ LENC_MT_CTRL_077	0x80	RW	Bit[7:0]: LENC matrix, G channel, GB0~GB9
0x5578~ 0x55EF	LENC_MT_CTRL_078~ LENC_MT_CTRL_0EF	0x80	RW	Bit[7:0]: LENC matrix, B channel, same as G channel, B00~BB9
0x55F0~ 0x5667	LENC_MT_CTRL_0F0~ LENC_MT_CTRL_167	0x80	RW	Bit[7:0]: LENC matrix, R channel, same as G channel, R00~RB9

6.22 WINC control [0x5800 - 0x5813]

table 6-22 WINC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5800	ISP_CTRL_0	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Window X start[12:8]
0x5801	ISP_CTRL_1	0x00	RW	Bit[7:0]: Window X start[7:0]
0x5802	ISP_CTRL_2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Window Y start[11:8]
0x5803	ISP_CTRL_3	0x00	RW	Bit[7:0]: Window Y start[7:0]
0x5804	ISP_CTRL_4	0x02	RW	Bit[7:5]: Not used Bit[4:0]: Window width[12:8]
0x5805	ISP_CTRL_5	0x80	RW	Bit[7:0]: Window width[7:0]
0x5806	ISP_CTRL_6	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Window height[11:8]

table 6-22 WINC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5807	ISP_CTRL_7	0xE0	RW	Bit[7:0]: Window height[7:0]
0x5808	ISP_CTRL_8	0x00	RW	Bit[7:4]: Embedded line number Bit[3]: Not used Bit[2]: emb_flag_sel 0: Start line 1: End line Bit[1]: Not used Bit[0]: win_man_en 0: Window size from window top 1: Window size from register
0x5809	ISP_CTRL_9	0xE0	RW	Bit[7:4]: Not used Bit[3:0]: Window height extent line number
0x580A	ISP_CTRL_10	0x00	RW	Bit[7:0]: Minus Y offset
0x5810	ISP_CTRL_16	–	R	Bit[7:5]: Not used Bit[4:0]: Pixel count[12:8]
0x5811	ISP_CTRL_17	–	R	Bit[7:0]: Pixel count[7:0]
0x5812	ISP_CTRL_18	–	R	Bit[7:4]: Not used Bit[3:0]: Line count[11:8]
0x5813	ISP_CTRL_19	–	R	Bit[7:0]: Line count[7:0]

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 30 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core for 2-lane MIPI up to 900 Mbps/lane)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current[b]		36		mA
I_{DD-IO}			3		mA
I_{DD-D}[c]			106		mA
$I_{DDS-SCCB}$	standby current[d]		1		mA
$I_{DDS-XSHUTDN}$			2		µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[e]	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.28	1.8	3.0	V

a. maximum active current is measured under typical supply voltage

b. DVDD is provided by the external regulator. DVDD and EVDD are tied together. DOVDD = 1.8V

c. data is based on ISP ON

d. standby current is measured at room temperature with external clock off

e. based on DOVDD = 1.8V

7.4 timing characteristics

table 7-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (EXTCLK)[a]	6	24	27	MHz
t_r, t_f	clock input rise/fall time			(see footnote [b])	ns
	clock input duty cycle	45	50	55	%

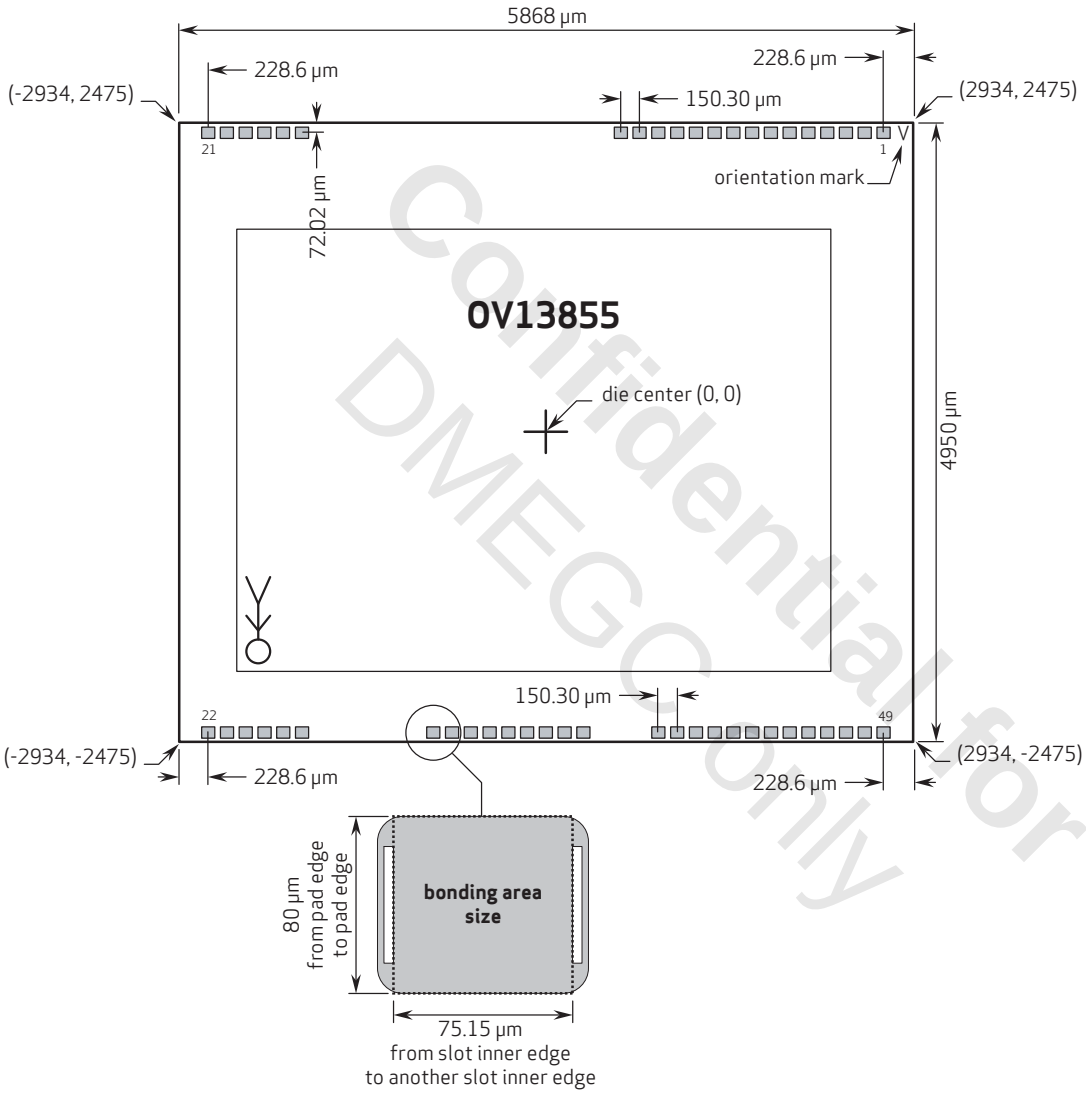
a. for input clock range 6~27MHz, the OV13855 can tolerate input clock period jitter up to 600ps peak-to-peak

b. for clock input rise/fall time, max is 27% of whole clock period

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note all dimensions and coordinates are in µm unless otherwise specified.

13855_COB_DS_8_1

table 8-1 pad location coordinates (sheet 1 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
1	DVDD	2705.400	2402.982	75.15x80
2	DOGND	2555.100	2402.982	75.15x80
3	AGND	2404.800	2402.982	75.15x80
4	AVDD	2254.500	2402.982	75.15x80
5	SID	2104.200	2402.982	75.15x80
6	FSIN	1953.900	2402.982	75.15x80
7	SDA	1803.600	2402.982	75.15x80
8	SCL	1653.300	2402.982	75.15x80
9	XSHUTDN	1503.000	2402.982	75.15x80
10	TM	1352.700	2402.982	75.15x80
11	DOVDD	1202.400	2402.982	75.15x80
12	EXTCLK	1052.100	2402.982	75.15x80
13	DOGND	901.800	2402.982	75.15x80
14	DVDD	751.500	2402.982	75.15x80
15	VSYNC	601.200	2402.982	75.15x80
16	DOGND	-1953.900	2402.982	75.15x80
17	DVDD	-2104.200	2402.982	75.15x80
18	DVDD	-2254.500	2402.982	75.15x80
19	DOGND	-2404.800	2402.982	75.15x80
20	AVDD	-2555.100	2402.982	75.15x80
21	AGND	-2705.400	2402.982	75.15x80
22	ATEST	-2705.400	-2402.982	75.15x80
23	AVDD	-2555.100	-2402.982	75.15x80
24	AGND	-2404.800	-2402.982	75.15x80
25	VH	-2254.500	-2402.982	75.15x80
26	VN1	-2104.200	-2402.982	75.15x80
27	VN2	-1953.900	-2402.982	75.15x80
28	DVDD	-901.800	-2402.982	75.15x80
29	DOGND	-751.500	-2402.982	75.15x80
30	MDP2	-601.200	-2402.982	75.15x80
31	MDN2	-450.900	-2402.982	75.15x80

table 8-1 pad location coordinates (sheet 2 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
32	MDP0	-300.600	-2402.982	75.15x80
33	MDN0	-150.300	-2402.982	75.15x80
34	EGND	0.000	-2402.982	75.15x80
35	PVDD	150.300	-2402.982	75.15x80
36	EVDD	300.600	-2402.982	75.15x80
37	MCP	901.800	-2402.982	75.15x80
38	MCN	1052.100	-2402.982	75.15x80
39	EGND	1202.400	-2402.982	75.15x80
40	MDP1	1352.700	-2402.982	75.15x80
41	MDN1	1503.000	-2402.982	75.15x80
42	EVDD	1653.300	-2402.982	75.15x80
43	MDP3	1803.600	-2402.982	75.15x80
44	MDN3	1953.900	-2402.982	75.15x80
45	DOVDD	2104.200	-2402.982	75.15x80
46	DVDD	2254.500	-2402.982	75.15x80
47	DVDD	2404.800	-2402.982	75.15x80
48	DOGND	2555.100	-2402.982	75.15x80
49	DOGND	2705.400	-2402.982	75.15x80

8.2 reconstructed wafer (RW) physical specifications

- maximum total die count: 829
- film frame: Compact Disco Stainless SUS420
- carrier tape: UV tape

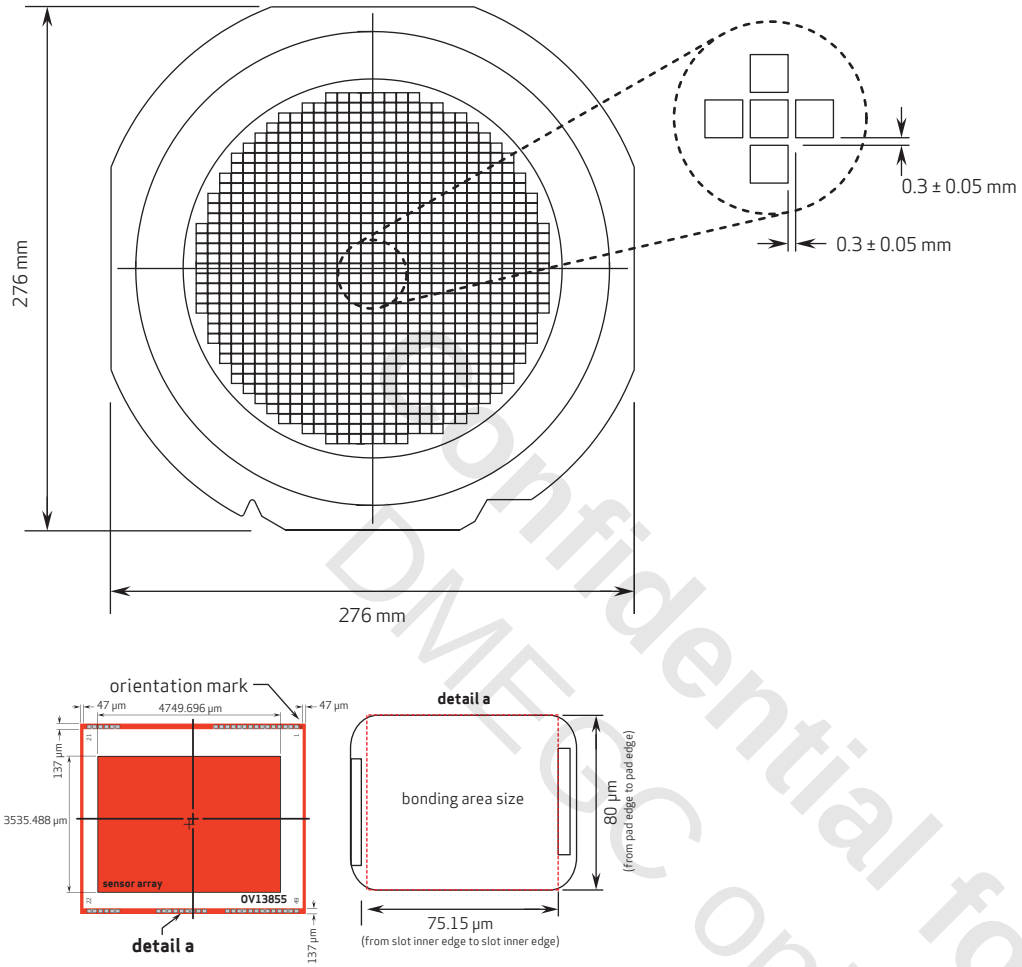
note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=4	200 µm ± 10 µm (7.9 mil ± 0.4 mil)
C=5	150 µm ± 10 µm (5.9 mil ± 0.4 mil)
reconstructed wafer street width	300 µm ± 50 µm (11.8 mil ± 2 mil)
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1.0 degree
singulated die size	
width	5918 µm ± 20 µm (232.99 mil ± 0.8 mil)
length	5000 µm ± 20 µm (196.85 mil ± 0.8 mil)
bond pad size	93.15 µm × 80 µm (3.67 mil × 3.1 mil)
minimum bond pad pitch	150.3 µm (5.9 mil)
bonding area size	75.15 µm × 80 µm (2.96 mil × 3.1 mil)
optical array	
die center	(0, 0)
optical center from die center[a]	-99 µm, -144 µm (-3.9 mil, -5.67 mil)

a. based on die orientation on frame with notch facing down position

figure 8-2 OV13855 RW physical diagram



note 1 bonding outside the defined bonding area is prohibited, it may potentially induce reliablity issues or functionality failure

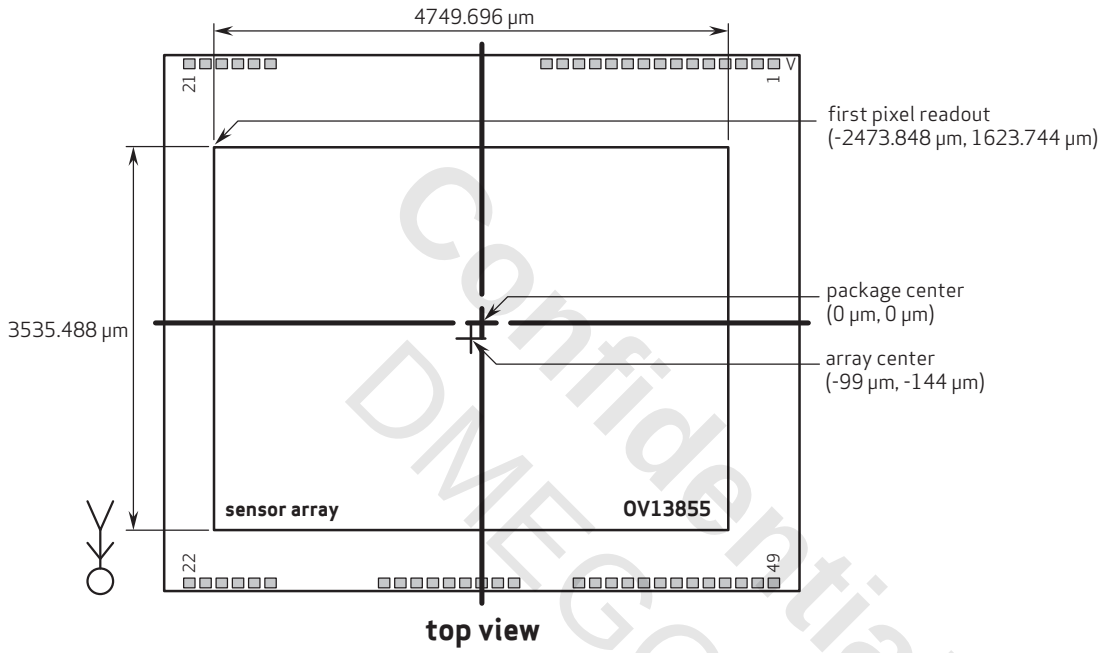
note 2 keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g. nozzle, collets, etc.)

13855_COB_DS_8_2

9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

13855_COB_DS_9_1

9.2 lens chief ray angle (CRA)

figure 9-2 chief ray angle (CRA)

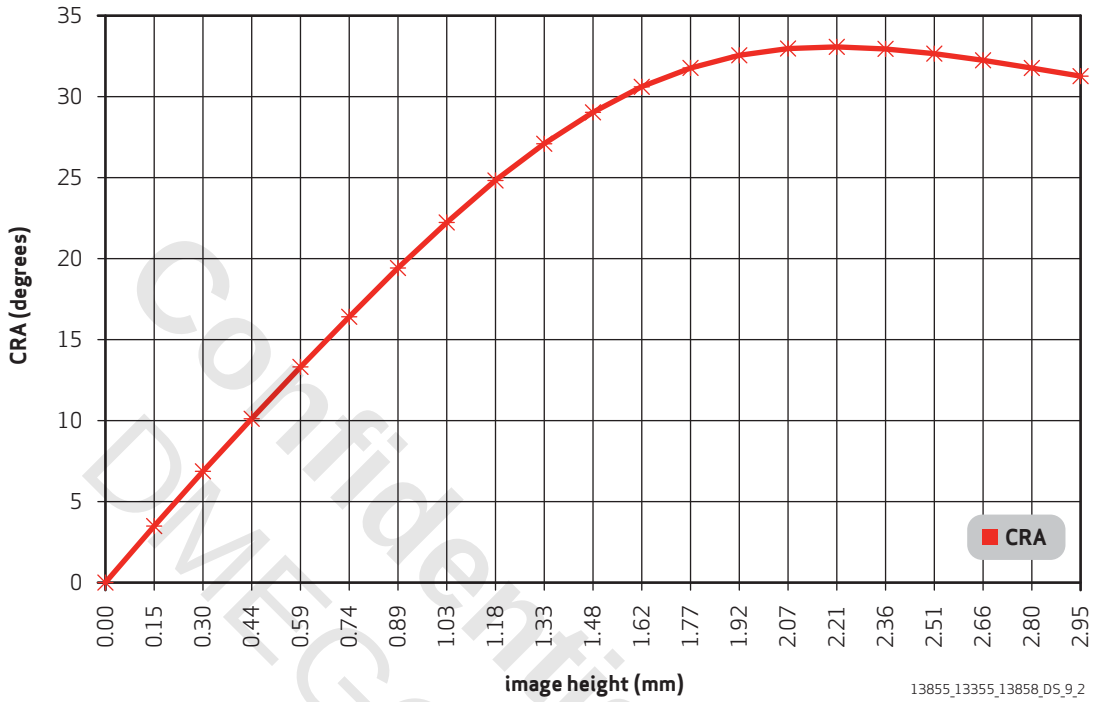


table 9-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.00	0
0.05	0.15	3.53
0.10	0.30	6.89
0.15	0.44	10.15
0.20	0.59	13.35
0.25	0.74	16.47
0.30	0.89	19.47
0.35	1.03	22.29
0.40	1.18	24.87
0.45	1.33	27.16

table 9-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.48	29.09
0.55	1.62	30.65
0.60	1.77	31.82
0.65	1.92	32.60
0.70	2.07	33.03
0.75	2.21	33.15
0.80	2.36	33.03
0.85	2.51	32.72
0.90	2.66	32.31
0.95	2.80	31.84
1.00	2.95	31.35

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends water cleaning to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 02.08.2016

- initial release

version 1.1 02.26.2016

- in key specifications, changed maximum exposure from VTS-4 to VTS-8
- in table 2-4, changed t1 constraint from "XSHUTDN rising – first SCCB transaction" to "XSHUTDN rising – system ready" and changed t1 minimum value from 8192 EXTCLK to 5 ms
- in sub-section 2.6.1, updated figure 2-3
- in table 5-2, changed bit description for 0x520A[4:0] from "White pixel threshold list[0]" to "Gain threshold list[0]", changed bit description for 0x520B[4:0] from "White pixel threshold list[1]" to "Gain threshold list[1]", and changed bit description for 0x520C[4:0] from "White pixel threshold list[2]" to "Gain threshold list[2]"
- in table 6-2, changed bit description for 0x3008[2] from "Reserved" to "io_sda_o", changed bit description for 0x3010[2] from "Reserved" to "io_sda_sel", replaced bit descriptions for 0x3012 with new bit descriptions, replaced bit descriptions for 0x3013 with new bit descriptions, replaced bit descriptions for 0x3018 with new bit descriptions, changed bit description for 0x301B[7] from "sclk_blc_en" to "sclk_blc enable", changed bit description for 0x301B[6] from "sclk_isp_en" to "sclk_isp enable", and changed bit description for 0x301B[5] from "sclk_testmode_en" to "ssclk_tpm enable"
- in table 6-6, changed bit description for 0x3663[2] from "P_VSYNC fix..." to "FSIN selection..." and changed bit description for 0x3663[1] from "P_VSYNC fix..." to "VSYNC selection..."
- in table 6-16, changed bit description for 0x5000[6] from "Not used" to "Reserved"
- in table 6-20, changed bit description for 0x520A[4:0] from "White pixel threshold list[0]" to "Gain threshold list[0]", changed bit description for 0x520B[4:0] from "White pixel threshold list[1]" to "Gain threshold list[1]", and changed bit description for 0x520C[4:0] from "White pixel threshold list[2]" to "Gain threshold list[2]"

version 1.2 04.22.2016

- in key specifications, changed active power requirements to 233mW (based on ISP ON), standby power requirements to 1mW, and XSHUTDN power requirements to <10µA
- in table 2-4, removed row for t4, changed t5 to t4 and changed description to “delay related to output frame rate and line timing”
- in figure 2-3, combined t4 and t5, changed to t4 (variable), and changed t6 to t5
- in section 3.1, changed second sentence in fourth paragraph to "Maximum exposure time is VTS-8..."
- in table 4-2, added "HTS must be multiple of 6" to description of registers 0x380C and 0x380D
- in table 4-2, updated all default values to match those in table 6-8
- in table 4-3, changed default value of register 0x4003 to 0x40
- in section 4.4, changed last sentence of first paragraph to "Out of 1024 bytes, 608 bytes are reserved for OmniVision and 416 bits are reserved for customers."

- in section 4.4, changed second sentence of fourth paragraph to "...and 0x73C0 ~ 0x73FF are reserved for OmniVision, while 0x7220 ~ 0x73BF (416 bytes) are reserved for customer use."
- in table 4-4, changed end address to 0x73BF and bytes usage to 416 in third row
- in table 4-4, changed start address to 0x73C0 and bytes usage to 64 in fourth row
- in table 6-8, added "HTS must be multiple of 6" to description of registers 0x380C and 0x380D
- in table 6-10, changed default value of register 0x4003 to 0x40
- in table 7-3, changed typ value for I_{DD-A} to 36mA, typ value for I_{DD-IO} to 3mA, typ value for I_{DD-D} to 106mA, $I_{DDS-SCCB}$ to 1mA, and $I_{DDS-XSHUTDN}$ to 2µA
- in table 7-3, added table footnote c

version 1.21 06.08.2016

- in key specifications, changed lens chief ray angle to 33.15 non-linear
- in chapter 9, updated figure 9-2 and table 9-1

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