Specification for Camera Serial Interface 2 (CSI-2SM)

Version ~~2.1~~3.0

~~14 December 2017~~31 May 2019

MIPI Board Adopted ~~9 April 2018~~10 September 2019

This document is a MIPI Specification. MIPI member companies' rights and obligations apply to this MIPI Specification as defined in the MIPI Membership Agreement and MIPI Bylaws.

~~This document is subject to further editorial and technical development.~~Further technical changes to this document are expected as work continues in the PHY Working Group.

NOTICE OF DISCLAIMER

The material contained herein is provided on an "AS IS" basis. To the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI Alliance Inc. ("MIPI") hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence. ALSO, THERE IS NO WARRANTY OR CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL.

IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI. Any license to use this material is granted separately from this document. This material is protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, service marks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance Inc. and cannot be used without its express prior written permission. The use or implementation of this material may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this material or otherwise.

Without limiting the generality of the disclaimers stated above, users of this material are further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this material; (b) does not monitor or enforce compliance with the contents of this material; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with MIPI specifications or related material.

Questions pertaining to this material, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane, Piscataway New Jersey 08854, United States
Attn: Managing Director

Contents

Figures

Tables

Release History

Date	Version	Description
2005-11-29	v1.00	Initial Board ~~-~~approved release.
2010-11-09	v1.01.00	Board ~~-~~approved release.
2013-01-22	v1.1	Board approved release.
2014-09-10	v1.2	Board approved release.
2014-10-07	v1.3	Board approved release.
2017-03-28	v2.0	Board approved release.
2018-04-09	v2.1	Board approved release.
2019-09-10	v3.0	Board approved release.

This page intentionally left blank.

1 Introduction

1.1 Scope

The Camera Serial Interface 2 Specification defines an interface between a peripheral device (camera) and a host processor (baseband, application engine). The purpose of this document is to specify a standard interface between a camera and a host processor for mobile applications.

This Revision of the Camera Serial Interface 2 Specification leverages C-PHY ~~version 1.2~~ ***[MIPI02]*** and D-PHY ~~version 2.1~~ ***[MIPI01]***. These enhancements enable higher interface bandwidth and more flexibility in channel layout. The CSI-2 version 1.3 Specification was designed to ensure interoperability with CSI-2 version 1.2 when the former uses the D-PHY physical layer. If the C-PHY physical layer only is used, then backwards compatibility cannot be maintained.

In this document, the term 'host processor' refers to the hardware and software that performs essential core functions for telecommunication or application tasks. The engine of a mobile terminal includes hardware and the functions, which enable the basic operation of the mobile terminal. These include, for example, the printed circuit boards, RF components, basic electronics, and basic software, such as the digital signal processing software.

1.2 Purpose

Demand for increasingly higher image resolutions is pushing the bandwidth capacity of existing host processor-to-camera sensor interfaces. Common parallel interfaces are difficult to expand, require many interconnects, and consume relatively large amounts of power. Emerging serial interfaces address many of the shortcomings of parallel interfaces while introducing their own problems. Incompatible, proprietary interfaces prevent devices from different manufacturers from working together. This can raise system costs and reduce system reliability by requiring "hacks" to force the devices to interoperate. The lack of a clear industry standard can slow innovation and inhibit new product market entry.

CSI-2 provides the mobile industry a standard, robust, scalable, low-power, high-speed, cost-effective interface that supports a wide range of imaging solutions for mobile devices.

2 Terminology

2.1 Use of Special Terms

The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

> The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform to the Specification and from which no deviation is permitted (*shall* equals *is required to*).
>
> The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.
>
> The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.
>
> The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).
>
> The word *may* is used to indicate a course of action permissible within the limits of the Specification (*may* equals *is permitted to*).
>
> The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

All sections are normative, unless they are explicitly indicated to be informative.

2.2 Definitions

CCI (I^2C): CCI supporting I^2C~~.~~ ***[NXP01]***.

CCI (I3C): CCI supporting I3C~~.~~ ***[MIPI03]***.

CCI (I3C SDR) means CCI supporting I3C SDR.

CCI (I3C DDR) means CCI supporting I3C DDR.

Filler: A CSI-2 protocol element that is inserted after CSI-2 Packets in order to ensure that data transmissions on all Lanes end at the same time.

Lane: A unidirectional, point-to-point, 2- or 3-wire interface used for high-speed serial clock or data transmission; the number of wires is determined by the PHY specification in use (i.e. either D-PHY or C-PHY, respectively). A CSI-2 camera interface using the D-PHY physical layer consists of one clock Lane and one or more data Lanes. A CSI-2 camera interface using the C-PHY physical layer consists of one or more Lanes, each of which transmits both clock and data information. Note that when describing features or behavior applying to both D-PHY and C-PHY, this specification sometimes uses the term data Lane to refer to both a D-PHY data Lane and a C-PHY Lane.

Message: In CCI (I^2C) or CCI (I3C SDR), a Message begins with a START or Repeated START condition, followed by the address of the targeted slave(s), R/W bit, other data, and ends with either a STOP or Repeated START condition. In the case of CCI (I3C SDR), a START or Repeated START condition followed by 7’h7E may be added to the beginning. In CCI (I3C DDR), a Message begins with either the I3C ENTHDR0 CCC or the I3C HDR Restart Pattern, followed by an HDR-DDR Command, HDR-DDR Data, and ends with either the I3C HDR Exit Pattern or the I3C HDR Restart Pattern.

Operation: An Operation is composed of one or more Messages in order to read or write.

Packet: A group of bytes organized in a specified way to transfer data across the interface. All packets have a minimum specified set of components. The byte is the fundamental unit of data from which packets are made.

Payload: Application data only – with all sync, header, ECC and checksum and other protocol-related information removed. This is the "core" of transmissions between application processor and peripheral.

Sleep Mode: Sleep mode (SLM) is a leakage level only power consumption mode.

Spacer: An optional CSI-2 protocol element that may be inserted after CSI-2 Packets and Fillers transmitted using CSI-2 LRTE; not to be confused with the C-PHY "Spacer Code" defined in ***[MIPI02]***.

Transmission: The time during which high-speed serial data is actively traversing the bus. A transmission is bounded by SoT (Start of Transmission) and EoT (End of Transmission) at beginning and end, respectively.

Virtual Channel: Multiple independent data streams for up to 32 peripherals are supported by this Specification. The data stream for each peripheral may be a Virtual Channel. These data streams may be interleaved and sent as sequential packets, with each packet dedicated to a particular peripheral or channel. Packet protocol includes information that links each packet to its intended peripheral.

2.3 Abbreviations

e.g.	For example (Latin: exempli gratia)
i.e.	That is (Latin: id est)

2.4 Acronyms

~~ALPS~~ALP	Alternate Low Power ~~State~~
BER	Bit Error Rate
CCI	Camera Control Interface
CIL	Control and Interface Logic
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CSPS	Chroma Shifted Pixel Sampling
DDR	Dual Data Rate
DI	Data Identifier
DT	Data Type
ECC	Error Correction Code
EoT	End of Transmission
EoTp	End of Transmission short packet
EPD	Efficient Packet Delimiter (PHY and / or Protocol generated signaling used in LRTE)
EXIF	Exchangeable Image File Format
FE	Frame End
FS	Frame Start
HS	High Speed; identifier for operation mode

HS-LPS-LS	High speed to Low Power State to High speed switching (includes LPS entry and exit latencies)
HS-RX	High-Speed Receiver
HS-TX	High-Speed Transmitter
I^{2}C	Inter-Integrated Circuit ***[NXP01]***
ILR	Interpacket Latency Reduction
JFIF	JPEG File Interchange Format
JPEG	Joint Photographic Expert Group
LE	Line End
LFSR	Linear Feedback Shift Register
LLP	Low Level Protocol
LS	Line Start
LSB	Least Significant Bit
LSS	Least Significant Symbol
LP	Low-Power; identifier for operation mode
LP-RX	Low-Power Receiver (Large-Swing Single Ended)
LP-TX	Low-Power Transmitter (Large-Swing Single Ended)
LRTE	Latency Reduction Transport Efficiency
LVLP	Low Voltage Low Power
MSB	Most Significant Bit
MSS	Most Significant Symbol
PDQ	Packet Delimiter Quick (PHY generated and consumed signaling used in LRTE)
PF	Packet Footer
PH	Packet Header
PI	Packet Identifier
PT	Packet Type
PHY	Physical Layer
PPI	PHY Protocol Interface
PRBS	Pseudo-Random Binary Sequence
RGB	Color representation (Red, Green, Blue)
RX	Receiver
SCL	Serial Clock (for CCI)
SDA	Serial Data (for CCI)

SLM	Sleep Mode
SoT	Start of Transmission
TX	Transmitter
ULPS	Ultra Low Power State
VGA	Video Graphics Array
YUV	Color representation (Y for luminance, U & V for chrominance)

3 References

[NXP01] UM10204, *I^2C bus specification and user manual*, Revision 6, NXP Semiconductors N.V., 4 April 2014.

[MIPI01] *MIPI Alliance Specification for D-PHY*, version 2.~~1~~5, MIPI Alliance, Inc., ~~28 March 2017~~In press.

[MIPI02] *MIPI Alliance Specification for C-PHY*, version ~~1.~~2.0, MIPI Alliance, Inc., 28 ~~March 2017~~ May 2019.

[MIPI03] *MIPI Alliance Specification for I3C (Improved Inter-Integrated Circuit)*, version 1.0, MIPI Alliance, Inc., 31 December 2016.

[MIPI04] *MIPI Alliance Specification for Camera Command Set (CCS)*, version 1.0, MIPI Alliance, Inc., 24 October 2017.

143 ~~[MIPI05] *MIPI Alliance Specification for D-PHY*, version 2.0, MIPI Alliance, Inc., 8 March 2016.~~

~~This page intentionally left blank.~~

4 Overview of CSI-2

The CSI-2 Specification defines standard data transmission and control interfaces between transmitter and receiver. Two high-speed serial data transmission interface options are defined.

The first option, referred to in this specification as the "D-PHY physical layer option," is typically a unidirectional differential interface with one 2-wire clock Lane and one or more 2-wire data Lanes. The physical layer of this interface is defined by the *MIPI Alliance Specification for D-PHY* ***[MIPI01]***. ***Figure 1*** illustrates the connections for this option between a CSI-2 transmitter and receiver, which typically are a camera module and a receiver module, part of the mobile phone engine.

The second high-speed data transmission interface option, referred to in this specification as the "C-PHY physical layer option," typically consists of one or more unidirectional 3-wire serial data Lanes, each of which has its own embedded clock. The physical layer of this interface is defined by the *MIPI Alliance Specification for C-PHY* ***[MIPI02]***. ***Figure 2*** illustrates the CSI transmitter and receiver connections for this option.

The Camera Control Interface (CCI) for both physical layer options is a bi-directional control interface compatible with the I^2C standard ***[NXP01]***.

Note that beginning with the CSI-2 v3.0 specification, Lane 1 of a D-PHY or C-PHY link interconnecting a camera with a host or application processor (i.e., Data1+ / Data1- in ***Figure 1***, or Data1_A / Data1_B / Data1_C in ***Figure 2***) is permitted to be bidirectional. For such links, there is no requirement to support a physically separate CCI. See ***Section 9.12***.

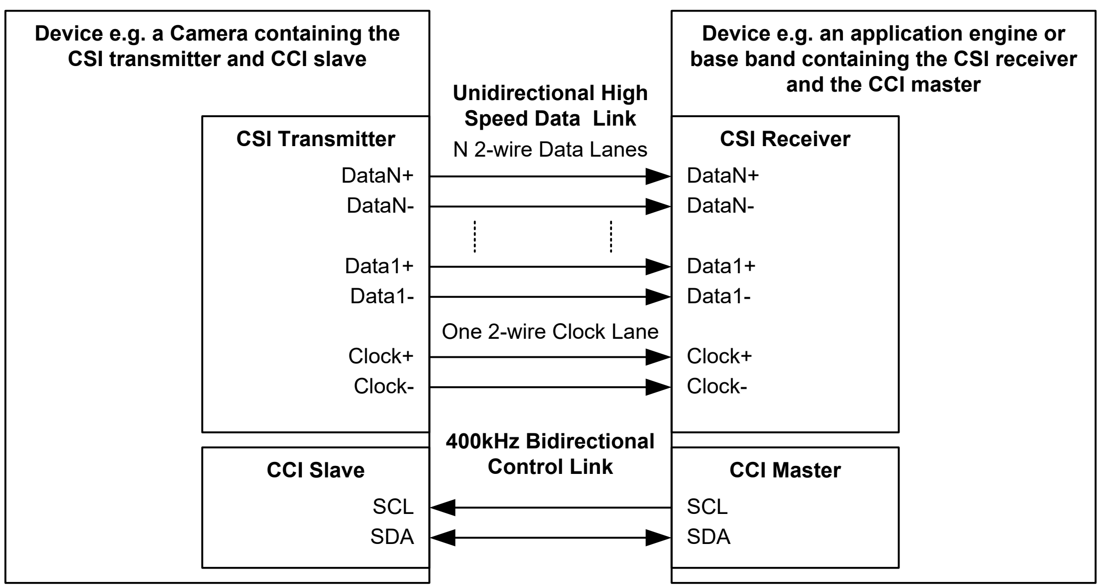


Figure 1 Typical CSI-2 and CCI Transmitter and Receiver Interface for D-PHY

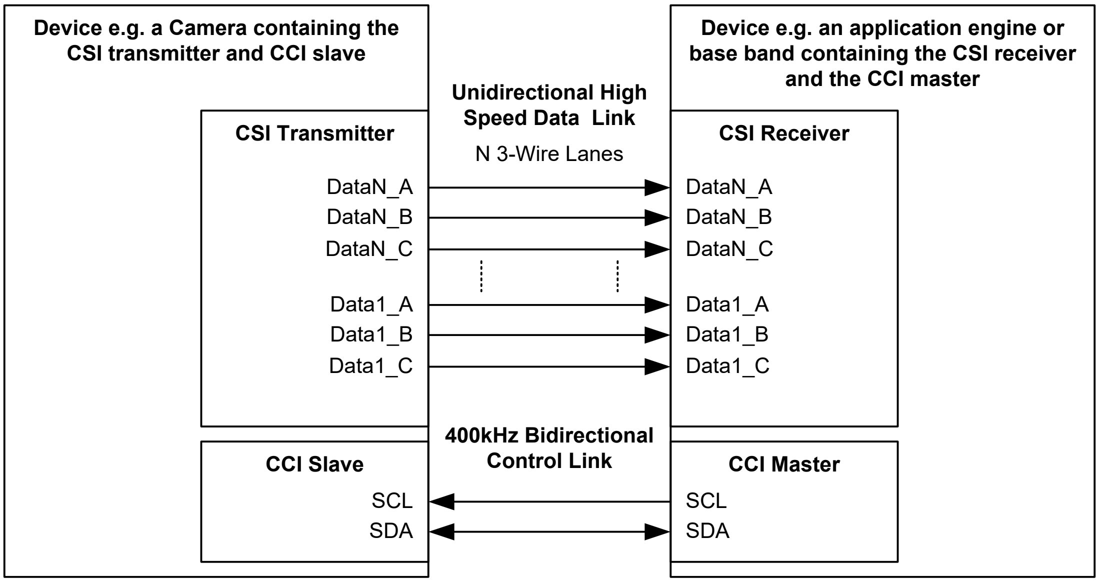


Figure 2 Typical CSI-2 and CCI Transmitter and Receiver Interface for C-PHY

5 CSI-2 Layer Definitions

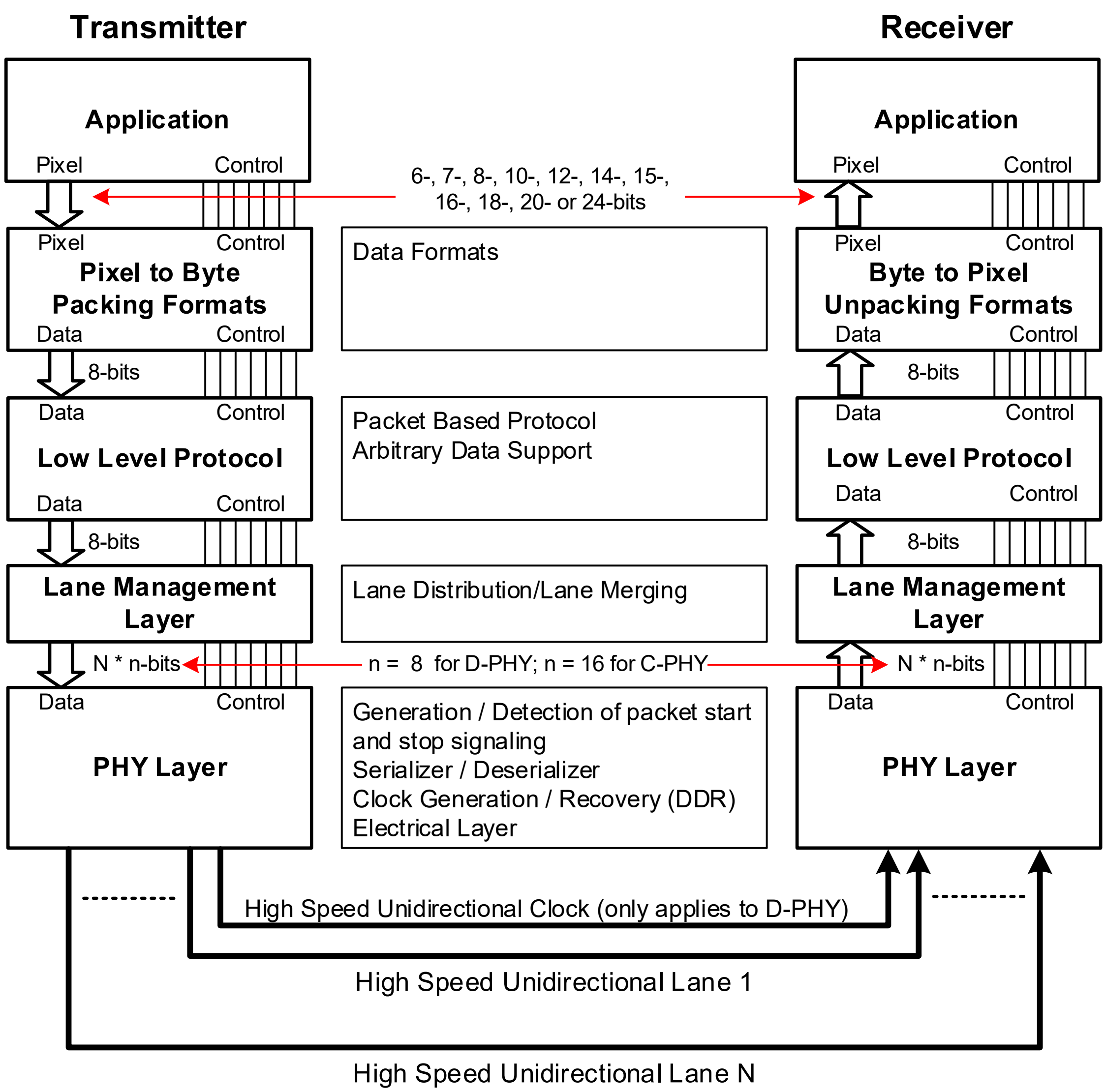


Figure 3 CSI-2 Layer Definitions

Figure 3 defines the conceptual layer structure typically used in CSI-2. The layers can be characterized as follows:

- **PHY Layer.** The PHY Layer specifies the transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures "ones" and "zeroes" from the serial bit stream. This part of the Specification documents the characteristics of the transmission medium, electrical parameters for signaling and for the D-PHY physical layer option, the timing relationship between clock and data Lanes.

  The mechanism for signaling Start of Transmission (SoT) and End of Transmission (EoT) is specified as well as other "out of band" information that can be conveyed between transmitting and receiving PHYs. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

  The PHY layer is described in ***[MIPI01]*** and ***[MIPI02]***.

- **Protocol Layer.** The Protocol layer is composed of several layers, each with distinct responsibilities. The CSI-2 protocol enables multiple data streams using a single interface on the host processor. The Protocol layer specifies how multiple data streams may be tagged and interleaved so each data stream can be properly reconstructed.
  - **Pixel/Byte Packing/Unpacking Layer.** The CSI-2 specification supports image applications with varying pixel formats. In the transmitter this layer packs pixels from the Application layer into bytes before sending the data to the Low Level Protocol layer. In the receiver this layer unpacks bytes from the Low Level Protocol layer into pixels before sending the data to the Application layer. Eight bits per pixel data is transferred unchanged by this layer.
  - **Low Level Protocol.** The Low Level Protocol (LLP) includes the means of establishing bit-level and byte-level synchronization for serial data transferred between SoT (Start of Transmission) and EoT (End of Transmission) events and for passing data to the next layer. The minimum data granularity of the LLP is one byte. The LLP also includes assignment of bit-value interpretation within the byte, i.e. the "Endian" assignment.
  - **Lane Management.** CSI-2 is Lane-scalable for increased performance. The number of data Lanes is not limited by this specification and may be chosen depending on the bandwidth requirements of the application. The transmitting side of the interface distributes ("distributor" function) bytes from the outgoing data stream to one or more Lanes. On the receiving side, the interface collects bytes from the Lanes and merges ("merger" function) them together into a recombined data stream that restores the original stream sequence. For the C-PHY physical layer option, this layer exclusively distributes or collects byte pairs (i.e. 16-bits) to or from the data Lanes. Scrambling on a per-Lane basis is an optional feature, which is specified in detail in ***Section 9.~~15~~17***.

  Data within the Protocol layer is organized as packets. The transmitting side of the interface appends header and error-checking information on to data to be transmitted at the Low Level Protocol layer. On the receiving side, the header is stripped off at the Low Level Protocol layer and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data.

- **Application Layer.** This layer describes higher-level encoding and interpretation of data contained in the data stream and is beyond the scope of this specification. The CSI-2 Specification describes the mapping of pixel values to bytes.

The normative sections of the Specification only relate to the external part of the Link, e.g. the data and bit patterns that are transferred across the Link. All internal interfaces and layers are purely informative.

6 Camera Control Interface (CCI)

CCI is a two-wire, bi-directional, half duplex, serial interface for controlling the transmitter. CCI is compatible with I^2C Fast-mode (Fm) or Fast-mode Plus (Fm+) ***[NXP01]*** variants, and with the I3C ***[MIPI03]*** interface's Single Data Rate (SDR) or Double Data Rate (DDR) protocols. CCI shall support up to 400kbps (Fm) operation and 7-bit slave addressing. In addition, CCI can optionally support up to 1Mbps (Fm+), 12.5Mbps (SDR), or 25Mbps (DDR).

This Section uses the following terms:

- **CCI (I^2C)** means CCI supporting I^2C
- **CCI (I3C)** means CCI supporting I3C
- **CCI (I3C SDR)** means CCI supporting I3C SDR
- **CCI (I3C DDR)** means CCI supporting I3C DDR
- **CCI** alone (without following parentheses) means both **CCI (I^2C)** and **CCI (I3C)**.

CCI can be used with or without CSI-2 over C/D-PHY. When CCI is used as part of a CSI-2 bus, a CSI-2 receiver shall be configured as a master and a CSI-2 transmitter shall be configured as a slave. When CCI is used without CSI-2 over C/D-PHY, the host should be used as a master. CCI is capable of handling multiple slaves on the bus.

In **CCI (I^2C)**, multi-master mode is not supported. Any I^2C commands not described in this section shall be ignored, and shall not cause unintended device operation.

In **CCI (I3C)**, any I3C mandatory functions and 'Required' CCC commands shall be supported, and any I3C optional functions and commands may be supported (e.g. Multi-Master, In-Band Interrupt, Hot-Join).

Note:

> *Do not confuse the CCI terms master and slave with similar terms in the C-PHY or D-PHY Specifications; they are not related.*

Typically, there is a dedicated CCI interface between the transmitter and the receiver.

CCI is a subset of the I^2C or I3C protocol that includes the minimum combination of obligatory features for I^2C/I3C slave devices specified in the I^2C or I3C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I^2C or I3C bus. However, care must be taken so that I^2C or I3C masters do not attempt to use I^2C or I3C features not supported by CCI masters or slaves.

A CCI transmitter may have additional features to support I^2C or I3C, but that is implementation-dependent. Further details can be found on a particular device's data sheet.

This specification does not attempt to define the contents of control Messages sent by the CCI master. Therefore, it is the responsibility of the implementer to define a set of control Messages and corresponding frame timing and any I^2C or I3C latency requirements that the CCI master must meet when sending such control Messages to the CCI slave.

CCI defines an additional data protocol layer on top of I^2C or I3C, as specified in the following sections.

6.1 CCI (I^{2}C) Data Transfer Protocol

The **CCI (I^{2}C)** data transfer protocol follows the I^{2}C specification. The START, REPEATED START, and STOP conditions, and the data transfer protocol, are all specified in ***[NXP01]***.

6.1.1 CCI (I^{2}C) Message Type

A basic **CCI (I^{2}C)** Message consists of:

- START or Repeated START condition
- Slave address with read/write bit
- Acknowledge from slave
- Sub address (INDEX) for pointing at a register inside the slave device (not used in Single Read from Current Location)
- Acknowledge signal from slave (not used in Single Read from Current Location)

And then either:

- For a write operation:
  - Data byte from master
  - Acknowledge/negative acknowledge from slave, and
  - STOP or Repeated START condition

Or:

- For a read operation:
  - Repeated START condition (not used in Single Read from Current Location)
  - slave address with read bit (not used in Single Read from Current Location)
  - acknowledge signal from slave (not used in Single Read from Current Location)
  - data byte from the slave
  - acknowledge or negative acknowledge from the master, and
  - STOP or Repeated START condition.

A CCI Slave may support back-to-back Messages by using Repeated START between CCI Messages instead of START and/or STOP as shown in this Section.

The slave address in **CCI (I^{2}C)** is 7 bits long.

CCI (I^{2}C) supports an 8-bit INDEX with 8-bit data, or a 16-bit INDEX with 8-bit data. The slave device in question defines what Message type is used.

6.1.2 CCI (I^2C) Read/Write Operations

A **CCI (I^2C)** compatible device shall support the four read operations and two write operations shown in ***Table 1***, as detailed in the following sub-sections:

Table 1 CCI (I^2C) Read/Write Operations

Type	Operation	Section
Read	Single Read from Random Location	***6.1.2.1***
	Sequential Read from Random Location	***6.1.2.2***
	Single Read from Current Location	***6.1.2.3***
	Sequential Read from Current Location	***6.1.2.4***
Write	Single Write to Random Location	***6.1.2.5***
	Sequential Write Starting from Random Location	***6.1.2.6***

The INDEX in the slave device must be auto-incremented after each read/write operation. This is also explained in the following sections.

6.1.2.1 CCI (I^2C) Single Read from Random Location

In a single read from a random location (see ***Figure 4***) the master does a dummy write operation to the desired INDEX, issues a Repeated START condition, and then addresses the slave again with the read operation. After acknowledging its slave address, the slave starts to output data onto the SDA line. The master terminates the read operation by setting a negative acknowledge and a STOP or Repeated START condition.

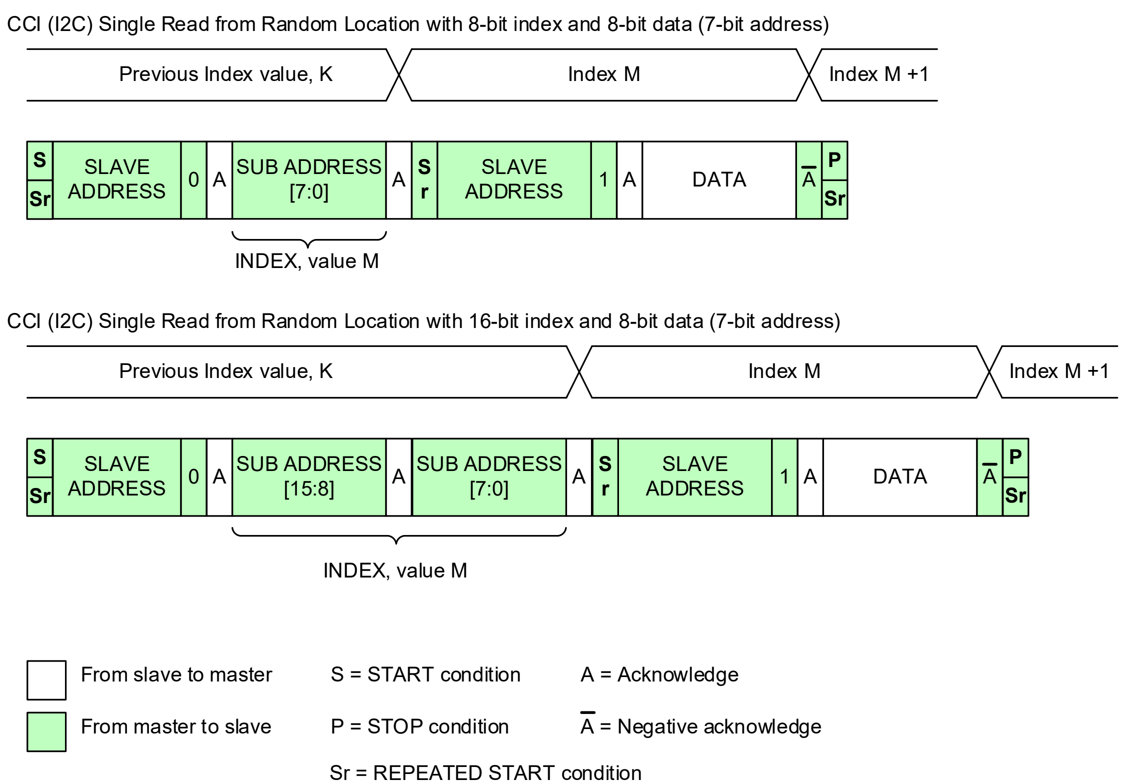


Figure 4 CCI (I^2C) Single Read from Random Location

6.1.2.2 CCI (I^{2}C) Single Read from Current Location

It is also possible to read from the last used INDEX, by addressing the slave with a read operation (see ***Figure 5***). The slave responds by sending the data from the last used INDEX to the SDA line. The master terminates the read operation by setting a negative acknowledge and a STOP or Repeated START condition.

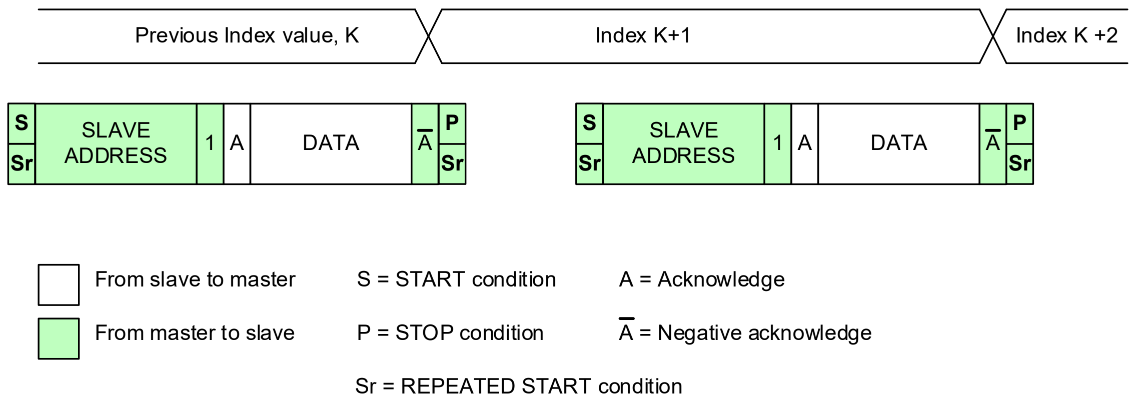


Figure 5 CCI (I^{2}C) Single Read from Current Location

6.1.2.3 CCI (I²C) Sequential Read Starting from Random Location

Sequential read starting from a random location is illustrated in ***Figure 6***. The master does a dummy write to the desired INDEX, issues a Repeated START condition after an acknowledge from the slave, and then addresses the slave again with a read operation. If a master issues an acknowledge after receiving data, this acts as a signal to the slave that the read operation is to continue from the next INDEX. When the master has read the last data byte, it issues a negative acknowledge and a STOP or Repeated START condition.

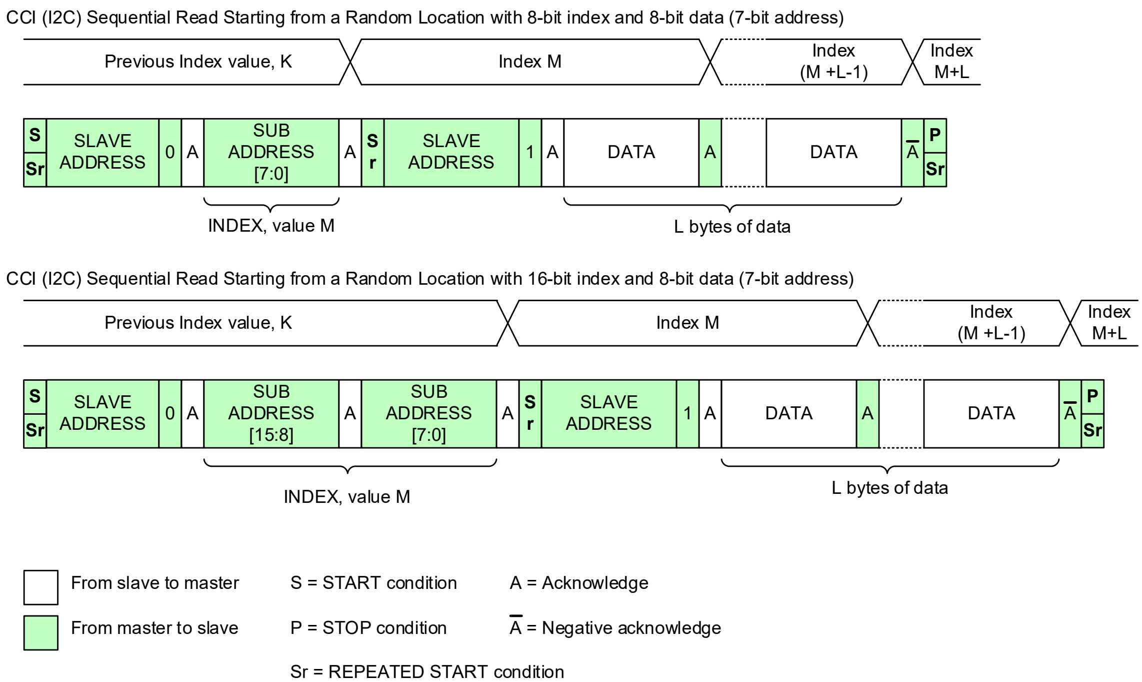


Figure 6 CCI (I²C) Sequential Read Starting from Random Location

6.1.2.4 CCI (I^2C) Sequential Read Starting from Current Location

A sequential read starting from the current location (see ***Figure** 7*) is similar to a sequential read from a random location. The only exception is there is no dummy write operation. The master terminates the read operation by issuing a negative acknowledge, and a STOP or Repeated START condition.

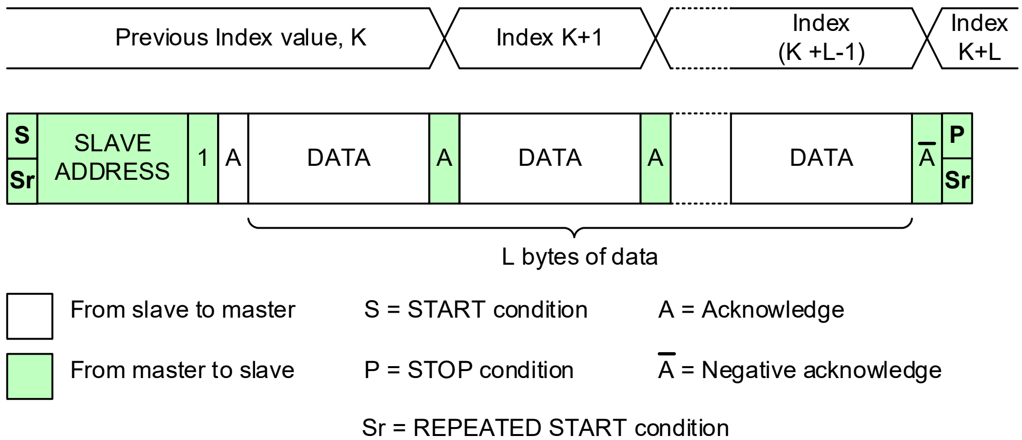


Figure 7 CCI (I^2C) Sequential Read Starting from Current Location

6.1.2.5 CCI (I^2C) Single Write to Random Location

A write operation to a random location is illustrated in ***Figure 8***. The master issues a write operation to the slave, then issues the INDEX and data after the slave has acknowledged the write operation. The write operation is terminated with a stop or Repeated START condition from the master.

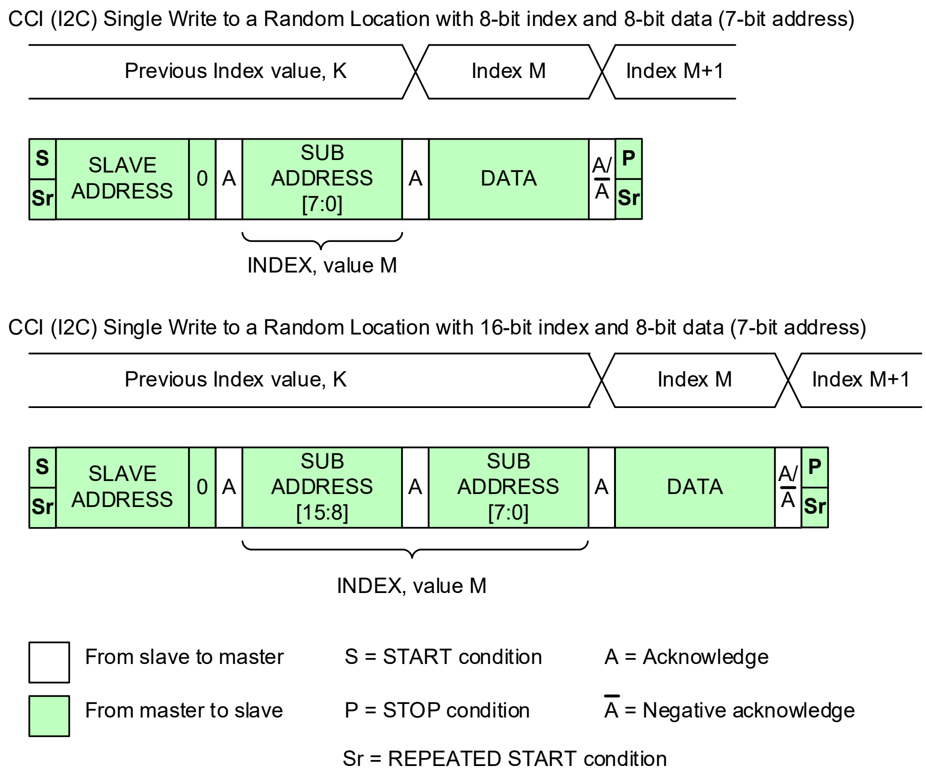


Figure 8 CCI (I^2C) Single Write to Random Location

6.1.2.6 CCI (I^2C) Sequential Write Starting from Random Location

The Sequential Write Starting from Random Location operation is illustrated in ***Figure 9***. The slave auto-increments the INDEX after each data byte is received. The Sequential Write Starting from Random Location operation is terminated with a STOP or Repeated START condition from the master.

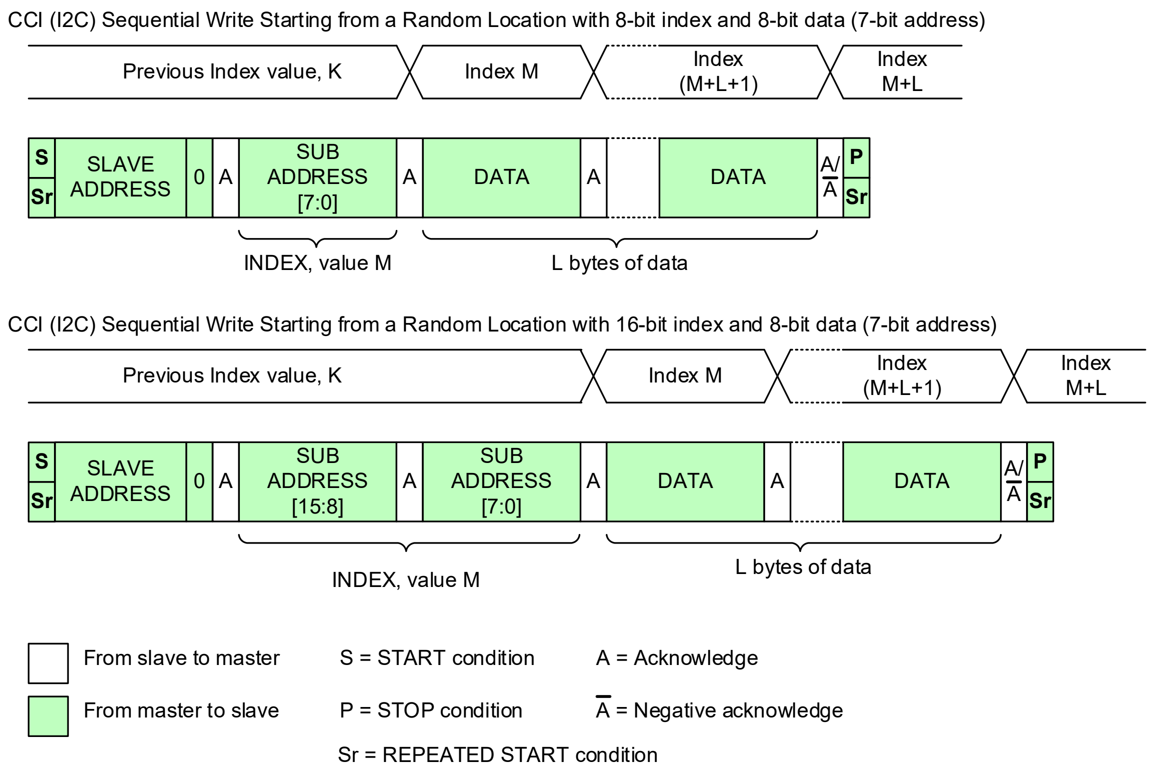


Figure 9 CCI (I^2C) Sequential Write Starting from Random Location

6.2 CCI (I3C) Data Transfer Protocol

The **CCI (I3C)** data transfer protocol follows the I3C Specification. The START, Repeated START, and STOP conditions, as well as data transfer protocol, are specified in ***[MIPI03]***.

If **CCI (I3C)** is supported, then CCI **(I3C SDR)** shall be supported and **CCI (I3C DDR)** may be supported. The master shall get the slave's Max Read Length (MRL) and Max Write Length (MWL) via transmitting I3C CCCs GETMRL and GETMWL prior to **CCI (I3C)** data transfer.

6.2.1 CCI (I3C SDR) Data Transfer Protocol

6.2.1.1 CCI (I3C SDR) Message Type

The **CCI (I3C SDR)** master normally should start a Message with 7'h7E, and may choose to start a Message with a slave address.

A basic **CCI (I3C SDR)** Message starting a Message with 7'h7E consists of:

- START condition
- 7'h7E with write bit
- Acknowledge from slave
- Repeated START condition
- Slave address with read/write bit
- Acknowledge from slave
- Sub-address (INDEX) of a register inside the slave device (not used in Single Read from Current Location)
- Transition bit (Parity bit) from master (not used in Single Read from Current Location)

  And then either:

  - For a write operation:
    - Data byte from master
    - Transition bit (Parity bit) from master
    - STOP or Repeated START condition;

  Or

  - For a read operation:
    - Repeated START condition (not used in Single Read from Current Location)
    - Slave address with read bit (not used in Single Read from Current Location)
    - Acknowledge from slave (not used in Single Read from Current Location)
    - Data byte from slave
    - Transition bit (End-of-Data) from master or slave
    - STOP or Repeated START condition.

Other **CCI (I3C SDR)** Messages starting a Message with a slave address consist of:

- START or Repeated START condition
- Slave address with read/write bit
- Acknowledge from slave
- Sub-address (INDEX) of a register inside the slave device (not used in Single Read from Current Location)
- Transition bit (Parity bit) from master (not used in Single Read from Current Location)

  And then either:

  - For a write operation:
    - Data byte from master
    - Transition bit (Parity bit) from master
    - STOP or Repeated START condition;

  Or:

  - For a read operation:
    - Repeated START condition (not used in Single Read from Current Location)
    - Slave address with read bit (not used in Single Read from Current Location)
    - Acknowledge from slave (not used in Single Read from Current Location)
    - Data byte from slave
    - Transition bit (End-of-Data) from master or slave
    - STOP or Repeated START condition.

The slave address in **CCI (I3C SDR)** is 7 bits long.

CCI (I3C SDR) supports an 8-bit INDEX with 8-bit data, or a 16-bit INDEX with 8-bit data. The slave device in question defines what Message type is used.

6.2.1.2 CCI (I3C SDR) Read/Write Operations

A **CCI (I3C SDR)** compatible device shall support the four read operations and two write operations shown in ***Table 2***, as detailed in the following sub-sections:

Table 2 CCI (I3C SDR) Read/Write Operations

Type	Operation	Section
Read	Single Read from Random Location	***6.2.1.2.1***
	Single Read from Current Location	***6.2.1.2.2***
	Sequential Read from Random Location	***6.2.1.2.3***
	Sequential Read from Current Location	***6.2.1.2.4***
Write	Single Write to Random Location	***6.2.1.2.5***
	Sequential Write Starting from Random Location	***6.2.1.2.6***

The INDEX in the slave device must be auto-incremented after each read/write operation. This is also explained in the following sections.

6.2.1.2.1 CCI (I3C SDR) Single Read from Random Location

In a single read from a random location (***Figure 10***), the master does a dummy write operation to the desired INDEX, issues a Repeated START condition, and then addresses the slave again with the read operation. After acknowledging its slave address, the slave starts to output data onto the SDA line. The master aborts the read operation by setting a Transition bit, and a STOP or Repeated START condition.

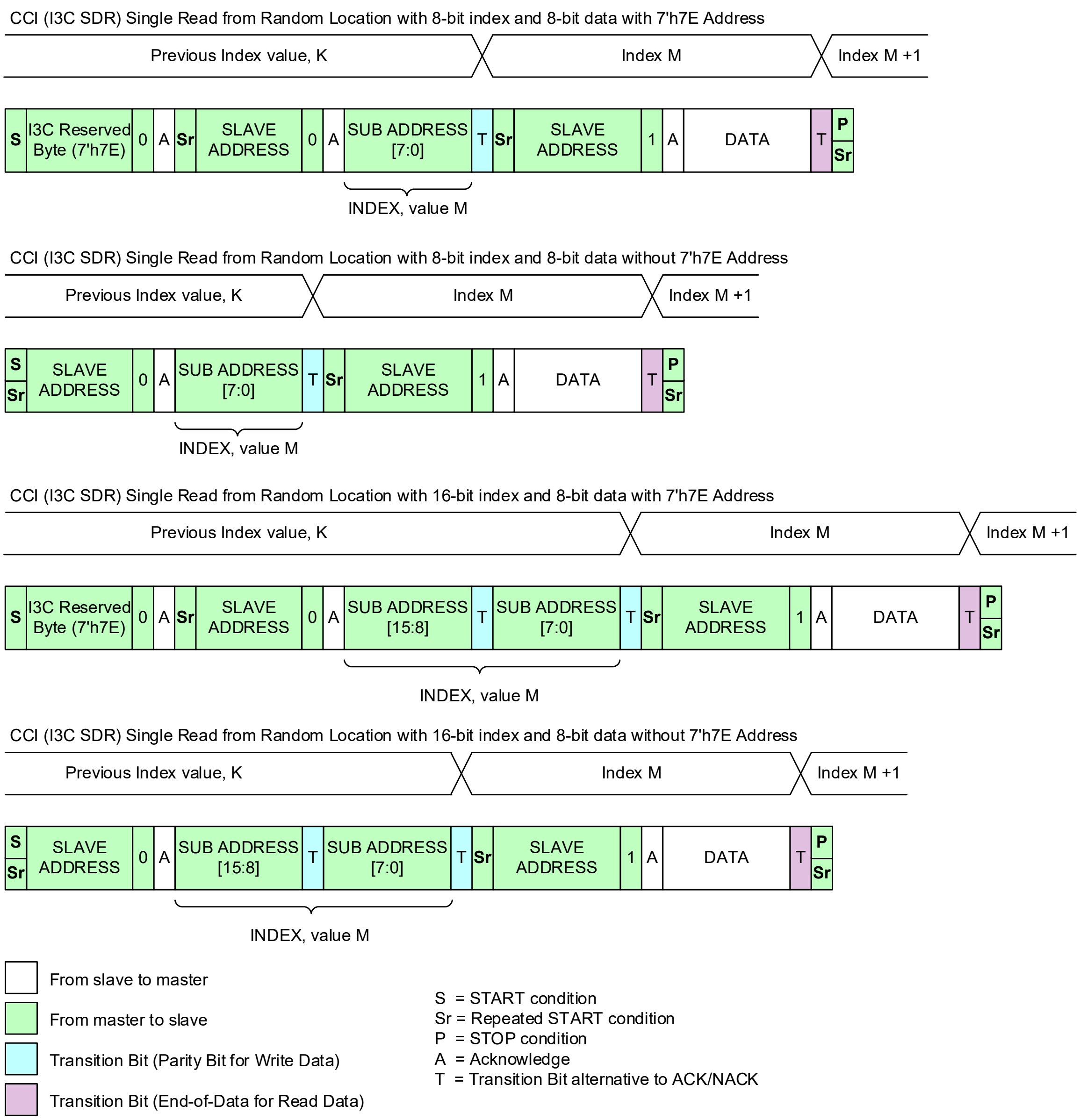


Figure 10 CCI (I3C SDR) Single Read from Random Location

6.2.1.2.2 CCI (I3C SDR) Single Read from Current Location

It is also possible to read from the last used INDEX by addressing the slave with a read operation (***Figure 11***). The slave responds by setting the data from last used INDEX to SDA line. The master aborts the read operation by setting a Transition bit, and a STOP or Repeated START condition.

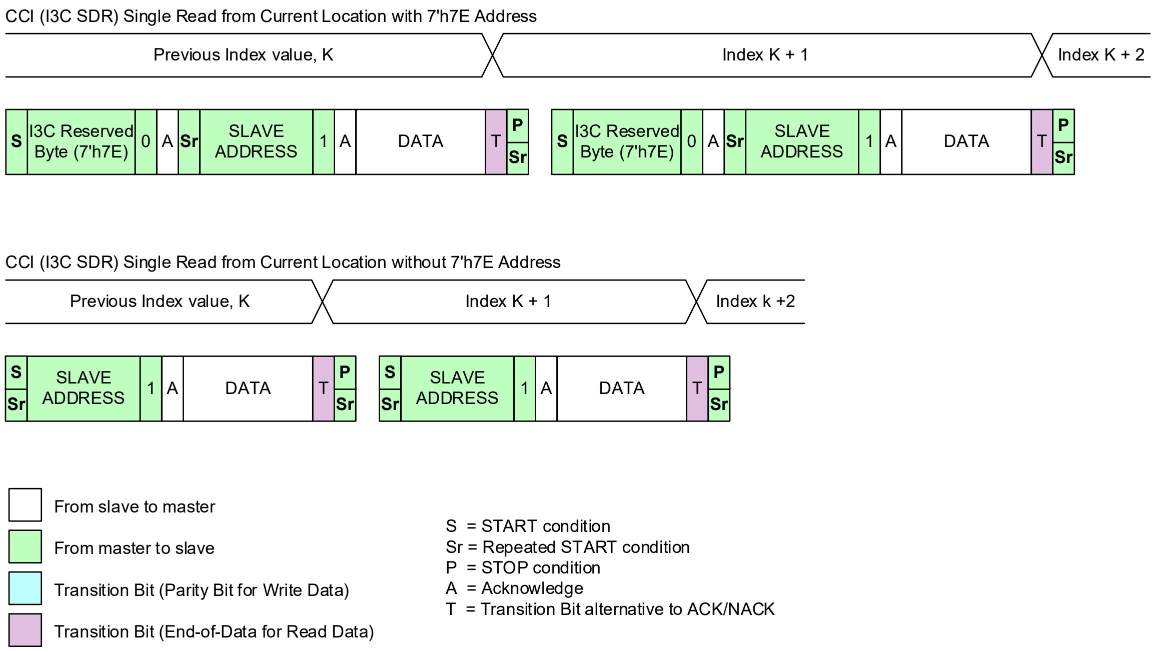


Figure 11 CCI (I3C SDR) Single Read from Current Location

6.2.1.2.3 CCI (I3C SDR) Sequential Read from Random Location

The sequential read starting from a random location is illustrated in ***Figure 12***. The master does a dummy write operation to the desired INDEX, issues a Repeated START condition, and then addresses the slave again with the read operation. After acknowledging its slave address, the slave starts to output data onto the SDA line. If a master doesn't abort the read transaction by using the transition bit, this acts as a signal for the slave to continue a read operation from the next INDEX. When the master has read the last data byte, it can abort a read transaction by setting the transition bit and then issuing a STOP or Repeated START condition. Furthermore, when the master reads a large amount of data exceeding the Max Read Length (MRL) limit (see the I3C Specification ***[MIPI03]***), the slave can also terminate a read transaction by setting the transition bit.

Note:

When selecting a suitable value for MRL, the designer of the slave device and the system designer should take into account the needs of the payload that the CCI will carry. For example, in the CCS Data Transfer Interface ***[MIPI04]****, it is beneficial to support an MRL of 64 bytes or larger (i.e. 64 bytes for Data payload).*

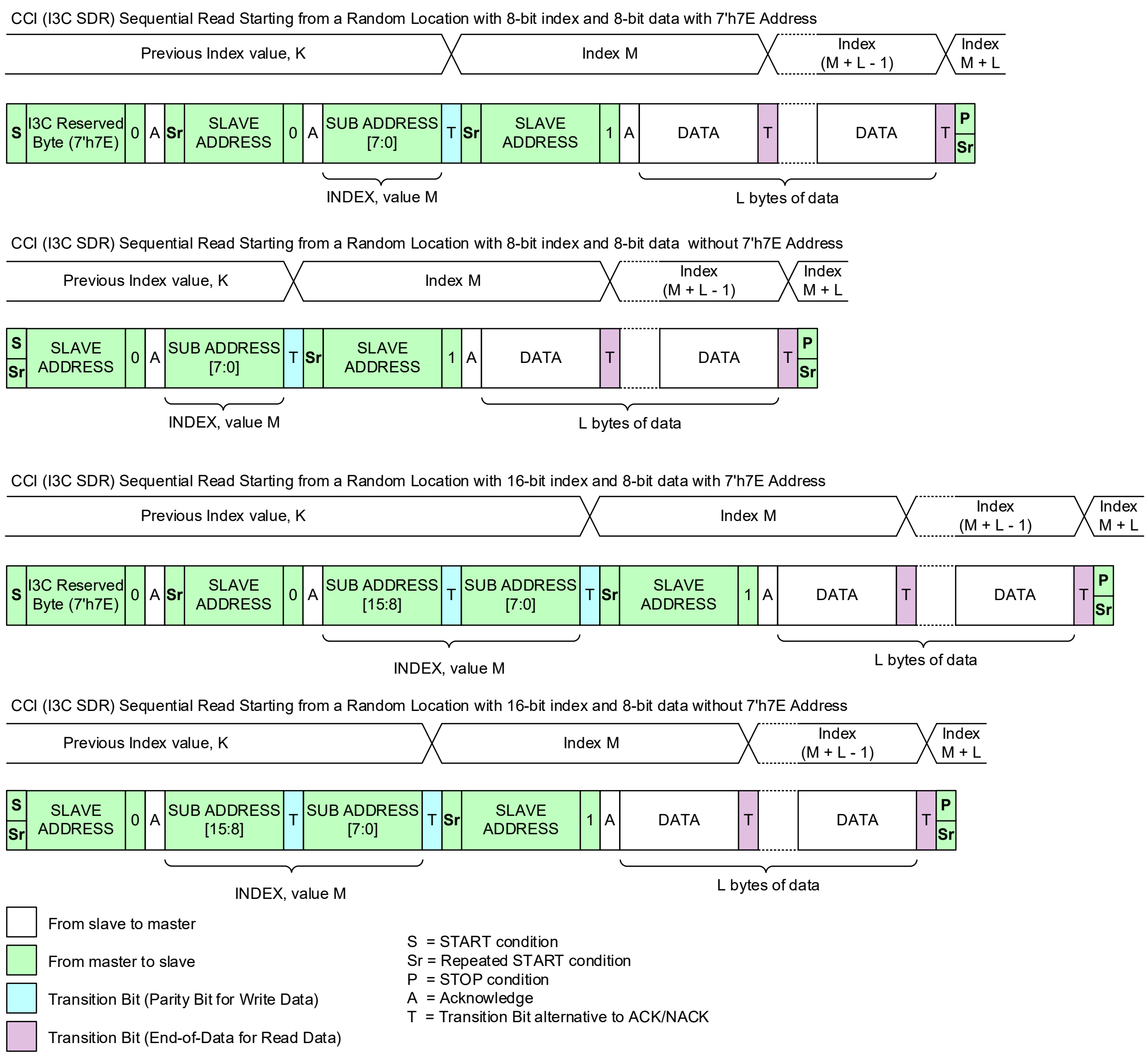


Figure 12 CCI (I3C SDR) Sequential Read Starting from Random Location

6.2.1.2.4 CCI (I3C SDR) Sequential Read from Current Location

A sequential read starting from the current location (***Figure 13***) is similar to a sequential read from a random location. The only exception is when there is no dummy write operation. The master or slave terminates a read transaction by setting the transition bit, and then issues a STOP or Repeated START condition.

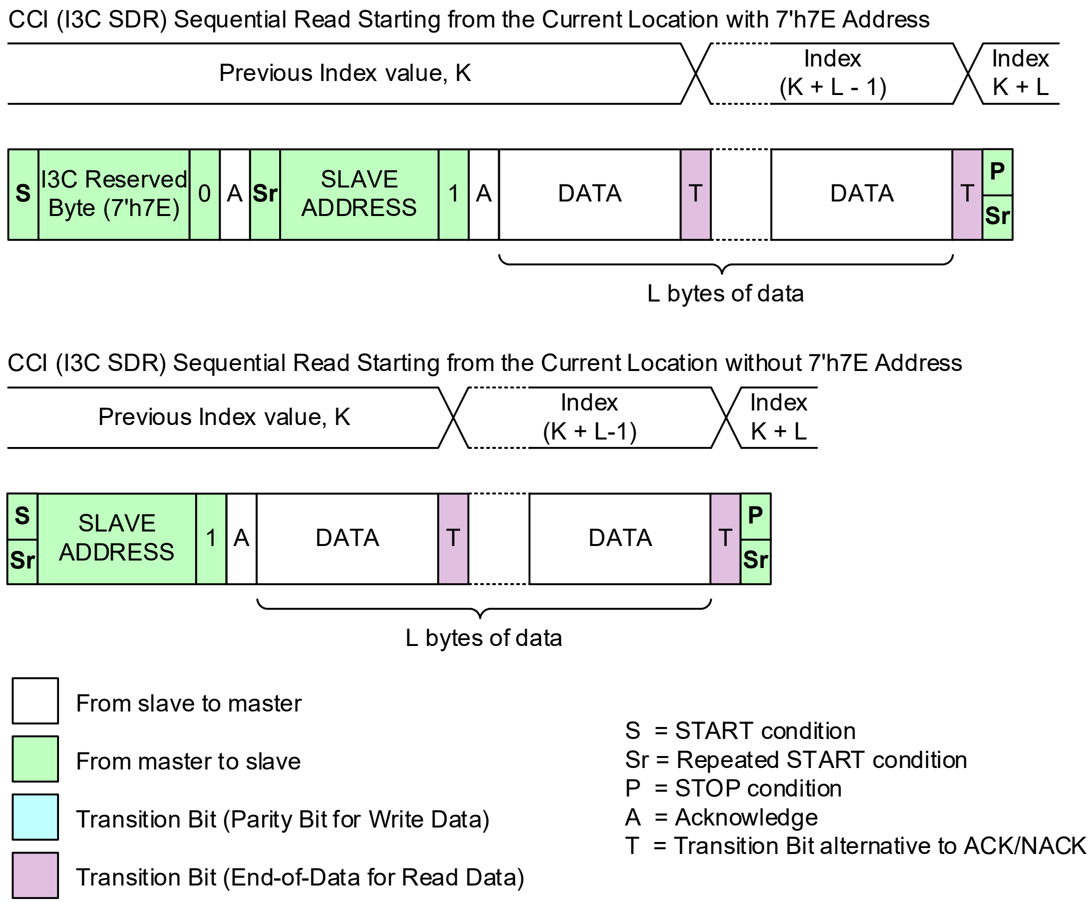


Figure 13 CCI (I3C SDR) Sequential Read Starting from Current Location

6.2.1.2.5 CCI (I3C SDR) Single Write to Random Location

A write operation to a random location is illustrated in ***Figure 14***. The master issues a write operation to the slave, then issues the INDEX and data after the slave has acknowledged the write operation. The write operation is terminated with a STOP or Repeated START condition from the master.

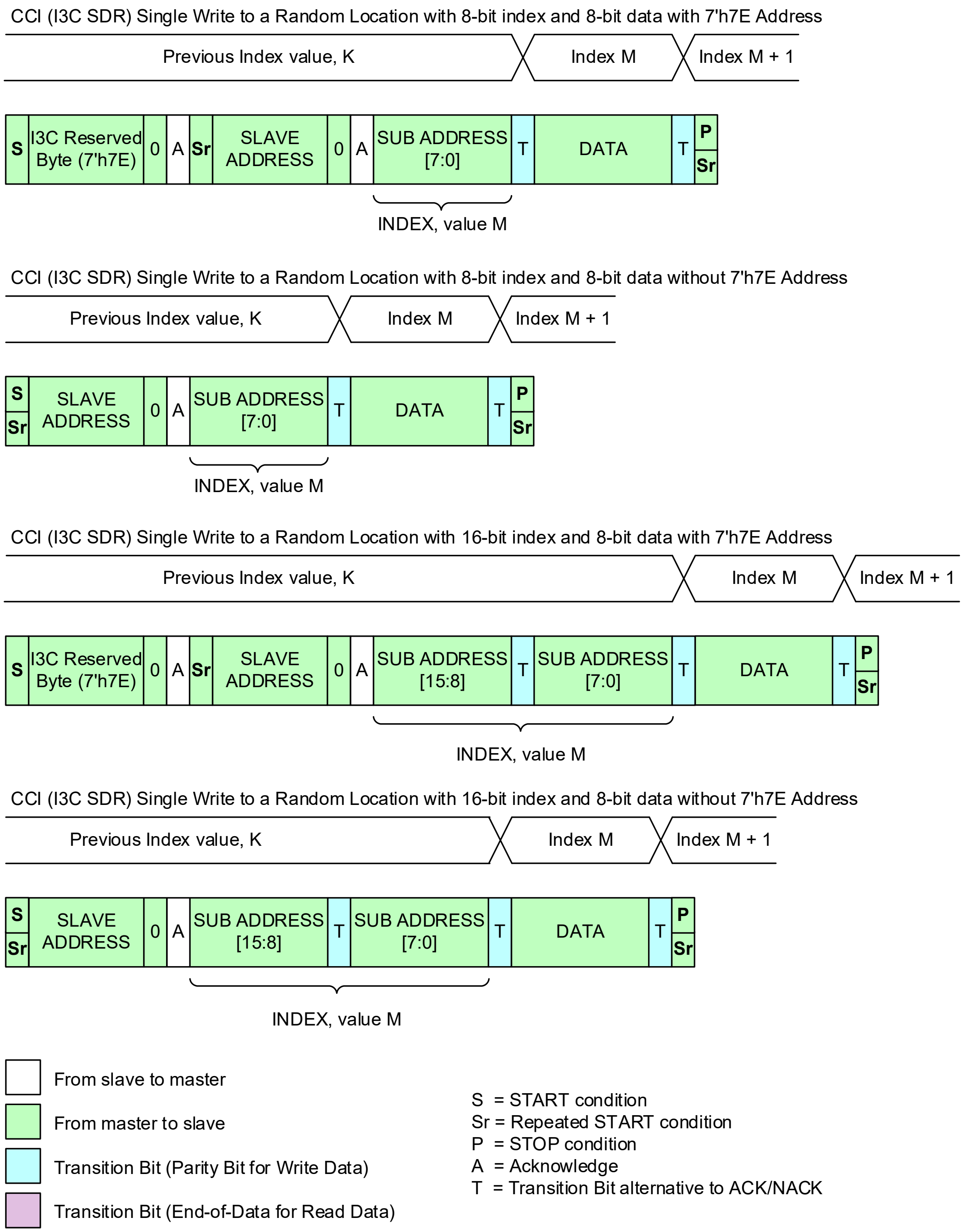


Figure 14 CCI (I3C SDR) Single Write to Random Location

6.2.1.2.6 CCI (I3C SDR) Sequential Write Starting from Random Location

The Sequential Write Starting from Random Location operation is illustrated in ***Figure 15***. The slave auto-increments the INDEX after each data byte is received. The Sequential Write Starting from Random Location operation is terminated with a STOP or Repeated START condition from the master.

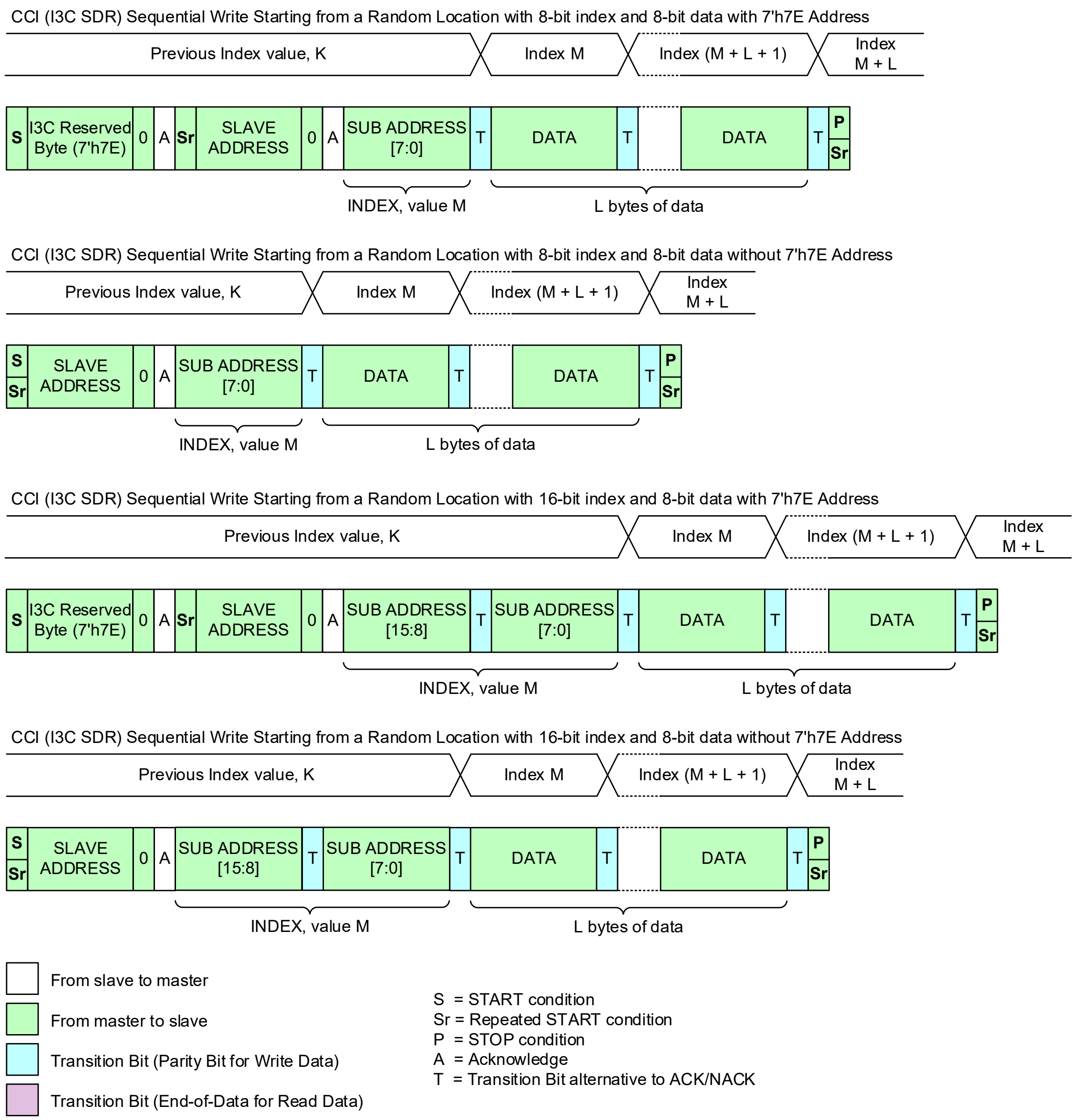


Figure 15 CCI (I3C SDR) Sequential Write Starting from Random Location

6.2.2 CCI (I3C DDR) Data Transfer Protocol

6.2.2.1 CCI (I3C DDR) Message Type

The **CCI (I3C DDR)** master shall start a DDR Message with either the I3C ENTHDR0 CCC, or the I3C HDR Restart Pattern. The **CCI (I3C DDR)** master shall end a DDR Message by issuing either the I3C HDR Restart Pattern, or the I3C HDR Exit Pattern.

Two Message types are defined for DDR Messages: DDR Write Message and DDR Read Message.

CCI (I3C DDR) supports either:

- 8-bit LENGTH and 8-bit INDEX with 8-bit data

  Both the LENGTH and the INDEX shall be included in the first data word of the DDR Write Message.

or:

- 16-bit LENGTH and 16-bit INDEX with 8-bit data

  The LENGTH shall be included in the first data word of the DDR Write Message, and the INDEX shall be included in the second data word of the DDR Write Message.

The slave device in question defines what Message type is used.

The LENGTH field defines the number of 8-bit data bytes in the Read or Write Data Words. The LENGTH field is zero-based, i.e. if the master wishes to read or write N bytes, then the value in the LENGTH field must be N–1.

Examples:

- 0 LENGTH means 1 byte
- 255 LENGTH means 256 bytes

When a multi-byte register is accessed via **CCI (I3C DDR)**, the transmission byte order described in ***Section 6.6*** shall be the same as for **CCI (I^2C)** and **CCI (I3C SDR)**.

Example:

For the 16-bit register read shown in ***Figure 17***, the DATA0 byte contains bits Data[15:8] and the DATA1 byte contains bits Data[7:0].

6.2.2.2 CCI (I3C DDR) Read/Write Operations

A **CCI (I3C DDR)** compatible device shall support the two read operations and one write operation shown in ***Table 3***, as detailed in the following sub-sections:

Table 3 CCI (I3C DDR) Read/Write Operations

Type	Operation	Section
Read	Sequential Read from Random Location	***6.2.2.2.2***
	Concatenated Sequential Read from Random Location	***6.2.2.2.3***
Write	Sequential Write Starting from Random Location	***6.2.2.2.4***

The INDEX in the slave device must be auto-incremented after each read/write operation. This is also explained in the following sections.

6.2.2.2.1 CCI (I3C DDR) Command Definitions

As defined in the I3C Specification ***[MIPI03]***, bit[15] of the HDR-DDR Command Word is the R/W bit and bits[14:8] contain the Command Code. Command Code values are reserved per application, and **CCI (I3C DDR)** defines one such Command Code: 7'b0000000.

This single Command Code is sufficient, because the slave can still distinguish between three different R/W operations. Consider the example of 16-bit LENGTH and 16-bit INDEX:

- If the slave receives a Data Word greater than 4 bytes, then the operation is "Sequential Write Starting from Random Location".
- If the slave receives a Data Word of 4 bytes before the HDR Restart Pattern, then there are two possibilities:
  - If the value of the LENGTH field is ≤ MRL–1, then the operation is "Sequential Read Starting from a Random Location".
  - If the value of the LENGTH field is > MRL–1, then the operation is "Concatenated Sequential Read Starting from a Random Location".

Table 4 defines the I3C HDR-DDR Command Codes (including R/W bit) for each **CCI (I3C DDR)** Read/Write operation.

For **CCI (I3C DDR)**, the slave address is 7 bits long, and appears in bits[7:1] of the HDR-DDR Command Word.

Table 4 CCI (I3C DDR) Read/Write Operation Command Codes

Type	Operation	Command Code Position	R/W Bit and Command Code *See Note 1*	Section
Write	Sequential Write Starting from Random Location	Command Word	0x00	***6.2.2.2.4***
Read	Sequential Read Starting from Random Location	Command Word for LENGTH & INDEX	0x00	***6.2.2.2.2***
		Command Word for ReadData	0x80	
	Concatenated Sequential Read Starting from Random Location	Command Word for LENGTH & INDEX	0x00	***6.2.2.2.3***
		Command Word for ReadData	0x80	

Note:

1. In all five cases, the 7-bit Command Code in the low seven bits is 7'b0000000. Only the R/W bit, which is the high bit of the byte, changes.

6.2.2.2.2 CCI (I3C DDR) Sequential Read From Random Location

In a sequential read from a random location (***Figure 16*** and ***Figure 17***):

- The master shall transmit:
  - The HDR-DDR Command Word for LENGTH and INDEX
  - The HDR-DDR Data Word, including LENGTH and INDEX
  - The HDR-DDR CRC Word
  - The HDR Restart Pattern
  - The HDR-DDR Command Word for ReadData
- Then the slave shall send one or more HDR-DDR Read Data Words followed by the HDR-DDR CRC Word
- Finally the master shall send either the HDR Restart Pattern or the HDR Exit Pattern.

If the number of 8-bit data words read is odd (i.e. the value in the LENGTH field is even), then the slave shall insert one padding byte in the second byte of the last data word, with value 8'h00. The slave shall not increment INDEX by the padding byte. The master shall take into account that the data includes the padding byte in odd transfers, and that the INDEX is not incremented by the padding byte.

The master shall load the Sub Address into the INDEX and auto-increment the INDEX after each data byte is received. The master can identify the padding byte from the value of the LENGTH field and the number of the received 8-bit data words, and shall ignore the padding byte. Note that the INDEX is not incremented by the padding byte.

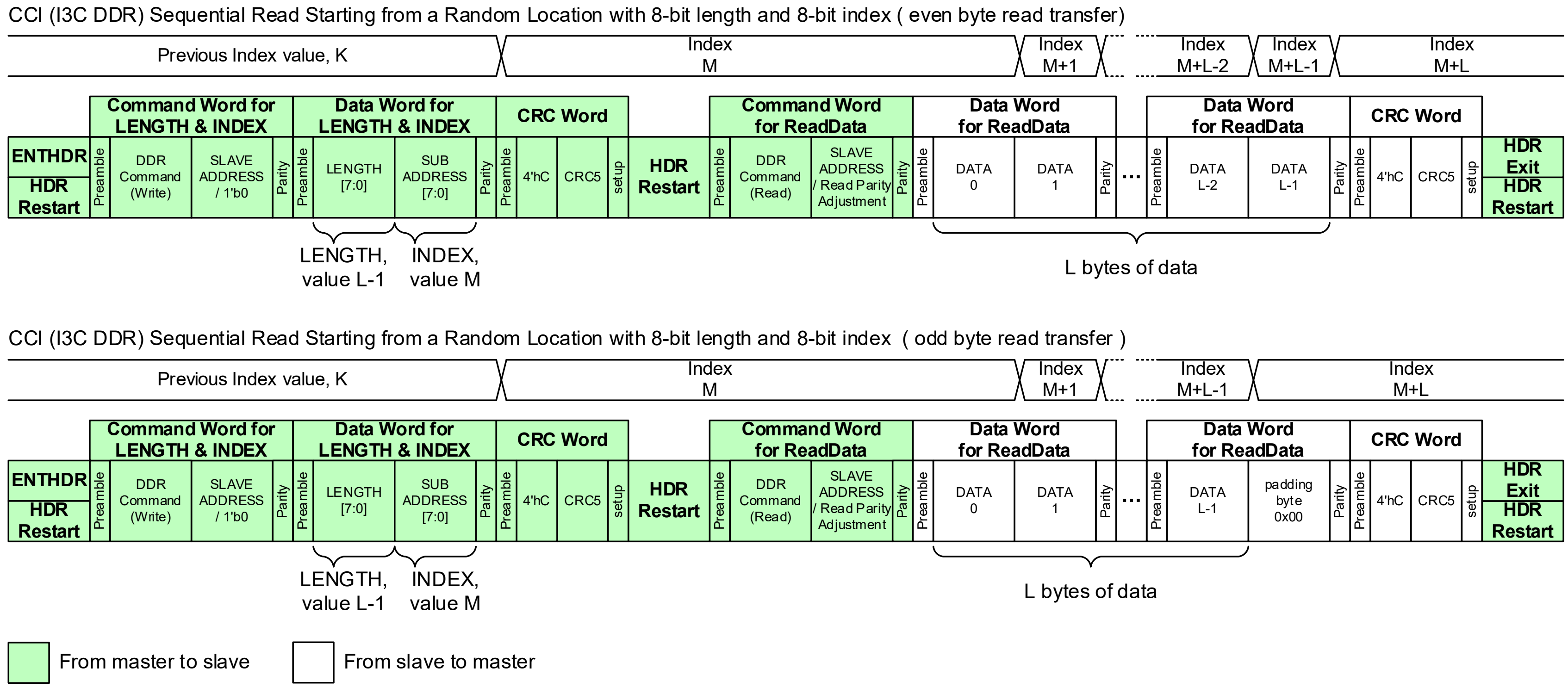


Figure 16 CCI (I3C DDR) Sequential Read from Random Location: 8-bit LENGTH & INDEX

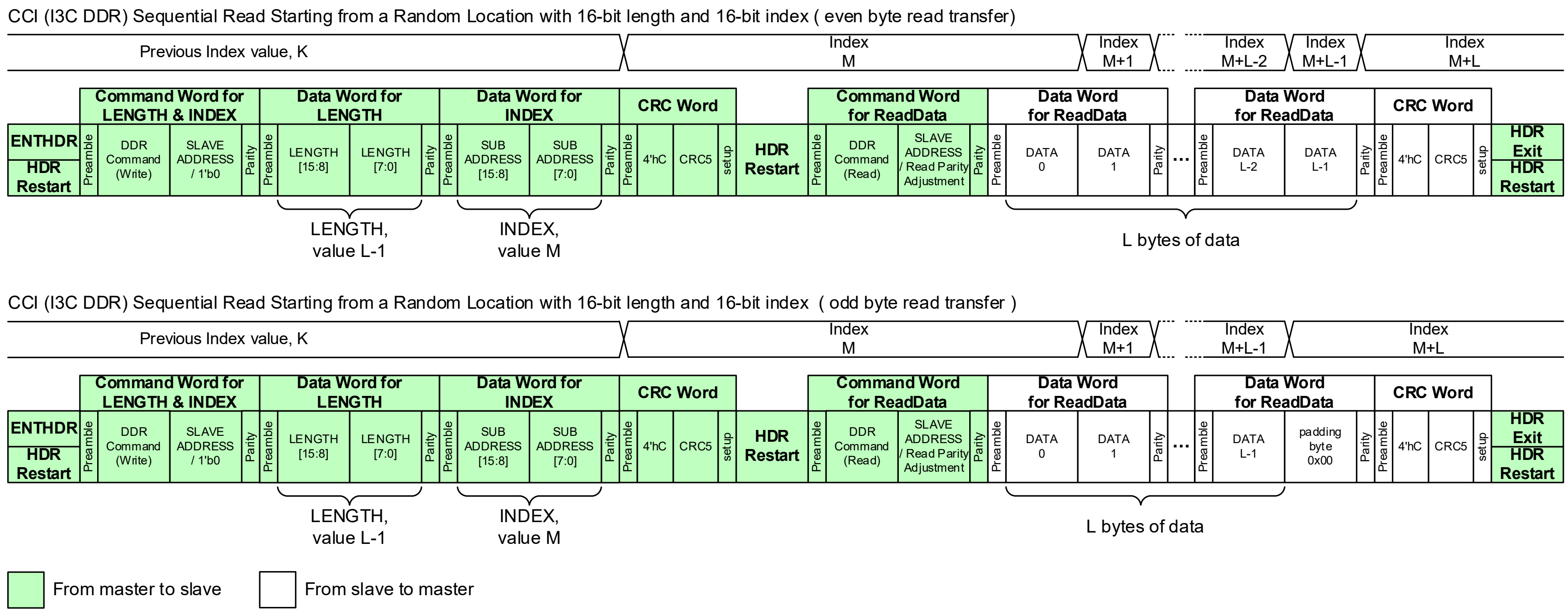


Figure 17 CCI (I3C DDR) Sequential Read from Random Location: 16-bit LENGTH & INDEX

6.2.2.2.3 CCI (I3C DDR) Concatenated Sequential Read from Random Location

When the master desires to read data longer than the slave's I3C Max Read Length (MRL) ***[MIPI03]***, the master can divide the data into multiple units, and efficiently read the data using the Concatenated Sequential Read from Random Location operation (***Figure 18*** and ***Figure 19***). The master shall divide the data into multiple units, where all units except the last unit shall use the MRL size, and the last unit shall use a size less than or equal to the MRL. The MRL size is programmable.

In a Concatenated Sequential Read Starting from Random Location:

- The master shall first transmit the total LENGTH for the data to be read.
- The master shall use multiple read Messages. The slave shall transmit the initial read Messages to the master using the programmed MRL data bytes. And the slave may use no more than the programmed MRL data bytes to transfer the last Message.
  - If the full amount of requested data has not been received yet, then the master shall transmit another read Message, but without LENGTH and INDEX.
  - After receiving the read Message without LENGTH and INDEX, the slave shall continue transmission of the read data to the master, resuming from the previous LENGTH and INDEX.

The master shall continue to transmit read Messages without LENGTH and INDEX multiple times, until the last data is received.

Note:

> *When selecting a suitable value for MRL, the designer of the slave device and the system designer should take into account the needs of the payload that the CCI will carry. For example, in the CCS Data Transfer Interface **[MIPI04]**, it is beneficial to support an MRL of 64 bytes or larger (i.e. 64 bytes for Data payload).*

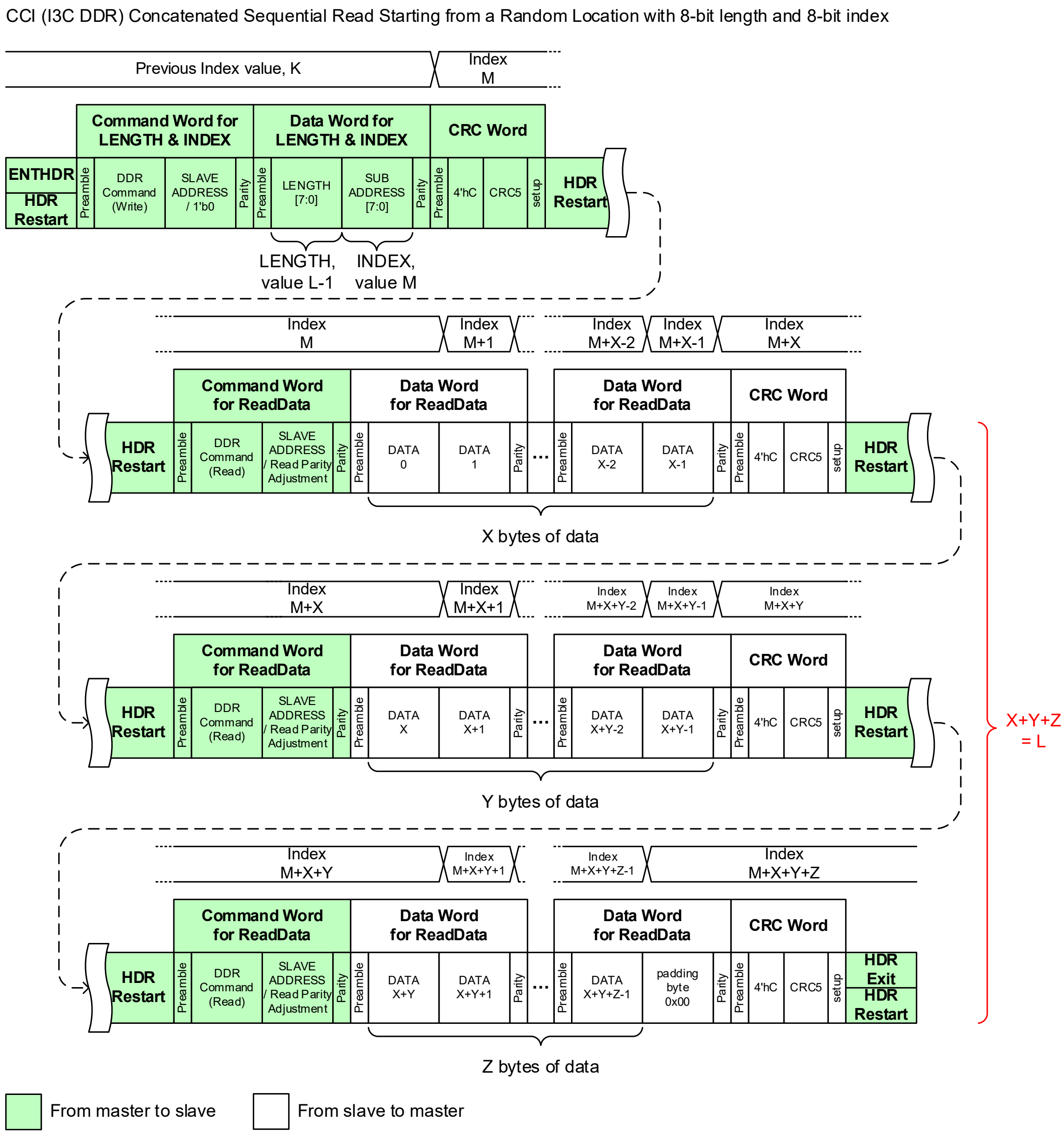


Figure 18 CCI (I3C DDR) Concatenated Sequential Read, Random Location: 8-bit LENGTH & INDEX

CCI (I3C DDR) Concatenated Sequential Read Starting from a Random Location with 16-bit length and 16-bit index

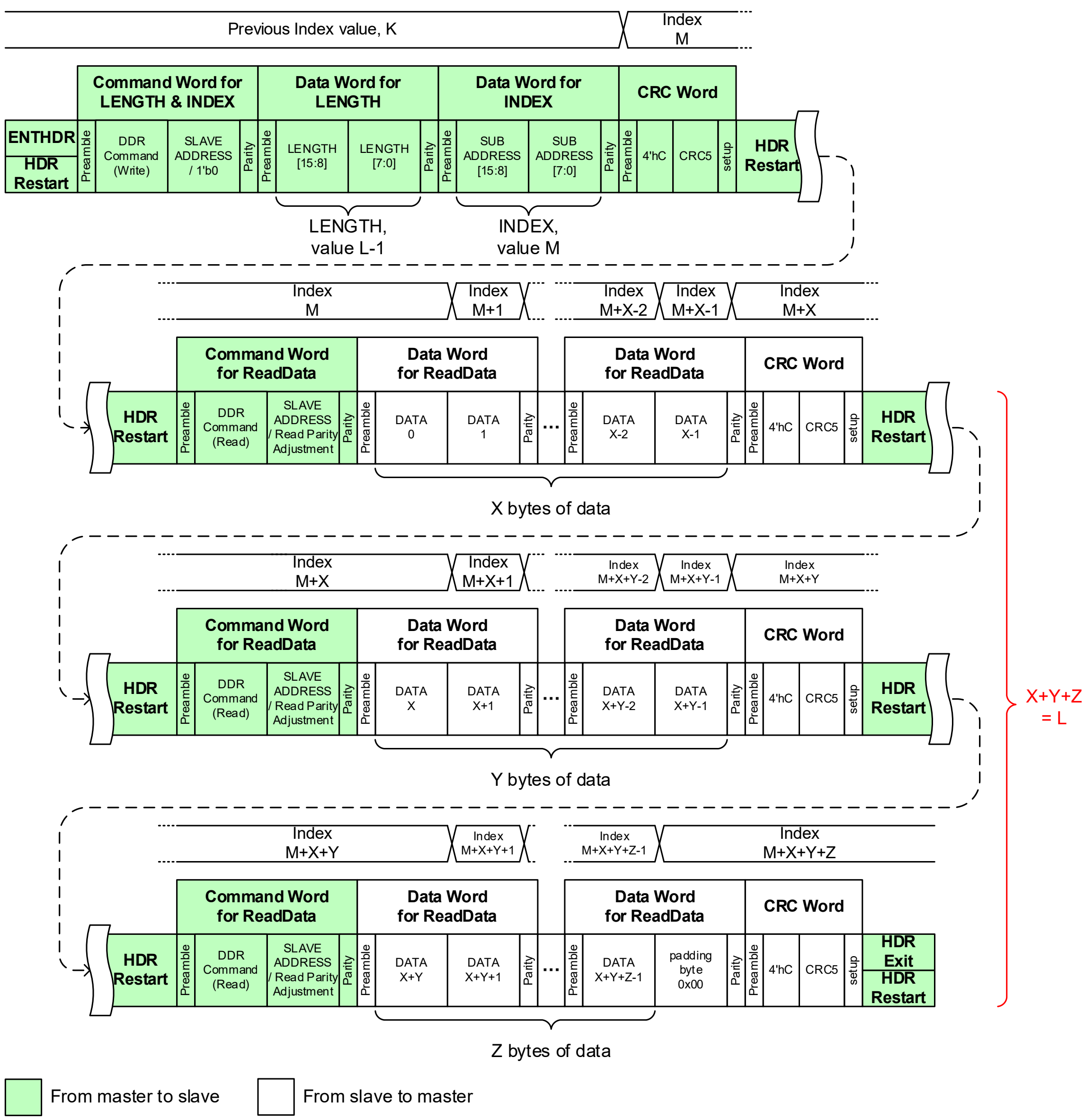


Figure 19 CCI (I3C DDR) Concatenated Sequential Read, Random Location: 16-bit LENGTH & INDEX

6.2.2.2.4 CCI (I3C DDR) Sequential Write Starting from Random Location

In a Sequential Write Starting from Random Location (***Figure 20***), the master shall transmit:

- The HDR-DDR Command Word
- The HDR-DDR Data Word including LENGTH and INDEX
- One or more HDR-DDR Write Data Words, and
- The HDR-DDR CRC Word.

If the number of 8-bit data words written is odd (i.e. the value in the LENGTH field is even), then the master shall insert one padding byte in the second byte of the last data word, with value 8'h00. When the slave receives the Sub Address, the slave loads it into the INDEX and auto-increments the INDEX after each data byte is received.

The slave can identify the padding byte from the value of the LENGTH field and the number of 8-bit data words received, and shall ignore the padding byte. Note that the INDEX is not incremented by the padding byte.

In a Sequential Write Starting from Random Location, the value of LENGTH shall be set such that the master does not exceed the maximum data byte length limit defined by the slave's I3C Max Write Length (MWL) ***[MIPI03]***. Note that the total number of bytes of "Data Word for INDEX", "Data Word for LENGTH", and "Data Word for Write Data" shall not exceed MWL.

Example:

For a slave with MWL of 8 bytes, using 16-bit INDEX (so "Data Word for INDEX" is 2 bytes) and 16-bit LENGTH (so "Data Word for LENGTH" is 2 bytes), the maximum number of "Data Word for Write Data" is 8 – (2 + 2) bytes = 4 bytes. Since the LENGTH field is zero-based, it would contain the value 3 (16'd3).

The slave cannot terminate the DDR Write Message, and shall receive all HDR-DDR Write Data sent by the master.

Note:

*When selecting a suitable value for MWL, the designer of the slave device and the system designer should take into account the needs of the payload that the CCI will carry. For example, in the CCS Data Transfer Interface **[MIPI04]**, it is beneficial to support an MWL of 68 bytes or larger (i.e. 64 bytes for Data payload + 2 bytes for a Data Word for INDEX + 2 bytes for a Data Word for LENGTH).*

Figure 20 CCI (I3C DDR) Sequential Write Starting from Random Location

6.3 CCI (I3C) Error Detection and Recovery

6.3.1 CCI (I3C SDR) Error Detection and Recovery Method

The error detection and recovery methods specified in this Section are provided in order to avoid fatal conditions when errors occur. The CCI (I3C SDR) error detection and recovery methods follow the I3C Specification. The I3C error detection and recovery method for the Slave and Master are specified in ***[MIPI03]***. A CCI (I3C SDR) compatible device shall support both the methods defined by I3C and the methods defined in this Section regarding CCI (I3C SDR), respectively.

6.3.1.1 Error Detection and Recovery Method for CCI (I3C SDR) Slave Devices

The SS0 error summarized in ***Table 5*** shall be supported for all CCI (I3C SDR) Slave Devices. If the CCI Slave detects the SS0 error, the CCI Slave shall set to 1'b1 in Protocol Error Flag of GETSTATUS. Details of the SS0 error are described in ***Section 6.3.1.1.2***.

Table 5 CCI (I3C SDR) Slave Error Types

Error Type	Description	Error Detection Method	Error Recovery Method
SS0	**Read without INDEX Error**	Detect an error if the Slave receives the Slave's Dynamic Address (except 7'h7E) with a Read (R/W bit is 1) correctly but it does not have the INDEX.	Enable STOP or Repeated START detector and neglect other patterns.

6.3.1.1.1 Clearing the INDEX After Detecting I3C Error

The CCI (I3C SDR) Slave shall clear the INDEX value when the I3C Slave detects S2 ***[MIPI03]*** or S6 (***[MIPI03]***, optional) during the "CCI (I3C SDR) Read/Write Operations" in ***Table 2***. Note that this rule shall not be applicable to other Operations (e.g., I3C CCC Transfers). As defined in the I3C specification, the I3C Slave sets to 1'b1 in the Protocol Error Flag of GETSTATUS (defined in the I3C specification) when the I3C Slave detects an error.

Clearing the INDEX due to S2 and S6 errors in the CCI (I3C SDR) Write Operations (Single Write to Random Location, Sequential Write Starting from Random Location) is described below:

- If an S2 error occurs in the CCI (I3C SDR) Write Operations, the CCI Slave cannot count up the INDEX because the CCI Slave cannot receive the correct write data. As a result, the INDEX in the CCI Slave may be different from the INDEX value that the Master is expecting. In order to avoid this situation, the CCI Slave shall clear the INDEX value.
- When the I3C Master doesn't have the collision detector and the I3C Slave has it, the INDEX in the CCI Slave may be different from the INDEX value that the Master is expecting in case of an S6 error. This is because the CCI Master assumes the INDEX counter in the Slave to be counting up, but the CCI Slave stops the counter. In order to avoid this situation, the CCI Slave shall clear the INDEX value.

Clearing the INDEX due to an S2 error in the CCI (I3C SDR) Read Operations (Single/Sequential Read to Random Location) is described below:

- If an S2 error occurs in the CCI (I3C SDR) Single/Sequential Read from Random Location during sub address, the CCI Slave cannot update the value of INDEX because the I3C Slave cannot get the correct sub address. This could cause slave to send undefined or wrong data. In order to avoid this situation, the CCI Slave shall clear the INDEX value.

6.3.1.1.2 SS0 Error

The CCI Slave shall detect an SS0 error if the CCI Slave receives the slave address (except 7’h7E) with a Read (R/W bit is 1) correctly but it does not have the INDEX value. After detecting the SS0 error, the CCI Slave shall replace ACK generated by the I3C Slave with NACK during SS0 error and then wait for STOP or Repeated START. ***Figure 21*** illustrates how NACK is generated in CCI (I3C SDR) Sequential Read from Random Location, when SS0 error occurs during this Message.

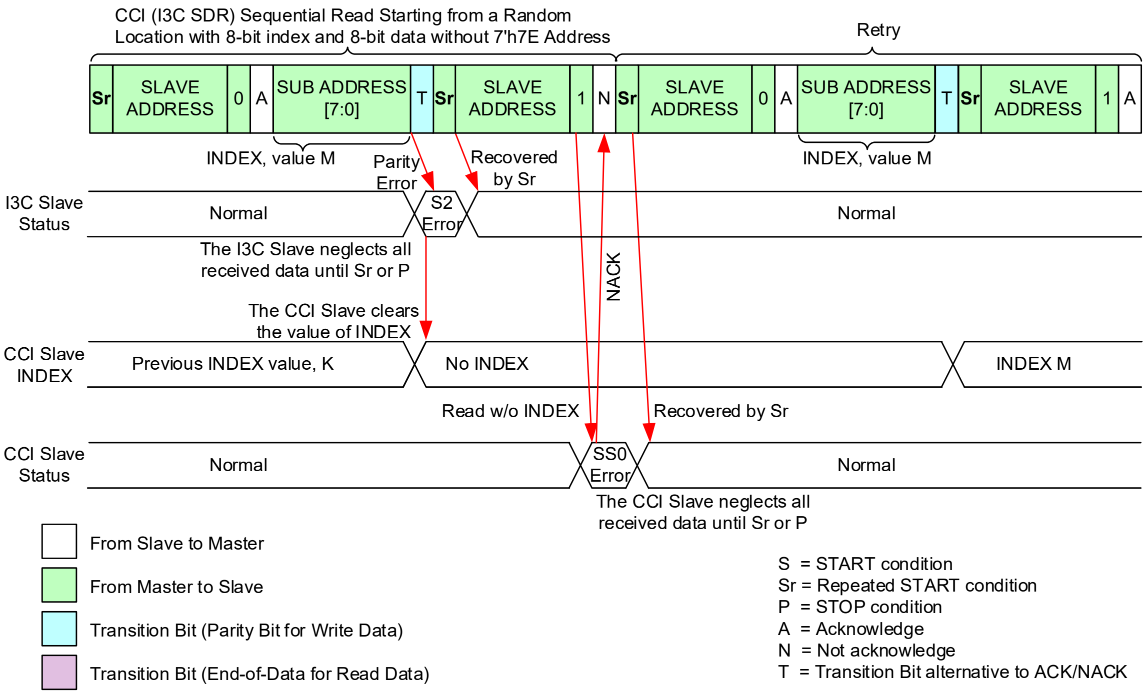


Figure 21 Example of SS0 Error Detection

6.3.2 CCI (I3C DDR) Error Detection and Recovery Method

The error detection and recovery methods specified in this Section are provided in order to avoid fatal conditions when errors occur. The CCI (I3C DDR) error detection and recovery methods follow the I3C Specification. The I3C error detection and recovery method for the Slave and Master are specified in ***[MIPI03]***. A CCI (I3C DDR) compatible device shall support both the methods defined by I3C and the methods defined in this section regarding CCI (I3C DDR) respectively.

6.3.2.1 Error Detection and Recovery Method for CCI (I3C DDR) Slave Devices

The two Error Types summarized in ***Table 6*** shall be supported for all CCI (I3C DDR) Slave Devices. Each Error Type is further explained below the table. If the Slave detects an SD0 or SD1 error, the Slave shall set the Protocol Error Flag in GETSTATUS (defined in the I3C specification) to 1'b1. Details of the SD0 and SD1 errors are described in ***Section 6.3.2.1.2*** and ***Section 6.3.2.1.3***, respectively.

Table 6 CCI (I3C DDR) Slave Error Types

Error Type	Description	Error Detection Method	Error Recovery Method
SD0	**Read without INDEX Error**	Detect an error if the Slave receives the DDR command Word[15] = 1 (Read) correctly, but it does not have the INDEX	Enable HDR Exit or HDR Restart detector and neglect other patterns
SD1	**Write over LENGTH Error**	Detect an error if the value of Preamble following LENGTH +1 bytes of the Write Data is 2b11	Clear INDEX value. Enable HDR Exit or HDR Restart detector and neglect other patterns

6.3.2.1.1 Clearing INDEX After Detecting I3C Error

The CCI Slave shall clear the INDEX value when the I3C Slave detects an I3C DDR error defined in the I3C specification (Framing Error, Parity Error, CRC5 Error, or optional Monitoring Error) during the "CCI (I3C DDR) Read/Write Operations" in ***Table 3***. Note that this rule shall not be applicable to other Operations (e.g., I3C CCC Transfers). As defined in the I3C specification, when the I3C Slave detects an error it sets the Protocol Error Flag in GETSTATUS (defined in the I3C specification) to 1'b1.

If a parity error occurs during the sub address in a CCI (I3C DDR) Read Operation (i.e. Sequential or Concatenated Sequential Read from Random Location), the CCI Slave cannot update the value of INDEX because the I3C Slave cannot get the correct sub address. This could cause slave to send undefined or wrong data. In order to avoid this situation, the CCI Slave shall clear the INDEX value.

6.3.2.1.2 SD0 Error

The CCI Slave shall detect an SD0 error if the CCI Slave receives a DDR command with Read (DDR command Word[15] = 1) correctly, but no INDEX value. After detecting the SD0 error, the CCI Slave shall replace the ACK generated by the I3C Slave with a NACK during SD0 error, and then wait for HDR Exit or HDR Restart. ***Figure 22*** illustrates how NACK is generated in a CCI (I3C DDR) Sequential Read from Random Location.

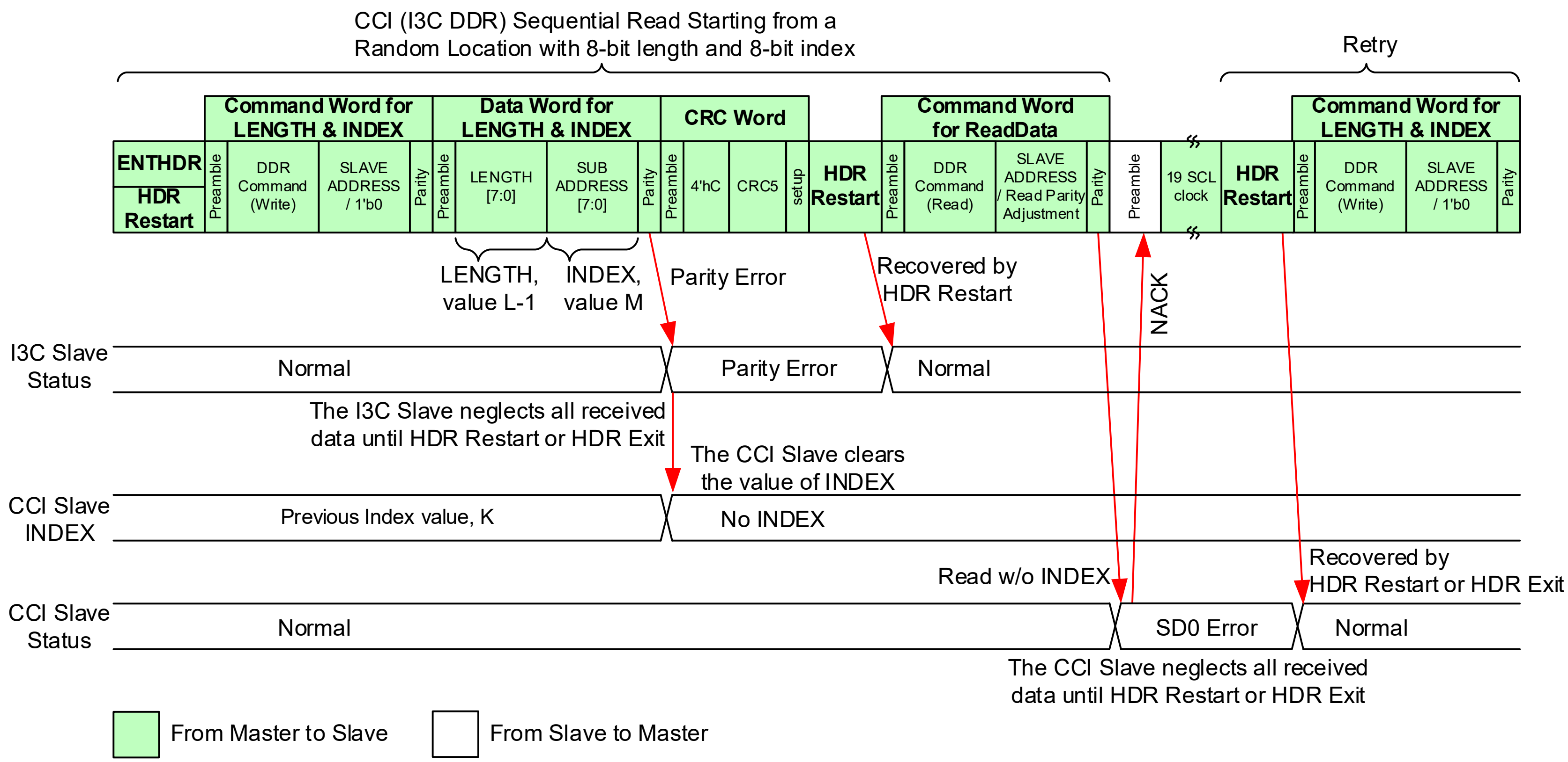


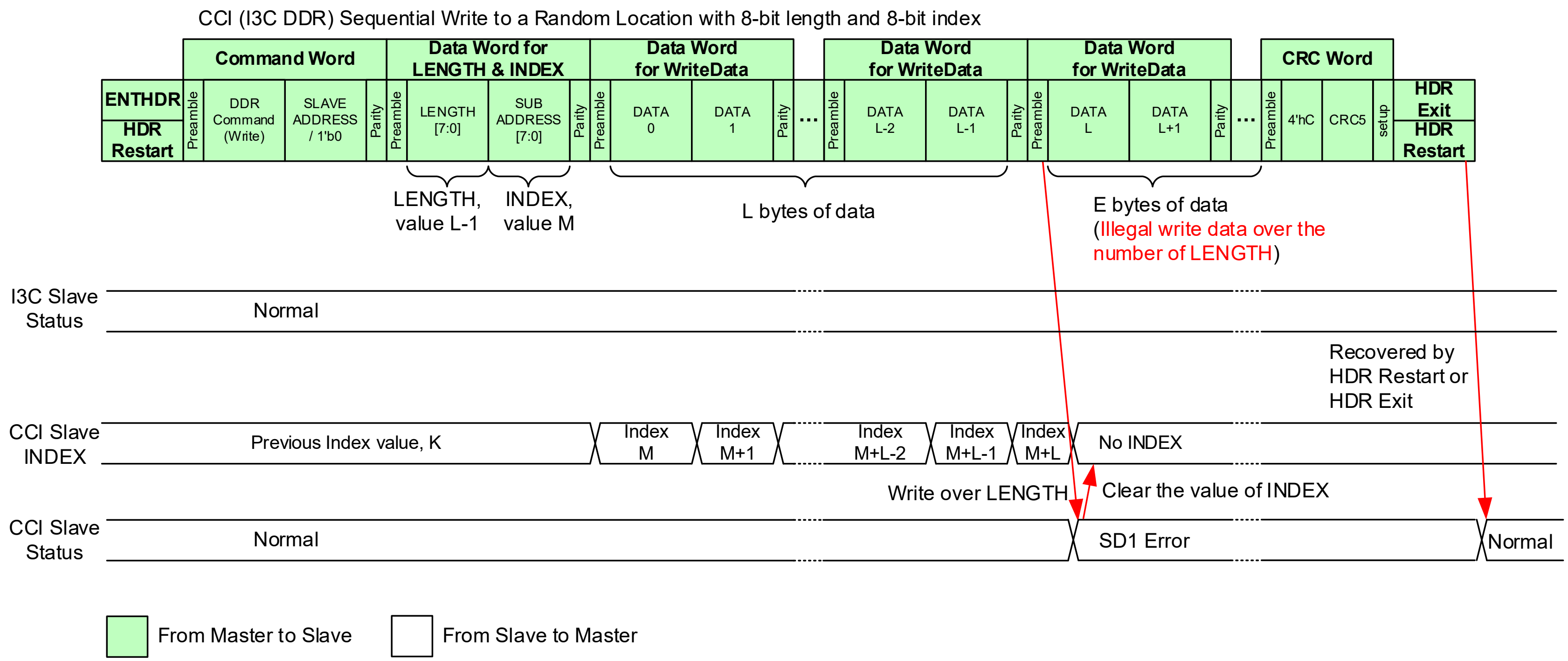
Figure 22 Example of SD0 Error Detection

6.3.2.1.3 SD1 Error

In CCI (I3C DDR), the LENGTH is included in the structure. If the CCI Slave receives data exceeding the LENGTH, the Slave shall discard the extra data and detect this as an error condition.

In order to inform the Master of the error condition, the CCI Slave shall detect the SD1 error if the CCI Slave receives a Preamble with value 2'b11 after receiving L bytes of WriteData. After detecting the SD1 error, the CCI Slave shall clear the value of INDEX and then wait for HDR Exit or HDR Restart. ***Figure 23*** illustrates how INDEX is cleared in CCI (I3C DDR) Sequential Write to Random Location.

582



583

Figure 23 Example of SD1 Error Detection

6.3.2.2 Error Detection and Recovery Method for CCI (I3C DDR) Master Devices

The MD0 Error Type summarized in ***Table 7*** may be supported for all CCI (I3C DDR) Master Devices. Each Error Type is further explained below ***Table 7***. Details of MD0 error are described in ***Section 6.3.2.2.1***.

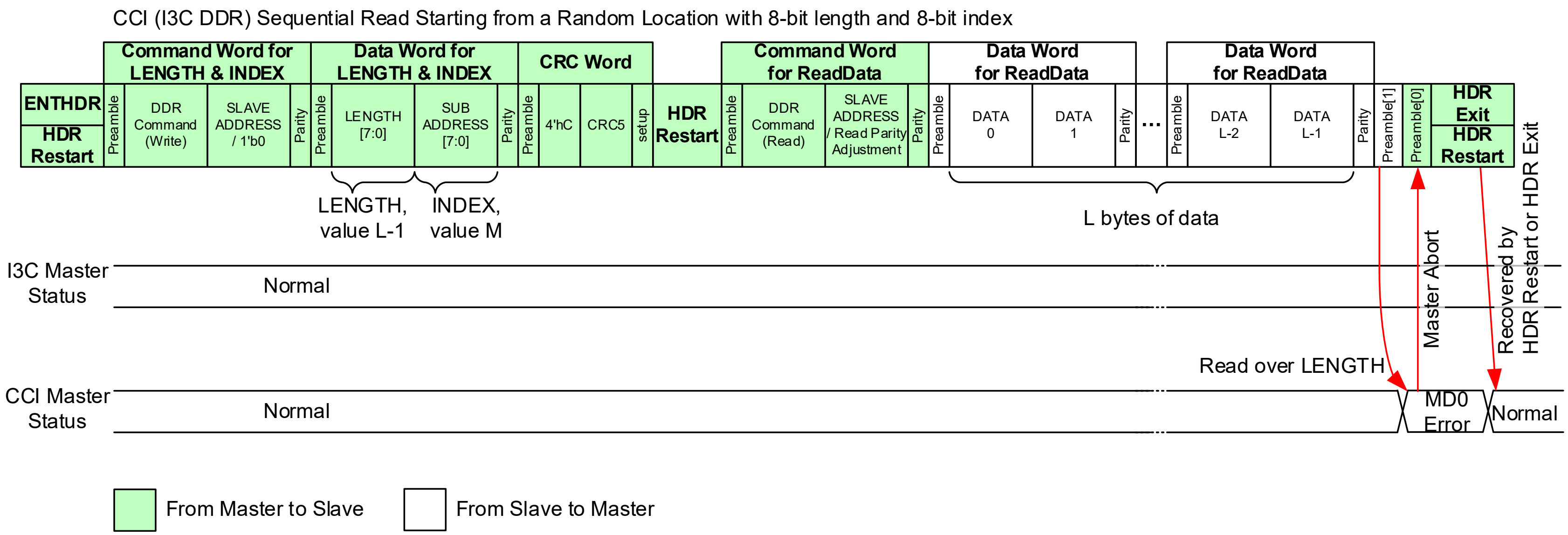
Table 7 CCI (I3C DDR) Master Error Type

Error Type	Description	Error Detection Method	Error Recovery Method
MD0 (optional)	**Read over LENGTH Error**	Detect an error if the value of Preamble[1] following LENGTH +1 bytes of the Read Data is 1b1	Send Master Abort and then HDR Exit or HDR Restart

6.3.2.2.1 MD0 Error

In CCI (I3C DDR), the LENGTH is included in the structure. If the CCI Master receives read data exceeding the LENGTH, it might cause big issues because memory leakage may occur, depending on the implementation. In order to avoid fatal problems, the CCI Master may detect the MD0 error if the CCI Master receives Preamble[1]=1'b1 after receiving LENGTH+1 bytes of ReadData. After detecting the MD0 Error, the CCI Master may send Master Abort, and then send HDR Exit or HDR Restart, as illustrated in ***Figure 24***.

593



594

Figure 24 Example of MD0 Error Detection

6.3.3 Error Detection and Recovery for CCI (I3C) Master Devices

In many cases, the Master can detect an error inside the Slave by receiving NACK. However, for example in case of an S2 or S6 error in the CCI (I3C SDR) Write Operations, the Master cannot detect it by receiving NACK because there is no chance for the Slave to send NACK by the end of the operation (STOP or Repeated START). Therefore if high reliability is required, the Master may transmit GETSTATUS (defined in the I3C specification) at each important point.

Note:

E.g., the important point is that after critical CCI (I3C SDR) Write Operations, after CCI (I3C SDR) Write Operations before moving to CCI (I3C DDR), after multiple CCI (I3C SDR) Read/Write Operations before long pause if the last message is CCI (I3C SDR) Write Operations.

As a result, the Master can detect each error by the following methods:

1. Slave's error by receiving NACK
2. Slave's error during CCI (I3C SDR) or CCI (I3C DDR) Write Operations by sending GETSTATUS
3. Master's I3C SDR Error defined in the I3C specification (M0, M1 or M2 error)
4. Master's I3C DDR Error defined in the I3C specification (including the Master sending HDR Exit or HDR Restart pattern)

After detecting an error, the Master should try the following error recovery method:

1. The Master may retry sending the same CCI (I3C SDR) Read/Write Operations or CCI (I3C DDR) Read/Write Operations again.
2. The Master may send certain other CCI (I3C SDR) Read/Write Operations or CCI (I3C DDR) Read/Write Operations, except CCI (I3C SDR) Single/Sequential Read From Current Location because the Slave would generate NACK again due to an SS0 or SD0 error.

In addition to, or instead of, a retry, the Master may read GETSTATUS, or try Escalation Handling as defined in the I3C specification.

6.4 CCI (I^2C) Slave Addresses

For camera modules having only raw Bayer output the 7-bit slave address should be 7'b011011*X*, where *X* = either 1'b0 or 1'b1. For all other camera modules the 7-bit slave address should be 7'b011110*X*.

6.5 CCI (I3C) Slave Addresses

All camera modules shall use their own Dynamic Address as assigned by the I3C Master.

6.6 CCI Multi-Byte Registers

The description in this Section applies to both **CCI (I^2C)** and **CCI (I3C)**.

6.6.1 Overview

Peripherals contain a wide range of different register widths for various control and setup purposes. This Specification supports the following register widths:

- **8-bit:** Generic setup registers
- **16-bit:** Parameters like line-length, frame-length and exposure values
- **32-bit:** High precision setup values
- **64-bit:** For needs of future sensors

In general, the byte-oriented access protocols described in the previous sections provide an efficient means to access multi-byte registers. However, the registers should reside in a byte-oriented address space, and the address of a multi-byte register should be the address of its first byte. Thus, addresses of contiguous multi-byte registers will not be contiguous. For example, a 32-bit register with its first byte at address 0x8000 can be read by means of a sequential read of four bytes, starting at random address 0x8000. If there is an additional 4-byte register with its first byte at 0x8004, then it could then be accessed using a four-byte Sequential Read from the Current Location protocol.

The motivation for a generalized multi-byte protocol (rather than fixing register widths at 16 bits) is flexibility. The protocol described below provides a way of transferring 16-bit, 32-bit, or 64-bit values over a 16-bit INDEX, 8-bit data, two-wire serial link while ensuring that the bytes of data transferred for a multi-byte register value are always consistent (temporally coherent).

Using this protocol, a single CCI Message can contain one, two, or all of the different register widths used within a device.

The MS byte of a multi-byte register shall be located at the lowest address, and the LS byte shall be located at the highest address.

The address of the first byte of a multi-byte register is not necessarily related to register size (i.e., not required to be an integer multiple of register size in bytes). Register address alignment represents an implementation choice between processing-optimized vs. bandwidth-optimized organizations. There are no restrictions on the number or mix of multi-byte registers within the available 64K by 8-bit INDEX space, with the exception of certain rules for the valid locations for the MS bytes and LS bytes of registers.

Partial access to multi-byte registers is not allowed. A multi-byte register shall only be accessed by a single sequential Message. When a multi-byte register is accessed, its bytes shall be accessed in ascending address order (i.e. first byte is accessed first, second byte is accessed second, etc.).

When a multi-byte register is accessed, the following re-timing rules shall be followed:

- For a Write operation, the updating of the register shall be deferred to a time when the last bit of the last byte has been received.
- For a Read operation, the value read shall reflect the status of all bytes at the time that the first bit of the first byte was read.

Section 6.6.3 describes example re-timing behavior for multi-byte register accesses.

Figure 25 and ***Figure 26*** illustrate that without re-timing, data could be corrupted.

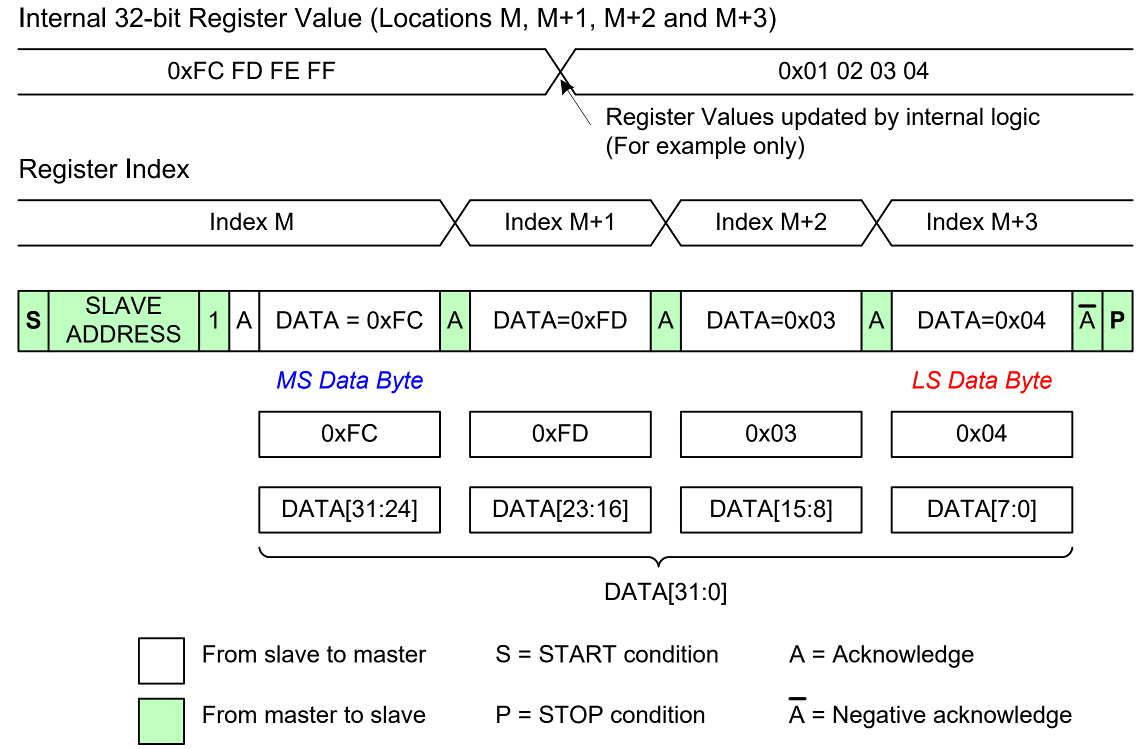


Figure 25 Corruption of 32-bit Register During Read Message

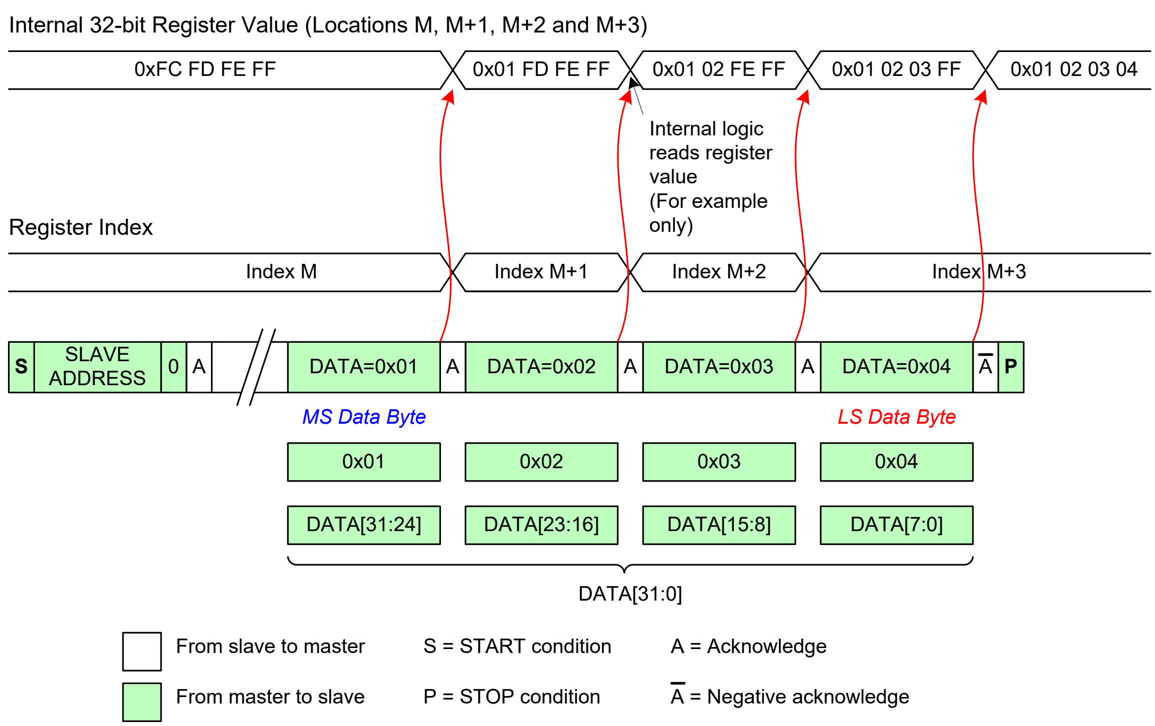


Figure 26 Corruption of 32-bit Register During Write Message

6.6.2 Transmission Byte Order for Multi-Byte Register Values

Figure 27, ***Figure 28***, and ***Figure 29*** illustrate the requirement that the first byte of a CCI Message shall always be the MS byte of a multi-byte register, and the last byte of the CCI Message shall always be the LS byte of the multi-byte register.

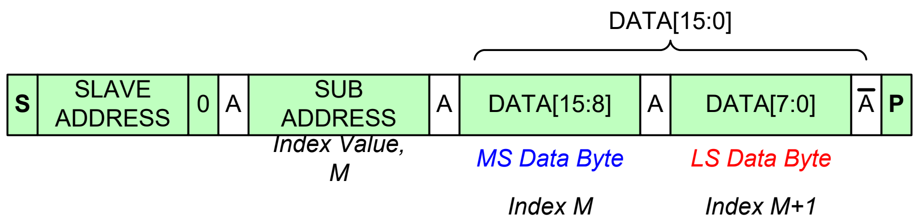


Figure 27 Example 16-bit Register Write

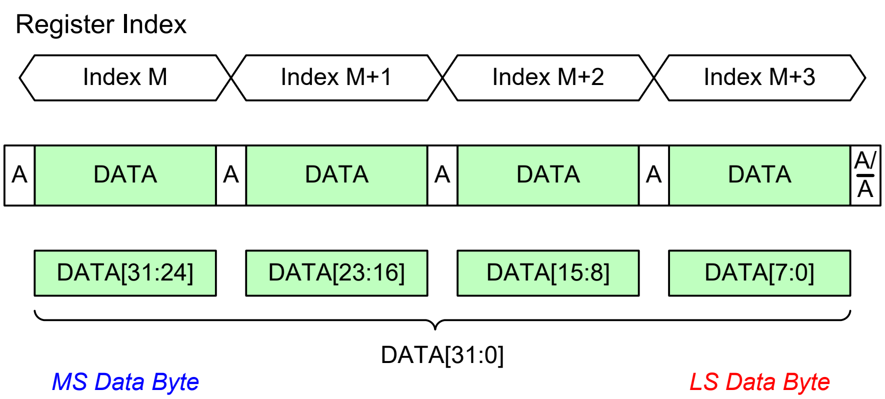


Figure 28 Example 32-bit Register Write (Address Not Shown)

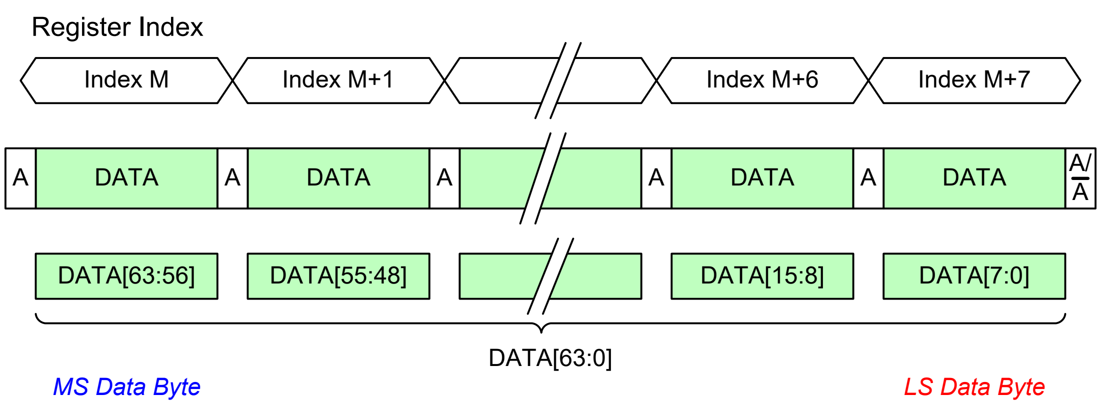


Figure 29 Example 64-bit Register Write (Address Not Shown)

6.6.3 Multi-Byte Register Protocol (Informative)

Each device may have both single-byte registers and multi-byte registers. Internally a device must understand what addresses correspond to the different register widths.

6.6.3.1 Reading Multi-Byte Registers

To ensure that the value read from a multi-byte register is consistent (i.e., that all of the transmitted bytes are temporally coherent), the device can internally transfer the register contents into a temporary buffer at the time when the register's MS byte is read. The contents of the temporary buffer can then be sent out as a sequence of bytes on the SDA line. ***Figure 30*** and ***Figure 31*** illustrate multi-byte register read operations.

The temporary buffer is always updated, except in the case of a read operation that is incremental within the same multi-byte register.

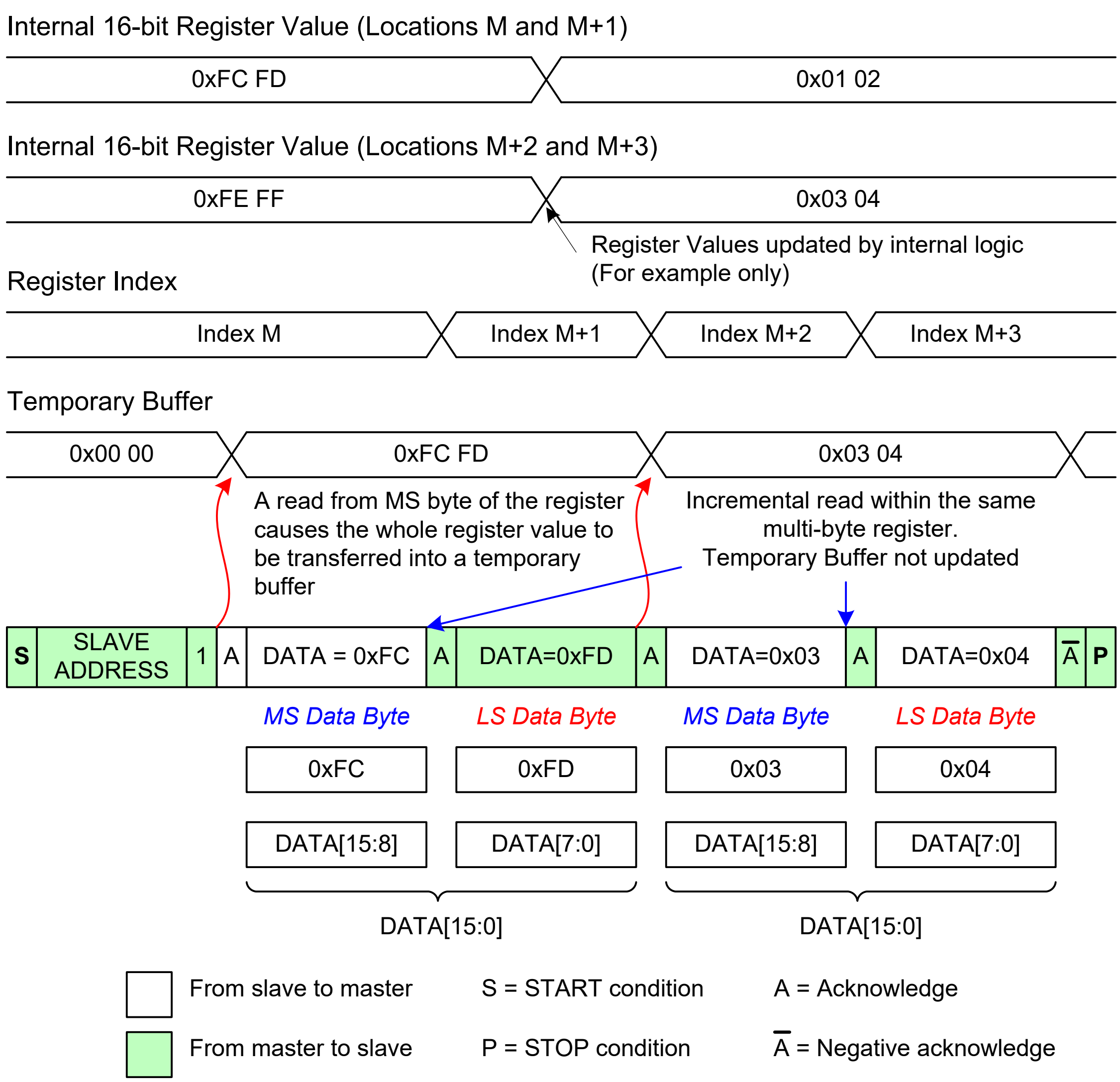


Figure 30 Example 16-bit Register Read

In this definition no distinction is made between a register being accessed incrementally via multiple separate single-byte read Messages with no intervening data writes, vs. a register being accessed via a single multi-location read Message. This protocol purely relates to the behavior of the INDEX value.

Examples of when the temporary buffer is updated include:

- When the MS byte of a register is accessed
- When the INDEX has crossed a multi-byte register boundary
- Successive single-byte reads from the same INDEX location
- When the INDEX value for the byte about to be read is ≤ the previous INDEX

Note that the values read back are only guaranteed to be consistent if the contents (bytes) of the multi-byte register are accessed in an incremental manner.

The contents of the temporary buffer are reset to zero by START and STOP conditions.

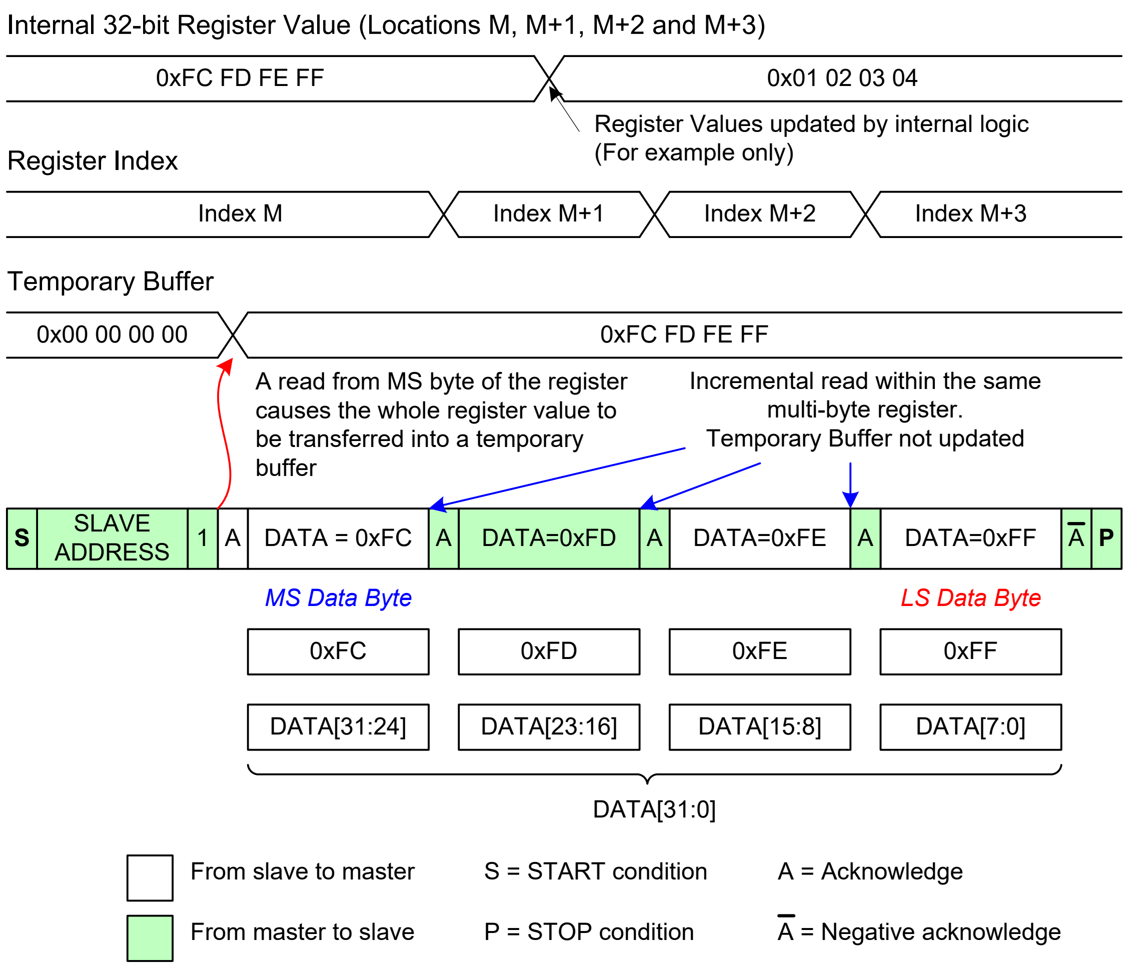


Figure 31 Example 32-bit Register Read

6.6.3.2 Writing Multi-Byte Registers

To ensure that the value written is consistent, the bytes of data from a multi-byte register are written into a temporary buffer. Only after the LS byte of the register is written is the full multi-byte value transferred into the internal register location.

Figure 32 and ***Figure 33*** illustrate multi-byte register write operations.

CCI Messages that only write to the LS or MS byte of a multi-byte register are not allowed. Single byte writes to a multi-byte register addresses may cause undesirable behavior in the device.

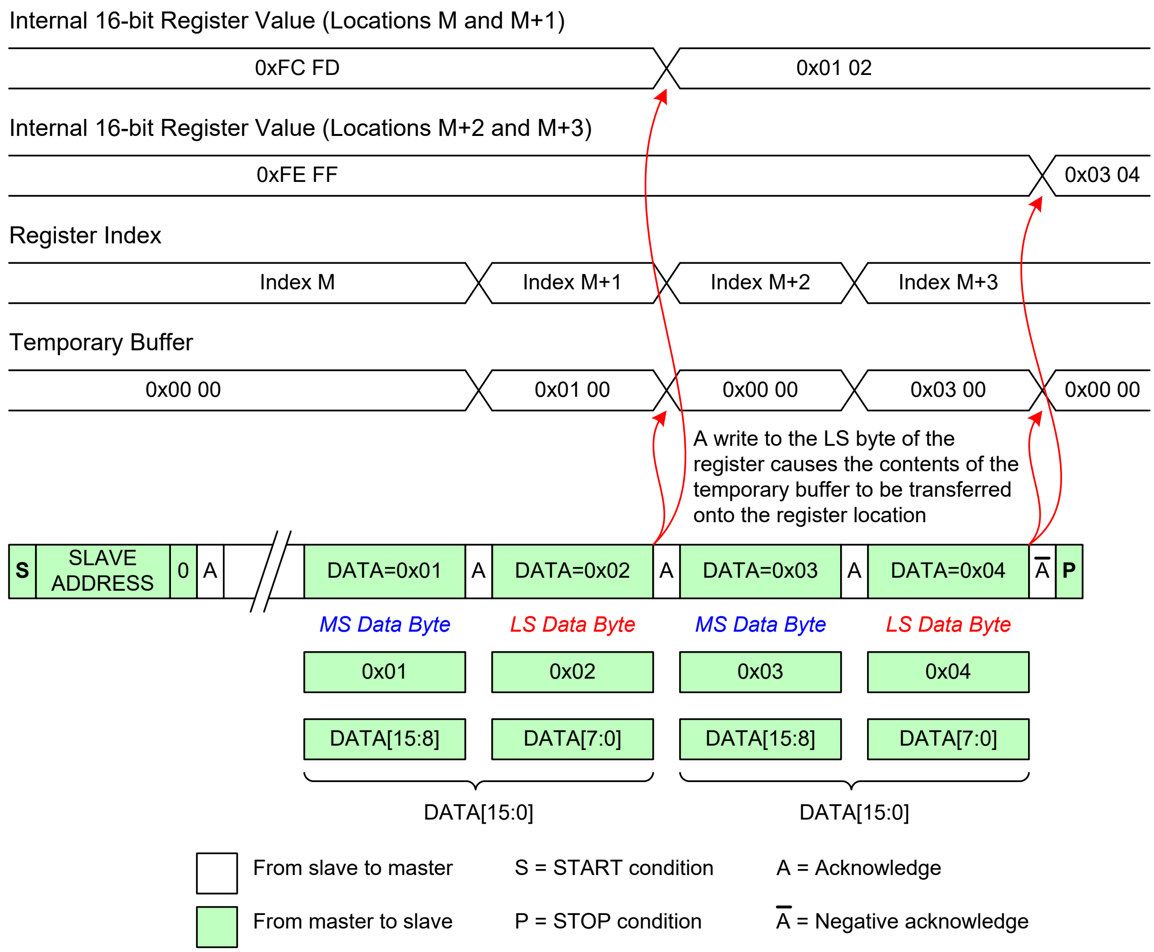
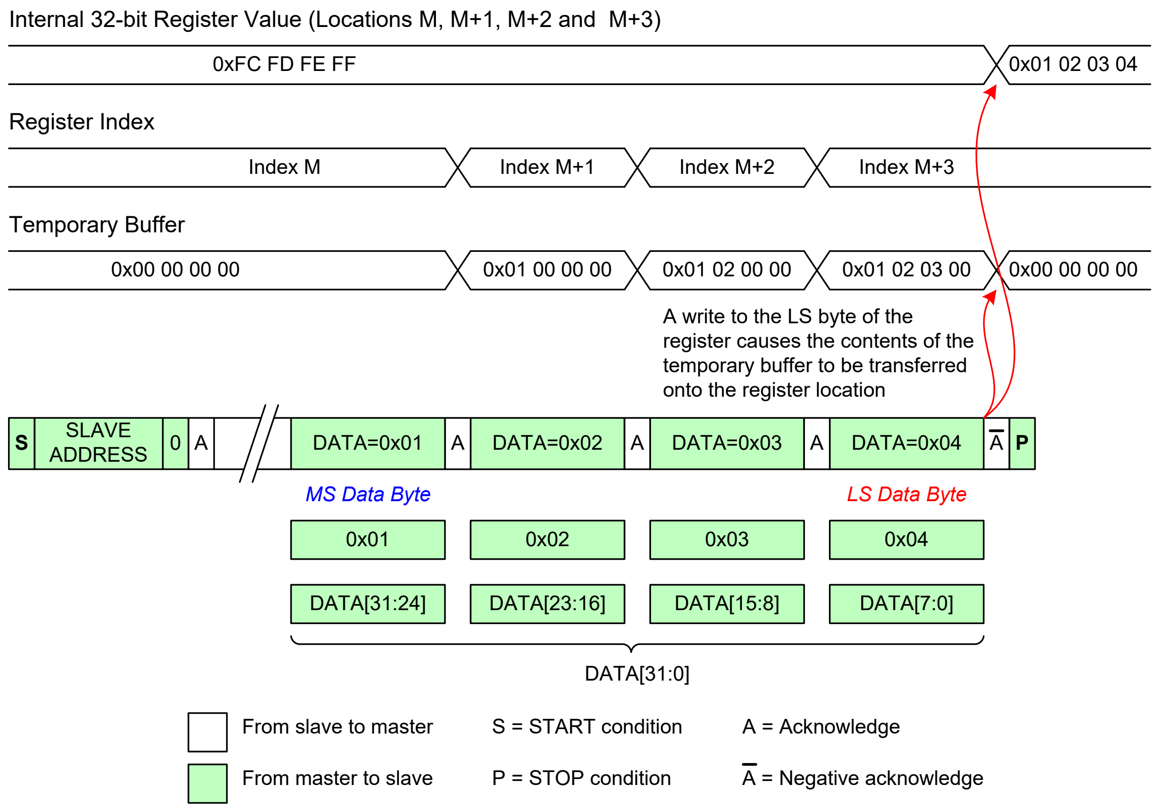


Figure 32 Example 16-bit Register Write



695

Figure 33 Example 32-bit Register Write

6.7 CCI I/O Electrical and Timing Specifications

696 The CCI I/O stages electrical specifications (***Table 8***) and timing specifications (***Table 9***) conform to I²C
697 Fast-mode and Fast-mode Plus devices. Information presented in ***Table 8*** is from ***[NXP01]***.

698 The CCI timings specified in ***Table 9*** are illustrated in ***Figure 34***.

699 **Table 8 CCI I/O Electrical Specifications**

Parameter	Symbol	Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage	V_{IL}	-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	V
HIGH level input voltage	V_{IH}	0.7V_{DD}	Note 1	0.7V_{DD}	Note 1	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05V_{DD}	-	0.05V_{DD}	-	V
LOW level output voltage (open drain) at 2mA sink current V_{DD} > 2V V_{DD} < 2V	 V_{OL1} V_{OL3}	 0 0	 0.4 0.2V_{DD}	 0 0	 0.4 0.2V_{DD}	V
Output fall time from V_{IHmin} to V_{ILmax} with bus capacitance from 10 pF to 400 pF	t_{OF}	20 x (V_{DD} / 5.5 V)	250	20 x (V_{DD} / 5.5 V)	120	ns
Pulse width of spikes which shall be suppressed by the input filter	t_{SP}	0	50	0	50	ns
Input current each I/O pin with an input voltage between 0.1 V_{DD} and 0.9 V_{DD}	I_I	-10 Note 2	10 Note 2	-10 Note 2	10 Note 2	µA
Input/Output capacitance (SDA)	$C_{I/O}$	-	10	-	10	pF
Input capacitance (SCL)	CI	-	10	-	10	pF

Note:

1. *Maximum VIH = V_{DDmax} + 0.5V*
2. *I/O pins of Fast-mode and Fast-mode Plus devices shall not obstruct the SDA and SCL line if V_{DD} is switched off*

Table 9 CCI I/O Timing Specifications

Parameter	Symbol	Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	0.26	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	0.5	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	0.26	-	µs
Setup time for a repeated START condition	$t_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$t_{HD;DAT}$	0 Note 2	- Note 3	0	-	µs
Data set-up time	$t_{SU;DAT}$	100 Note 4	-	50	-	ns
Rise time of both SDA and SCL signals	t_R	20	300	-	120	ns
Fall time of both SDA and SCL signals	t_F	20 x (V_{DD} / 5.5 V)	300	20 x (V_{DD} / 5.5 V)	120	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	0.5	-	µs
Capacitive load for each bus line	C_B	-	400	-	550	pF
Data valid time Note 5	$t_{VD;DAT}$	-	0.9 Note 3	-	0.45 Note 3	µs
Data valid acknowledge time Note 6	$t_{VD;ACK}$	-	0.9 Note 3	-	0.45 Note 3	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1 x V_{DD}	-	0.1 x V_{DD}	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 x V_{DD}	-	0.2 x V_{DD}	-	V

Note:

1. *All values referred to $V_{IHmin} = 0.7V_{DD}$ and $V_{ILmax} = 0.3V_{DD}$*
2. *A device shall internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL*
3. *The maximum $t_{HD;DAT}$ could be 0.9 µs and 0.45 µs for Fast-mode and Fast-mode Plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, then the data must be valid by the set-up time before it releases the clock.*
4. *A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU:DAT} \geq 250$ ns shall be then met. This will be automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the low period of SCL signal, it shall output the next data bit to the SDA line $t_{rMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C Bus specification **[NXP01]**) before the SCL line is released.*
5. *$t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, whichever is worse).*
6. *$t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, whichever is worse)*

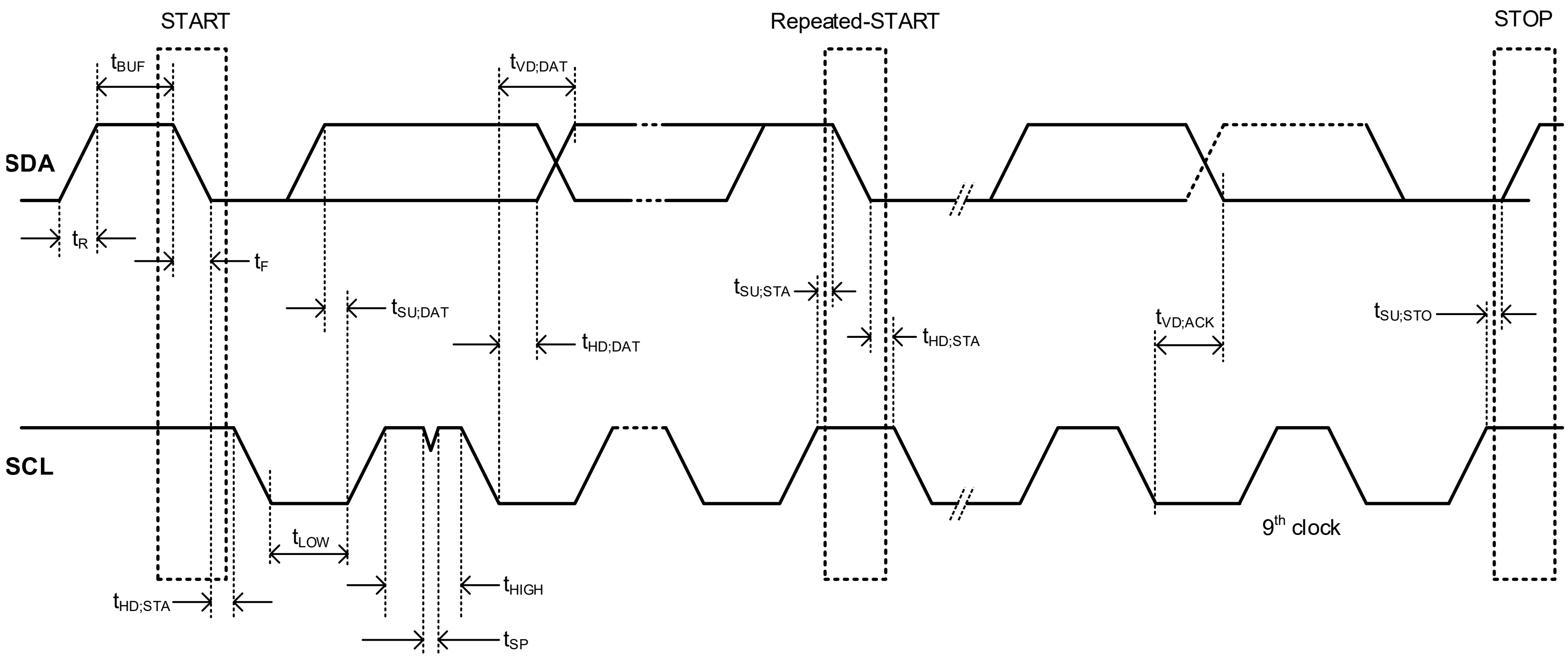


Figure 34 CCI I/O Timing

This page intentionally left blank.

~~This page intentionally left blank.~~

7 Physical Layer

The CSI-2 lane management layer interfaces with the D-PHY and/or C-PHY physical layers described in ***[MIPI01]*** and ***[MIPI02]***, respectively. A device shall implement either the C-PHY ~~1.~~2.0 or the D-PHY 2.~~1~~5 physical layer and may implement both. A practical constraint is that the PHY technologies used at both ends of the Link need to match: a D-PHY transmitter cannot operate with a C-PHY receiver, or vice versa.

7.1 D-PHY Physical Layer Option

The D-PHY physical layer for a CSI-2 implementation is typically composed of a number of unidirectional data Lanes and one clock Lane. All CSI-2 transmitters and receivers implementing the D-PHY physical layer shall support continuous clock behavior on the Clock Lane, and optionally may support non-continuous clock behavior.

For continuous clock behavior the Clock Lane remains in high-speed mode, generating active clock signals between the ~~transmission~~transmissions of data packets.

For non-continuous clock behavior the Clock Lane enters the LP-11 state between the ~~transmission~~transmissions of data packets.

The minimum D-PHY physical layer requirement for a CSI-2 transmitter is

- Data Lane Module: Unidirectional master, HS-TX, LP-TX and a CIL-MFEN function
- Clock Lane Module: Unidirectional master, HS-TX, LP-TX and a CIL-MCNN function

The minimum D-PHY physical layer requirement for a CSI-2 receiver is

- Data Lane Module: Unidirectional slave, HS-RX, LP-RX, and a CIL-SFEN function
- Clock Lane Module: Unidirectional slave, HS-RX, LP-RX, and a CIL-SCNN function

All CSI-2 implementations supporting the D-PHY physical layer option shall support forward escape ULPS on all D-PHY Data Lanes.

To enable higher data rates and higher number of lanes the physical layer described in ***[MIPI01]*** includes an independent deskew mechanism in the Receive Data Lane Module. To facilitate deskew calibration at the receiver the transmitter Data Lane Module provides a deskew sequence pattern.

Since deskew calibration is only valid at a given transmit frequency:

For initial calibration sequence the Transmitter shall be programmed with the desired frequency for calibration. It will then transmit the deskew calibration pattern and the Receiver will autonomously detect this pattern and tune the deskew function to achieve optimum performance.

For any transmitter frequency changes the deskew calibration shall be rerun.

Some transmitters and/or receivers may require deskew calibration to be rerun periodically and it is suggested that it can be optimally done within vertical or frame blanking periods.

For low transmit frequencies or when a receiver described in ***[MIPI01]*** is paired with a previous version transmitter not supporting the deskew calibration pattern the receiver may be instructed to bypass the deskew mechanism.

The D-PHY v2.~~1~~5 physical layer ~~***[MIPI05]***~~***[MIPI01]*** provides both Alternate Low Power ~~State (ALPS) using~~(ALP) Mode and Low Voltage Low Power (LVLP) signaling, either of which may optionally replace the legacy Low Power State (LPS). Use of ALP Mode or LVLP signaling can help alleviate current leakage and electrical overstress issues with image sensors and applications processors. ALP Mode can also help achieve longer reach for CSI-2 imaging interface channels, and is also central to the CSI-2 Unified Serial Link (USL) feature described in ***Section 9.12***. USL D-PHY support requirements are described in ***Section 7.3.1***.

~~7.1.1 D-PHY v2.1 Compatibility with D-PHY v2.0 (Informative)~~

~~A D-PHY v2.0 ***[MIPI05]*** or earlier physical layer and a D-PHY v2.1 physical layer are fully interoperable.~~

~~For bit rates above 2.5 Gbps per Lane, a D-PHY v2.0 ***[MIPI05]*** or earlier physical layer and a D-PHY v2.1 physical layer are fully interoperable, provided certain new D-PHY v2.1 features are disabled as permitted by the D-PHY v2.1 specification. Such features include the Alternate Calibration Sequence, Preamble Sequence, and Extended Sync pattern as described in ***Section 6.13*** and ***Section 6.14*** of ***[MIPI01]***.~~

~~These features allow system interfaces to more robustly compensate for variations such as temperature and voltage when operating at bit rates above 2.5 Gbps but are not supported by D-PHY v2.0.~~

7.2 C-PHY Physical Layer Option

The C-PHY physical layer for a CSI-2 implementation is typically composed of one or more unidirectional Lanes.

The minimum C-PHY physical layer requirement for a CSI-2 transmitter Lane module is:

- Unidirectional master, HS-TX, LP-TX and a CIL-MFEN function
- Support for Sync Word insertion during data payload transmission

The minimum C-PHY physical layer requirement for a CSI-2 receiver Lane module is:

- Unidirectional slave, HS-RX, LP-RX, and a CIL-SFEN function
- Support for Sync Word detection during data payload reception

All CSI-2 implementations supporting the C-PHY physical layer option shall support forward escape ULPS on all C-PHY Lanes.

The C-PHY Physical Layer provides both Alternate Low Power ~~State (ALPS) signaling using~~(ALP) Mode and Low Voltage Low Power (LVLP) signaling~~ or Alternate Low Power (ALP) Embedded Codes,~~, either of which may optionally replace the legacy Low Power State (LPS). Use of ~~ALPS~~ALP Mode or LVLP signaling can help alleviate current leakage and electrical overstress issues with image sensors and applications processors. ~~ALPS using the ALP Embedded Codes~~ALP Mode (which replaces LVLP or legacy LP signaling through the use of high-speed embedded codes) can also help achieve longer reach for CSI-2 imaging interface channels before re-drivers and re-timers become necessary. ALP Mode is also central to the CSI-2 Unified Serial Link (USL) feature described in ***Section 9.12***. USL C-PHY support requirements are described in ***Section 7.3.2***.

7.3 PHY Support for the CSI-2 Unified Serial Link (USL) Feature

The CSI-2 USL feature, as described in ***Section 9.12***, requires the D-PHY and C-PHY physical layers to support bidirectional data communications on Lane 1 plus additional features as described below in ***Section 7.3.1*** and ***Section 7.3.2***, respectively. In case of any conflict between this ***Section 7.3*** and ***Section 7.1*** or ***Section 7.2***, this section takes precedence. The physical layers of all USL implementations shall support PHY LP and/or LVLP Mode signaling and should support ALP Mode signaling.

7.3.1 D-PHY Support Requirements for USL Feature

The D-PHY physical layer for a CSI-2 USL implementation is composed of one bidirectional data Lane (i.e., data Lane 1), zero or more unidirectional data Lanes, and one clock Lane. All CSI-2 transmitters and receivers implementing the D-PHY physical layer for the USL feature shall support continuous clock behavior on the clock Lane, and optionally may support non-continuous clock behavior.

For continuous clock behavior, the clock Lane remains in high-speed mode, generating active clock signals between data packet transmissions.

For non-continuous clock behavior, the clock Lane may enter the Stop state between data packet transmissions as determined by the image sensor and controlled by the host processor.

The minimum D-PHY LP/LVLP Mode physical layer requirement for a USL image sensor is:

- **Clock Lane Module:** Unidirectional master, HS-TX, LP-TX, and CIL-MCNN function
- **Data Lane 1 Module:** Bidirectional master, HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MFAA function; Escape Mode LPDT shall be supported in both the forward and reverse direction
- **Data Lane n Module** (for n > 1)**:** Unidirectional master, HS-TX, LP-TX, and CIL-MFEN function

The minimum D-PHY LP/LVLP Mode physical layer requirement for a USL host is:

- **Clock Lane Module:** Unidirectional slave, HS-RX, LP-RX, and CIL-SCNN function
- **Data Lane 1 Module:** Bidirectional slave, HS-RX, LP-TX, LP-RX, LP-CD, and CIL-SFAA function; Escape Mode LPDT shall be supported in both the forward and reverse direction
- **Data Lane n Module** (for n > 1)**:** Unidirectional slave, HS-RX, LP-RX, and CIL-SFEN function

For USL implemented using D-PHY LP/LVLP Mode, forward direction Escape Mode LPDT transmissions shall use data Lane 1 only, and all reverse direction transmissions shall only use data Lane 1 and LPDT. The USL host shall be capable of receiving both LPDT and High Speed (HS) transmissions. Note that transmission bandwidth is substantially reduced when transmitting using LPDT.

The minimum D-PHY ALP Mode physical layer requirement for a USL image sensor is:

- **Clock Lane Module:** Unidirectional master, HS-TX and CIL-MCNN function
- **Data Lane 1 Module:** Bidirectional master, HS-TX, HS-RX, ALP-ED, and CIL-MREN function (CIL-MREE with ALP-ULPS in both forward and reverse direction is recommended)
- **Data Lane n Module** (for n > 1)**:** Unidirectional master, HS-TX and CIL-MFEN function

The minimum D-PHY ALP Mode physical layer requirement for a USL host is:

- **Clock Lane Module:** Unidirectional slave, HS-RX, ALP-ED, and CIL-SCNN function
- **Data Lane 1 Module:** Bidirectional slave, HS-TX, HS-RX, ALP-ED, and CIL-SREN function (CIL-SREE with ALP-ULPS in both forward and reverse direction is recommended)
- **Data Lane n Module** (for n > 1)**:** Unidirectional slave, HS-RX, ALP-ED, and CIL-SFEN function

Note that D-PHY ALP Mode does not define a contention detection function for bidirectional Lane modules.

All USL implementations supporting the D-PHY physical layer option shall support forward direction ULPS on all data Lanes. For data Lane 1, support for both reverse direction ULPS and the reverse direction ALP-wake pulse transmission is recommended; see ***Section 9.12.5.6*** and ***Section 9.12.5.8*** for additional guidance.

7.3.2 C-PHY Support Requirements for USL Feature

The C-PHY physical layer for a CSI-2 USL implementation is composed of one bidirectional Lane (i.e., Lane 1) and zero or more unidirectional Lanes.

The minimum C-PHY LP/LVLP Mode physical layer requirement for a USL image sensor is:

- **Lane 1 Module:** Bidirectional master, HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MFAA function; Escape Mode LPDT shall be supported in both the forward and reverse direction
- **Lane n Module** (for n > 1)**:** Unidirectional master, HS-TX, LP-TX, and CIL-MFEN function

The minimum C-PHY LP/LVLP Mode physical layer requirement for a USL host is:

- **Lane 1 Module:** Bidirectional slave, HS-RX, LP-TX, LP-RX, LP-CD, and CIL-SFAA function; Escape Mode LPDT shall be supported in both the forward and reverse direction
- **Lane n Module** (for n > 1)**:** Unidirectional slave, HS-RX, LP-RX, and CIL-SFEN function

For USL implemented using C-PHY LP/LVLP Mode, forward direction Escape Mode LPDT transmissions shall use Lane 1 only, and all reverse direction transmissions shall only use Lane 1 and LPDT. The USL host shall be capable of receiving both LPDT and High Speed (HS) transmissions. Note that transmission bandwidth is substantially reduced when transmitting using LPDT.

The minimum C-PHY ALP Mode physical layer requirement for a USL image sensor is:

- **Lane 1 Module:** Bidirectional master, HS-TX, HS-RX, and CIL-MREN function (CIL-MREE with ALP-ULPS in both forward and reverse direction is recommended)
- **Lane n Module** (for n > 1)**:** Unidirectional master, HS-TX and CIL-MFEN function

The minimum C-PHY ALP Mode physical layer requirement for a USL host is:

- **Lane 1 Module:** Bidirectional slave, HS-TX, HS-RX, and CIL-SREN function (CIL-SREE with ALP-ULPS in both forward and reverse direction is recommended)
- **Lane n Module** (for n > 1)**:** Unidirectional slave, HS-RX and CIL-SFEN function

Note that C-PHY ALP Mode does not define a contention detection function for bidirectional Lane modules.

All CSI-2 USL implementations supporting the C-PHY physical layer option shall support forward direction ULPS on all Lanes. For Lane 1, additional C-PHY ALP Mode support for reverse direction ULPS is recommended; see ***Section 9.12.5.8*** for additional guidance.

8 Multi-Lane Distribution and Merging

CSI-2 is a Lane-scalable specification. Applications requiring more bandwidth than that provided by one data Lane, or those trying to avoid high clock rates, can expand the data path to a higher number of Lanes and obtain approximately linear increases in peak bus bandwidth. The mapping between data at higher layers and the serial bit or symbol stream is explicitly defined to ensure compatibility between host processors and peripherals that make use of multiple data Lanes.

Conceptually, between the PHY and higher functional layers is a layer that handles multi-Lane configurations. As shown in ***Figure 35*** and ***Figure 36*** for the D-PHY and C-PHY physical layer options, respectively, the CSI-2 transmitter incorporates a Lane Distribution Function (LDF) which accepts a sequence of packet bytes from the low level protocol layer and distributes them across N Lanes, where each Lane is an independent unit of physical-layer logic (serializers, etc.) and transmission circuitry. Similarly, as shown in ***Figure 37*** and ***Figure 38*** for the D-PHY and C-PHY physical layer options, respectively,the CSI-2 receiver incorporates a Lane Merging Function (LMF) which collects incoming bytes from N Lanes and consolidates (merges) them into complete packets to pass into the packet decomposer in the receiver's low level protocol layer.

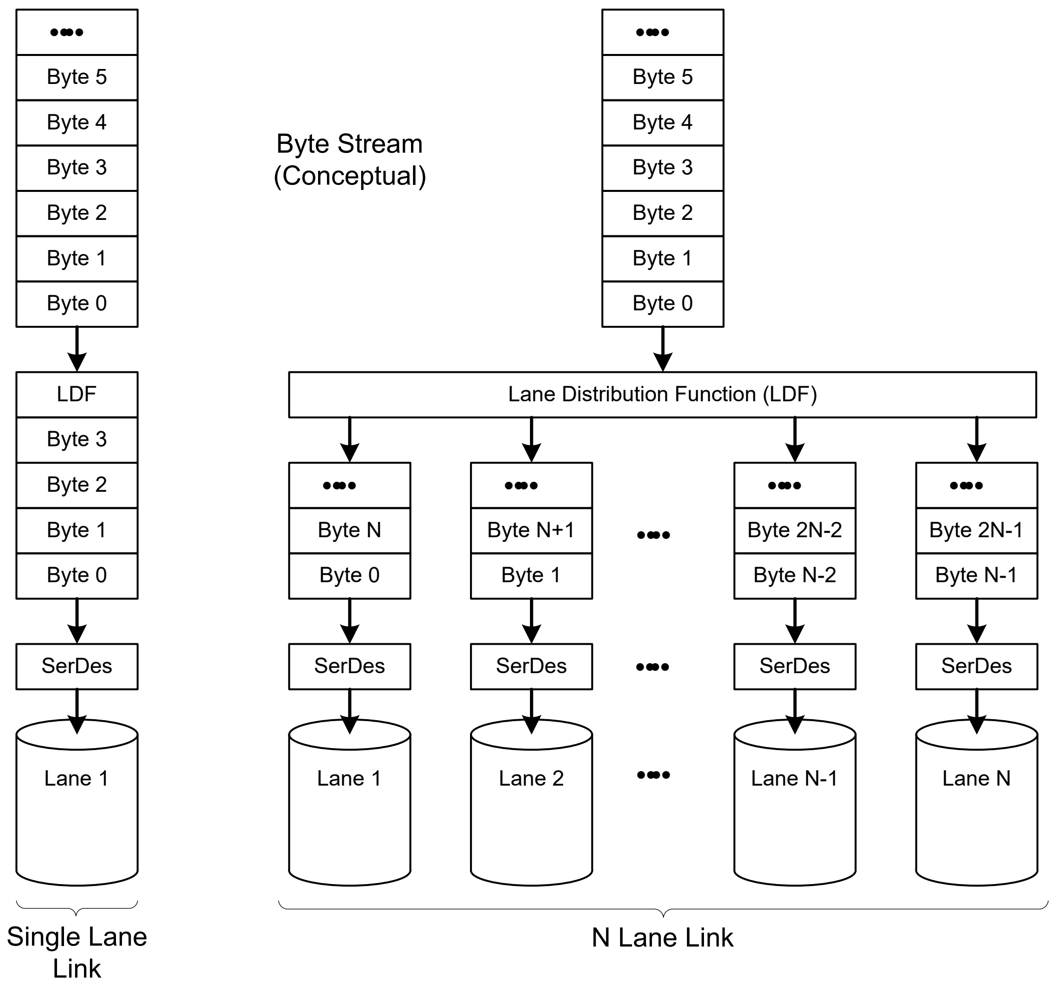
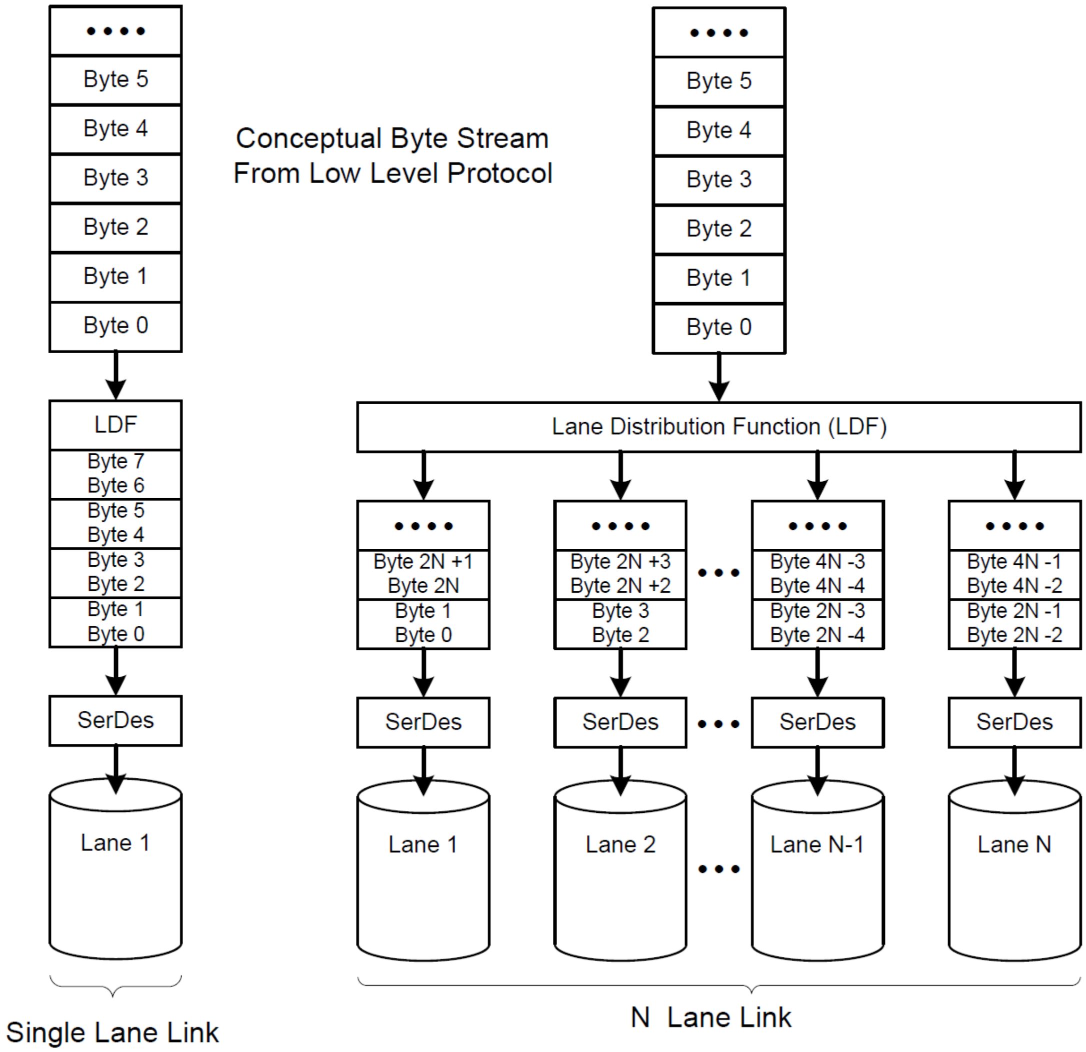


Figure 35 Conceptual Overview of the Lane Distributor Function for D-PHY

852


Conceptual Byte Stream
From Low Level Protocol
••••
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
LDF
Byte 7
Byte 6
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
SerDes
Lane 1
Single Lane Link
Lane Distribution Function (LDF)
Byte 2N +1
Byte 2N
Byte 1
Byte 0
Byte 2N +3
Byte 2N +2
Byte 3
Byte 2
Byte 4N -3
Byte 4N -4
Byte 2N -3
Byte 2N -4
Byte 4N -1
Byte 4N -2
Byte 2N -1
Byte 2N -2
SerDes
Lane 1
Lane 2
Lane N-1
Lane N
N Lane Link

853

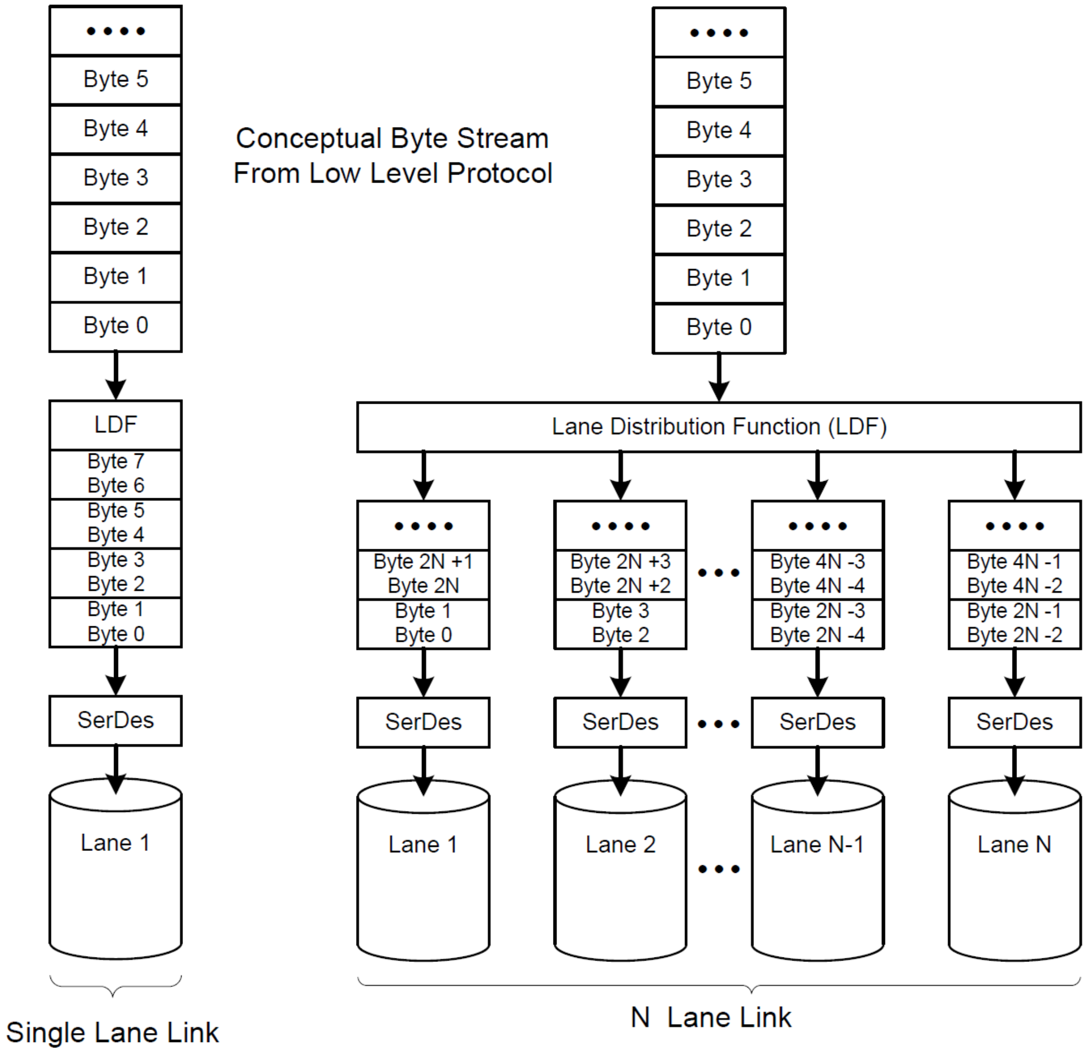
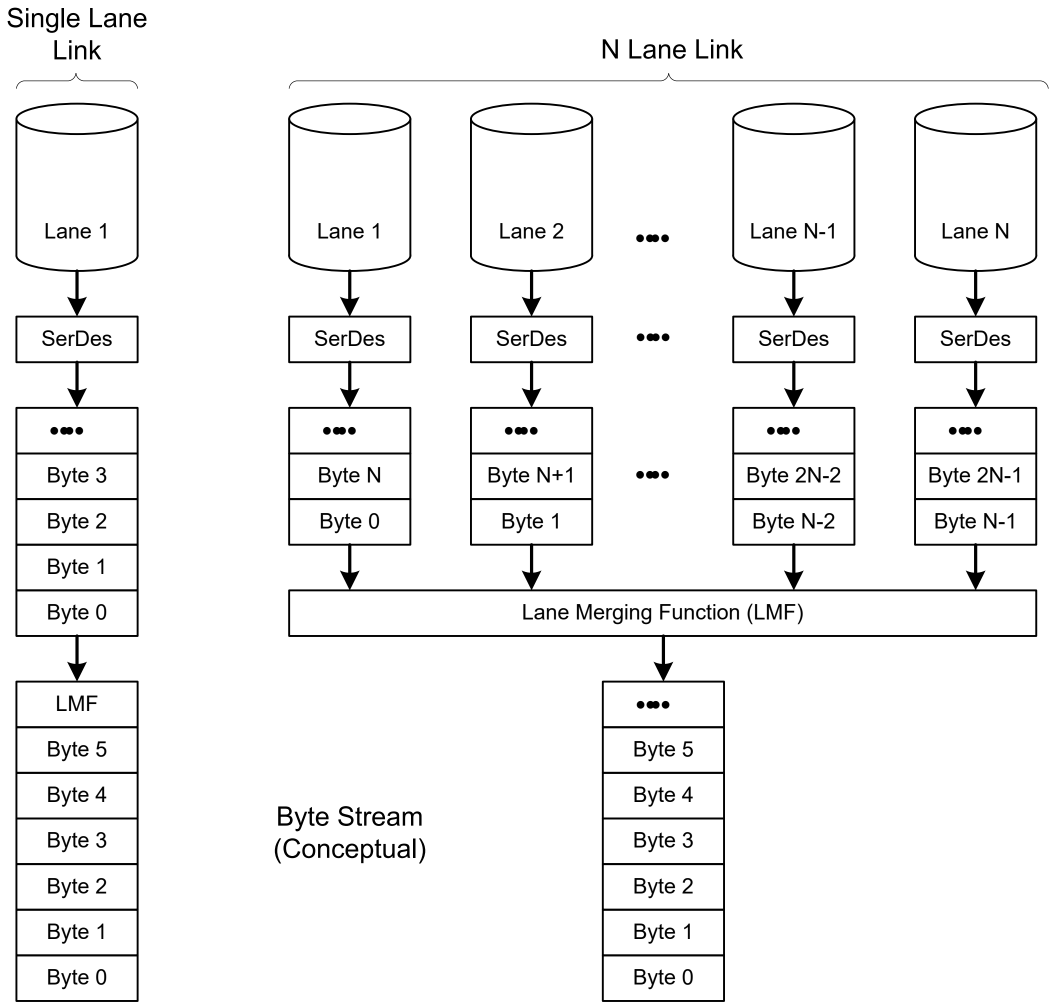
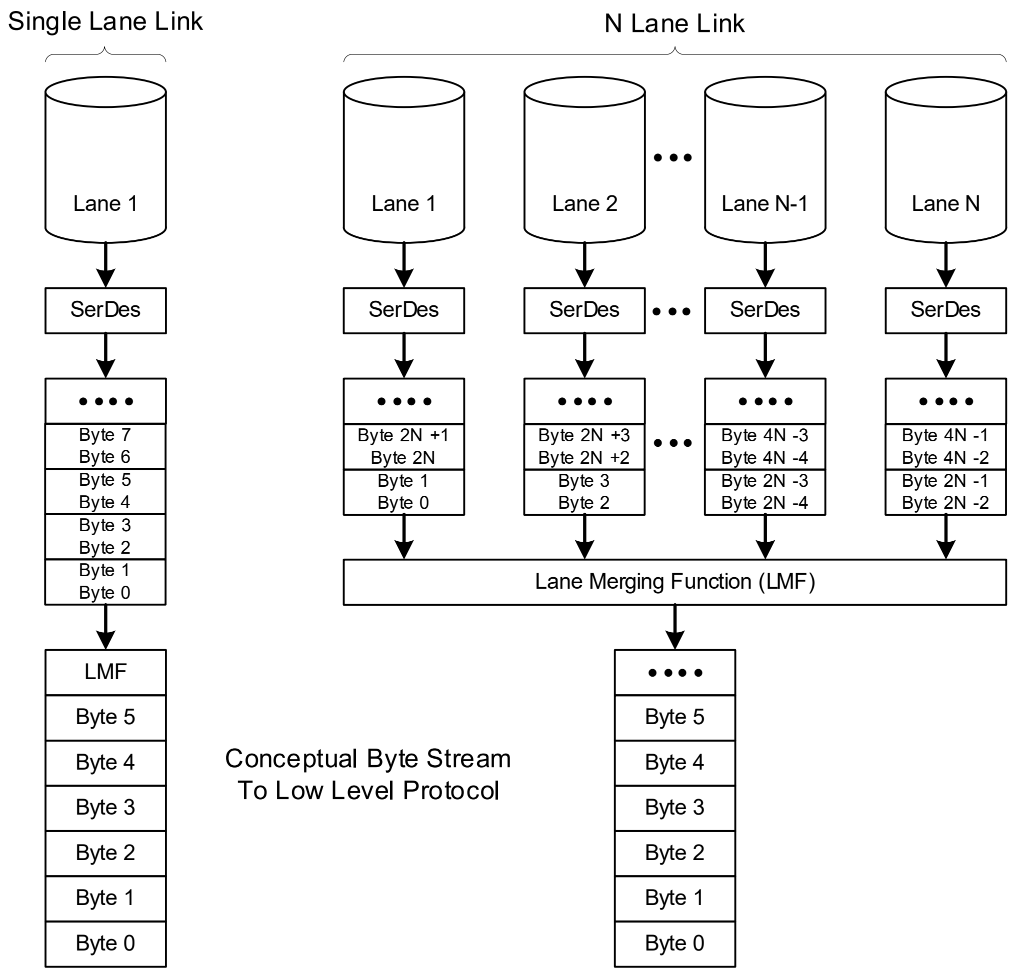


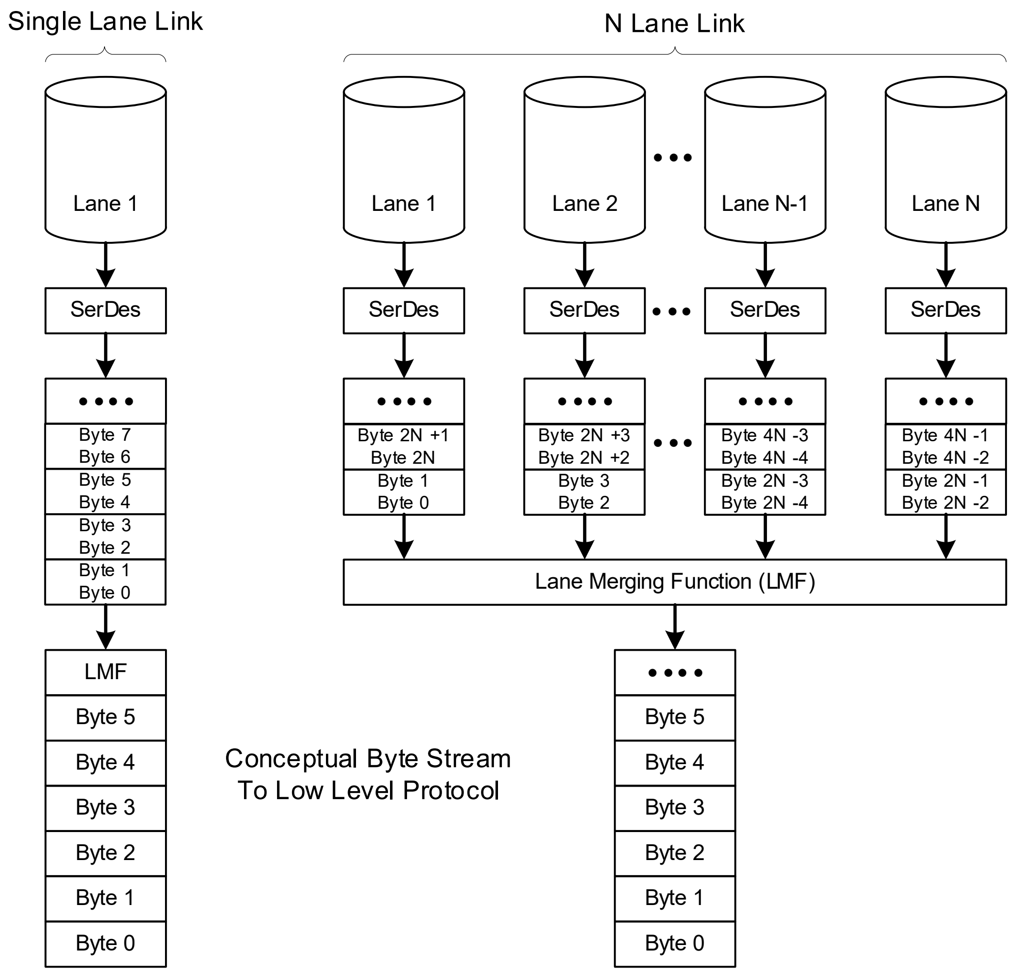
Figure 36 Conceptual Overview of the Lane Distributor Function for C-PHY



854

Figure 37 Conceptual Overview of the Lane Merging Function for D-PHY


Single Lane Link
N Lane Link
Lane 1
Lane 1
Lane 2
Lane N-1
Lane N
SerDes
Byte 7
Byte 6
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Byte 2N +1
Byte 2N
Byte 1
Byte 0
Byte 2N +3
Byte 2N +2
Byte 3
Byte 2
Byte 4N -3
Byte 4N -4
Byte 2N -3
Byte 2N -4
Byte 4N -1
Byte 4N -2
Byte 2N -1
Byte 2N -2
Lane Merging Function (LMF)
LMF
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Conceptual Byte Stream
To Low Level Protocol


Single Lane Link
N Lane Link
Lane 1
Lane 1
Lane 2
Lane N-1
Lane N
SerDes
SerDes
SerDes
SerDes
SerDes
Byte 7
Byte 6
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Byte 2N +1
Byte 2N
Byte 1
Byte 0
Byte 2N +3
Byte 2N +2
Byte 3
Byte 2
Byte 4N -3
Byte 4N -4
Byte 2N -3
Byte 2N -4
Byte 4N -1
Byte 4N -2
Byte 2N -1
Byte 2N -2
Lane Merging Function (LMF)
LMF
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Conceptual Byte Stream
To Low Level Protocol
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0

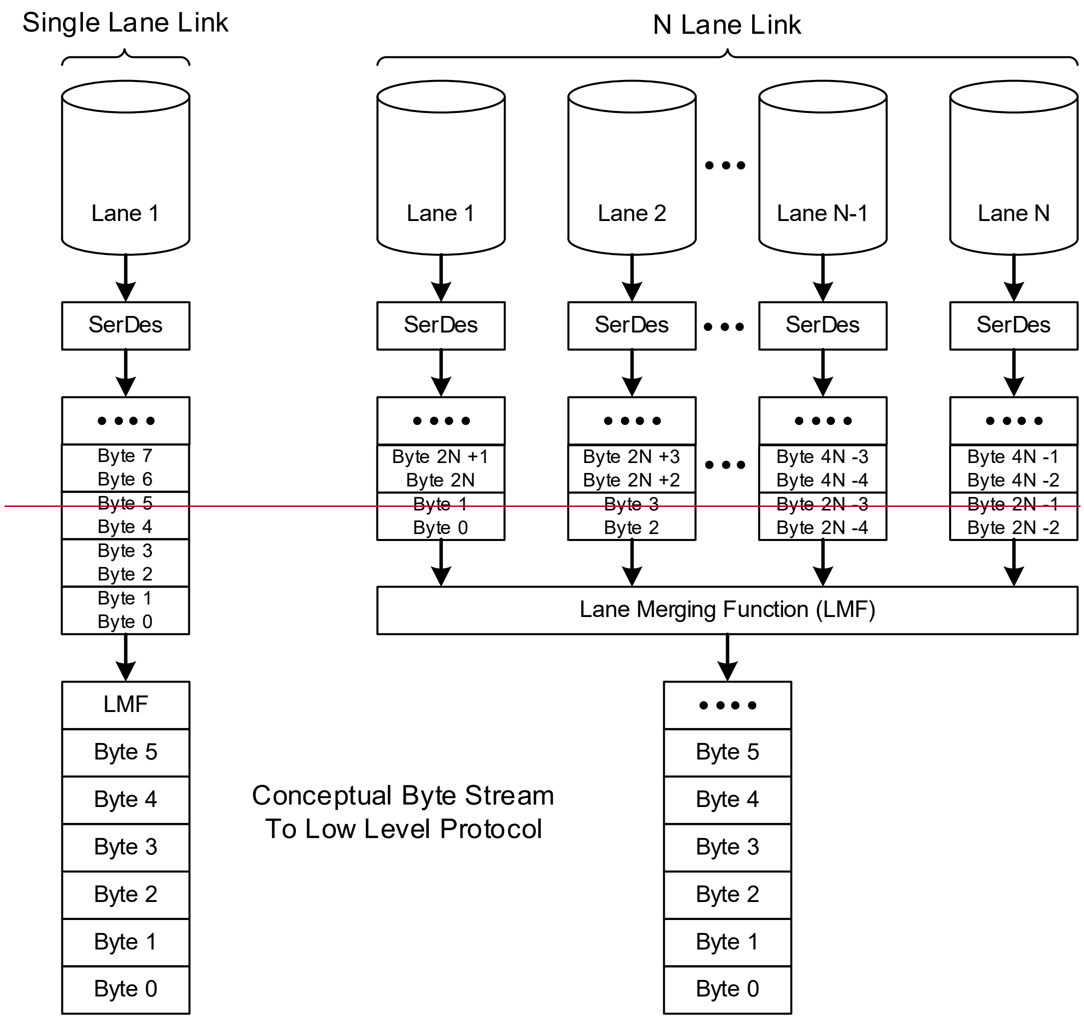


Figure 38 Conceptual Overview of the Lane Merging Function for C-PHY

The Lane distributor takes a transmission of arbitrary byte length, buffers up N*b bytes (where N = number of Lanes and b = 1 or 2 for the D-PHY or C-PHY physical layer option, respectively), and then sends groups of N*b bytes in parallel across N Lanes with each Lane receiving b bytes. Before sending data, all Lanes perform the SoT sequence in parallel to indicate to their corresponding receiving units that the first byte of a packet is beginning. After SoT, the Lanes send groups of successive bytes from the first packet in parallel, following a round-robin process.

8.1 Lane Distribution for the D-PHY Physical Layer Option

Examples are shown in ***Figure 39***, ***Figure 40***, ***Figure 41***, and ***Figure 42***:

- 2-Lane system (***Figure 39***): byte 0 of the packet goes to Lane 1, byte 1 goes to Lane 2, byte 2 to Lane 1, byte 3 goes to Lane 2, byte 4 goes to Lane 1, and so on.
- 3-Lane system (***Figure 40***): byte 0 of the packet goes to Lane 1, byte 1 goes to Lane 2, byte 2 to Lane 3, byte 3 goes to Lane 1, byte 4 goes to Lane 2, and so on.
- N-Lane system (***Figure 41***): byte 0 of the packet goes to Lane 1, byte 1 goes to Lane 2, byte N-1 goes to Lane N, byte N goes to Lane 1, byte N+1 goes to Lane 2, and so on.
- N-lane system (***Figure 42***) with N>4 short packet (4 bytes) transmission: byte 0 of the packet goes to Lane 1, byte 1 goes to Lane 2, byte 2 goes to Lane 3, byte 3 goes to Lane 4, and Lanes 5 to N do not receive bytes and stay in LPS state.

At the end of the transmission, there may be "extra" bytes since the total byte count may not be an integer multiple of the number of Lanes, N. One or more Lanes may send their last bytes before the others. The Lane distributor, as it buffers up the final set of less-than-N bytes in parallel for sending to N data Lanes, de-asserts its "valid data" signal into all Lanes for which there is no further data. For systems with more than 4 data Lanes sending a short packet constituted of 4 bytes the Lanes which do not receive a byte for transmission shall stay in LPS state.

Each D-PHY data Lane operates autonomously.

Although multiple Lanes all start simultaneously with parallel "start packet" codes, they may complete the transaction at different times, sending "end packet" codes one cycle (byte) apart.

The N PHYs on the receiving end of the link collect bytes in parallel, and feed them into the Lane-merging layer. This reconstitutes the original sequence of bytes in the transmission, which can then be partitioned into individual packets for the packet decoder layer.

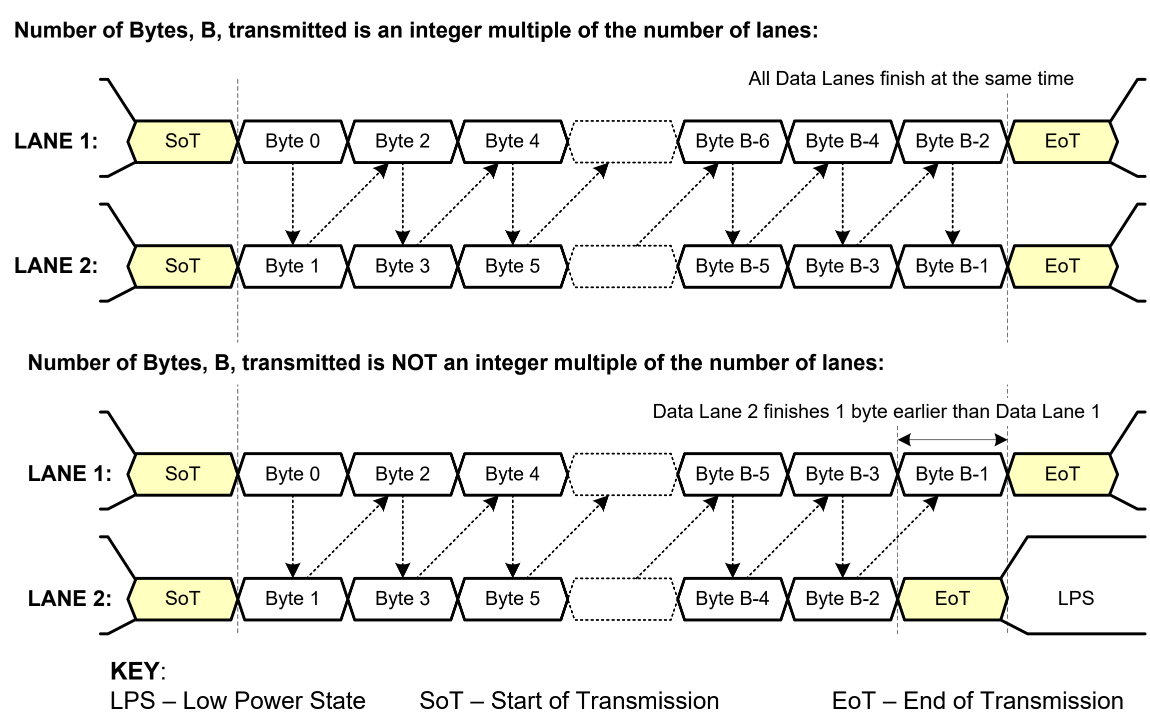


Figure 39 Two Lane Multi-Lane Example for D-PHY

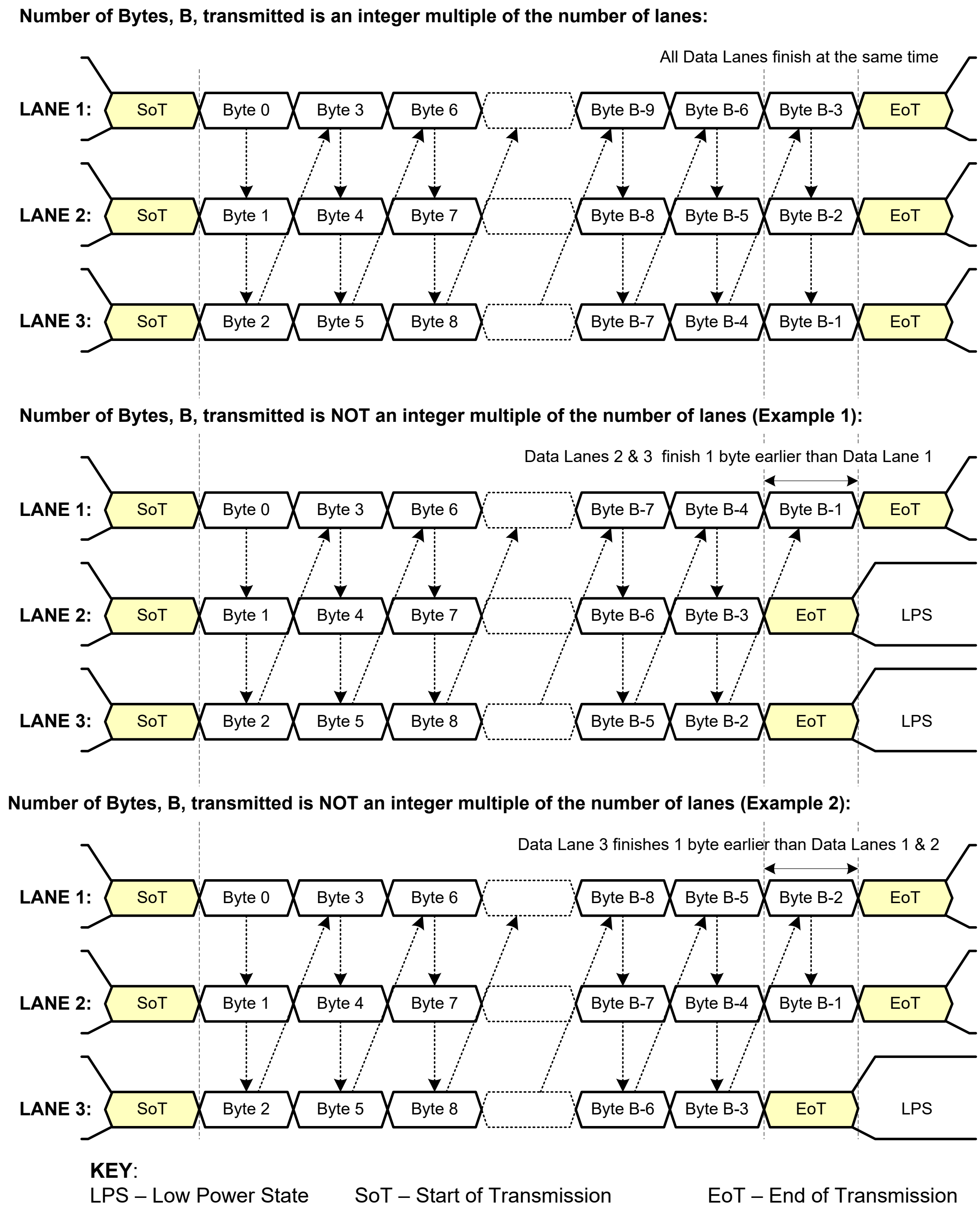
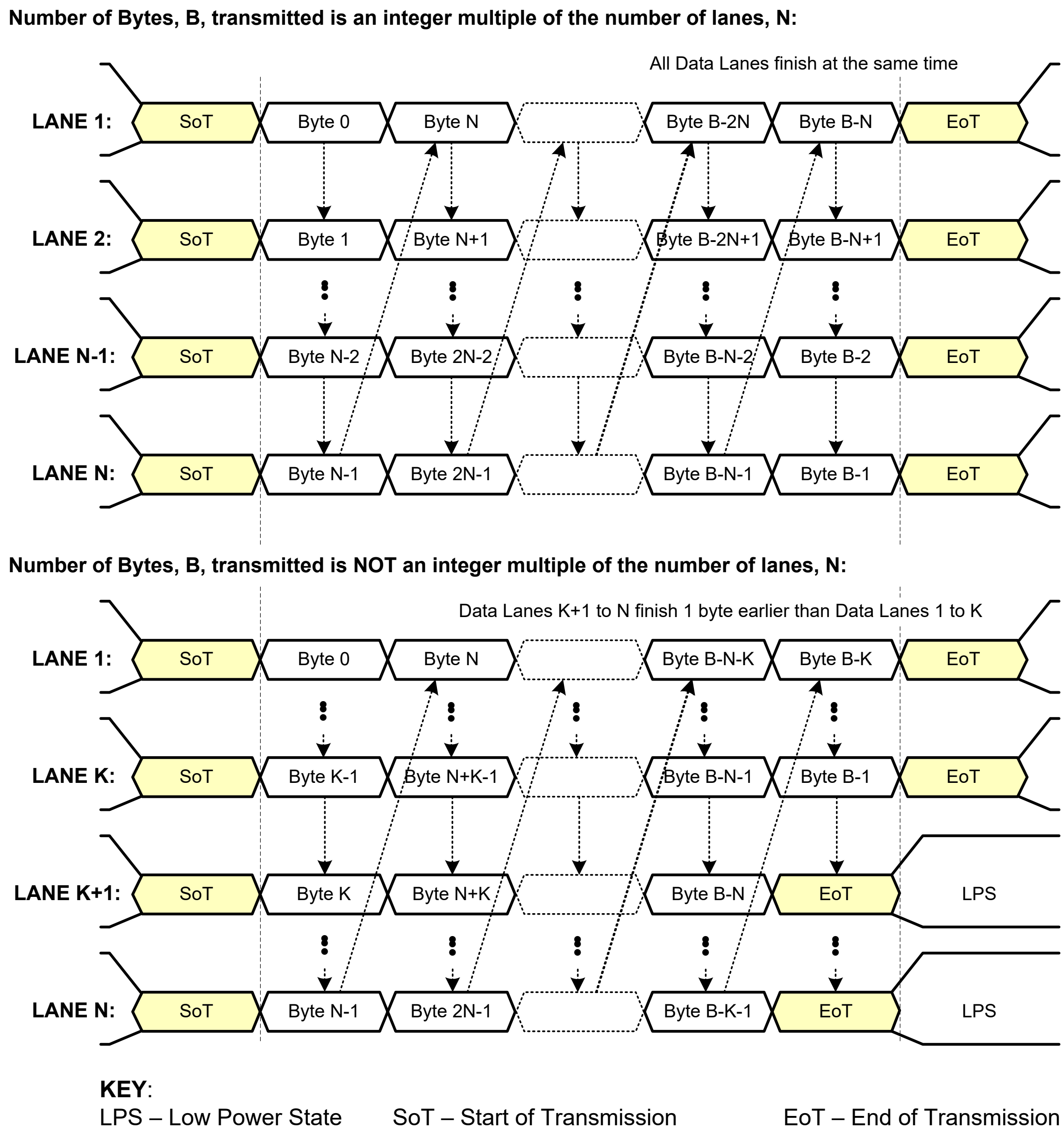


Figure 40 Three Lane Multi-Lane Example for D-PHY



888

Figure 41 N-Lane Multi-Lane Example for D-PHY

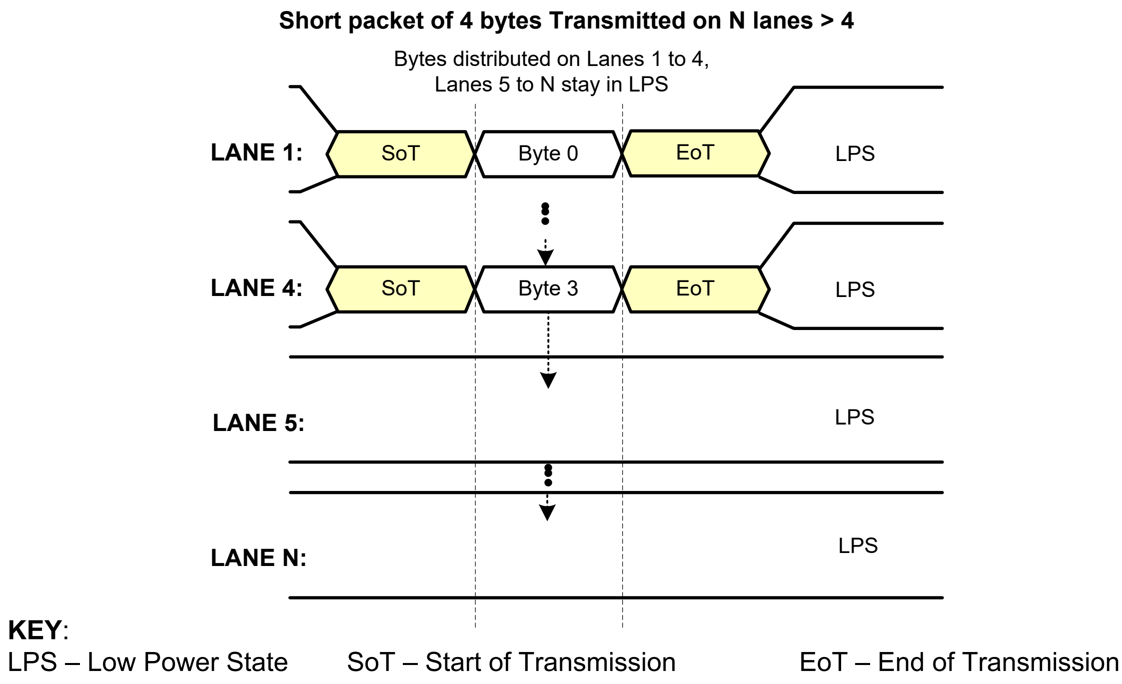


Figure 42 N-Lane Multi-Lane Example for D-PHY Short Packet Transmission

8.2 Lane Distribution for the C-PHY Physical Layer Option

Examples are shown in ***Figure 43*** and ***Figure 44***:

- 2-Lane system (***Figure 43***): bytes 1 and 0 of the packet are sent as a 16-bit word to the Lane 1 C-PHY module, bytes 3 and 2 are sent to Lane 2, bytes 5 and 4 are sent to Lane 1, bytes 7 and 6 are sent to Lane 2, bytes 9 and 8 are sent to Lane 1, and so on.
- 3-Lane system (***Figure 44***): bytes 1 and 0 of the packet are sent as a 16-bit word to the Lane 1 C-PHY module, bytes 3 and 2 are sent to Lane 2, bytes 5 and 4 are sent to Lane 3, bytes 7 and 6 are sent to Lane 1, bytes 9 and 8 are sent to Lane 2, and so on.

Figure 45 illustrates normative behavior for an N-Lane system where N ≥ 1: bytes 1 and 0 of the packet are sent as a 16-bit word to the Lane 1 C-PHY module, bytes 3 and 2 are sent to Lane 2, bytes 2N-1 and 2N-2 are sent to Lane N, bytes 2N+1 and 2N are sent to Lane 1, and so on. The last two bytes B-1 and B-2 are sent to Lane N, where B is the total number of bytes in the packet.

For an N-Lane transmitter, the C-PHY module for Lane n (1 ≤ n ≤ N) shall transmit the following sequence of {ms byte : ls byte} byte pairs from a B-byte packet generated by the low level protocol layer: {Byte 2*(k*N+n)-1 : Byte 2*(k*N+n)-2}, for k = 0, 1, 2, …, B/(2N) - 1, where Byte 0 is the first byte in the packet. The low level protocol shall guarantee that B is an integer multiple of 2N.

That is, at the end of the packet transmission, there shall be no "extra" bytes since the total byte count is always an even multiple of the number of Lanes, N. The Lane distributor, after sending the final set of 2N bytes in parallel to the N Lanes, simultaneously de-asserts its "valid data" signal to all Lanes, signaling to each C-PHY Lane module that it may start its EoT sequence.

Each C-PHY Lane module operates autonomously, but packet data transmission starts and stops at the same time on all Lanes.

The N C-PHY receiver modules on the receiving end of the link collect byte pairs in parallel, and feed them into the Lane-merging layer. This reconstitutes the original sequence of bytes in the transmission, which can then be partitioned into individual packets for the packet decoder layers.

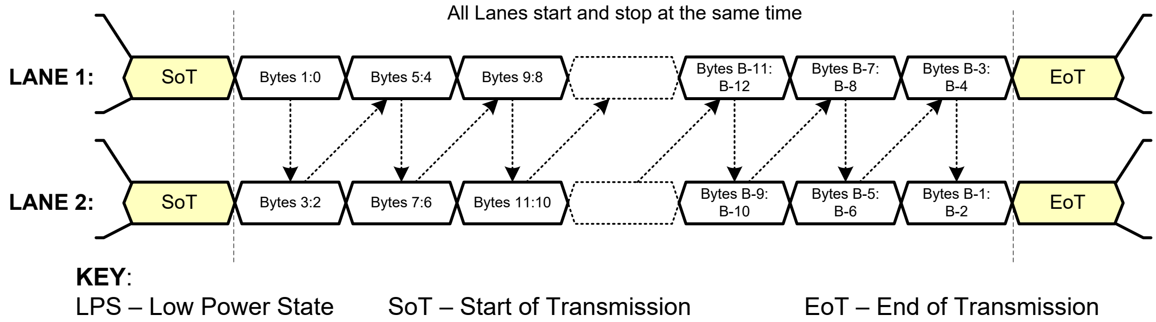


Figure 43 Two Lane Multi-Lane Example for C-PHY

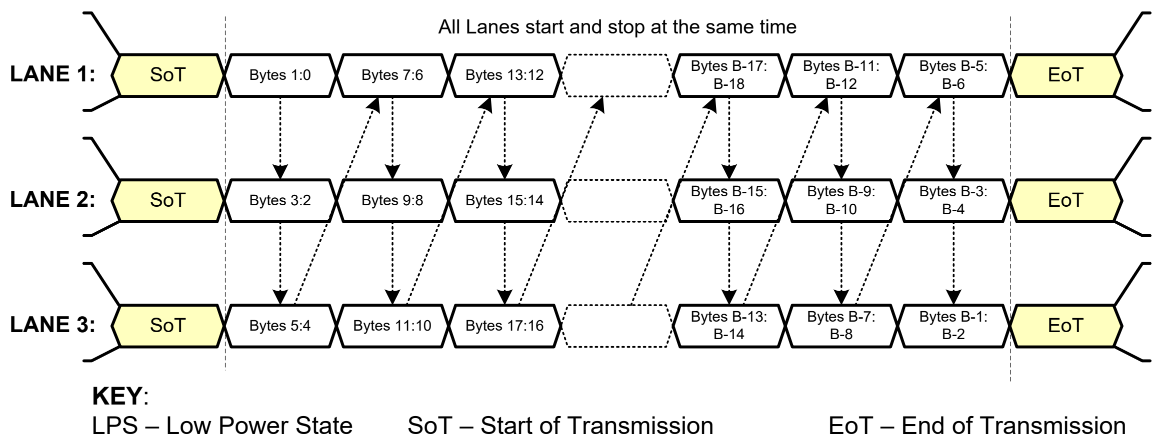


Figure 44 Three Lane Multi-Lane Example for C-PHY

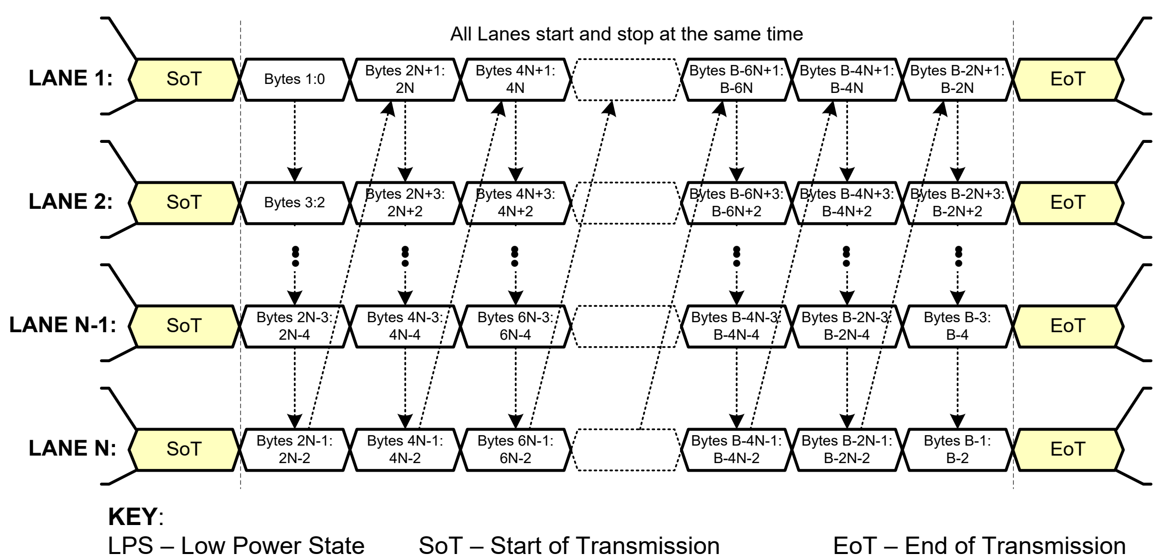


Figure 45 General N-Lane Multi-Lane Distribution for C-PHY

8.3 Multi-Lane Interoperability

The Lane distribution and merging layers shall be reconfigurable via the Camera Control Interface when more than one data Lane is used.

An "N" data Lane receiver shall be connected with an "M" data Lane transmitter, by CCI configuration of the Lane distribution and merging layers within the CSI-2 transmitter and receiver when more than one data Lane is used. Thus, if M<=N a receiver with N data Lanes shall work with transmitters with M data Lanes. Likewise, if M>=N a transmitter with M Lanes shall work with receivers with N data Lanes. Transmitter Lanes 1 to M shall be connected to the receiver Lanes 1 to N.

Two cases:

- If M<=N then there is no loss of performance – the receiver has sufficient data Lanes to match the transmitter (***Figure 46*** and ***Figure 47***).
- If M> N then there may be a loss of performance (e.g. frame rate) as the receiver has fewer data Lanes than the transmitter (***Figure 48*** and ***Figure 49***).
- Note that while the examples shown are for the D-PHY physical layer option, the C-PHY physical layer option is handled similarly, except there is no clock Lane.

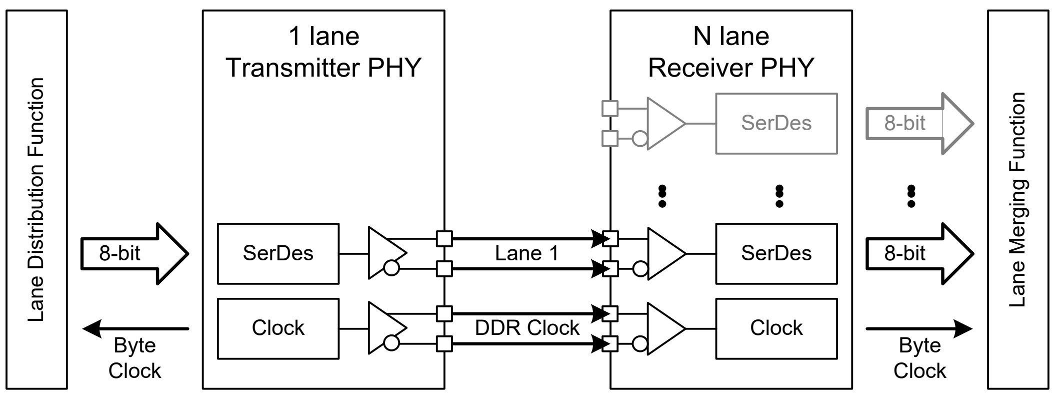


Figure 46 One Lane Transmitter and N-Lane Receiver Example for D-PHY

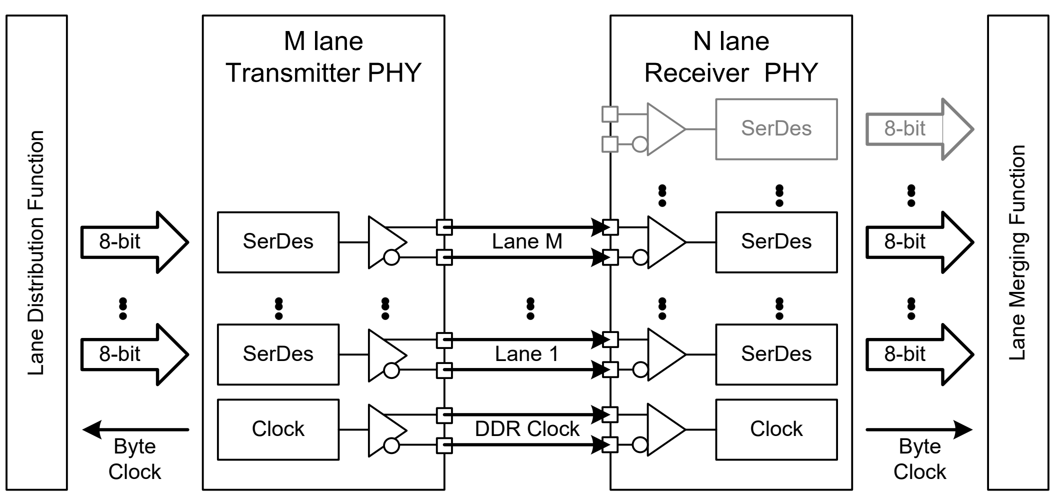


Figure 47 M-Lane Transmitter and N-Lane Receiver Example (M<N) for D-PHY

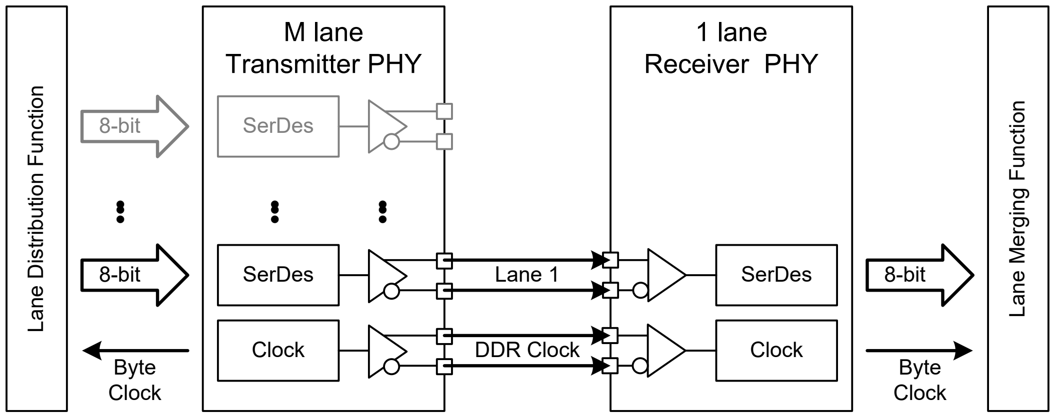
933 

Figure 48 M-Lane Transmitter and One Lane Receiver Example for D-PHY

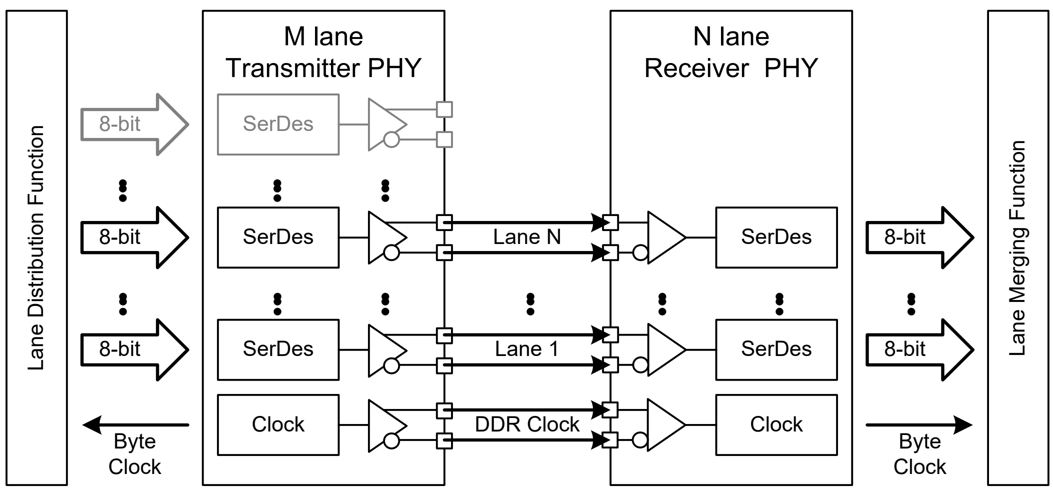
934 

Figure 49 M-Lane Transmitter and N-Lane Receiver Example (N<M) for D-PHY

8.3.1 C-PHY Lane De-Skew

The PPI definition in the C-PHY Specification ***[MIPI02]*** defines one RxWordClkHS per Lane, and does not address the use of a common receive RxWordClkHS for all Lanes within a Link. ***Figure 50*** shows a mechanism for clocking data from the elastic buffers, in order to align (De-Skew) all RxDataHS to one RxWordClkHS.

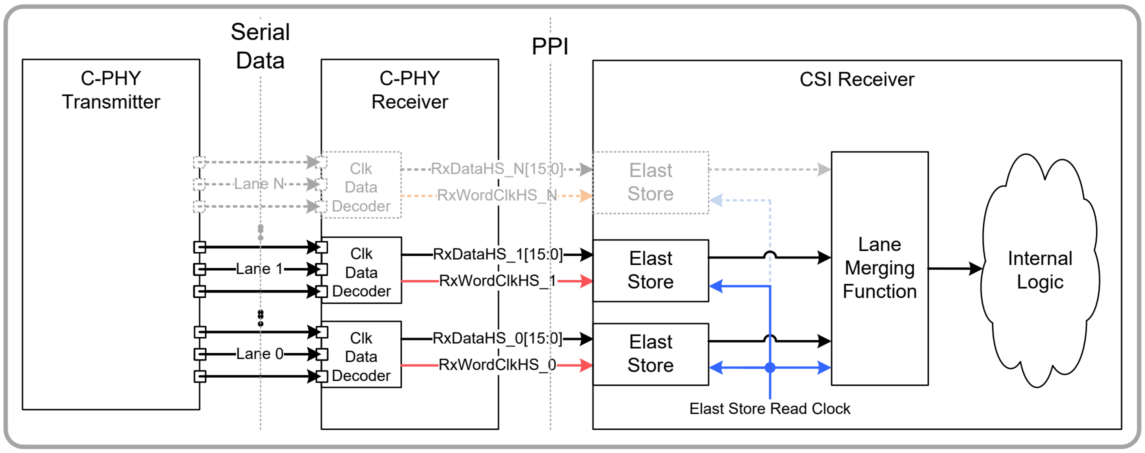


Figure 50 Example of Digital Logic to Align All RxDataHS

This page intentionally left blank.

9 Low Level Protocol

The Low Level Protocol (LLP) is a byte orientated, packet based protocol that supports the transport of arbitrary data using Short and Long packet formats. For simplicity, all examples in this section are single Lane configurations unless specified otherwise.

Basic Low Level Protocol Features:

- Transport of arbitrary data (Payload independent)
- 8-bit word size
- Support for up to sixteen interleaved virtual channels on the same D-PHY Link, or up to 32 interleaved virtual channels on the same C-PHY Link
- Special packets for frame start, frame end, line start and line end information
- Descriptor for the type, pixel depth and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection.
- 6-bit Error Correction Code for error detection and correction (D-PHY physical layer only)

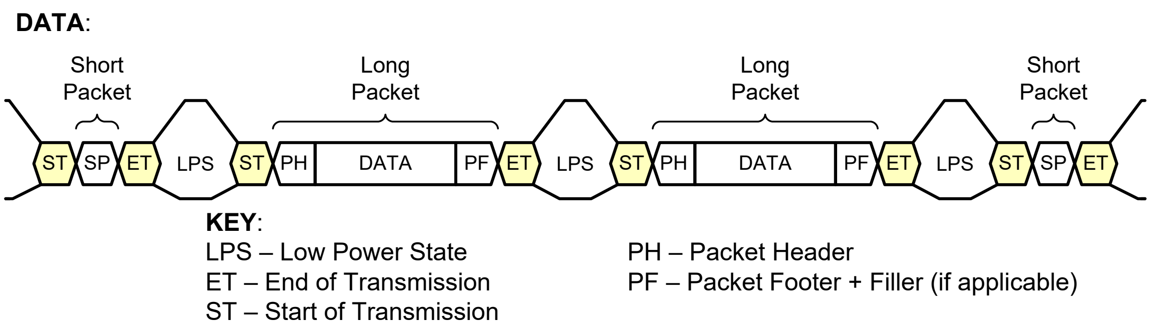


Figure 51 Low Level Protocol Packet Overview

9.1 Low Level Protocol Packet Format

As shown in ***Figure 51***, two packet structures are defined for low-level protocol communication: Long packets and Short packets. The format and length of Short and Long Packets depends on the choice of physical layer. For each packet structure, exit from the low power state followed by the Start of Transmission (SoT) sequence indicates the start of the packet. The End of Transmission (EoT) sequence followed by the low power state indicates the end of the packet.

9.1.1 Low Level Protocol Long Packet Format

Figure 52 shows the structure of the Low Level Protocol Long Packet for the D-PHY physical layer option. A Long Packet shall be identified by Data Types 0x10 to ~~0x37~~0x38. See ***Table 10*** for a description of the Data Types. A Long Packet for the D-PHY physical layer option shall consist of three elements: a 32-bit Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, and a 16-bit Packet Footer (PF). The Packet Header is further composed of four elements: an 8-bit Data Identifier, a 16-bit Word Count field, a 2-bit Virtual Channel Extension field, and a 6-bit ECC. The Packet footer has one element, a 16-bit checksum (CRC). See ***Section 9.2*** through ***Section 9.5*** for further descriptions of the packet elements.

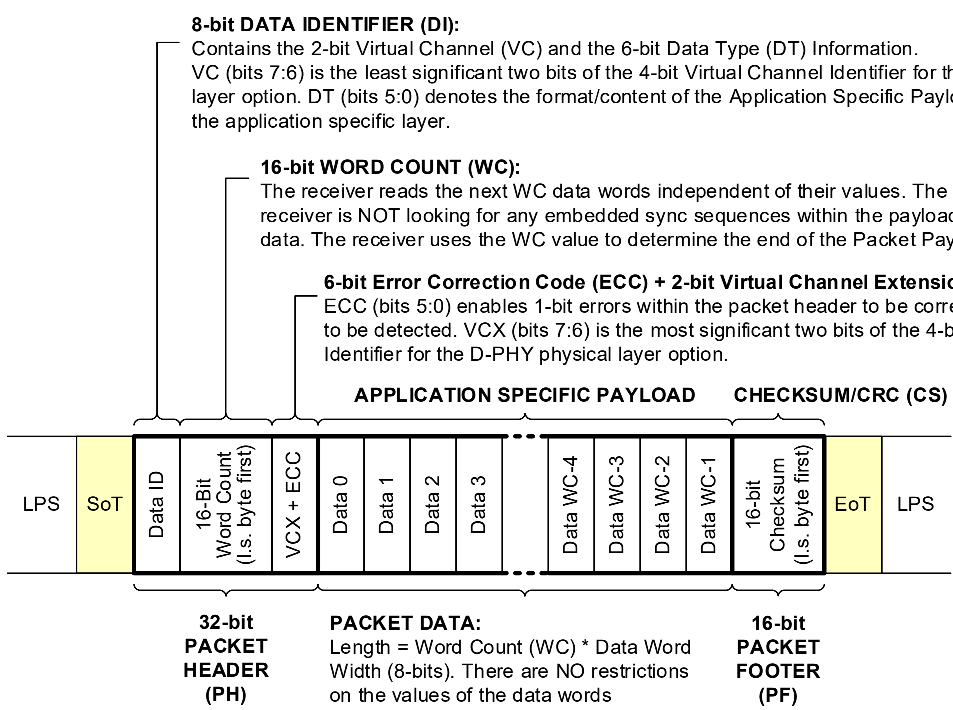


Figure 52 Long Packet Structure for D-PHY Physical Layer Option

Figure 53 shows the Long Packet structure for the C-PHY physical layer option; it shall consist of four elements: a Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, a 16-bit Packet Footer (PF), and zero or more Filler bytes (FILLER). The Packet Header is 6N x 16-bits long, where N is the number of C-PHY physical layer Lanes. As shown in ***Figure 53***, the Packet Header consists of two identical 6N-byte halves, where each half consists of N sequential copies of each of the following fields: a 16-bit field containing five Reserved bits, a 3-bit Virtual Channel Extension (VCX) field, and the 8-bit Data Identifier (DI); the 16-bit Packet Data Word Count (WC); and a 16-bit Packet Header checksum (PH-CRC) which is computed over the previous four bytes. The value of each Reserved bit shall be zero. The Packet Footer consists of a 16-bit checksum (CRC) computed over the Packet Data using the same CRC polynomial as the Packet Header CRC and the Packet Footer used in the D-PHY physical layer option. Packet Filler bytes are inserted after the Packet Footer, if needed, to ensure that the Packet Footer ends on a 16-bit word boundary and that each C-PHY physical layer Lane transports the same number of 16-bit words (i.e. byte pairs).

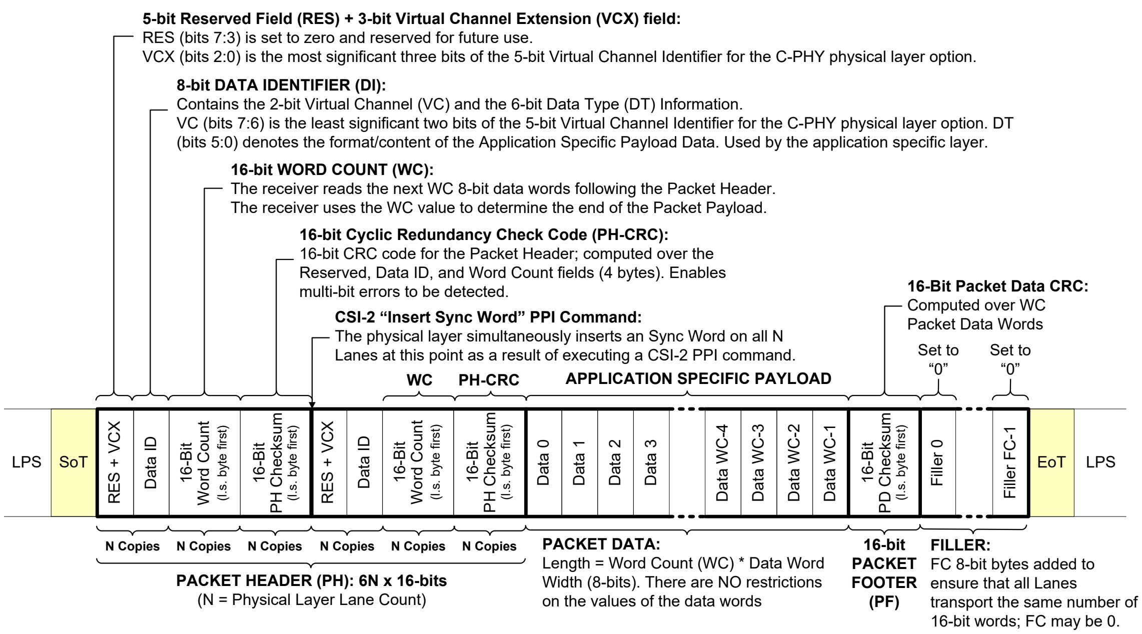


Figure 53 Long Packet Structure for C-PHY Physical Layer Option

As shown in ***Figure 54***, the Packet Header structure depicted in ***Figure 53*** effectively results in the C-PHY Lane Distributor broadcasting the same six 16-bit words to each of N Lanes. Furthermore, the six words per Lane are split into two identical three-word groups which are separated by a mandatory C-PHY Sync Word as described in ***[MIPI02]***. The Sync Word is inserted by the C-PHY physical layer in response to a CSI-2 protocol transmitter PPI command.

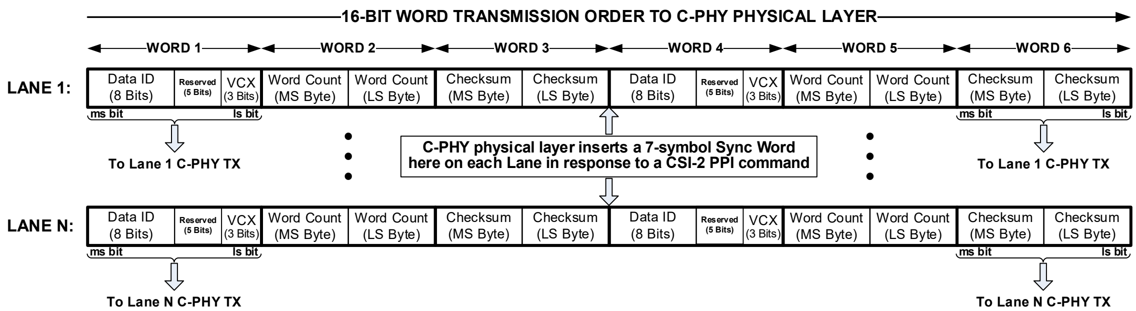


Figure 54 Packet Header Lane Distribution for C-PHY Physical Layer Option

For both physical layer options, the 8-bit Data Identifier field defines the 2-bit Virtual Channel (VC) and the Data Type for the application specific payload data. The Virtual Channel Extension (VCX) field is also common to both options, but is a 2-bit field for D-PHY and a 3-bit field for C-PHY. Together, the VC and VCX fields comprise the 4- or 5-bit Virtual Channel Identifier field which determines the Virtual Channel number associated with the packet (see ***Section 9.3***).

For both physical layer options, the 16-bit Word Count (WC) field defines the number of 8-bit data words in the Data Payload between the end of the Packet Header and the start of the Packet Footer. No Packet Header, Packet Footer, or Packet Filler bytes shall be included in the Word Count.

For the D-PHY physical layer option, the 6-bit Error Correction Code (ECC) allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes the Data Identifier, Word Count, and Virtual Channel Extension field values.

The ECC field is not used by the C-PHY physical layer option because a single symbol error on a C-PHY physical link can cause multiple bit errors in the received CSI-2 Packet Header, rendering an ECC ineffective. Instead, a CSI-2 protocol transmitter for the C-PHY physical layer option computes a 16-bit CRC over the four bytes composing the Reserved, Virtual Channel Extension, Data Identifier, and Word Count Packet Header fields and then transmits multiple copies of all these fields, including the CRC, to facilitate their recovery by the CSI-2 protocol receiver in the event of one or more C-PHY physical link errors. The multiple Sync Words inserted into the Packet Header by the C-PHY physical layer (as shown in ***Figure 54***) also facilitate Packet Header data recovery by enabling the C-PHY receiver to recover from lost symbol clocks; see ***[MIPI02]*** for further information about the C-PHY Sync Word and symbol clock recovery.

For both physical layer options, the CSI-2 receiver reads the next WC 8-bit data words of the Data Payload following the Packet Header. While reading the Data Payload the receiver shall not look for any embedded sync codes. Therefore, there are no limitations on the value of an 8-bit payload data word. In the generic case, the length of the Data Payload shall always be a multiple of 8-bit data words. In addition, each Data Type may impose additional restrictions on the length of the Data Payload, e.g. require a multiple of four bytes.

For both physical layer options, once the CSI-2 receiver has read the Data Payload, it then reads the 16-bit checksum (CRC) in the Packet Footer and compares it against its own calculated checksum to determine if any Data Payload errors have occurred.

Filler bytes are only inserted by the CSI-2 transmitter's low level protocol layer in conjunction with the C-PHY physical layer option. The value of any Filler byte shall be zero. If the Packet Data Word Count (WC) is an odd number (i.e. LSB is "1"), the CSI-2 transmitter shall insert one Packet Filler byte after the Packet Footer to ensure that the Packet Footer ends on a 16-bit word boundary. The CSI-2 transmitter shall also insert additional Filler bytes, if needed, to ensure that each C-PHY Lane transports the same number of 16-bit words. The latter rules require the total number of Filler bytes, FC, to be greater than or equal to $(WC \bmod 2) + \{\{N - (([WC + 2 + (WC \bmod 2)] / 2) \bmod N)\} \bmod N\} * 2$, where N is the number of Lanes. Note that it is possible for FC to be zero.

Figure 55 illustrates the Lane distribution of the minimal number of Filler bytes required for packets of various lengths transmitted over three C-PHY Lanes. The total number of Filler bytes required per packet ranges from 0 to 5, depending on the value of the Packet Data Word Count (WC). In general, the minimal number of Filler bytes required per packet ranges from 0 to 2N-1 for an N-Lane C-PHY system.

For the D-PHY physical layer option, the CSI-2 Lane Distributor function shall pass each byte to the physical layer which then serially transmits it least significant bit first.

For the C-PHY physical layer option, the Lane Distributor function shall group each pair of consecutive bytes 2n and 2n+1 (for $n \geq 0$) received from the Low Level Protocol into a 16-bit word (whose least significant byte is byte 2n) and then pass this word to a physical layer Lane module. The C-PHY Lane module maps each 16-bit word into a 7-symbol word which it then serially transmits least significant symbol first.

For both physical layer options, payload data may be presented to the Lane Distributor function in any byte order restricted only by data format requirements. Multi-byte protocol elements such as Word Count, Checksum and the Short packet 16-bit Data Field shall be presented to the Lane Distributor function least significant byte first.

After the EoT sequence the receiver begins looking for the next SoT sequence.


Total Packet Data Word Count (WC) = 6n
Total Packet Data Word Count (WC) = 6n+1
Total Packet Data Word Count (WC) = 6n+2
Total Packet Data Word Count (WC) = 6n+3
Total Packet Data Word Count (WC) = 6n+4
Total Packet Data Word Count (WC) = 6n+5
KEY:
SoT – Start of Transmission
SYN – 7-Symbol Sync Word
EoT – End of Transmission
PH – Packet Header (6 Bytes)
PF – Packet Footer (2 Bytes)

Figure 55 Minimal Filler Byte Insertion Requirements for Three Lane C-PHY

9.1.2 Low Level Protocol Short Packet Format

Figure 56 and ***Figure 57*** show the Low Level Protocol Short Packet structures for the D-PHY and C-PHY physical layer options, respectively. For each option, the Short Packet structure matches the Packet Header of the corresponding Low Level Protocol Long Packet structure with the exception that the Packet Header Word Count (WC) field shall be replaced by the Short Packet Data Field. A Short Packet shall be identified by Data Types 0x00 to 0x0F. See ***Table 10*** for a description of the Data Types. A Short Packet shall contain only a Packet Header; neither Packet Footer nor Packet Filler bytes shall be present.

For Frame Synchronization Data Types the Short Packet Data Field shall be the frame number. For Line Synchronization Data Types the Short Packet Data Field shall be the line number. See ***Table 13*** for a description of the Frame and Line synchronization Data Types.

For Generic Short Packet Data Types the content of the Short Packet Data Field shall be user defined.

For the D-PHY physical layer option, the Error Correction Code (ECC) field allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet. For the C-PHY physical layer option, the 16-bit Checksum (CRC) allows one or more bit errors to be detected in the Short Packet but does not support error correction; the latter is facilitated by transmitting multiple copies of the various Short Packet fields and by C-PHY Sync Word insertion on all Lanes.

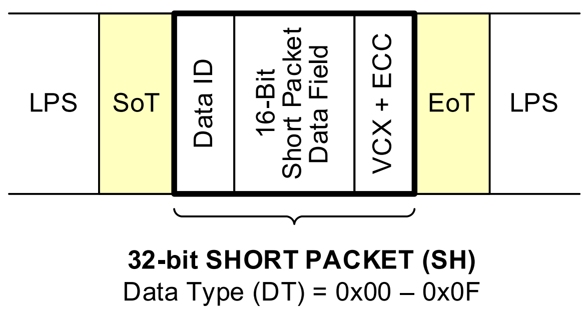


Figure 56 Short Packet Structure for D-PHY Physical Layer Option

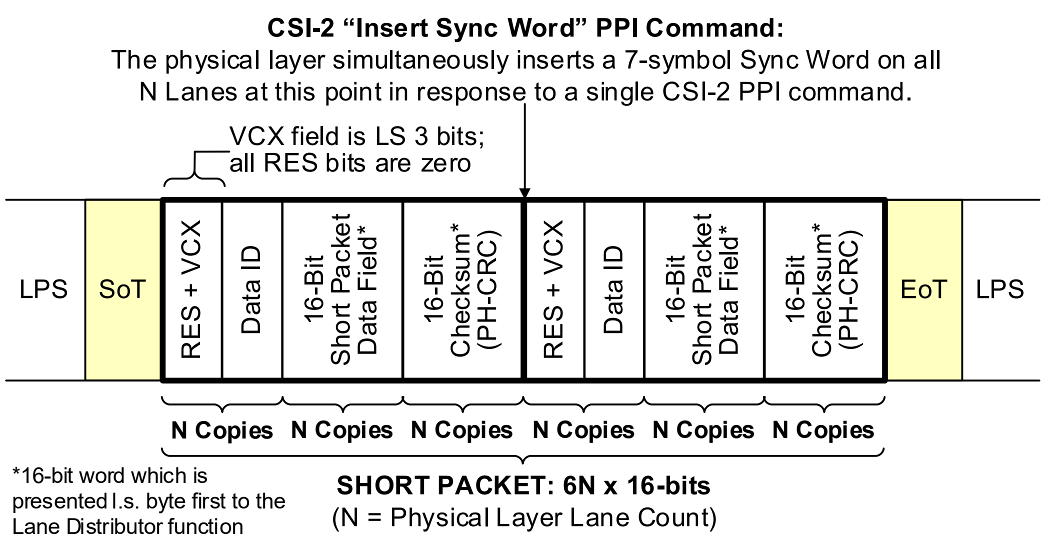


Figure 57 Short Packet Structure for C-PHY Physical Layer Option

9.2 Data Identifier (DI)

The Data Identifier byte contains the Virtual Channel (VC) and Data Type (DT) fields as illustrated in ***Figure 58***. The Virtual Channel field is contained in the two MS bits of the Data Identifier Byte. The Data Type field is contained in the six LS bits of the Data Identifier Byte.

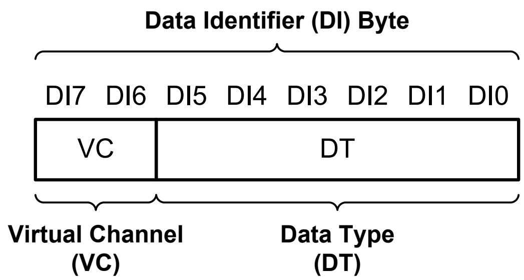


Figure 58 Data Identifier Byte

9.3 Virtual Channel Identifier

The purpose of the 4- or 5-bit Virtual Channel Identifier is to provide a means for designating separate logical channels for different data flows that are interleaved in the data stream.

As shown in ***Figure 59***, the least significant two bits of the Virtual Channel Identifier shall be copied from the 2-bit VC field, and the most significant two or three bits shall be copied from the VCX field. The VCX field is located in the Packet Header as shown in ***Figure 52*** and ***Figure 53***, respectively, for the D-PHY and C-PHY physical layer options. The Receiver shall extract the Virtual Channel Identifier from incoming Packet Headers and de-multiplex the interleaved video data streams to their appropriate channel. A maximum of N data streams is supported, where N = 16 or 32, respectively, for the D-PHY or C-PHY physical layer option; valid channel identifiers are 0 to N-1. The Virtual Channel Identifiers in peripherals should be programmable to allow the host processor to control how the data streams are de-multiplexed.

Host processors receiving packets from peripherals conforming to previous CSI-2 Specification versions not supporting the VCX field shall treat the received value of VCX in all such packets as zero. Similarly, peripherals conforming to this CSI-2 Specification version shall set the VCX field to zero in all packets transmitted to host processors conforming with previous versions not supporting the VCX field. The means by which host processors and peripherals meet these requirements are outside the scope of this Specification.

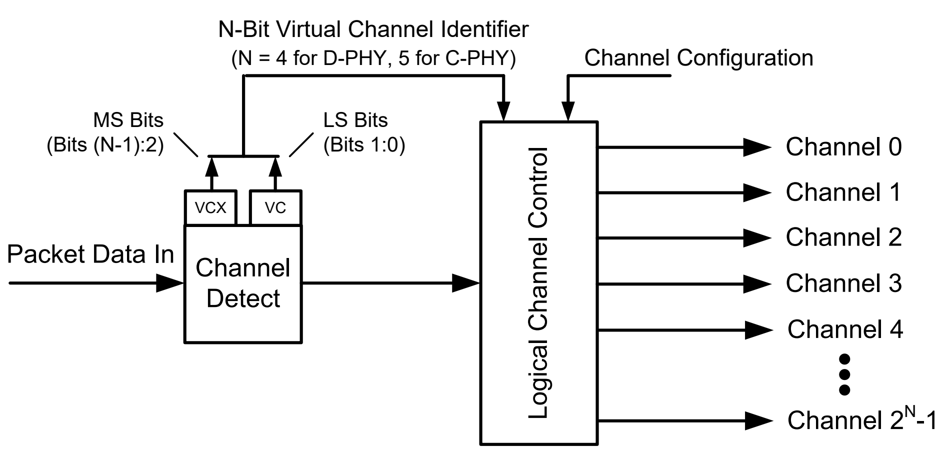


Figure 59 Logical Channel Block Diagram (Receiver)

1076 ***Figure 60*** illustrates an example of data streams utilizing virtual channel support.

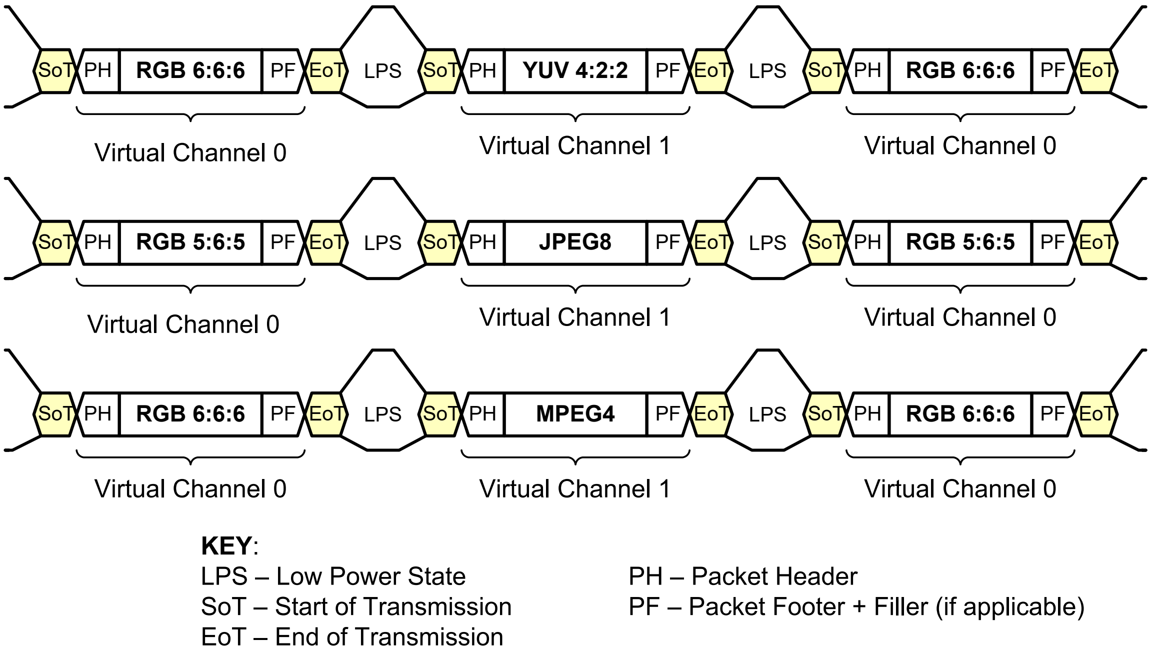
1077 

Figure 60 Interleaved Video Data Streams Examples

9.4 Data Type (DT)

The Data Type value specifies the format and content of the payload data. A maximum of sixty-four data types are supported.

There are eight different data type classes as shown in ***Table 10***. Within each class there are up to ~~eight~~nine different data type definitions. The first two classes denote short packet data types. The remaining six classes denote long packet data types.

For details on the short packet data type classes refer to ***Section 9.8***.

For details on the five long packet data type classes refer to ***Section 11***.

Table 10 Data Type Classes

Data Type	Description
0x00 to 0x07	Synchronization Short Packet Data Types
0x08 to 0x0F	Generic Short Packet Data Types
0x10 to 0x17	Generic Long Packet Data Types
0x18 to 0x1F	YUV Data
0x20 to ~~0x27~~0x26	RGB Data
~~0x28~~0x27 to 0x2F	RAW Data
0x30 to 0x37	User Defined Byte-based Data
0x38	USL Commands (See ***Section 9.12***)
0x39 to 0x3E	Reserved for future use
~~0x38 to~~ 0x3F	For CSI-2 over C-PHY: Reserved for future use For CSI-2 over D-PHY: Unavailable (0x3F is used for LRTE EPD Spacer)

9.5 Packet Header Error Correction Code for D-PHY Physical Layer Option

The correct interpretation of the Data Identifier, Word Count, and Virtual Channel Extension fields is vital to the packet structure. The 6-bit Packet Header Error Correction Code (ECC) allows single-bit errors in the latter fields to be corrected, and two-bit errors to be detected for the D-PHY physical layer option; the ECC is not available for the C-PHY physical layer option. A 26-bit subset of the Hamming-Modified code described in ***Section 9.5.2*** shall be used. The error state ~~resuts~~results of ECC decoding shall be available at the Application layer in the receiver.

The Data Identifier field DI[7:0] shall map to D[7:0] of the ECC input, the Word Count LS Byte (WC[7:0]) to D[15:8], the Word Count MS Byte (WC[15:8]) to D[23:16], and the Virtual Channel Extension (VCX) field to D[25:24]. This mapping is shown in ***Figure 61***, which also serves as an ECC calculation example.

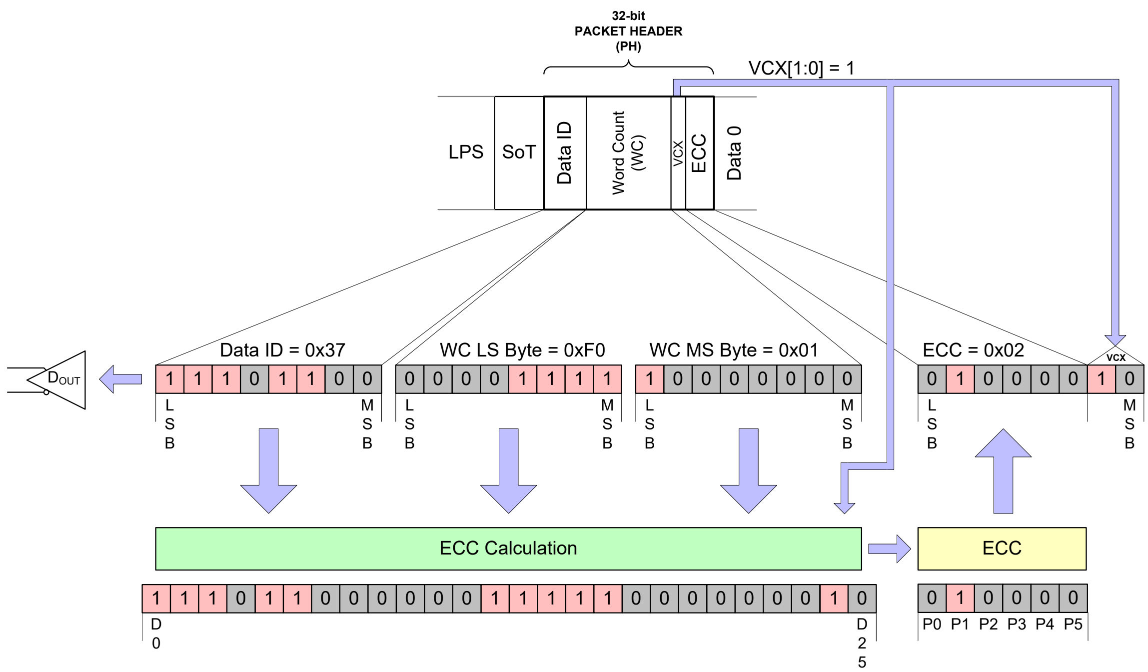


Figure 61 26-bit ECC Generation Example

9.5.1 General Hamming Code Applied to Packet Header

The number of parity or error check bits required is given by the Hamming rule, and is a function of the number of bits of information transmitted. The Hamming rule is expressed by the following inequality:

$d + p + 1 \leq 2^p$, where d is the number of data bits and p is the number of parity bits.

The result of appending the computed parity bits to the data bits is called the Hamming code word. The size of the code word c is obviously $d + p$, and a Hamming code word is described by the ordered set (c, d). A Hamming code word is generated by multiplying the data bits by a generator matrix **G**. The resulting product is the code-word vector (c1, c2, c3 … cn), consisting of the original data bits and the calculated parity bits. The generator matrix **G** used in constructing Hamming codes consists of **I** (the identity matrix) and a parity generation matrix **A**:

$$\mathbf{G} = [\ \mathbf{I} \mid \mathbf{A}\ ]$$

The packet header plus the ECC code can be obtained as: PH = p***G** where p represents the header (26 or 64 bits) and **G** is the corresponding generator matrix.

Validating the received code word r, involves multiplying it by a parity check to form s, the syndrome or parity check vector: s = **H***PH where PH is the received packet header and **H** is the parity check matrix:

$$\mathbf{H} = [\ \mathbf{A}^{\mathbf{T}} \mid \mathbf{I}\ ]$$

If all elements of s are zero, the code word was received correctly. If s contains non-zero elements, then at least one error is present. If a single bit error is encountered then the syndrome s is one of the elements of **H** which will point to the bit in error. Further, in this case, if the bit in error is one of the parity bits, then the syndrome will be one of the elements on **I**, else it will be the data bit identified by the position of the syndrome in $\mathbf{A}^{\mathbf{T}}$.

9.5.2 Hamming-Modified Code

The error correcting code used is a 7+1 bits Hamming-modified code (72,64) and the subset of it is 5+1 bits or (32,26). Hamming codes use parity to correct one error or detect two errors, but they are not capable of doing both simultaneously, thus one extra parity bit is added. The code used allows the same 6-bit syndromes to correct the first 26-bits of a 64-bit sequence. To specify a compact encoding of parity and decoding of syndromes, the matrix shown in ***Table 11*** is used:

Table 11 ECC Syndrome Association Matrix

	d2d1d0							
d5d4d3	**0b000**	**0b001**	**0b010**	**0b011**	**0b100**	**0b101**	**0b110**	**0b111**
0b000	0x07	0x0B	0x0D	0x0E	0x13	0x15	0x16	0x19
0b001	0x1A	0x1C	0x23	0x25	0x26	0x29	0x2A	0x2C
0b010	0x31	0x32	0x34	0x38	0x1F	0x2F	0x37	0x3B
0b011	0x3D	0x3E	0x46	0x49	0x4A	0x4C	0x51	0x52
0b100	0x54	0x58	0x61	0x62	0x64	0x68	0x70	0x83
0b101	0x85	0x86	0x89	0x8A	0x43	0x45	0x4F	0x57
0b110	0x8C	0x91	0x92	0x94	0x98	0xA1	0xA2	0xA4
0b111	0xA8	0xB0	0xC1	0xC2	0xC4	0xC8	0xD0	0xE0

Each cell in the matrix represents a syndrome, and the first 26 cells (the orange cells) use the first three or five bits to build the syndrome. Each syndrome in the matrix is MSB left aligned:

e.g. 0x07 = 0b0000_0111 = P7 P6 P5 P4 P3 P2 P1 P0

The top row defines the three LSB of data position bit, and the left column defines the three MSB of data position bit (there are 64-bit positions in total).

e.g. 37th bit position is encoded 0b100_101 and has the syndrome 0x68.

To derive the parity P0 for 26-bits, the P0's in the orange cells will define whether the corresponding bit position is used in P0 parity or not.

e.g. $P0_{24\text{-bits}}$ = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23^D24

Similarly, to derive the parity P0 for 64-bits, all P0's in ***Table 12*** will define the corresponding bit positions to be used.

To correct a single data bit error, the syndrome must be one of the syndromes in ***Table 11***. These syndromes identify the bit position in error. The syndrome is calculated as:

$S = P_{SEND} \wedge P_{RECEIVED}$, where P_{SEND} is the 8/6-bit ECC field in the header and $P_{RECEIVED}$ is the calculated parity of the received header.

Table 12 represents the same information as the matrix in ***Table 11***, organized so as to provide better insight into the way in which parity bits are formed out of data bits. The orange area of the table is used to form the ECC needed to protect a 26-bit header, whereas the whole table must be used to protect a 64-bit header.

Previous CSI-2 specification versions not supporting the Virtual Channel Extension (VCX) field utilize a 30-bit Hamming-modified code word with 24 data bits and 5+1 parity bits based on the first 24 bit positions of ***Table 12*** [i.e. a (30,24) ECC]. Packet Header bits 24 and 25 are set to zero by transmitters, and ignored by receivers conforming to such Specifications.

When receiving Packet Headers with a (30,24) ECC, receivers conforming to this CSI-2 Specification version shall ignore the contents of bits 24 and 25 in such Packet Headers. The intent is for such receivers to ignore any errors occurring at these bit positions, in order to match the behavior of previous receivers. (See ***Section 9.5.4*** for implementation recommendations.)

Table 12 ECC Parity Generation Rules

Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B
24	0	0	1	1	1	1	0	1	0x3D
25	0	0	1	1	1	1	1	0	0x3E
26	0	1	0	0	0	1	1	0	0x46
27	0	1	0	0	1	0	0	1	0x49
28	0	1	0	0	1	0	1	0	0x4A
29	0	1	0	0	1	1	0	0	0x4C
30	0	1	0	1	0	0	0	1	0x51
31	0	1	0	1	0	0	1	0	0x52

Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
32	0	1	0	1	0	1	0	0	0x54
33	0	1	0	1	1	0	0	0	0x58
34	0	1	1	0	0	0	0	1	0x61
35	0	1	1	0	0	0	1	0	0x62
36	0	1	1	0	0	1	0	0	0x64
37	0	1	1	0	1	0	0	0	0x68
38	0	1	1	1	0	0	0	0	0x70
39	1	0	0	0	0	0	1	1	0x83
40	1	0	0	0	0	1	0	1	0x85
41	1	0	0	0	0	1	1	0	0x86
42	1	0	0	0	1	0	0	1	0x89
43	1	0	0	0	1	0	1	0	0x8A
44	0	1	0	0	0	0	1	1	0x43
45	0	1	0	0	0	1	0	1	0x45
46	0	1	0	0	1	1	1	1	0x4F
47	0	1	0	1	0	1	1	1	0x57
48	1	0	0	0	1	1	0	0	0x8C
49	1	0	0	1	0	0	0	1	0x91
50	1	0	0	1	0	0	1	0	0x92
51	1	0	0	1	0	1	0	0	0x94
52	1	0	0	1	1	0	0	0	0x98
53	1	0	1	0	0	0	0	1	0xA1
54	1	0	1	0	0	0	1	0	0xA2
55	1	0	1	0	0	1	0	0	0xA4
56	1	0	1	0	1	0	0	0	0xA8
57	1	0	1	1	0	0	0	0	0xB0
58	1	1	0	0	0	0	0	1	0xC1
59	1	1	0	0	0	0	1	0	0xC2
60	1	1	0	0	0	1	0	0	0xC4
61	1	1	0	0	1	0	0	0	0xC8
62	1	1	0	1	0	0	0	0	0xD0
63	1	1	1	0	0	0	0	0	0xE0

9.5.3 ECC Generation on TX Side

This is an informative section.

The ECC can be easily implemented using a parallel approach as depicted in ***Figure 62*** for a 64-bit header.

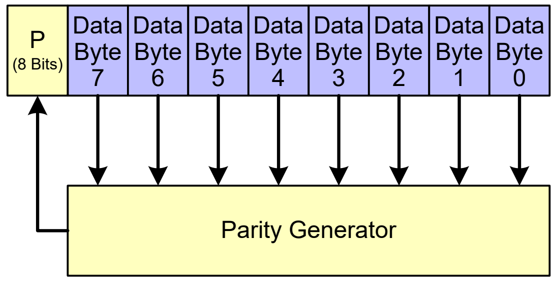


Figure 62 64-bit ECC Generation on TX Side

And ***Figure 63*** for a 26-bit header:

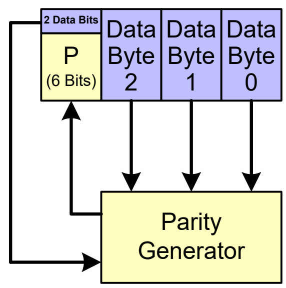


Figure 63 26-bit ECC Generation on TX Side

The parity generators are based on ***Table 12***.

e.g. $P3_{26\text{-bit}}$ = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23^D24^D25

For backwards-compatibility, transmitters conforming to this CSI-2 Specification version should always set Packet Header bits 24 and 25 (the VCX field) to zero in any packets sent to receivers conforming to previous CSI-2 Specification versions incorporating a (30,24) ECC.

9.5.4 Applying ECC on RX Side (Informative)

Applying ECC on RX side involves generating a new ECC for the received Packet Header, computing the syndrome using the new ECC and the received ECC, decoding the syndrome to find if a single-error has occurred, and if so, correcting it. ***Figure 64*** depicts ECC processing for 64 received Packet Header data bits, using 8 parity bits.

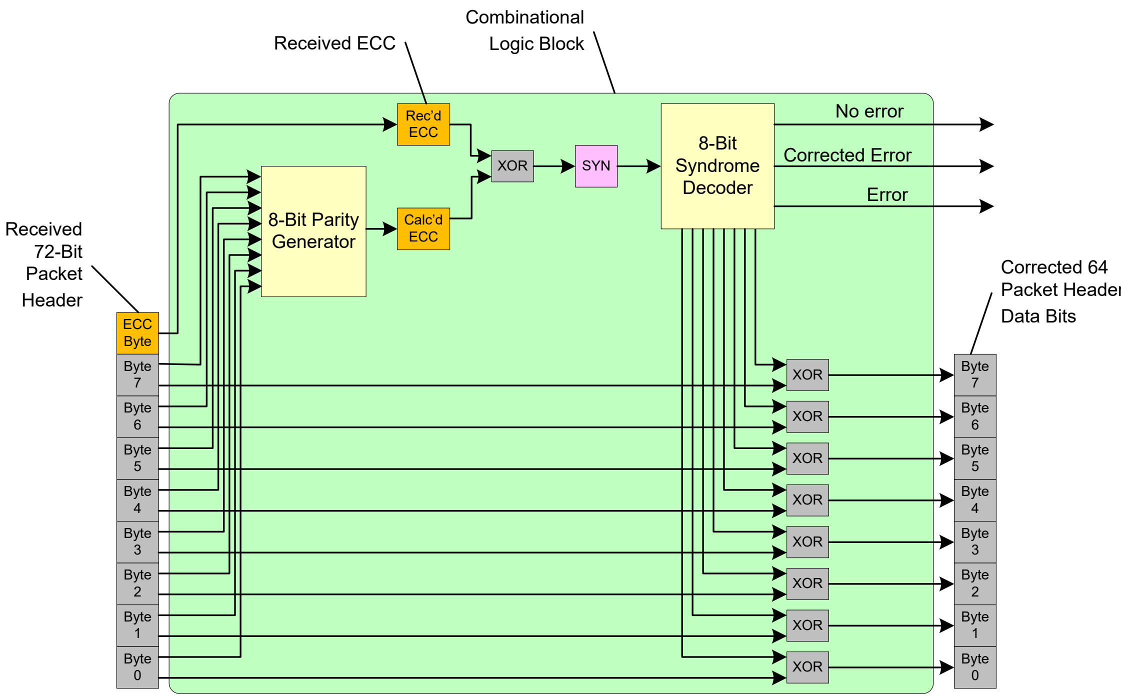


Figure 64 64-bit ECC on RX Side Including Error Correction

Decoding the syndrome has four possible outcomes:

1. If the syndrome is 0, no errors are present.
2. If the syndrome matches one of the matrix entries in the ***Table 11***, then a single bit error has occurred and the corresponding bit position may be corrected by inverting it (e.g. by XORing with '1').
3. If the syndrome has only one bit set, then a single bit error has occurred at the parity bit located at that syndrome bit position, and the rest of the received packet header bits are error-free.
4. If the syndrome does not fit any of the other outcomes, then an uncorrectable error has occurred, and an error flag should be set (indicating that the Packet Header is corrupted).

The 26-bit implementation shown in ***Figure 65*** uses fewer terms to calculate the parity, and thus the syndrome decoding block is much simpler than the 64-bit implementation.

Receivers conforming to this CSI-2 Specification version that receive Packet Headers from transmitters without the VCX field should forcibly set received bits 24 and 25 to zero in such Packet Headers prior to any parity generation or syndrome decoding (this is the function of the "VCX Override" block shown in ***Figure 65***). This guarantees that the receiver will properly ignore any errors occurring at bit positions 24 and 25, in order to match the behavior of receivers conforming to previous versions of this Specification.

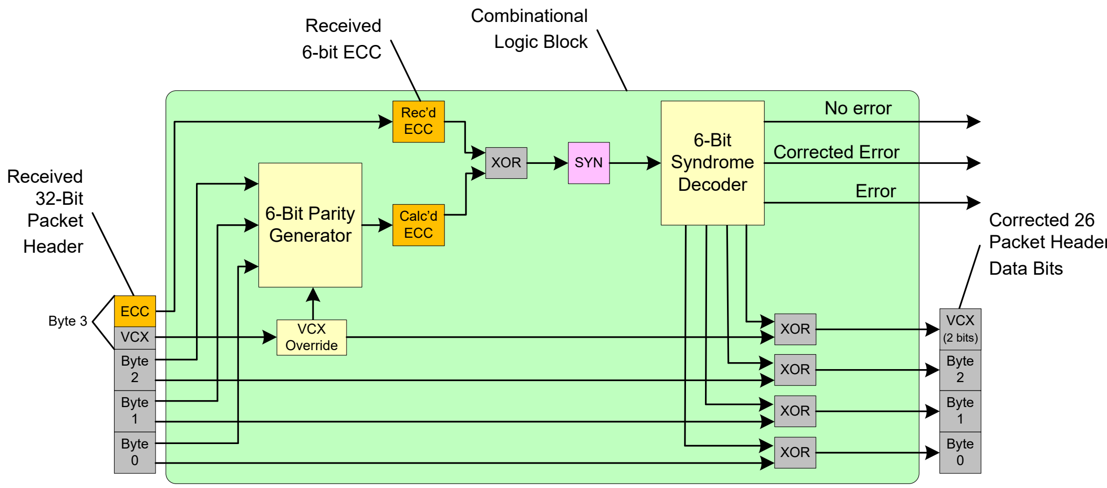


Figure 65 26-bit ECC on RX Side Including Error Correction

9.6 Checksum Generation

To detect possible errors in transmission, a checksum is calculated over the WC bytes composing the Packet Data of every Long Packet; a similar checksum is calculated over the four bytes composing the Reserved, Virtual Channel Extension, Data Identifier, and Word Count fields of every Packet Header for the C-PHY physical layer option. In all cases, the checksum is realized as 16-bit CRC based on the generator polynomial $x^{16}+x^{12}+x^5+x^0$ and is computed over bytes in the order in which they are presented to the Lane Distributor function by the low level protocol layer as shown in ***Figure 52***, ***Figure 53***, and ***Figure 57***.

The order in which the checksum bytes are presented to the Lane Distributor function is illustrated in ***Figure 66***.

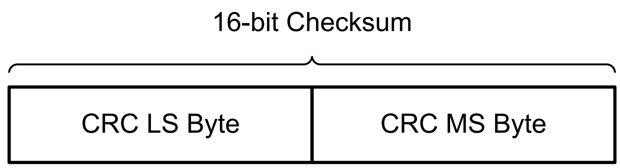


Figure 66 Checksum Transmission Byte Order

When computed over the Packet Data words of a Long Packet, the 16-bit checksum sequence is transmitted as part of the Packet Footer. When the Word Count is zero, the CRC shall be 0xFFFF. When computed over the Reserved, Virtual Channel Extension, Data Identifier, and Word Count fields of a Packet Header for the C-PHY physical layer option, the 16-bit checksum sequence is transmitted as part of the Packet Header CRC (PH-CRC) field.

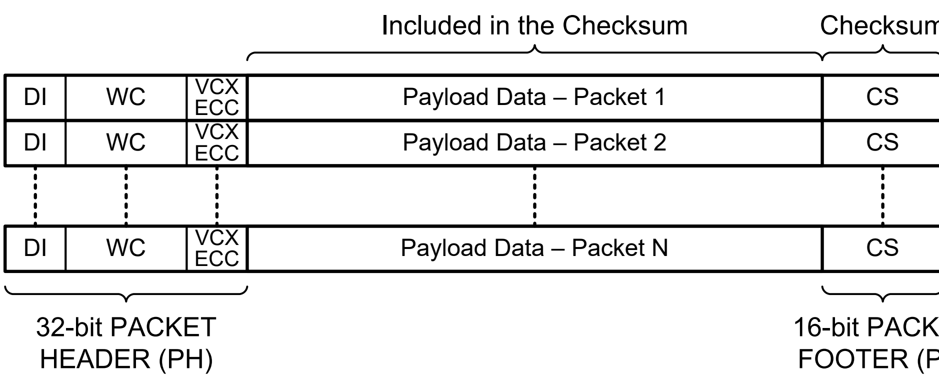
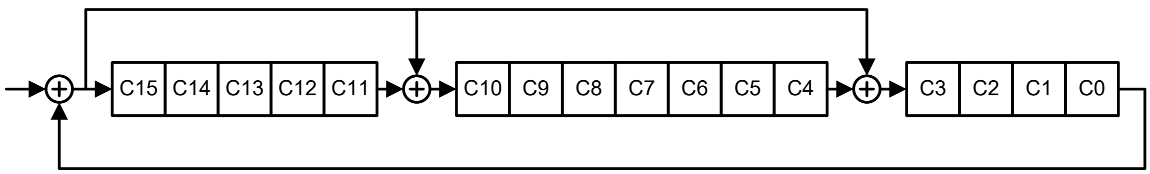


Figure 67 Checksum Generation for Long Packet Payload Data

The definition of a serial CRC implementation is presented in ***Figure 68***. The CRC implementation shall be functionally equivalent with the C code presented in ***Figure 69***. The CRC shift register is initialized to 0xFFFF at the beginning of each packet. Note that for the C-PHY physical layer option, if the same circuitry is used to compute both the Packet Header and Packet Footer CRC, the CRC shift register shall be initialized twice per packet, i.e. once at the beginning of the packet and then again following the computation of the Packet Header CRC. After all payload data has passed through the CRC circuitry, the CRC circuitry contains the checksum. The 16-bit checksum produced by the C code in ***Figure 69*** equals the final contents of the C[15:0] shift register shown in ***Figure 68***. The checksum is then transmitted by the CSI-2 physical layer to the CSI-2 receiver to verify that no errors have occurred in the transmission.



Polynomial: $x^{16} + x^{12} + x^{5} + x^{0}$

Note: C15 represents x^0, C0 represents x^{15}

Figure 68 Definition of 16-bit CRC Shift Register

```
#define POLY 0x8408   /* 1021H bit reversed */

unsigned short crc16(char *data_p, unsigned short length)
{
   unsigned char i;
   unsigned int data;
   unsigned int crc = 0xffff;

   if (length == 0)
      return (unsigned short)(crc);
   do
   {
      for (i=0, data=(unsigned int)0xff & *data_p++;
        i < 8;i++, data >>= 1)
      {
         if ((crc & 0x0001) ^ (data & 0x0001))
            crc = (crc >> 1) ^ POLY;
         else
            crc >>= 1;
      }
   } while (--length);

   // Uncomment to change from little to big Endian
// crc = ((crc & 0xff) << 8) | ((crc & 0xff00) >> 8);

   return (unsigned short)(crc);
}
```

Figure 69 16-bit CRC Software Implementation Example

Beginning with index 0, the contents of the input data array in ***Figure 69*** are given by WC 8-bit payload data words for packet data CRC computations and by the four 8-bit [Reserved, VCX], Data Identifier, WC (LS byte), and WC (MS byte) fields for packet header CRC computations.

CRC computation examples:

```
Input Data Bytes:
FF 00 00 02 B9 DC F3 72 BB D4 B8 5A C8 75 C2 7C 81 F8 05 DF FF 00 00 01
Checksum LS byte and MS byte:
F0 00

Input Data Bytes:
FF 00 00 00 1E F0 1E C7 4F 82 78 C5 82 E0 8C 70 D2 3C 78 E9 FF 00 00 01
Checksum LS byte and MS byte:
69 E5
```

9.7 Packet Spacing

All CSI-2 implementations shall support a transition into and out of the Low Power State (LPS) between Low Level Protocol packets; however, implementations may optionally remain in the High Speed State between packets as described in ***Section 9.11***. ***Figure 70*** illustrates the packet spacing with the LPS.

The packet spacing illustrated in ***Figure 70*** does not have to be a multiple of 8-bit data words, as the receiver will resynchronize to the correct byte boundary during the SoT sequence prior to the Packet Header of the next packet.

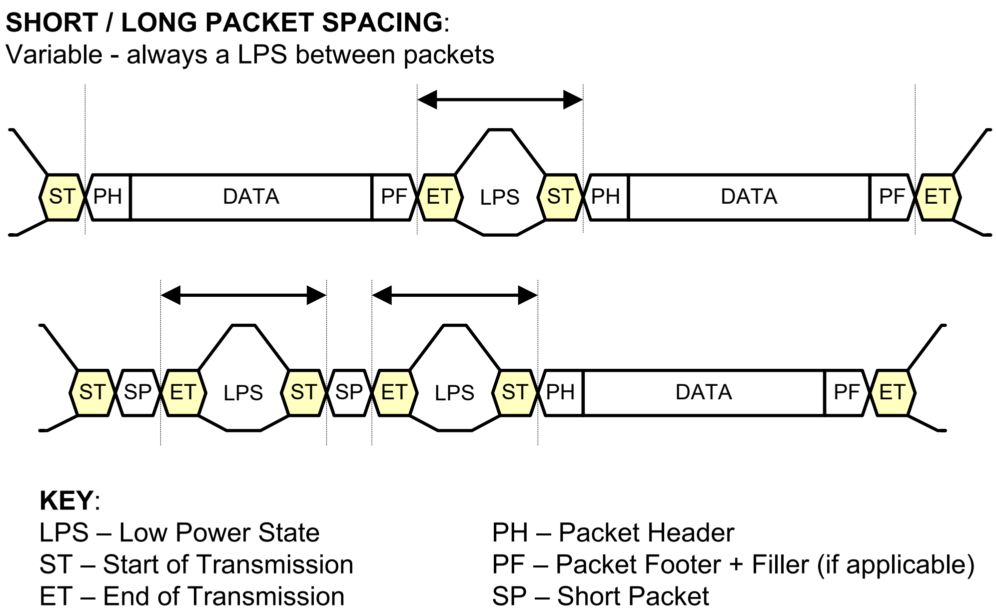


Figure 70 Packet Spacing

9.8 Synchronization Short Packet Data Type Codes

Short Packet Data Types shall be transmitted using only the Short Packet format. See ***Section 9.1.2*** for a format description.

Table 13 Synchronization Short Packet Data Type Codes

Data Type	Description
0x00	Frame Start Code
0x01	Frame End Code
0x02	Line Start Code (Optional)
0x03	Line End Code (Optional)
0x04	End of Transmission Code (Optional) See ***Section 9.11.1.2.5*** for description.
~~0x04~~0x05 to 0x07	Reserved

9.8.1 Frame Synchronization Packets

Each image frame shall begin with a Frame Start (FS) Packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data and zero or more short packets containing synchronization codes. Each image frame shall end with a Frame End (FE) Packet containing the Frame End Code. See ***Table 13*** for a description of the synchronization code data types.

For FS and FE synchronization packets the Short Packet Data Field shall contain a 16-bit frame number. This frame number shall be the same for the FS and FE synchronization packets corresponding to a given frame.

The 16-bit frame number, when used, shall be non-zero to distinguish it from the use-case where frame number is inoperative and remains set to zero.

The behavior of the 16-bit frame number shall be one of the following:

- Frame number is always zero – frame number is inoperative.
- Frame number increments by 1 or 2 for every FS packet with the same Virtual Channel and is periodically reset to one; e.g. 1, 2, 1, 2, 1, 2, 1, 2 or 1, 2, 3, 4, 1, 2, 3, 4 or 1, 3, 5, 1, 3, 5 or 1, 2, 4, 1, 3, 4. Frame number may be incremented by 2 only when an image frame is masked (i.e. not transmitted) due to corruption. To accommodate such cases, increments by 1 or 2 may be freely intermixed within a sequence of frame numbers as needed.

9.8.2 Line Synchronization Packets

Line synchronization short packets are optional on a per-image-frame basis. If an image frame includes Line Start (LS) and Line End (LE) line synchronization short packets~~,~~ with one long packet having a given data type and virtual channel number, then it shall include ~~both Line Start (LS) synchronization~~LS and LE short packets ~~and Line End (LE) synchronization~~with all long packets ~~in each line of~~having that same data type and virtual channel number within the same image frame.

For LS and LE synchronization packets, the Short Packet Data Field shall contain a 16-bit line number. This line number shall be the same for the LS and LE packets corresponding to a given line. Line numbers are logical line numbers and are not necessarily equal to the physical line numbers.

The 16-bit line number, when used, shall be non-zero to distinguish it from the case where line number is inoperative and remains set to zero.

The behavior of the 16-bit line number within the same Data Type and Virtual Channel shall be one of the following.

Either:

1. Line number is always zero – line number is inoperative.

Or:

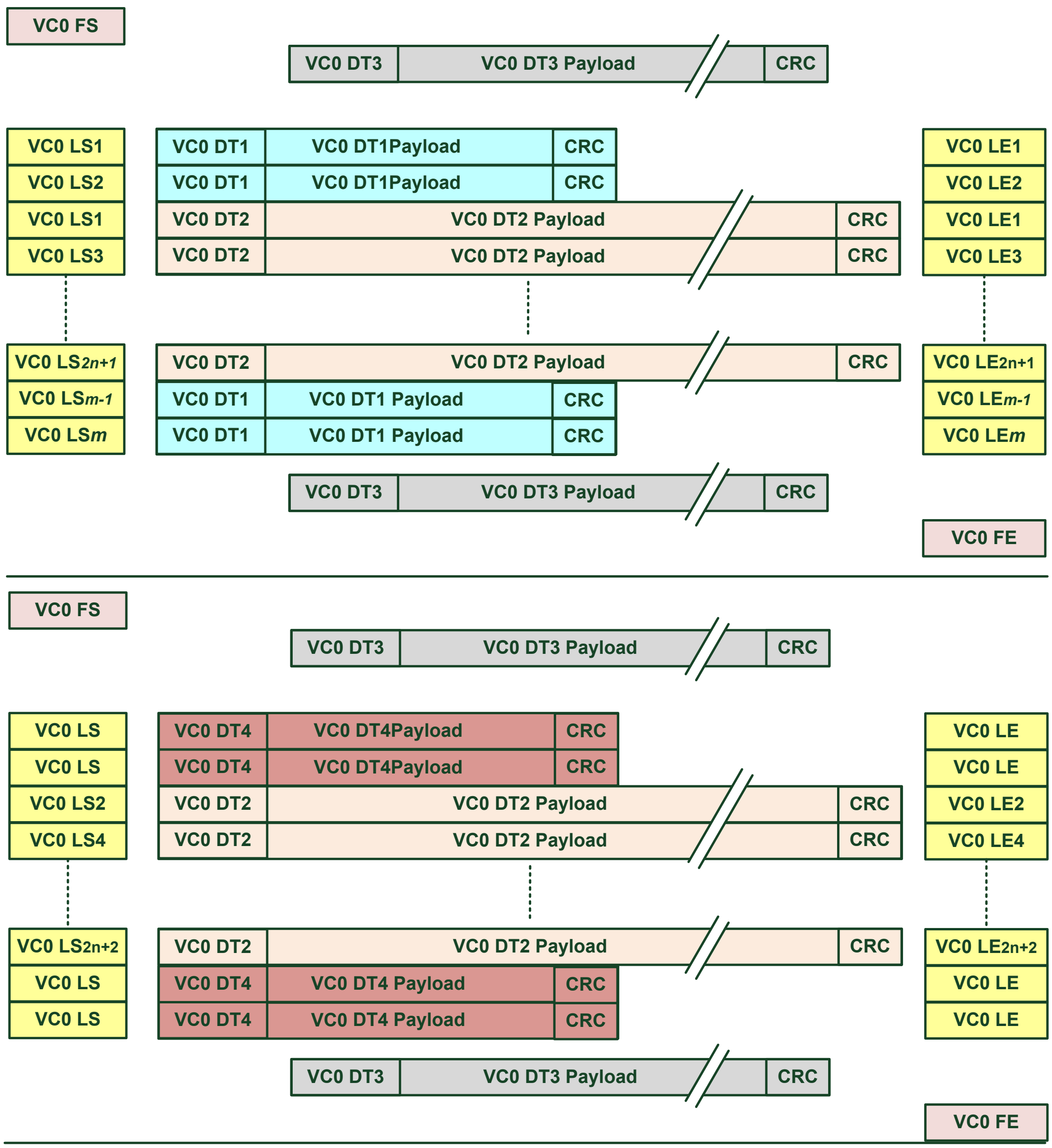
2. Line number increments by one for every LS packet within the same Virtual Channel and the same Data Type. The line number is periodically reset to one for the first LS packet after a FS packet. The intended usage is for progressive scan (non- interlaced) video data streams. The line number must be a non-zero value.

Or:

3. Line number increments by the same arbitrary step value greater than one for every LS packet within the same Virtual Channel and the same Data Type. The line number is periodically reset to a non-zero arbitrary start value for the first LS packet after a FS packet. The arbitrary start value may be different between successive frames. The intended usage is for interlaced video data streams.

Figure 71 contains examples for the use of optional LS/LE packets within an interlaced frame with pixel data and additional embedded types. The Figure illustrates the use cases:

1. VC0 DT2 Interlaced frame with line counting incrementing by two. Frame1 starting at 1 and Frame2 starting at 2.
2. VC0 DT1 Progressive scan frame with line counting.
3. VC0 DT4 Progressive scan frame with non-operative line counting.
4. VC0 DT3 No LS/LE operation.



Note:

- For VC0 DT2 Odd Frames LS2n+1 and Even Frames LS2n+2 (where n=0,1,2,3...) the first line n=0
- For VC0 DT1 LSm+1(where m=0,1,2,3...) the first line m=0

Figure 71 Example Interlaced Frame Using LS/~~SE~~LE Short Packet and Line Counting

9.9 Generic Short Packet Data Type Codes

Table 14 lists the Generic Short Packet Data Types.

Table 14 Generic Short Packet Data Type Codes

Data Type	Description
0x08	Generic Short Packet Code 1
0x09	Generic Short Packet Code 2
0x0A	Generic Short Packet Code 3
0x0B	Generic Short Packet Code 4
0x0C	Generic Short Packet Code 5
0x0D	Generic Short Packet Code 6
0x0E	Generic Short Packet Code 7
0x0F	Generic Short Packet Code 8

The intention of the Generic Short Packet Data Types is to provide a mechanism for including timing information for the opening/closing of shutters, triggering of flashes, etc., within the data stream. The intent of the 16-bit User defined data field in the generic short packets is to pass a data type value and a 16-bit data value from the transmitter to application layer in the receiver. The CSI-2 receiver shall pass the data type value and the associated 16-bit data value to the application layer.

9.10 Packet Spacing Examples Using the Low Power State

Packets discussed in this section are separated by an EoT, LPS, SoT sequence as defined in ***[MIPI01]*** for the D-PHY physical layer option and ***[MIPI02]*** for the C-PHY physical layer option.

Figure 72 and ***Figure 73*** contain examples of data frames composed of multiple packets and a single packet, respectively.

Note that the VVALID, HVALID and DVALID signals in the figures in this section are only concepts to help illustrate the behavior of the frame start/end and line start/end packets. The VVALID, HVALID and DVALID signals do not form part of the Specification.

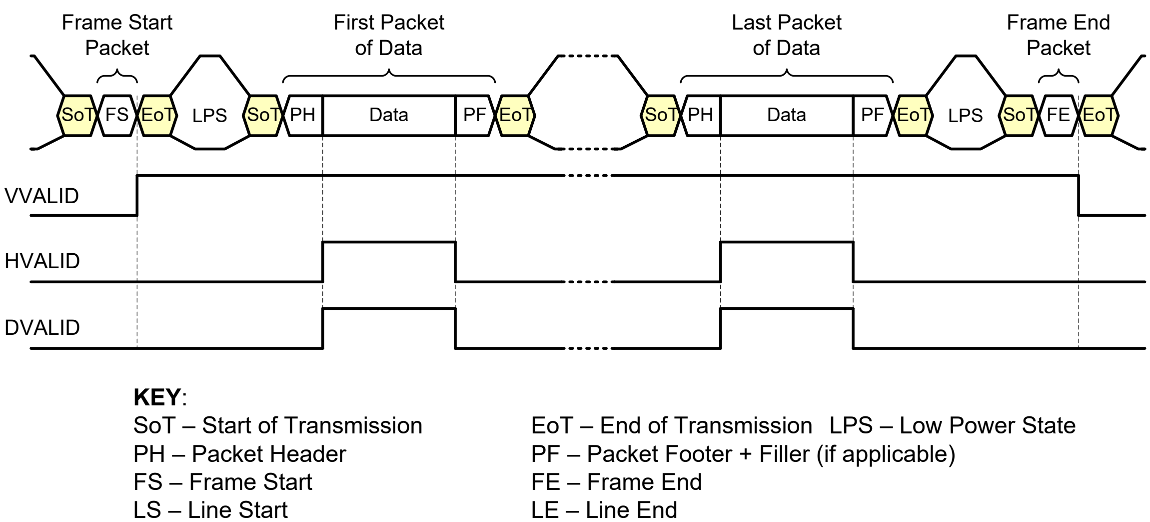


Figure 72 Multiple Packet Example

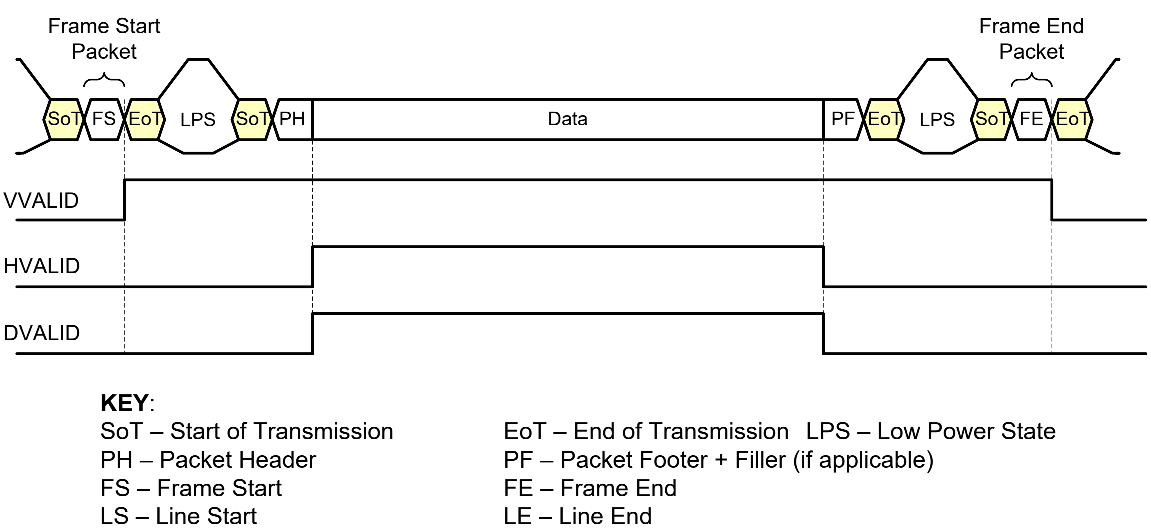


Figure 73 Single Packet Example

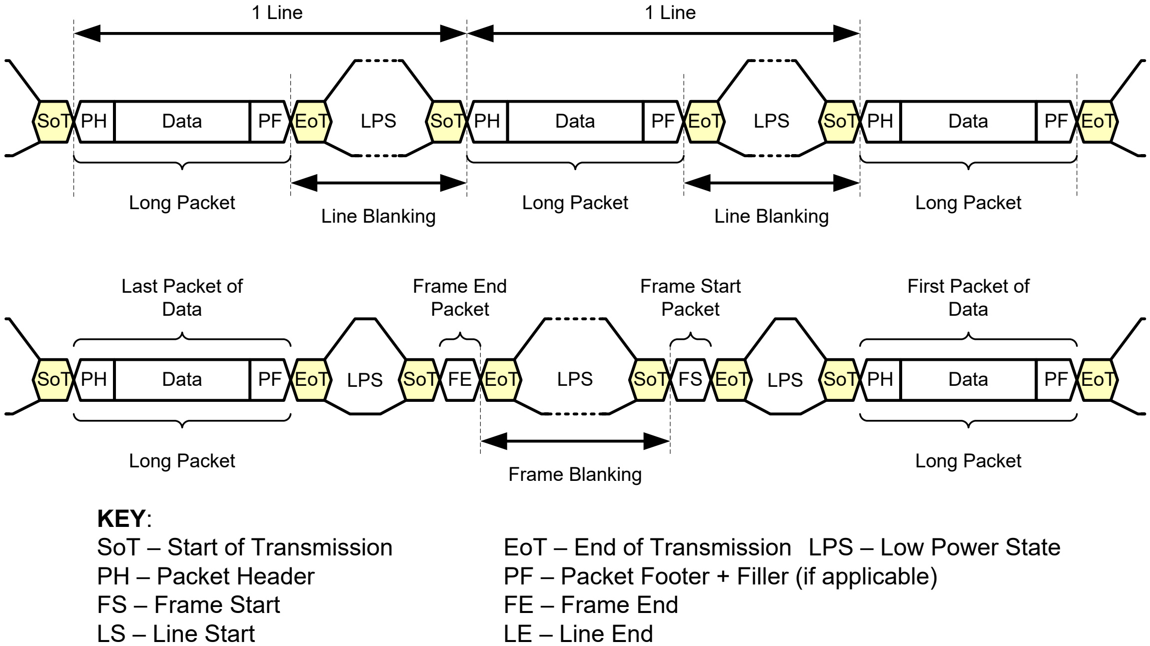


Figure 74 Line and Frame Blanking Definitions

The period between the end of the Packet Footer (or the Packet Filler, if present) of one long packet and the Packet Header of the next long packet is called the Line Blanking Period.

The period between the Frame End packet in frame N and the Frame Start packet in frame N+1 is called the Frame Blanking Period (***Figure 74***).

The Line Blanking Period is not fixed and may vary in length. The receiver should be able to cope with a near zero Line Blanking Period as defined by the minimum inter-packet spacing defined in ***[MIPI01]*** or ***[MIPI02]***, as appropriate. The transmitter defines the minimum time for the Frame Blanking Period. The Frame Blanking Period duration should be programmable in the transmitter.

Frame Start and Frame End packets shall be used.

Recommendations (informative) for frame start and end packet spacing:

- The Frame Start packet to first data packet spacing should be as close as possible to the minimum packet spacing
- The last data packet to Frame End packet spacing should be as close as possible to the minimum packet spacing

The intention is to ensure that the Frame Start and Frame End packets accurately denote the start and end of a frame of image data. A valid exception is when the positions of the Frame Start and Frame End packets are being used to convey pixel level accurate vertical synchronization timing information.

The positions of the Frame Start and Frame End packets can be varied within the Frame Blanking Period in order to provide pixel level accurate vertical synchronization timing information. See ***Figure 75***.

If pixel level accurate horizontal synchronization timing information is required, Line Start and Line End packets should be used to achieve it.

The positions of the Line Start and Line End packets, if present, can be varied within the Line Blanking Period in order to provide pixel accurate horizontal synchronization timing information. See ***Figure 76***.

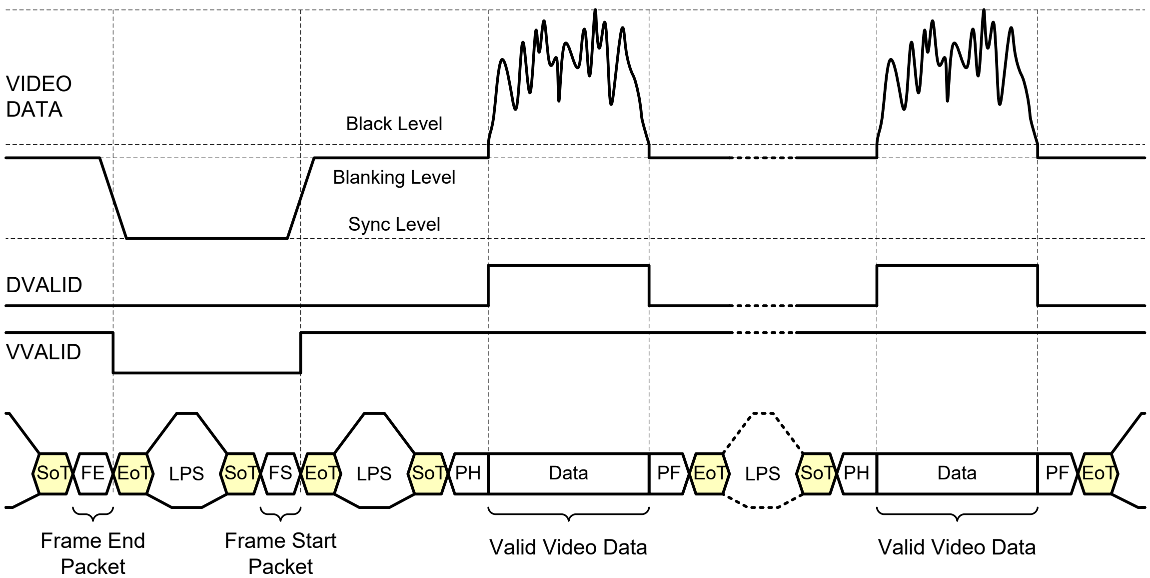


Figure 75 Vertical Sync Example

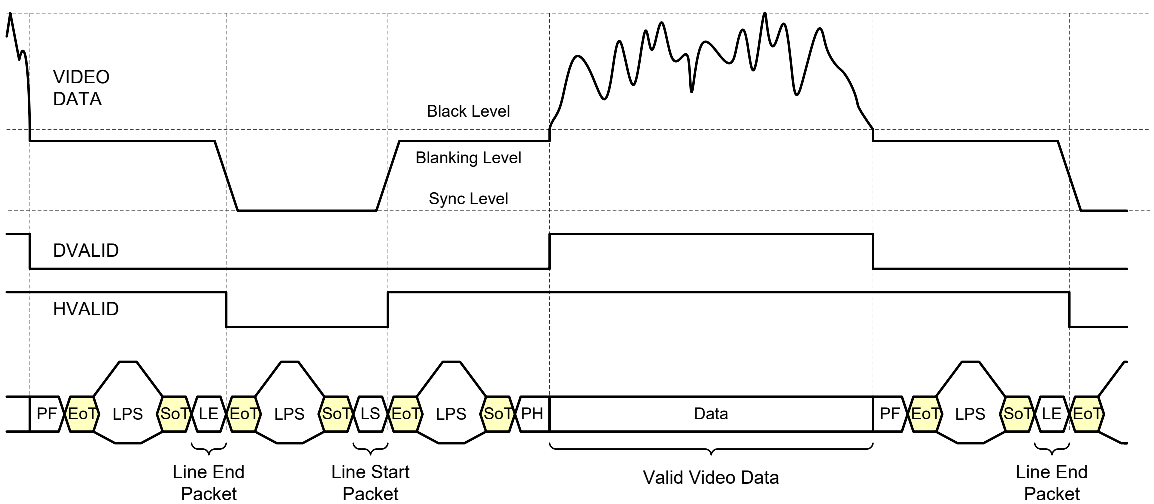


Figure 76 Horizontal Sync Example

9.11 Latency Reduction and Transport Efficiency (LRTE)

Latency Reduction and Transport Efficiency (LRTE) is an optional CSI-2 feature that facilitates optimal transport, in order to support a number of emerging imaging applications.

LRTE has two parts, further detailed in this Section:

- Interpacket Latency Reduction (ILR)
- Enhanced Transport Efficiency

9.11.1 Interpacket Latency Reduction (ILR)

As per ***[MIPI01]*** for the D-PHY physical layer option, and ***[MIPI02]*** for the C-PHY physical layer option, CSI-2 Short Packets and Long Packets are separated by EoT, LPS, and SoT packet delimiters. Advanced imaging applications, PDAF (Phase Detection Auto Focus), Sensor Aggregation, and Machine Vision can substantially benefit from the effective speed increases produced by reducing the overhead of these delimiters.

~~Interpacket~~As shown in ***Figure 77***, interpacket latency reduction ~~replaces~~may be used to replace legacy EoT, LPS, and SoT packet delimiters with a more Efficient Packet Delimiter (EPD) signaling mechanism that avoids the need for HS-LPS-HS transitions. An EPD consists of PHY layer and/or protocol layer elements. The PHY-generated EPD element is referred to as "Packet Delimiter Quick" (PDQ). Protocol-generated EPD elements are called Spacers and may optionally precede PDQs.

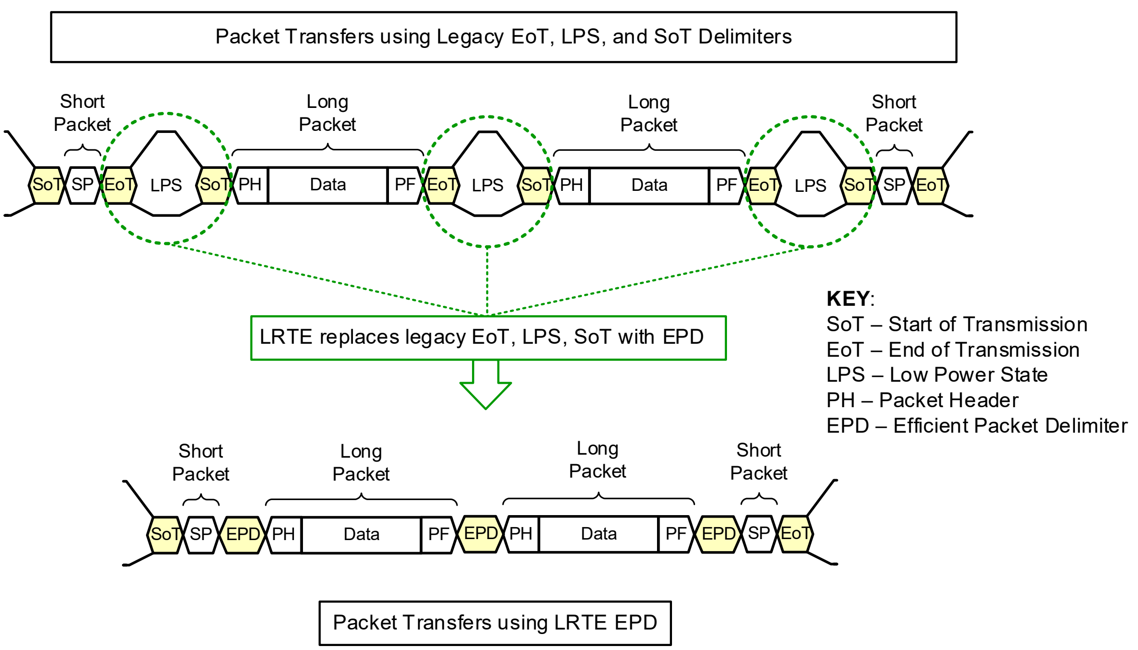


Figure 77 Interpacket Latency Reduction Using LRTE EPD

As shown in ***Figure 77***, LRTE requires an EPD to be inserted between adjacent CSI-2 packets during PHY high-speed signaling, but does not permit an EPD to be inserted after a CSI-2 packet just prior to PHY EoT. However, as described later in this section, it is possible under certain conditions to insert Spacers, but without PHY-generated PDQ signaling, after a CSI-2 packet just prior to PHY EoT.

9.11.1.1 EPD for C-PHY Physical Layer Option

The EPD for the C-PHY physical layer option ~~uses~~consists of one or more instances of the PHY-generated and PHY-consumed 7-UI Sync Word for the Packet Delimiter Quick (PDQ) signaling~~.~~, optionally preceded by CSI-2 protocol-generated and protocol-consumed Spacer Words. The PDQ is generated and consumed by the transmitter and receiver physical layers, respectively, and as a result serves as a robust CSI-2 packet delimiter. An image sensor should reuse "TxSendSyncHS" at the PPI in order to generate the PDQ control code by the C-PHY transmitter. Upon reception of the PDQ control code by the C-PHY receiver, an application processor should reuse "RxSyncHS" at the PPI in order to notify the CSI-2 protocol layer. The duration of the 7-UI PDQ control code is directly proportional to the C-PHY Symbol rate.

The EPD for C-PHY receivers can also benefit from optional CSI-2 protocol-generated and CSI-2 protocol-consumed Spacer insertion(s) prior to PDQ, because it facilitates optimal interpacket latency for imaging applications. The value of the Spacer Word for CSI-2 over C-PHY shall be 0xFFFF, and when present, Spacer Words shall be generated across all Lanes within a Link.

The image sensor (transmitter) shall include the following two 16-bit registers, in order to facilitate the optimal interpacket latency for imaging applications:

1. **TX_REG_CSI_EPD_EN_SSP** (EPD Enable and Short Packet Spacer) **Register**
   - The MS bit of this register shall be used to enable EPD with 7-UI PDQ (Sync Word) insertion between two CSI-2 packets and optional Spacer insertions for Short Packets and Long Packets.
     - 1'b0: C-PHY legacy EoT, LPS, SoT Packet Delimiter
     - 1'b1: Enable C-PHY EPD (Efficient Packet Delimiter)
   - ~~The~~If C-PHY EPD is enabled, the remaining 15 bits of this register (bits [14:0]) shall ~~be used to generate~~ specify the minimum number (up to 32,767) of Spacer Word insertions per Lane following CSI-2 Short Packets.
2. **TX_REG_CSI_EPD_OP_SLP** (Long Packet Spacer) **Register**
   - The MS bit of this register is reserved for future use.
   - ~~The~~If C-PHY EPD is enabled, the remaining 15 bits of this register (bits [14:0]) shall ~~be used to generate~~ specify the minimum number (up to 32,767) of Spacer Word insertions per Lane following CSI-2 Long Packets.

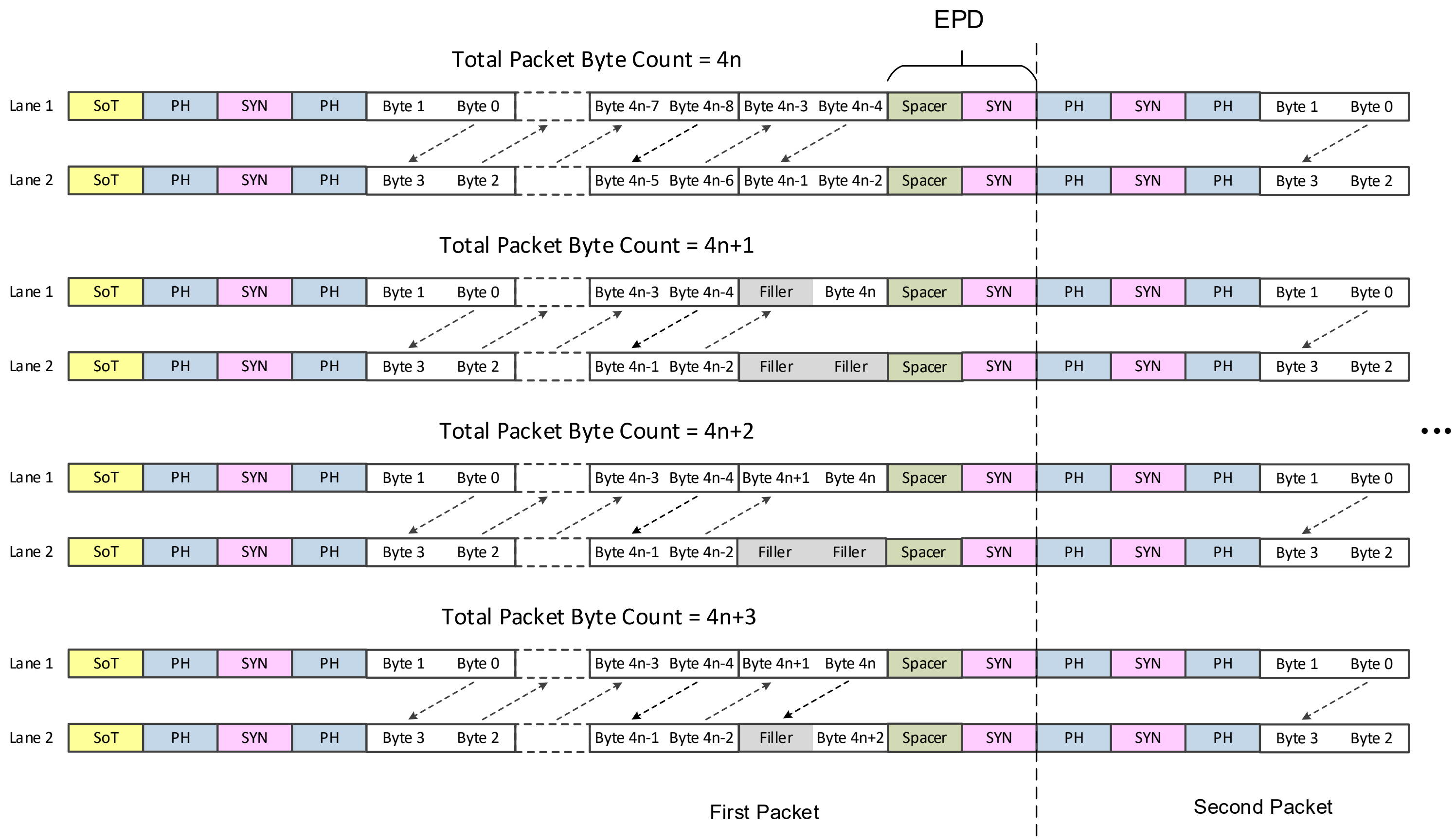
If the C-PHY EPD is enabled, then the following applies to the fifteen least significant bits of both EPD registers:

- A register value of 15'd0 ~~produces no Spacer generation (~~generates zero or more Spacers~~ inserted)~~.
- A register value of 15'd5 generates ~~five~~at least 5 Spacers, resulting in a minimum duration of 5 x 7 UI.
- The maximum register value of 15'd32,767 generates at least 32,767 Spacers, resulting in a minimum duration of 32,767 x 7 UI.

The transmitter shall support at least one non-zero value of the Spacer insertion count field in each of the **TX_REG_CSI_EPD_EN_SSP** and **TX_REG_CSI_EPD_OP_SLP** registers.

Spacer Words without PDQ signaling may be inserted after CSI-2 packets just prior to C-PHY EoT only if C-PHY EPD is enabled and bit 7 of the **TX_REG_CSI_EPD_MISC_OPTIONS** register is set to 1; see ***Table 16***. If this register bit is not implemented by an image sensor, its contents shall be treated as 0 by this specification. The minimum number of Spacer Word insertions just prior to C-PHY EoT is determined by the fifteen least significant bits of the **TX_REG_CSI_EPD_EN_SSP** and **TX_REG_CSI_EPD_OP_SLP** registers.

Note that C-PHY EPDs and Spacer Words without PDQ signaling are completely compatible with C-PHY ALP Mode high speed burst transmissions as described in ***[MIPI02]***.



KEY:

SoT – Start of Transmission

EoT – End of Transmission

EPD – Efficient Packet Delimiter contains optional Spacer word insertion followed by a mandatory PDQ (Sync Word). An EPD consisting of single Spacer followed by one PDQ shown for illustration.

SYN – Sync Word

PH – Packet Header

Figure 78 LRTE Efficient Packet Delimiter Example for CSI-2 Over C-PHY (2 Lanes)

9.11.1.2 EPD for D-PHY Physical Layer Option

There are two EPD options for CSI-2 over the D-PHY physical layer option, as detailed in the following sub-sections.

When EPD is enabled, CSI-2 over the D-PHY physical layer option shall align all Lanes corresponding to a Link using the minimum number of ~~filler~~Filler byte(s) for both options. The value of the ~~filler~~Filler byte shall be 0x00. The process of aligning Lanes within a Link through the use of ~~filler~~Filler bytes is similar to native EOT alignment of CSI-2 over C-PHY.

9.11.1.2.1 D-PHY EPD Option 1

~~The EPD for the~~ D~~-~~-PHY ~~v2.~~EPD Option 1 ~~physical layer option uses~~ consists of PHY-generated and PHY-consumed D-PHY HS-Idle ~~for the~~ Packet Delimiter Quick (PDQ) signaling, ~~with optional~~optionally preceded by CSI-2 protocol-generated and protocol-consumed Filler bytes (as needed) plus zero or more Spacer ~~Byte insertions prior to PDQ.~~bytes. The value of the Spacer ~~Byte~~byte for CSI-2 over D-PHY shall be 0xFF, and when present, Spacer ~~Bytes~~bytes shall be generated across all Lanes within a Link. The PDQ is generated and consumed by the transmitter and receiver physical layers, respectively, and as a result serves as a robust CSI-2 packet delimiter. D-PHY receivers can benefit from protocol-generated and protocol-consumed Spacer(s), because additional clock cycles might be needed to flush the payload content through the pipelines before the forwarded clock is disabled for PDQ signaling. Note that D-PHY HS-Idle is not supported by ALP mode in ***[MIPI01]***.

Under D-PHY Option 1, an EPD may not be inserted after a CSI-2 packet just prior to D-PHY EoT, but Spacer Bytes without PDQ signaling may be inserted after such packets if bit 7 of the **TX_REG_CSI_EPD_MISC_OPTIONS** register is 1. The minimum number of Spacer byte insertions just prior to D-PHY EoT is determined by the fifteen least significant bits of the **TX_REG_CSI_EPD_EN_SSP** and **TX_REG_CSI_EPD_OP_SLP** registers. See ***Table 17***.

The image sensor should use “TxHSIdleClkHS” at the PPI in order to generate the PDQ sequence by the D-PHY transmitter. Upon reception of the PDQ sequence by the D-PHY receiver, an application processor should use “RXSyncHS” at the PPI to notify the CSI-2 protocol layer. Additionally, “RxClkActiveHS” may also be used to provide an advance indication of the EPD.

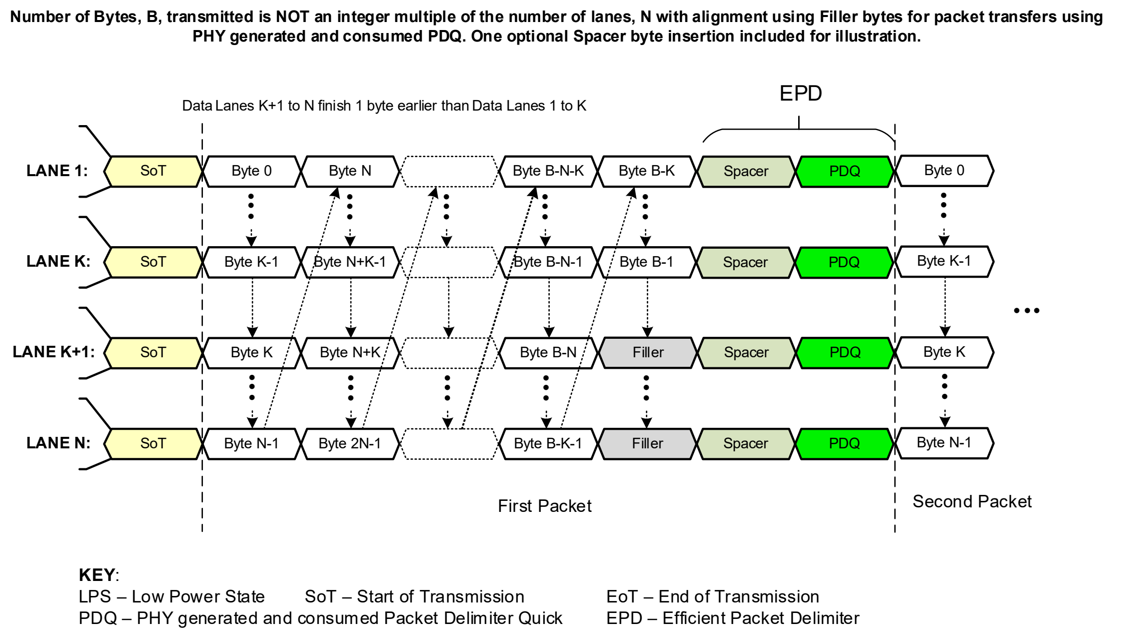


Figure 79 Example of LRTE EPD for CSI-2 Over D-PHY – Option 1

9.11.1.2.2 D-PHY EPD Option 2

D-PHY EPD Option 2 is limited to ~~optional~~the insertion of CSI-2 protocol-generated and CSI-2 protocol-consumed ~~Spacers~~Filler bytes (as needed) plus zero or more Spacer bytes for use between multiple back-to-back packet transfers within the same D-PHY high-speed burst transfer (i.e., there is no use of PHY-generated and PHY-consumed PDQ). Option 2 is primarily intended for use with ~~legacy~~ D-PHYs ~~not~~ supporting legacy LP or LVLP mode that don't support Option 1~~.~~; however, it may also be used with ALP Mode as described in ***[MIPI01]***. Depending on the use case (i.e., the sizes and number of CSI-2 packets being concatenated), the lack of D-PHY-generated and D-PHY-consumed ~~PDQ~~ packet delimiters could compromise CSI-2 link integrity. Option 2 is not intended to completely ~~replace the standard~~eliminate D-PHY~~-based LPS~~ LP, LVLP, or ALP Mode packet delimiters ~~provided by legacy D-PHYs~~. It is also recommended that one or more Spacers be included following a Short Packet or a Long Packet when using D-PHY EPD Option 2.

D-PHY EPD Option 2 may also be applied to packets transmitted using C-PHY or D-PHY Escape Mode LPDT in connection with the Unified Serial Link (USL) feature described in ***Section 9.12***.

Under D-PHY Option 2, an EPD (i.e., one or more Spacers) shall not be inserted immediately after the last CSI-2 short or long packet in any high-speed burst or LPDT payload, including after the EoTp short packet described in ***Section 9.11.1.2.5***.

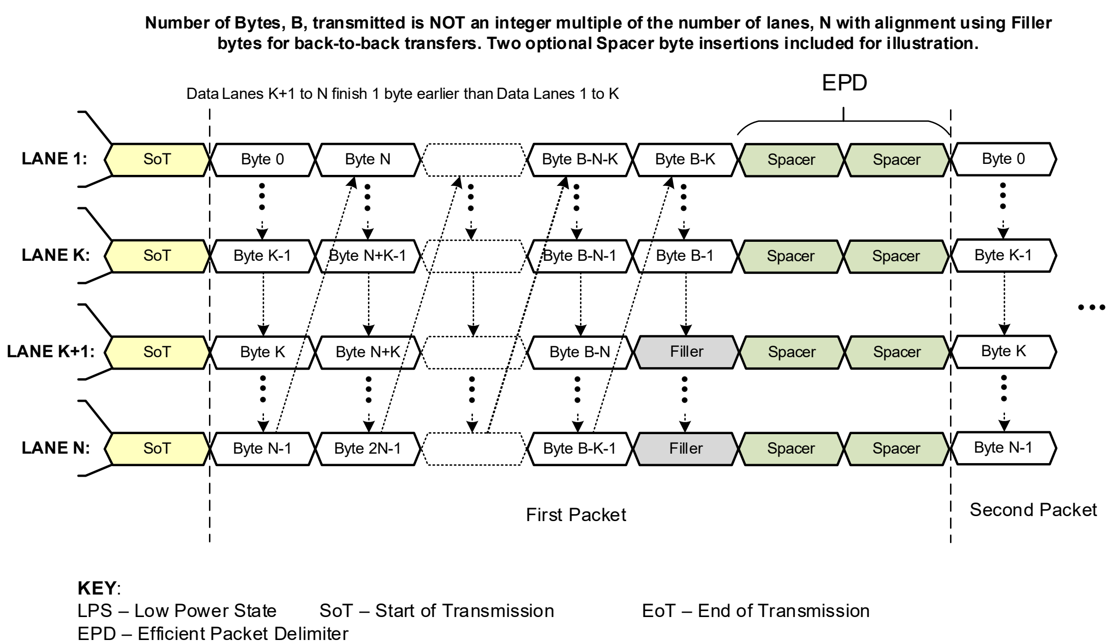


Figure 80 Example of LRTE EPD for CSI-2 Over D-PHY – Option 2

9.11.1.2.3 D-PHY EPD Specifications (for EPD Options 1 and 2)

The image sensor (transmitter) shall include the following two 16-bit registers, in order to facilitate the optimal interpacket latency for imaging applications:

1. **TX_REG_CSI_EPD_EN_SSP** (EPD Enable and Short Packet Spacer) **Register**
   - The MS bit of this register shall be used to enable EPD insertion between two CSI-2 packets.
     - 1'b0: D-PHY legacy EoT, LPS, SoT Packet Delimiter
     - 1'b1: Enable D-PHY EPD (Efficient Packet Delimiter)
   - ***Variable-length Spacer insertions following Short Packets:***
     If D-PHY EPD is enabled~~, then the remaining fifteen bits~~ and either Option 1 is selected (i.e., bit 15 of ~~this~~ register ~~(~~**TX_REG_CSI_EPD_OP_SLP** is 0) or Option 2 is selected with bit 5 or bit 4 of register **TX_REG_CSI_EPD_MISC_OPTIONS** in ***Table 17*** set to 1, then bits [14:0~~]) shall be used to generate~~] of register **TX_REG_CSI_EPD_EN_SSP** shall specify the minimum number (up to 32,767) of Spacer insertions per Lane following CSI-2 Short Packets. ~~These Spacer insertions for CSI-2 Short Packets apply~~The number of Spacers actually inserted per Lane may vary from one Short Packet to ~~both~~another. For D~~-~~-PHY EPD ~~options~~Option 2, both the contents of register **TX_REG_CSI_EPD_EN_SSP** and the actual number of Spacers inserted per Lane shall be multiples of the value selected in bits [5:4] of register **TX_REG_CSI_EPD_MISC_OPTIONS**.
   - ***Fixed-length Spacer Insertions following Short Packets:***
     If D-PHY EPD is enabled, and Option 2 is selected (i.e., bit 15 of register **TX_REG_CSI_EPD_OP_SLP** is 1) with bit 5 and bit 4 of register **TX_REG_CSI_EPD_MISC_OPTIONS** set to 0, then bits [14:0] of register **TX_REG_CSI_EPD_EN_SSP** shall specify the exact number (up to 32,767) of Spacer insertions per Lane following CSI-2 Short Packets. The number of Spacers inserted shall not vary from one Short Packet to another.
2. **TX_REG_CSI_EPD_OP_SLP** (EPD Option and Long Packet Spacer) **Register**
   - The MS bit of this register shall be used to select the D-PHY EPD option.
     - 1'b0: D-PHY EPD Option 1
     - 1'b1: D-PHY EPD Option 2
   - ***Variable-length Spacer insertions following Long Packets:***
     If D~~-~~-PHY EPD is enabled~~, then the remaining fifteen bits~~ and either Option 1 is selected (i.e., bit 15 of ~~this~~ register ~~(~~**TX_REG_CSI_EPD_OP_SLP** is 0) or Option 2 is selected with bit 5 or bit 4 of register **TX_REG_CSI_EPD_MISC_OPTIONS** set to 1, then bits [14:0~~]) shall be used to generate~~] of register **TX_REG_CSI_EPD_OP_SLP** shall specify the minimum number (up to 32,767 ~~optional~~) of Spacer insertions per Lane following CSI-2 Long Packets. ~~These Spacer insertions for CSI-2 Long Packets~~The number of Spacers actually inserted per Lane may vary from one Long Packet to another. For D-PHY EPD Option 2, both the contents of register **TX_REG_CSI_EPD_EN_SLP** and the actual number of Spacers inserted per Lane shall be multiples of the value selected in bits [5:4] of register **TX_REG_CSI_EPD_MISC_OPTIONS**.
   - ***Fixed-length Spacer insertions following Long Packets:***
     If D-PHY EPD is enabled, and Option 2 is selected (i.e., bit 15 of register **TX_REG_CSI_EPD_OP_SLP** is 1), with bit 5 and bit 4 of register **TX_REG_CSI_EPD_MISC_OPTIONS** set to 0, then bits [14:0] of register **TX_REG_CSI_EPD_OP_SLP** shall specify the exact number (up to 32,767) of Spacer insertions per Lane following CSI-2 Long Packets. The number of Spacers inserted shall not vary from one Long Packet to another.

~~•~~ The following examples apply to ~~both D-PHY EPD options.~~

~~The following applies to~~ the least significant fifteen bits of the two EPD registers:

- ***For variable-length Spacer insertions:***
  - A register value of 15’d0 ~~produces no Spacer generation (~~generates zero or more Spacers ~~inserted).~~.
  - A register value of 15’d5 generates at least 5 Spacers.
  - ~~The maximum~~A register value of 15’d32,767 generates at least 32,767 Spacers.
- ***For fixed-length Spacer insertions:***
  - A register value of 15’d0 generates no Spacers.
  - A register value of 15’d5 generates exactly 5 Spacers.
  - A register value of 15’32,767 generates exactly 32,767 Spacers.

The transmitter shall support at least one non-zero value of the Spacer insertion count field in each of the **TX_REG_CSI_EPD_EN_SSP** and **TX_REG_CSI_EPD_OP_SLP** registers. The duration of the PDQ sequence is directly proportional to the D-PHY Link rate, and is configured using ~~register~~the HS-Idle timing parameters defined in ***[MIPI01]*** for the D-PHY physical layer option.

For D-PHY EPD, the **TX_REG_CSI_EPD_MISC_OPTIONS** register is required for image sensors (transmitters) supporting the insertion of Spacers-without-PDQ under Option 1 or the insertion of EoTp (see ***Section 9.11.1.2.5***) or a variable number of Spacer bytes under Option 2. If this register is not implemented, then its value shall be treated as zero by this specification.

Note that registers **TX_REG_CSI_EPD_EN_SSP**, **TX_REG_CSI_EPD_OP_SLP**, and **TX_REG_CSI_EPD_MISC_OPTIONS** are not intended to control image sensor LRTE when applied to USL packets transmitted using Escape Mode LPDT; see ***Section 9.12***.

9.11.1.2.4 Robust Variable-Length Spacer Detection under D-PHY EPD Option 2 (Informative)

CSI-2 transmitters inserting a variable number of Spacer bytes per Lane between packets under D-PHY EPD Option 2 require CSI-2 receivers to examine, rather than simply count, potential Spacer bytes in order not to confuse them with packet header bytes. Since Spacer bytes are required to be distributed across all data Lanes beginning with Lane 1, CSI-2 receivers may detect them by scanning for bytes with the value 0xFF between packets only on Lane 1. However, truly reliable detection also requires these bytes to be error-free because a bit error in an intended Spacer byte (with value 0xFF) on Lane 1 can cause it to appear as a packet header Data Identifier byte. Conversely, a bit error in an intended packet header Data Identifier byte can cause it to appear as a Spacer byte.

If Lane-merged groups of four sequential Spacer bytes are processed as potential 32-bit packet headers by a CSI-2 receiver, then the results of the ECC calculation can be used to detect and correct errors in the Spacer bytes just as it does in packet header bytes. This is possible because the value 0x3F in the least significant six bits of each transmitted group of four Spacer bytes also happens to be the 6-bit ECC of the value 0x3FFFFFF in the most significant 26 bits.

Spacer byte insertion and detection schemes leveraging the latter principle may vary, depending upon the total number of data Lanes (N) in the link. Requiring the CSI-2 transmitter to insert Spacers in multiples of M = LCM(N,4) / N bytes per Lane, where LCM is the least common multiple function, always guarantees that the CSI-2 receiver will observe an integer multiple of four Spacer bytes between packets. As shown in ***Table 15***, only values of M equal to 1, 2, and 4 are possible and programmable on the CSI-2 transmitter using bits 5:4 of the **TX_REG_CSI_EPD_MISC_OPTIONS** register shown in ***Table 17***.

Table 15 Minimum Spacer Bytes per Lane for ECC Calculation

Number of Data Lanes (N)	Minimum Spacer Bytes per Lane M = LCM(N, 4) / N
1 + 4n	4
2 + 4n	2
3 + 4n	4
4 + 4n	1
Note: *n = 0, 1, 2, …*	

Note that the CSI-2 receiver only needs to check the data integrity of one out of every M potential Spacer bytes on Lane 1; i.e., once the first byte in a group of M bytes on Lane 1 has been confirmed as a Spacer byte, then the remaining M-1 bytes can be safely ignored by the CSI-2 receiver because it knows in advance that Spacer bytes are being inserted in groups of M. ***See Figure 81.***

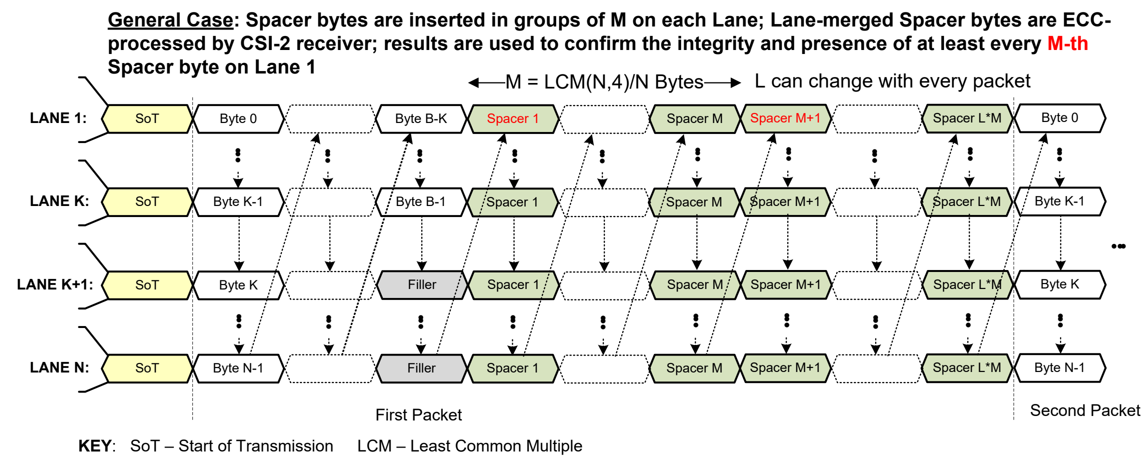


Figure 81 Enabling Robust Spacer Byte Detection: General Case

However, for N > 4, it is possible to program the CSI-2 transmitter to always insert an arbitrary number of Spacer bytes per Lane (i.e., to set M = 1) if the CSI-2 receiver examines bytes from the first four Lanes and, upon confirming a Spacer byte in Lane 1, ignores bytes from the remaining Lanes. See ***Figure 82***.

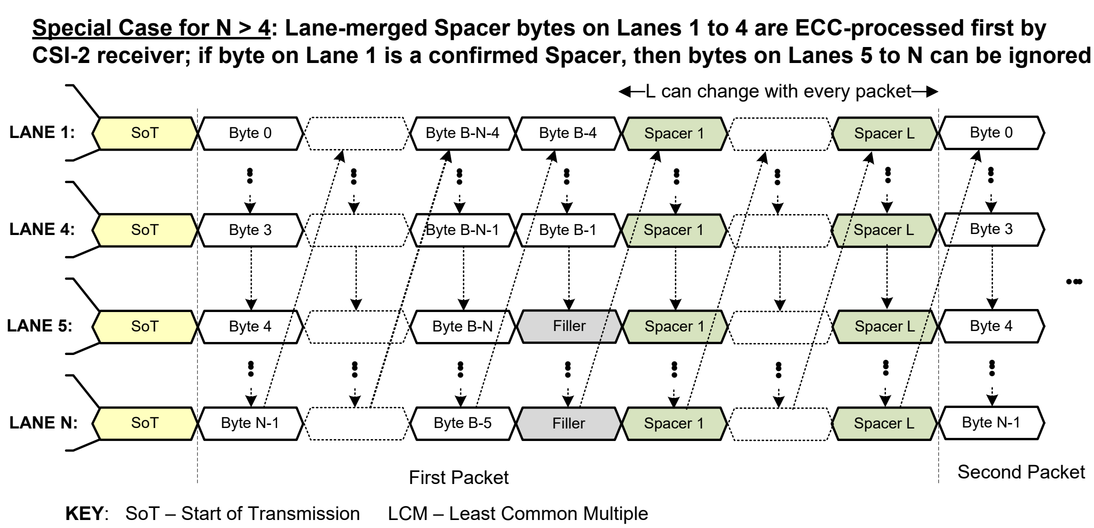


Figure 82 Enabling Robust Spacer Byte Detection: Special Case

9.11.1.2.5 End-of-Transmission Short Packet (EoTp)

When multiple CSI-2 packets are transmitted in a single D-PHY high-speed (HS) burst payload using D-PHY EPD Option 2, proper operation requires the host to be able to reliably detect the last CSI-2 packet in the burst under all circumstances. In many implementations, this requires the CSI-2 host protocol receiver to perform additional End-of-Transmission (EoT) processing on HS trailer and other bits passed to it from the D-PHY physical layer receiver.

Such EoT processing can be even more complex if HS trailer bits are followed by a small but potentially unknown number of bits with indeterminate values sampled, for instance, during the D-PHY HS to LP or LVLP voltage transition.

For D-PHY EPD Option 2, the End-of-Transmission short packet (EoTp) removes the need for the CSI-2 protocol receiver to perform EoT processing by unambiguously signaling the last CSI-2 packet in a D-PHY high-speed burst payload.

EoTp has the following short packet field definitions:

- DT shall be set to 0x04.
- All VC, VCX, and WC bits shall be set to zero.

Other rules pertaining to EoTp are as follows:

- EoTp generation or detection is mandatory for all devices conforming to this version of the CSI-2 specification that also support D-PHY EPD Option 2 for HS transmissions. EoTp shall not be used in conjunction with C-PHY EPD, D-PHY EPD Option 1, or packet transmissions using Escape Mode LPDT (see ***Section 9.12***).
- Devices conforming to CSI-2 specification v2.1 or earlier do not support EoTp. In order to ensure interoperability with earlier devices, EoTp-supporting devices shall provide a means to enable or disable EoTp generation or detection; for image sensors, this capability shall be supplied via bit 6 of the **TX_REG_CSI_EPD_MISC_OPTIONS** register shown in ***Table 17***. This permits the EoTp feature to be effectively disabled by the system designer whenever a device on either side of the Link does not support EoTp.
- When the EoTp feature is enabled, exactly one EoTp shall be present in every high-speed burst payload as the last CSI-2 packet following all other short and/or long packets, including payloads with only one CSI-2 short or long packet in addition to the EoTp short packet itself.
- Spacers are not permitted after an EoTp because this packet is always immediately followed by D-PHY EoT, and never by another CSI-2 packet.
- The contents of EoTp VC, VCX, and WC fields shall be ignored by CSI-2 protocol receivers.

See ***Figure 83*** for EoTp usage examples.

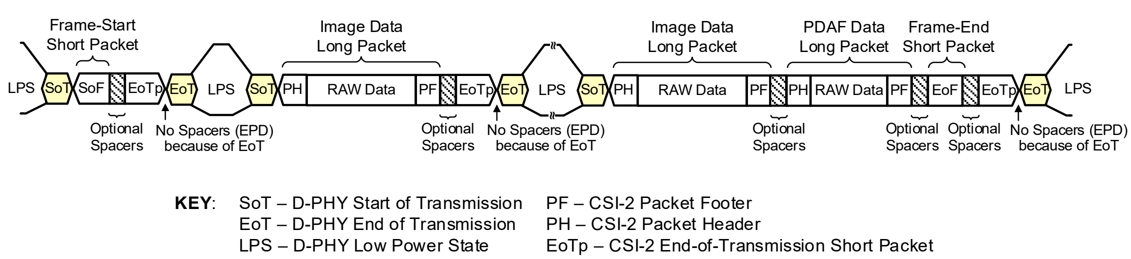
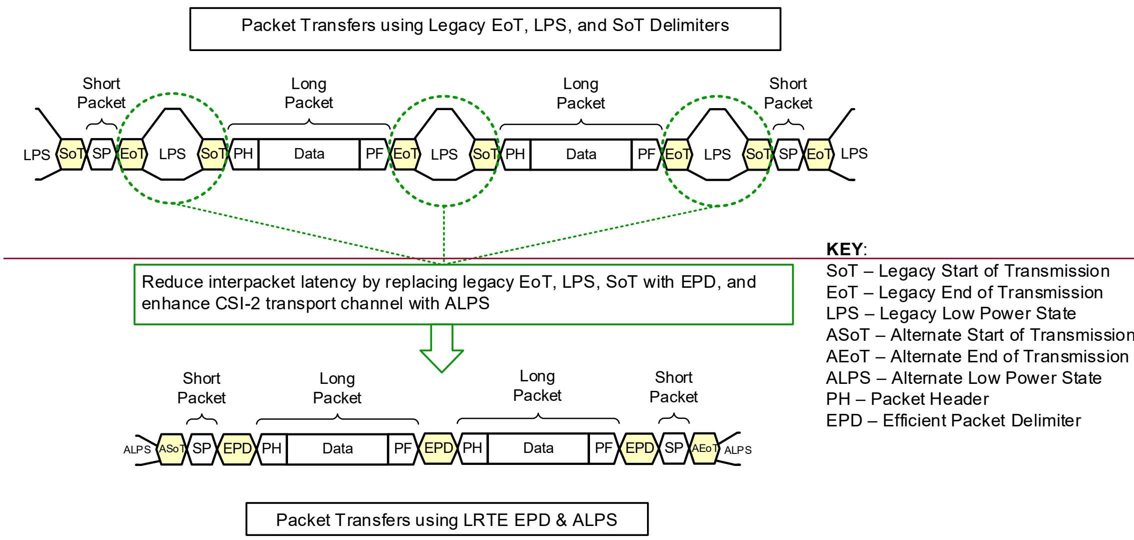


Figure 83 EoTp Usage Examples

9.11.2 Using ILR and Enhanced Transport Efficiency Together

EPD ~~and ALPS, the two LRTE provisions referred to in *Section 7*,~~ may be used together with LVLP or ALP Mode signaling in many imaging applications in order to benefit from CSI-2 ILR and enhanced channel transport.



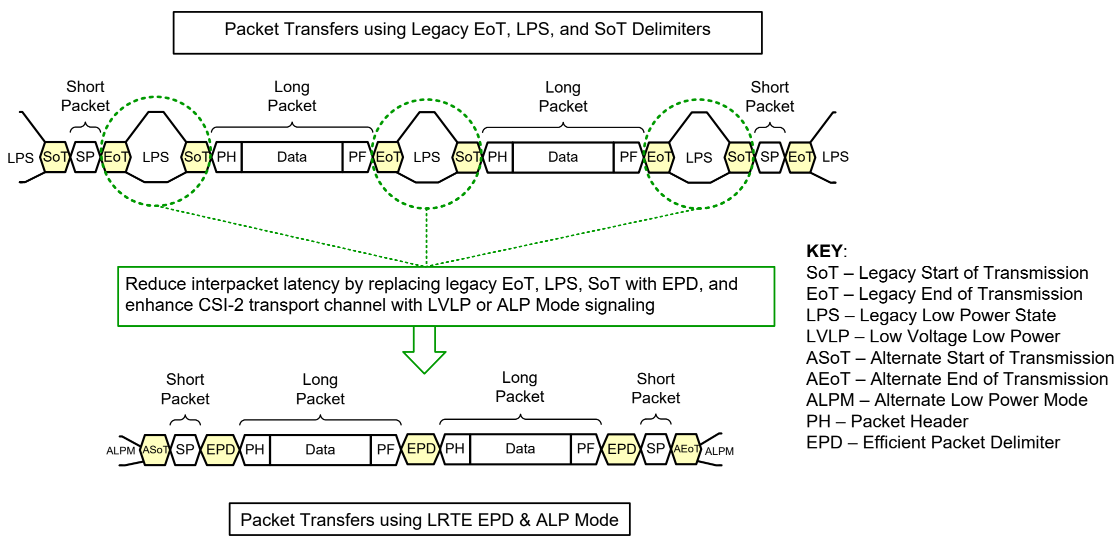


Figure 84 Using EPD ~~and ALPS Together~~with LVLP or ALP Mode Signaling

9.11.3 LRTE Register Tables

The CSI-2 over C-PHY Spacer Words and the CSI-2 over D-PHY Spacer Bytes shall be generated across all Lanes within a Link as specified in ***Table ~~15~~16*** and ***Table ~~16~~17***.

Table 16 LRTE Transmitter Registers for CSI-2 Over C-PHY

Transmitter Register		**Description**
TX_REG_CSI_EPD_EN_SSP [15:0]		Write-only. Required.
Bit [15]: Enable or disable Efficient Packet Delimiter using PHY-generated and PHY-consumed PDQ with optional minimum Spacer Insertion(s)	**Value 1'b0:** Disable Efficient Packet Delimiter **Value 1'b1:** Enable Efficient Packet Delimiter	CSI-2 over C-PHY EPD operation uses PHY-generated and PHY-consumed PDQ (7-UI Sync Word). Optional minimum Spacers may be Inserted for Short Packets and Long Packets. See ***Figure 78***.
Bits [14:0]: EPD Short Packet Spacers	The minimum number of Spacer Words per Lane following a Short packet. **Examples:** **Value 15'd0:** ~~No~~ Zero or more Spacer Words ~~…~~ … **Value 15'd7:** ~~Seven~~At least 7 Spacer Words ~~…~~ … **Value 15'd32767:** At least 32,767 Spacer Words	The Short Packet Spacers insertions are enabled by the C-PHY EPD (TX_REG_CSI_EPD_EN_SSP[15]). ~~The Short Packet Spacers may range from 0 to 32,767 Words.~~
TX_REG_CSI_EPD_OP_SLP [15:0]		Write-only. Required
Bit [15]: Reserved	Reserved	Reserved for future use
Bits [14:0]: EPD Long Packet Spacers	The minimum number of Spacer Words per Lane following a Long packet. **Examples:** **Value 15'd0:** ~~No~~ Zero or more Spacer Words ~~…~~ … **Value 15'd7:** ~~Seven~~At least 7 Spacer Words ~~…~~ … **Value 15'd32767:** At least 32,767 Spacer Words	The Long Packet Spacers insertions are enabled by the C-PHY EPD (TX_REG_CSI_EPD_EN_SSP[15~~])~~ ~~The Long Packet Spacers may range from 0 to 32,767 Words.~~]).
TX_REG_CSI_EPD_MISC_OPTIONS [7:0]		Write-only. Optional.

Bit [7]: Enable insertion of Spacers-without-PDQ after CSI-2 packets just prior to C-PHY EoT.	**Value 1'b0:** Disable Spacers without-PDQ (default) **Value 1'b1:** Enable Spacers without-PDQ	Required for image sensors supporting C-PHY EPD with Spacers-without-PDQ.
Bits [6:0]: Reserved	–	–

Table 17 LRTE Transmitter Registers for CSI-2 Over D-PHY

Transmitter Register		Description
TX_REG_CSI_EDP_EN_SSP [15:0]		Write-only. Required
Bit [15]: Enable or disable EPD (Efficient Packet Delimiter) operation	**Value 1'b0:** Disable EPD **Value 1'b1:** Enable EPD	See ***Figure 79***. If EPD is enabled, the D-PHY EPD Options are determined by **TX_REG_CSI_EPD_OP_SLP[15]**.
Bits [14:0]: EPD Short Packet Spacers	**For D-PHY EPD Option 1**~~:~~ **-or-** **For Option 2 with Variable Spacers:** Minimum number of Spacer Bytes per Lane following a Short packet. ~~**For D-PHY EPD Option 2:** Fixed number of Spacer Bytes per Lane following a Short packet.~~ **Examples:** **Value 15'd0:** ~~No~~Zero or more Spacer Bytes ~~…~~ … **Value 15'd7:** ~~Seven~~At least 7 Spacer Bytes ~~…~~ … **Value 15'd32767:** At least 32,767 Spacer Bytes **Otherwise, for D-PHY EPD Option 2:** Fixed number of Spacer Bytes per Lane following a Short packet.	The Short Packet Spacers insertions are enabled by the D-PHY EPD (**TX_REG_CSI_EPD_EN_SSP[15]**). ~~The Short Packet Spacers may range from 0 to 32,767 Bytes.~~ See ***Figure 79*** and ***Figure 80***.
TX_REG_CSI_EPD_OP_SLP [15:0]		Write-only. Required.
Bit [15]: D-PHY EPD Option Select	**Value 1'b0:** D-PHY EPD Option 1 **Value 1'b1:** D-PHY EPD Option 2	**D-PHY EPD Option 1:** CSI-2 over D-PHY EPD operation using PHY-generated and PHY-consumed PDQ (using forwarded clock signaling) and optional Spacer Insertion(s). See ***Figure 79***. **D-PHY EPD Option 2:** CSI-2 over D-PHY EPD operation using optional Spacer Insertion(s). See ***Figure 80***.

Transmitter Register		Description
Bits [14:0]: Long Packet Spacers	**For D-PHY EPD Option 1** **-or-** **For Option 2 with Variable Spacers:** Minimum number of Spacer Bytes per Lane following a Long packet. ~~**For D-PHY EPD Option 2:** Fixed number of Spacer Bytes per Lane following a Long packet.~~ **Examples:** **Value 15'd0:** ~~No~~Zero or more Spacer Bytes ~~…~~ … **Value 15'd7:** ~~Seven~~At least 7 Spacer Bytes ~~…~~ … **Value 15'd32767:** At least 32,767 Spacer Bytes **Otherwise, for D-PHY EPD Option 2:** Fixed number of Spacer Bytes per Lane following a Long packet.	The Long Packet Spacers insertions are enabled by the D-PHY EPD (**TX_REG_CSI_EPD_EN_SSP[15]**). ~~The Long Packet Spacers may range from 0 to 32,767 Bytes.~~ See ***Figure 79*** and ***Figure 80***.

Transmitter Register		Description
TX_REG_CSI_EPD_MISC_OPTIONS [7:0]		Write-only. Optional.
Bit [7]: For D-PHY EPD Option 1: Enable insertion of Spacers-without-PDQ after CSI-2 packets just prior to D-PHY EoT	**Value 1'b0:** Disable Spacers without-PDQ (default) **Value 1'b1:** Enable Spacers-without-PDQ	Required for image sensors supporting D-PHY EPD Option 1 with Spacers-without-PDQ.
Bit [6]: For D-PHY EPD Option 2: Enable EoTp	**Value 1'b0:** Disable EoTp (default) **Value 1'b1:** Enable EoTp	Required for image sensors supporting D-PHY EPD Option 2 with EoTp short packets.
Bit [5:4]: For D-PHY EPD Option 2: Enable variable-length Spacer insertions with a multiple of n Spacer bytes per Lane	**Value 2'b00:** Enable fixed-length Spacers (default) **Value 2'b01:** Enable variable-length Spacers with n = 1 **Value 2'b10:** Enable variable-length Spacers with n = 2 **Value 2'b11:** Enable variable-length Spacers with n = 4	Required for image sensors supporting D-PHY EPD Option 2 with variable-length Spacers.
Bits [3:0]: Reserved	–	–

9.12 Unified Serial Link (USL)

Unified Serial Link (USL, see ***Figure 85***) is an optional CSI-2 feature that reduces the number of interface wires and helps to natively support longer reach.

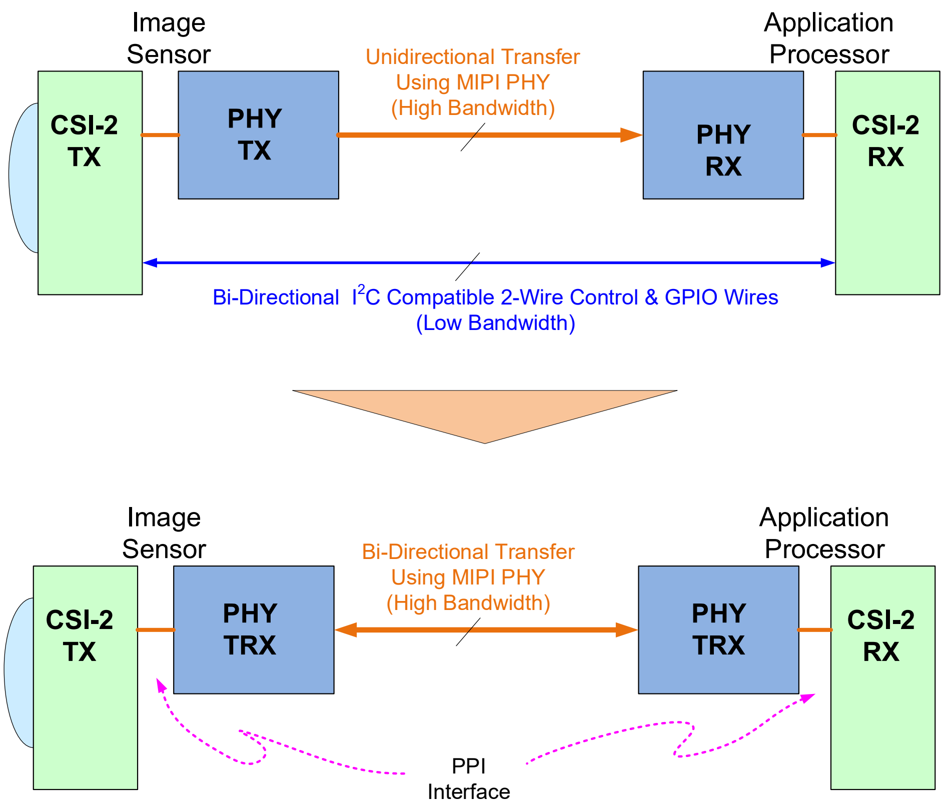
USL builds upon the benefits provided by the LRTE features (***Section 9.11***). USL alleviates the need to use any additional I^{2}C, I3C, and/or SPI interconnect for the Camera Command Interface (CCI), or GPIO wires for camera module control signaling. This is accomplished by using CSI-2 encapsulation with the Bus Turn Around (BTA) capabilities of the natively supported C-PHY 2.0 (or beyond) and D-PHY v2.5 (or beyond) transport layer options.

MIPI PHY bandwidths are many orders of magnitude greater than those provided by the I^{2}C-compatible 2-wire bi-directional control bus. Moreover, there are natural blanking intervals (i.e., idle cycles) between transferring horizontal rows (i.e., horizontal blanking), and between transferring frames (i.e., vertical blanking), that can be used to update the image sensor shadow registers.

In this Section:

- The term **SNS** refers to an image sensor, or an image sensor module comprising a CMOS image sensor plus additional complementary devices (i.e., non-imaging devices).
- The term **APP** refers to an SoC application processor (AP) containing any combination of computer vision engine(s) and/or image processing unit(s), or to a host processor.

The reverse link throughput from an APP to a SNS does not require high bandwidth, which substantially relaxes timing constraints and margins for receiver implementations on the SNS transceiver. Mapping all CSI-2 transactions via MIPI C-PHY/D-PHY can reduce the number of wires, support long reach, help secure channel implementations, and reduce engineering development costs.



1587

Figure 85 USL System Diagram

9.12.1 USL Technical Overview

Lane Usage: The vast majority of imaging applications using USL are expected to be mapped to a conduit with a single bi-directional lane (Lane 1). However, if a conduit requires multiple Lanes, then the first Lane (Lane 1) shall be bi-directional, and the remaining Lanes shall be uni-directional and configured as TX for image sensors. In multi-Lane conduits, all Lanes within a link are utilized for USL_FWD Mode operations, and only the first Lane (Lane 1) is utilized for USL_REV Mode operations. Transceiver functionality is always limited to one Lane (Lane 1). USL physical layer requirements are detailed in ***Section 7.3***.

USL Commands and Transactions: The 0x38 PH Data Type (see ***Table 10***) and the CSI-2 Long Packet Format shall be used for USL command operations and transactions. A “USL packet” is any long packet with Data Type 0x38.

Virtual Channels: In order to facilitate sensor aggregation on system platforms, the SNS shall support USL packets with Virtual Channel Identifiers ranging from 0 to 15 for D-PHY, and 0 to 31 for C-PHY. CSI-2 Frame Start and Frame End short packets shall not be transmitted for any Virtual Channel Identifiers used exclusively in USL packets. Virtual Channel Identifiers used in USL packets are permitted to be used in CSI-2 packets with Data Type codes other than 0x38 (i.e., non-USL packets). However, a pair of CSI-2 Frame Start and Frame End short packets is required to enclose all non-USL packets for each shared Virtual Channel Identifier within each image frame.

9.12.2 USL Command Payload Constructs

All USL transport operations shall use the existing CSI-2 Long Packet (LgP) constructs. The encapsulated USL payload fields (Size_Bytes, Slave_Address, Sub_Address, Write_data, Read_data, USL_CTL, TSEQ) shall map LSB data to Bit0 (see ***Figure 3***). All multi-byte USL payload fields shall be transmitted least significant byte first.

USL Commands are used to map register Read/Write requests from the APP to the SNS, and read completions from the SNS to the APP, using the CSI-2 LgP. The LgP Packet Header Data Type field shall be set to the value 0x38 when an APP or SNS generates USL Command register R/W requests or completions, respectively. For all C-PHY or D-PHY high-speed (HS) Mode transmissions, the encapsulated R/W requests are mapped into the LgP Packet Data Field Application Specific Payload of USL packets, per ***Figure 52*** for the D-PHY physical layer option, and per ***Figure 53*** for the C-PHY physical layer option. The Long Packet Padding and Filler insertions shall be preserved for the C/D-PHYs as defined in ***Section 9.1***.

As described in ***Section 7.3***, all USL implementations shall support PHY LP or LVLP Mode signaling, and should support ALP Mode signaling. USL systems are normally configured prior to power-up to support one of these signaling Modes under either D-PHY or C-PHY.

If USL is configured to use C-PHY or D-PHY LP/LVLP Mode, then all USL packets transmitted using forward or reverse direction Escape Mode LPDT have the same format as USL packets transmitted using D-PHY HS Mode; each byte is also transmitted least significant bit first. The APP shall be capable of receiving USL packets both as HS Mode transmissions distributed over all active Lanes, and as Escape Mode LPDT Transmissions driven only over Lane 1.

During USL_REV Mode, the SNS shall support buffering for a minimum of 32 register read requests (single and contiguous) from an APP. During USL_REV Mode, the SNS shall support a minimum of 64 register write requests (single and contiguous) with a minimum of 1024 bits of write data from an APP.

If USL is configured to use C-PHY or D-PHY ALP Mode, then while in USL_REV Mode, the APP may concatenate multiple USL packets into a single HS burst transmission over Lane 1 using C-PHY EPD or D-PHY EPD Option 2, respectively, provided the applicable LRTE EPD features are supported (see ***Section 9.11***). SNS HS Mode receiver LRTE capabilities may be understood from the SNS datasheet, or discovered in some other fashion. Similarly, while in USL_FWD Mode, the SNS may concatenate multiple USL and/or non-USL packets into a single HS burst transmission distributed over all active Lanes using one of the latter EPD alternatives.

If USL is configured to use C-PHY or D-PHY LP/LVLP Mode, then while in USL_FWD Mode, the SNS may concatenate multiple USL and/or non-USL packets into a single HS burst transmission distributed over all active Lanes using any supported C-PHY or D-PHY LRTE EPD feature (including D-PHY EPD Option 1). While in either USL_FWD or USL_REV Mode, LRTE D-PHY EPD Option 2 may be used to concatenate multiple USL packets transmitted using Escape Mode LPDT, but only with zero or more fixed length Spacers between packets and without the insertion of EoTp short packets. SNS Spacer generation for USL packets transmitted using LPDT may be controlled by the APP using the register in ***Table 18***. SNS LP/LVLP Mode receiver LRTE capabilities may be understood from the SNS datasheet, or discovered in some other fashion.

The existing LgP 16-bit Checksum shall be used to preserve transport integrity for all USL transitions. USL Command transactions do not require the legacy CCI “S” (Start), “P” (Stop), and “A” (Acks), because the LgP transport handles these functions.

A 16-bit Size_Bytes field contains the number of sequential bytes of data to write or read. A Read_Data field contains the byte based read data.

A Write_Data field contains the byte based write data.

A 7-bit Slave_Address field contains the device address where the commands are to be send or to be received. For example, CCI (I^2C) Slave Address e.g. 0x6C was used to communicate with an image sensor and similarly with USL the same e.g. 0x6C would apply. This field is transmitted as the most significant 7 bits of a byte whose LSB is analogous to the CCI R/W bit.

A 16-bit Sub_Address field is used for pointing at a register inside the slave device. Product-specific imaging systems may use an 8-bit and/or 16-bit Sub_Address on an as-needed basis, since Sub_Address is device-specific and is known at platform level. Note that systems using a single USL link to communicate with multiple devices, e.g. via local I^2C bus, may require using both 8-bit and 16-bit indexes, depending on the devices.

An 8-bit USL Control (USL_CTL) (***Table 19***) is used to ensure transport integrity with guaranteed delivery of commands from the APP to the SNS using ACK, and to improve transport efficiency with support for contiguous R/W operations often used for imaging and vision firmware uploads from APP to SNS.

A 16-bit Transaction Sequence (TSEQ) field contains a unique non-zero USL command identification number generated by the SNS and APP. The SNS and APP generate and clear the Transaction Sequence field upon successful reception of a USL Packet (as detailed in sections below).

Table 18 Image Sensor LPDT LRTE Control Register

Register Name	Type	RW	Comment
SNS_USL_LPDT_LRTE	8-bit unsigned integer	RW	**Bit 7** 1: Enable image sensor LRTE for USL packets transmitted using Escape Mode LPDT **Bits 6-0** If LRTE is enabled, specifies the fixed number of Spacers inserted between all USL packets (0 to 127)

Table 19 USL Transport Control (USL_CTL) Bit Description

USL_CTL[7:0]	Name	Description	Initiator
Bits [1:0]	**ACK_NAK_INT Generation**	**Values:** **2'b01:** ACK generation. SNS transmits the TSEQ of the last successful reception an USL command. **2'b10:** NAK generation. SNS transmits the TSEQ of the R/W command resulting in an illegal or invalid operation. **2'b00:** Neither ACK nor NAK generation (i.e., Read completions) **2'b11:** In-band interrupt	SNS
Bit [2]	**Force Command**	**Values:** **1'b0:** The requested command from APP shall not be executed by the SNS if a prior command request was NAK'ed during USL_REV_Mode. **1'b1:** Force command operation even if a prior command was NAK'ed during USL_REV_mode.	APP
Bit [3]	**Sequential R/W Enable**	**Values:** **1'b1:** USL command includes sequential R/W request or response. The requested size (in bytes) shall be determined from Size_Bytes[15:0] field. **1'b0:** USL command includes single R/W request or response.	APP
Bit [4]	**Initiate BTA**	**Values:** **1'b1:** Command bit used to turn around the bus. Generated by the Initiator. **1'b0:** NOP	APP during USL_REV Mode, SNS during USL_FWD Mode
Bits [7:5]	Reserved for future use	Reserved for future use	–

Note:

The USL_CTL[7:5] bits are reserved for future expansion.

9.12.3 USL Operation Procedures

For simplification, the following examples show:

- A 16-bit `Sub_Address[15:0]`
- A 16-bit Transaction Sequence (`TSEQ`) containing a unique non-zero USL command identification number generated by the APP

9.12.3.1 APP Initiated USL Transactions

This example procedure illustrates the APP initiating four valid USL Command transactions (USL_REV Mode).

1. ACK Generation

TSEQ is used by the system to ensure guaranteed delivery of USL commands. An APP shall include a 16-bit register to store the last successful TSEQ received from the SNS during USL_FWD Mode. Upon entering USL_REV Mode, the APP shall generate ACK twice immediately using the following format:

- LgP Packet Header Data ID = 0x38
- LgP Packet Data format for ACK generation:

```
{USL_CTL[7:0], TSEQ[15:0]}
```

2. Register Write Request with Write Data

- LgP Packet Header Data ID = `0x38`
- LgP Packet Data format for all writes:

```
{USL_CTL[7:0], TSEQ[15:0], Size_Bytes[15:0],
 Slave_Address[7:1],[W=0],
 Sub_Address[15:0],
 Write_Data [16'd Size_Bytes-1:0]}
```

3. Register Read Request

- LgP Packet Header Data ID = `0x38`
- LgP Packet Data format for all read requests:

```
{USL_CTL[7:0], TSEQ[15:0], Size_Bytes[15:0],
 Slave_Address[7:1],[R=1],
 Sub_Address[15:0]}
```

4. Initiate BTA

Upon completing the R/W register commands, the APP shall generate the Initiate BTA packet twice to switch the link from USL_REV to USL_FWD mode.

The Initiate BTA bit in the USL_CTL shall be set to 1'b1.

- LgP Packet Header Data ID = `0x38`
- LgP Packet Data format for initializing BTA, and switch from USL_REV to USL_FWD:

```
{USL_CTL[7:0], TSEQ[15:0]}
```

9.12.3.2 SNS Initiated USL Transactions

This example procedure illustrates the SNS initiating five valid USL Command transactions (USL_FWD Mode).

1. **NAK Generation**

   If an Image Sensor (SNS) receives an invalid or an illegal USL Command request from the Application Processor (APP), then the SNS shall generate a Negative Acknowledgement (NAK). By default, the SNS shall not execute any following R/W USL command requests from the APP after a NAK during an USL_REV_Mode, unless the USL_CTL Force Command bit is enabled by the APP. The SNS shall generate negative acknowledgement (NAK) for the first illegal or failed R/W request from an APP. The SNS may optionally generate additional NAKs resulting from "Force Command" requests. The NAK shall be transmitted twice to the APP immediately upon switching to USL_FWD_Mode using the following format:

   - LgP Packet Header Data ID = 0x38
   - LgP Packet Data format for NAK generation:

     `{USL_CTL[7:0], TSEQ[15:0]}`

2. **ACK Generation**

   TSEQ is used by the product imaging system to ensure guaranteed delivery of R/W commands from APP to SNS. An Image Sensor shall include a 16-bit register to store the last successful TSEQ received from the APP during USL_REV Mode. Upon entering USL_FWD Mode, the SNS shall generate ACK twice immediately following any NAK generation(s) using the following format:

   - LgP Packet Header Data ID = 0x38
   - LgP Packet Data format for ACK generation:

     `{USL_CTL[7:0], TSEQ[15:0]}`

3. **Register Read Completion**

   - LgP Packet Header Data ID = 0x38
   - LgP Packet Data format for all read completions:

     `{USL_CTL[7:0], TSEQ[15:0], Size_Bytes[15:0],`
     `Read_Data [16'd Size_Bytes-1:0]}`

4. **Interrupt Generation**

   Upon completing ACK/NAK generations, the SNS may generate in-band interrupt using USL_CTL[1:0] in the USL_FWD mode. It is strongly recommended for the SNS to prioritize and generate the interrupt notification at the earliest opportunity.

   The following format shall be used to also include optional information pertaining to the interrupt:

   - LgP Packet Header Data ID = 0x38
   - LgP Packet Data format for In-Band Interrupt generation:

     `{USL_CTL[7:0], Slave_Address[15:0], Interrupt_Information[15:0]}`

5. **Initiate BTA**

   The SNS shall generate the Initiate BTA packet twice prior to switching the link from USL_FWD to USL_REV mode. The Initiate BTA bit in the USL_CTL shall be set to 1'b1. The TSEQ shall be the 16-bit value from REG_USL_ACK_TSEQ.

   - LgP Packet Header Data ID = 0x38
   - LgP Packet Data format for initializing BTA, and switch from USL_REV to USL_FWD:

     `{USL_CTL[7:0], TSEQ[15:0]}`

9.12.4 Monitoring USL Command Transport Integrity

This section presents a stepwise procedure for monitoring the integrity of the USL Command Transport, using TSEQ and the two SNS registers defined in ***Table 20***.

1. [System Reset] [Power Cycle]

- The SNS shall reset registers REG_USL_ACK_TSEQ[15:0] and REG_USL_NAK_TSEQ[15:0] to the value 16’d0. The APP shall reset internal register APP_REG_USL_ACK_TSEQ[15:0].

2. [USL_REV Mode]

- Upon entering USL_FWD Mode, APP shall generate ACK twice using the 16-bit TSEQ from internal register APP_REG_USL_ACK_TSEQ[15:0].
- The APP shall generate a 16-bit, non-zero TSEQ value that increments with each USL Command R/W request it sends to the SNS.
- The SNS shall store the TSEQ of the last successful USL command into register REG_USL_TSEQ_ACK[15:0].
- The SNS shall store the TSEQ of the first illegal USL command into register REG_USL_TSEQ_NAK[15:0].

3. [USL_REV Mode Exit]

- The APP shall reset internal register APP_REG_USL_ACK_TSEQ[15:0] to the value 16’d0.

4. [USL_FWD Mode]

- Upon entering USL_FWD Mode, if any illegal operation was encountered in the prior USL_REV Mode, the SNS shall generate NAK twice using the 16-bit TSEQ from register REG_USL_TSEQ_NAK[15:0].
- Next, the SNS shall generate ACK twice using the 16-bit TSEQ from register REG_USL_TSEQ_ACK[15:0].
- An ACK with TSEQ value of 16’d0 shall be generated by the SNS if no USL commands were successfully received from the APP during USL_REV Mode.

Note:

SNS shall reset the internal state(s) used to block execution of subsequent command operations after a NAK.

5. [USL_FWD Mode Exit]

The SNS shall reset registers REG_USL_ACK_TSEQ[15:0] and REG_USL_NAK_TSEQ[15:0] to the value 16’d0.

Table 20 USL Transport Integrity ACK and NAK Registers with TSEQ

SNS USL Transport Integrity Registers	Description
REG_USL_ACK_TSEQ[15:0]	Required. Write / Read. See Above.
REG_USL_NAK_TSEQ[15:0]	Required. Write / Read. See Above.

9.12.5 USL Powerup / Reset, SNS Configuration, and Mode Switching

This section details the various stages of USL operations. Note that the current TX shall always initiate the BTA when switching USL modes.

9.12.5.1 USL Link Modes

The USL link is in **USL Reverse Mode** (USL_REV) when:

- SNS is configured as RX
- APP is configured as TX
- The channel is established to transfer payloads from APP to SNS

The USL link is in **USL Forward Mode** (USL_FWD) when:

- SNS is configured as TX
- APP is configured as RX
- The channel is established to transfer payloads from SNS to APP

9.12.5.2 USL Power-up / Reset

The link comes up in USL_FWD Mode after power-up or reset:

- The SNS shall initially configure each PHY Lane (including clock Lane, if present) as a transmitter (TX).
- The APP shall initially configure each PHY Lane (including clock Lane, if present) as a receiver (RX).
- The SNS and APP shall then initialize their Lane 1 PHYs following the appropriate PHY-defined procedure; all other Lanes are unidirectional and should remain uninitialized until needed.
- If USL is configured to use D-PHY ALP Mode, then the clock Lane shall also be initialized and started following its initialization in order to facilitate ALP Mode fast BTA and high-speed bidirectional data transfers over data Lane 1; see ***Section 9.12.5.6*** for additional guidance.
- If USL is configured to use D-PHY LP/LVLP Mode, then initialization and start-up of the clock Lane may be delayed until the SNS is first required to transmit packets to the APP using HS Mode. Note that in this case, all USL packet transmissions from the APP to the SNS over data Lane 1 use Escape Mode LPDT and don't require the clock Lane to be running.
- Once the SNS has completed internal power-up / reset calibration, the SNS shall initiate BTA on Lane 1 using the steps outlined in ***Section 9.12.3.2***. The SNS may optionally send the contents of TX_USL_SNS_BTA_ACK_TIMEOUT[15:0] using the read completion format from ***Section 9.12.3.2*** prior to initiating BTA.
- Upon completion of the BTA, the link is configured as USL_REV Mode to enable the APP to configure the SNS using Lane 1.
- During SNS configuration, the APP may select the total number of active Lanes in order to enable the correct number of unidirectional Lanes to be initialized and put into service when image streaming is started.

9.12.5.3 USL SNS Configuration

The APP may configure the SNS when the link is in USL_REV Mode using steps outlined in ***Section 9.12.3.1***.

- Once the APP has completed one or more SNS configuration operations, the APP shall initiate BTA using steps outlined in ***Section 9.12.3.1***.
- Upon completion of the BTA, the link is configured as USL_FWD Mode.

9.12.5.4 USL Mode Switching SNS Configuration

Upon entering USL_FWD Mode, the SNS generates the USL NAK (if needed) followed by the USL ACK using the steps outlined in ***Section 9.12.3.1***. The SNS generates the USL read completions as the content becomes available, and may be interleaved with non-USL payloads during USL_FWD Mode.

The SNS shall support the two 16-bit USL BTA Switch registers defined in ***Table 21*** and ***Table 22***. The APP shall configure these registers during USL_REV Mode.

The USL BTA switch may be initiated during vertical blanking for traditional photography and video applications, or after predefined LgPs (intra-frame) for more advanced vision applications. CSI-2 Imaging and Vision systems will require fast BTA durations mapped to the PHYs. ***Figure 86*** illustrates the USL_REV and USL_FWD State Diagram for both the APP and the SNS.

When a system is powered up, the SNS is configured as an RX (receiver) and the APP is configured as a TX (transmitter). Five USL modes are allowed for imaging applications, along with the transition arcs as defined in ***Figure 86***.

A USL SNS shall support the 16-bit Operational Register shown in ***Table 25***.

A USL SNS shall support one or more 16-bit GPIO Registers, per ***Table 26***.

Table 21 USL BTA Switch Registers

SNS USL BTA Registers		Description
TX_USL_REV_ENTRY [15:0]		Required. Write / Read. Enable USL_REV Mode Entry after the specified number of non-USL LgPs, non-USL Frames, or PPI Word/Byte clocks.
Bit [15:10]: **Select Mode Switch Triggers**	Bit[15]: **Clock Counter**	Increment Clock Counter using PPI Word/Byte clock in USL_FWD Mode. Switch to USL_REV mode when Clock Counter expires. Reinitialize the Clock Counter when exiting USL_FWD mode.
	Bit[14]: **LgP Counter**	Increment LgP Counter using non-USL LgPs in USL_FWD Mode. Switch to USL_REV mode when LgP Counter expires. Reinitialize the LgP Counter when exiting USL_FWD mode.
	Bit[13]: **Frame Counter**	Increment Frame Counter using non-USL FEs in USL_FWD Mode. Switch to USL_REV mode when Frame Counter expires. Reinitialize the Frame Counter and LgP Counter when exiting the USL_FWD mode.
	Bit[12]: **Chronological Timer**	The Chronological (duration in µs) Timer is initiated with the first non-USL transmission in USL_FWD mode. Switch to USL_REV mode once Chronological Duration timer expires and any inflight packet has completed transmission. Reinitialize the timer when exiting USL_FWD mode.
	Bit[11]: **Configure SNS**	Enable SNS to switch to REV_MODE immediately after the USL transmissions are completed (i.e., read completion, ACK, NAK). Non-USL (pixel data) transmissions are not allowed during the USL_FWD Mode.
	Bit[10]: **Smart SNS**	Enable SNS to switch to REV_MODE autonomously based on smart features. Smart SNS capability is optional for the SNS.
	Bit[9-0]: Reserved for future use	
TX_USL_Clock Counter [15:0]		Required. Write / Read. Counter used to trigger SNS switch from USL_FWD Mode to USL_REV Mode.
TX_USL_LGP Counter [15:0]		Required. Write / Read. Counter used to trigger SNS switch from USL_FWD Mode to USL_REV Mode.
TX_USL_Frame Counter [15:0]		Required. Write / Read. Counter used to trigger SNS switch from USL_FWD Mode to USL_REV Mode.

TX_USL_Chronological Timer [15:0]	Required. Write / Read. Counter used to trigger SNS switch from USL_FWD Mode to USL_REV Mode.

1826 **Table 22 Register TX_USL_REV_FWD_ENTRY**

SNS USL BTA Register		Description
TX_USL_FWD_ENTRY [15:0]		Required. Write / Read. Enable USL_FWD Mode Entry after the specified number of PPI Word/Byte clocks.
Bit [15]: **FWD_Switch_En**	**Value 1'b0:** Disable **Value 1'b1:** Initiate switch to USL_FWD Mode once the REV_MODE PPI Word / Byte clock counts match FWD_Counter [14:0]	**USL_REV Mode:** Upon completing the R/W requests, the APP shall initiate switching to USL_FWD mode by writing 1'b1 to FWD_Switch_En **USL_FWD Mode or SNS Reset:** The SNS shall reset FWD Switch_En bit by writing 1'b0.
Bits [14:0]: **FWD_Counter**	**Value 15'd0:** Initiate switch to USL_FWD mode immediately after APP writes 1'b1 to FWD_Switch_En. … **Value 15'd7:** Increment FWD_Counter using USL_REV Mode PPI Word / Byte clock when APP writes 1'b1 to USL_FWD Switch_En. Initiate switch to USL_FWD mode when FWD_Counter[14:0] = 15'd7. … **Value 15'd32767:** Increment FWD_Counter using USL_REV Mode PPI Word / Byte clock when APP writes 1'b1 to USL_FWD Switch_En. Initiate switch to USL_FWD mode when FWD_Counter[14:0] = 15'd32767.	**USL_REV Mode:** Increment FWD_Counter using the USL_REV PPI Byte / Word clock when APP writes 1'b1 to USL_FWD Switch_En. **USL_FWD Mode or SNS Reset:** The SNS may optionally reset the FWD_Counter by writing 15'd0.

1827

9.12.5.5 ALP Fast BTA Timeout Support

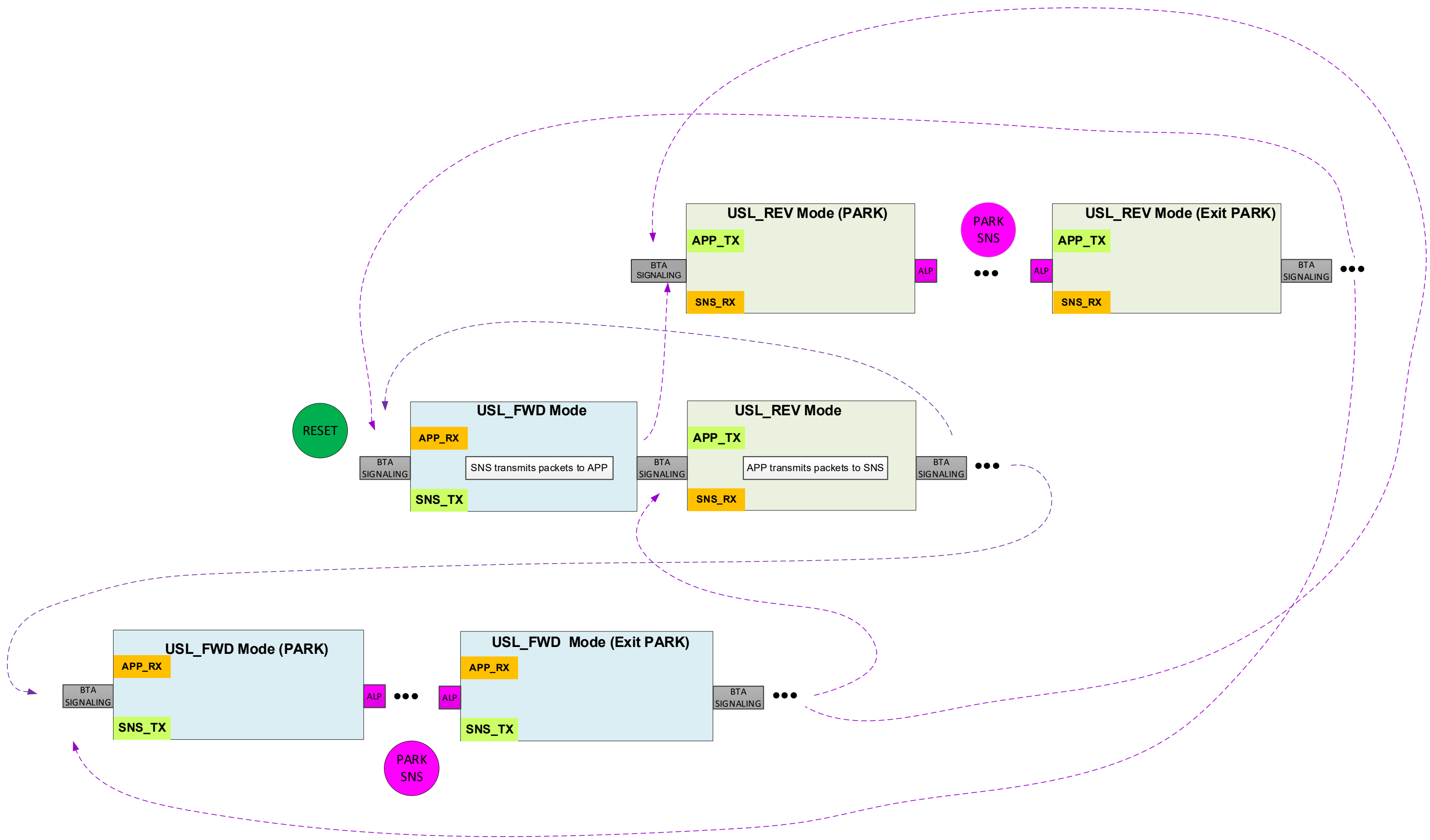
Since the target device PHY does not provide an acknowledgement electrical signaling upon receiving an "Initiate BTA" USL command request from an initiator, the following SNS timeout registers are utilized by the APP to alleviate potential deadlocks.

Table 23 Register TX_USL_SNS_BTA_ACK_TIMEOUT[15:0]

SNS USL BTA Register	Description
TX_USL_SNS_BTA_ACK_TIMEOUT[15:0]	Required. Read Only. Maximum time (in ns) required by SNS to send ACK in the USL_FWD Mode upon SNS receiving "Initiate BTA" USL command from APP in USL_REV Mode. Value of 16'd0 implies the timeout is disabled. Value of 16'd500 implies the SNS shall send ACK in the USL_FWD Mode within 500 ns upon reception of "Initiate BTA" USL command from APP in USL_REV Mode.

Table 24 Register TX_USL_APP_BTA_ACK_TIMEOUT[15:0]

SNS USL BTA Register	Description
TX_USL_APP_BTA_ACK_TIMEOUT[15:0]	Required. Write Only. Maximum time (in ns) required by APP to send ACK in the USL_REV Mode upon APP receiving "Initiate BTA" USL command from SNS in USL_FWD Mode. Value of 16'd0 implies the timeout is disabled. Value of 16'd500 implies the APP shall send ACK in the USL_REV Mode within 500 ns upon reception of "Initiate BTA" USL command from SNS in USL_FWD Mode.



1832

Figure 86 USL Modes Link Transitions

Table 25 USL Operation Registers

SNS USL Operational Register		**Description**
TX_USL_Operation [15:0]		Required. Write / Read. General purpose register mapped SNS operations
Bit [0]: **SNS Reset**	**Values:** **1'b0:** NOP **1'b1:** Reset SNS	In-band register mapped SNS reset
Bit [15:1]: **Reserved**	Reserved	Reserved for future use

Table 26 USL GPIO Registers

Bit [15:0]: **SNS USL GPIO Register0**		**Description**
TX_USL_GPIO [15:0]		Required. Write / Read. General purpose register mapped GPIO operations
Bit [0]: **GPIO_0 Configuration**	**Values:** **1'b0:** Low **1'b1:** High	In-band register mapped GPIO_0 configuration
…		
Bit [7]: **GPIO_7 Configuration**	**Values:** **1'b0:** Low **1'b1:** High	In-band register mapped GPIO_7 configuration
…		
Bit [15]: **GPIO_15 Configuration**	**Values:** **1'b0:** Low **1'b1:** High	In-band register mapped GPIO_15 configuration

9.12.5.6 USL Clock Lane Management Under D-PHY ALP Mode (Informative)

When USL is configured to use D-PHY ALP Mode as described in ***[MIPI01]***, a running high-speed clock Lane is required for any active data communications between SNS and APP. Such communications include the usual forward-direction SNS pixel streaming, as well as any bidirectional transactions on data Lane 1 related to USL packet transmissions (with DT code 0x38), or any low-level PHY fast BTA or ULPS entry commands initiated by either the SNS or APP. When USL is configured to use D-PHY LP or LVLP Mode, the clock Lane is only required to be running during SNS pixel streaming.

9.12.5.6.1 System Power-Up and/or Reset (Informative)

Following SNS ALP Mode TX and RX PHY initialization, the SNS will start up the clock Lane at some initial, implementation-dependent frequency prior to switching to USL_REV mode. For example, it may be advantageous to set this frequency equal to the SNS external reference clock frequency (or a submultiple thereof) since this avoids the need to start and lock a PLL, potentially saving hundreds of microseconds of start-up latency. Care must be taken to ensure that the selected clock Lane frequency is at least twice the minimum bit rate required by the D-PHY specification, since the D-PHY high-speed reverse-direction data transmissions used by USL occur at one-fourth the bit rate of forward-direction data transmissions. For example, a 2 MHz clock Lane frequency corresponds to a forward-direction bit rate of 4 Mbps and a reverse-direction bit rate of 1 Mbps.

Once the clock Lane is running, the SNS can use the USL protocol to switch to USL_REV mode in order to enable the APP to configure SNS CCI registers as needed, including the PLL control registers used for setting the clock Lane frequency required for image streaming. The last action taken by the APP will be to request the start of image streaming by writing to the appropriate CCI control register and then switching to USL_FWD mode; the SNS, in response, will stop the clock Lane, lock all PLLs to their configured frequencies, restart the clock Lane, and only then actually start image streaming.

9.12.5.6.2 Dynamic Clock Control (Informative)

As with legacy CSI-2 non-continuous clock mode, USL permits the clock Lane to be stopped during periods in which the system application either doesn't support or doesn't immediately anticipate data communications between SNS and APP.

Examples of such periods include:

- One or more of the "horizontal line blanking" (hblank) periods between image lines during image streaming (assuming such periods are sufficiently long enough to include the timing overhead entailed in stopping and then restarting the clock).
- All or part of the "vertical frame blanking" (vblank) period between image frames during image streaming.
- "Hard standby" periods during which image sensor power consumption is at a minimum and no CCI register accesses are possible. Hard standby entry and exit is typically controlled using a separate control signal (e.g., the XSHUTDOWN signal defined in ***[MIPI04]***).
- All or part of "soft standby" periods during which image streaming is temporarily halted to enable the APP to reconfigure CCI registers concerning fundamental SNS operating characteristics, such as output image resolution, pixel depth, frame rate, bit rate, active Lane count, etc.

Stopping and restarting the clock Lane may be performed by the SNS either automatically following conventions understood in advance by the APP, or in response to the APP triggering the SNS in an ad hoc manner. For example, when the clock Lane is running during USL_REV mode, the APP may command the SNS to stop the clock by writing to a special CCI control register on the SNS. Conversely, when the clock Lane is stopped during USL_REV mode (meaning no CCI register accesses are possible), the APP may request the SNS to restart the clock by transmitting a short D-PHY ALP Mode PHY-to-PHY Wake pulse to the SNS (as described in ***[MIPI01]***).

Note that changing the clock Lane frequency requires the SNS to stop the clock Lane, internally adjust the frequency (which may involve relocking a PLL), and then restart the clock Lane in accordance with the D-PHY specification. Needless to say, the latter actions can be collectively time consuming and are best avoided when switching from USL_FWD mode to USL_REV mode and then back again during relatively short time periods such as hblank. In other words, if the APP needs to access SNS CCI registers during hblank, then the ideal situation is one in which both the SNS and APP can support reverse-direction transmissions at one-fourth of the *full* bit rate used for streaming pixel data packets, thereby avoiding the need to change the clock Lane frequency twice during hblank.

Figure 87 illustrates examples of USL ALP Mode clock Lane management during the image streaming vblank period. Beginning at time “A” in the figure, the SNS automatically keeps the clock Lane running after transmitting the CSI-2 Frame End short packet and uses the USL protocol to enter USL_REV mode in order to enable the APP to start accessing SNS CCI registers. At this point, the APP may also wish to start an internal timer to warn it when the vblank period is about to end. At time “B”, when the APP is at least temporarily finished with CCI register accesses, the last access it performs is a write to the TX_USL_ALP_CTRL register (*Table 27*), for example, which commands the SNS to turn-off the clock Lane but also to expect a request to restart it at a later time. USL_REV mode is then maintained (with all D-PHY clock and data Lanes in the Stop state) until time “C” when the APP requests the clock Lane to be restarted by transmitting a short ALP Mode PHY-to-PHY Wake pulse to the SNS. In response, the SNS restarts the clock Lane and keeps it running while the APP performs more CCI accesses as needed. When finished at time “D”, the APP finally switches back to USL_FWD mode prior to the SNS having to transmit the Frame Start short packet at the beginning of the next image frame.

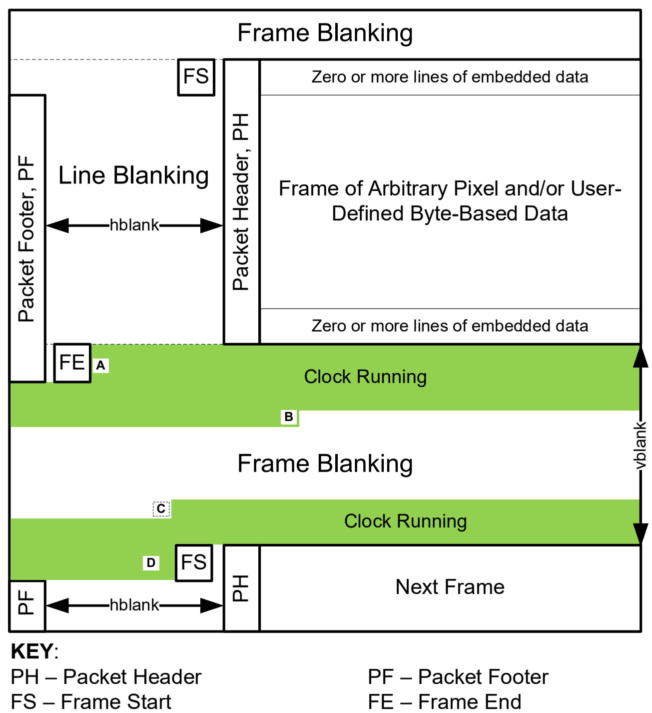


Figure 87 Examples of USL ALP Mode Clock Lane Management During Sensor Vblank

Table 27 USL Clock Lane Control Register

Register Name	**Type**	**RW**	**Comment**
TX_USL_ALP_CTRL	16-bit unsigned integer	RW	**Bit 0** 1: Shall trigger image sensor to pause the D-PHY clock Lane during ALP mode. The image sensor shall auto-clear the register after stopping the clock. **Other bits** Reserved for future use

9.12.5.7 USL Hard Standby Mode (Informative)

USL hard standby entry and exit may be controlled in essentially the same manner as with legacy non-USL image sensors. During hard standby mode, all Lanes (including the clock Lane, if applicable) are typically in the forward-direction ULPS state, and the APP cannot access any SNS CCI registers.

SNS entry into hard standby is usually triggered by a hardware input signal (e.g., XSHUTDOWN) which may be asserted asynchronously with respect to image streaming. Each Lane transitions to the forward-direction ULPS state more-or-less immediately; i.e., any in-progress image streaming simply terminates and no PHY ULPS entry command is transmitted. However, the APP normally puts the SNS into soft standby mode beforehand in order to cleanly stop image streaming and put the interface into the Stop state or ULPS. Lane 1 on both the SNS and APP should also be automatically switched to the forward direction when hard standby is triggered.

Exit from hard standby is triggered by the de-assertion of the same hardware input (e.g., XSHUTDOWN) used to trigger hard standby entry, causing each Lane to transition to the Stop state in accordance with applicable PHY initialization procedures in ***[MIPI01]*** and ***[MIPI02]***.

9.12.5.8 USL Soft Standby Mode and ULPS Entry/Exit (Informative)

Similar to legacy non-USL image sensors, USL supports SNS entry into soft standby mode by the APP writing to a CCI control register causing image streaming to be halted in an orderly manner. For USL, this CCI write operation must occur while in USL_REV mode during an hblank or vblank period. The APP then uses the USL protocol to switch back to USL_FWD mode, in order to enable the SNS to output all or part of the image frame that was in progress at the moment the control register was written, ending with all data Lanes in the Stop state (and the clock Lane still running in the D-PHY ALP Mode case). The SNS then switches to USL_REV mode to enable the APP to issue further commands to the SNS.

Once streaming is halted, the APP can choose different courses of action. For example, if performing a time-critical SNS mode change, the APP can then immediately update the required SNS CCI registers, concluding the process by writing to a CCI control register that requests the restart of image streaming, and then switching back to USL_FWD mode using the USL protocol. Once returned to USL_FWD mode, and prior to actually restarting image streaming, the SNS may have to disable, reconfigure, and relock one or more internal PLLs, possibly requiring the SNS to automatically stop and restart the clock Lane, if applicable.

Another possible course of action is for the APP to put the SNS into an extended sleep state while awaiting further commands from the APP. The preferred method for accomplishing this is for the APP to first transmit a PHY ULPS entry command to the SNS on Lane 1 followed by the SNS, in turn, transmitting the PHY ULPS entry command to the APP on all forward-direction data Lanes. This method is preferred because Lane 1 remains in USL_REV mode throughout ULPS, thereby enabling the APP to subsequently transmit ULPS wakeup signaling to the SNS over Lane 1 when needed; this is also the reason why “reverse direction ULPS” support is recommended for both D-PHY and C-PHY Lane 1 in ***Section 7.3***. With D-PHY ALP Mode, the SNS then stops the clock Lane and puts it into ULPS after all data Lanes have been put into ULPS. At this point, the SNS can internally power-down unnecessary circuitry while still retaining internal register states and remaining in USL_REV mode.

For D-PHY ALP mode, ULPS wakeup while in soft standby mode requires the APP to transmit a long ALP Wake pulse to the SNS as described in ***[MIPI01]***. Once the SNS starts receiving the latter pulse on data Lane 1 (as signaled by the PPI, for example), it can then start transmitting a long ALP Wake pulse to the APP on each unidirectional data Lane, resulting in a total round-trip wakeup latency which is about the same as the latency in either the forward or reverse direction. The SNS also wakes-up the clock Lane to the Stop state and then restarts it in order to enable the APP to access SNS CCI registers.

For C-PHY ALP mode, ULPS wakeup while in soft standby mode requires the APP to transmit an extended ALP-Pause Wake wire state to the SNS followed by an ALP “Stop” command as described in ***[MIPI02]***. At this point, the SNS can similarly signal ULPS wakeup on each unidirectional Lane. However, this results in a total round-trip wakeup latency which is about the twice the latency in either the forward or reverse direction. The impact of this can be reduced or eliminated by the APP performing more transactions (e.g., CCI register accesses) using Lane 1 while wakeup is in-progress on the other Lanes, effectively hiding the additional latency. Another possible solution is put either C-PHY Lane 1 or all the other Lanes into ULPS, but not both. For example, the APP could request ULPS by writing to a CCI control register using Lane 1; the SNS would then put all unidirectional Lanes into ULPS while leaving Lane 1 in the Stop state. Conversely, the APP could request ULPS by putting only Lane 1 into ULPS, with the SNS leaving all unidirectional Lanes in the Stop state.

~~9.12~~9.13 Data Scrambling

The purpose of Data Scrambling is to mitigate the effects of EMI and RF self-interference by spreading the information transmission energy of the Link over a possibly large frequency band, using a data randomization technique. The scrambling feature described in this Section is optional and normative: If a CSI-2 implementation includes support for scrambling, then the scrambling feature shall be implemented as described in this Section. The benefits of data scrambling are well-known, and it is strongly recommended to implement this data scrambling capability in order to minimize radiated emissions in the system.

Data Scrambling shall be applied on a per-Lane basis, as illustrated in ***Figure ~~82~~88***. Each output of the Lane Distribution Function shall be individually scrambled by a separate scrambling function dedicated to that Lane, before the Lane data is sent to the PHY function over the Tx PPI.

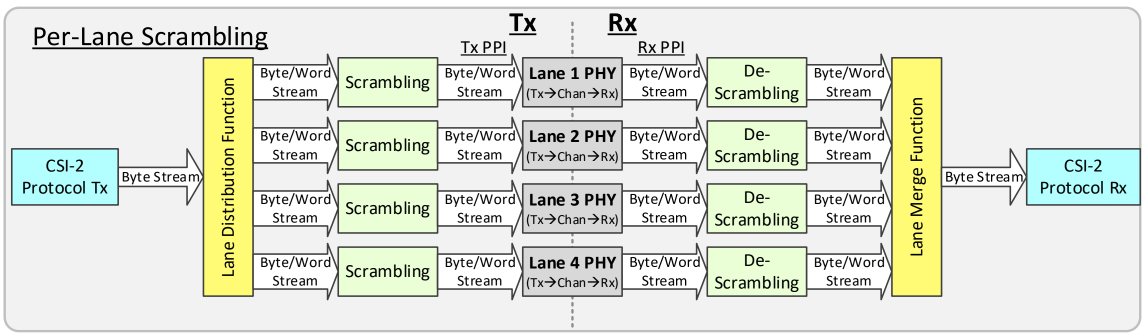


Figure 88 System Diagram Showing Per-Lane Scrambling

~~9.12.1~~9.13.1 CSI-2 Scrambling for D-PHY

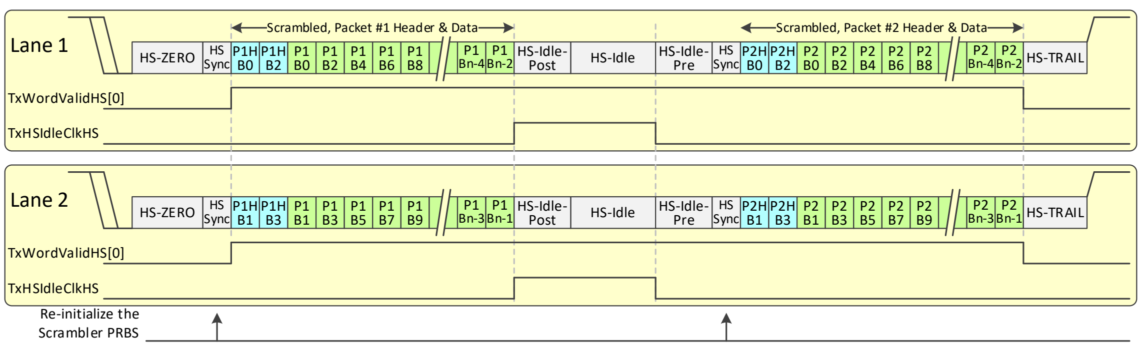
Figure ~~83~~89 shows the format of a burst transmission of two packets over two Lanes when the D-PHY physical layer is used. After the Start of Transmission, HS-ZERO and HS-SYNC are transmitted, the Packet Header and data payload are distributed across the two Lanes.

If the D-PHY physical layer is used, then the scrambler Linear Feedback Shift Register (LFSR) in each Lane shall be initialized with the Lane seed value under any of the following conditions:

1. At the beginning of the burst, which occurs immediately prior to the first byte transmitted following the HS-Sync that is generated by the D-PHY (applicable to both D-PHY EPD Option1 and Option 2).
2. Prior to the first byte transmitted following the HS-Sync that is generated whenever the optional D-PHY EPD Option 1 HS-Idle is transmitted.

The scrambler is not reinitialized between CSI-2 packets when using the optional D-PHY EPD Option 2.

When the scrambler is initialized, the LFSR shall be initialized using the sixteen-bit seed value assigned to each Lane.



Note: The Packet Footer at the end of every packet is scrambled.

Figure 89 Example of Data Bursts in Two Lanes Using the D-PHY Physical Layer

~~9.12.2~~9.13.2 CSI-2 Scrambling for C-PHY

Figure ~~84~~90 shows the format of a burst transmission of two packets over two Lanes when the C-PHY physical layer is used. After the Start of Transmission, Preamble, and Sync are transmitted, the Packet Header is replicated twice on each Lane, and data payloads of each packet are distributed across the two Lanes. If the C-PHY physical layer is used, then the scrambler LFSR in each Lane shall be initialized at the beginning of every Long Packet Header or Short Packet, using one of the sixteen-bit seed values assigned to each Lane. This initialization takes place each time the Sync Word is transmitted.

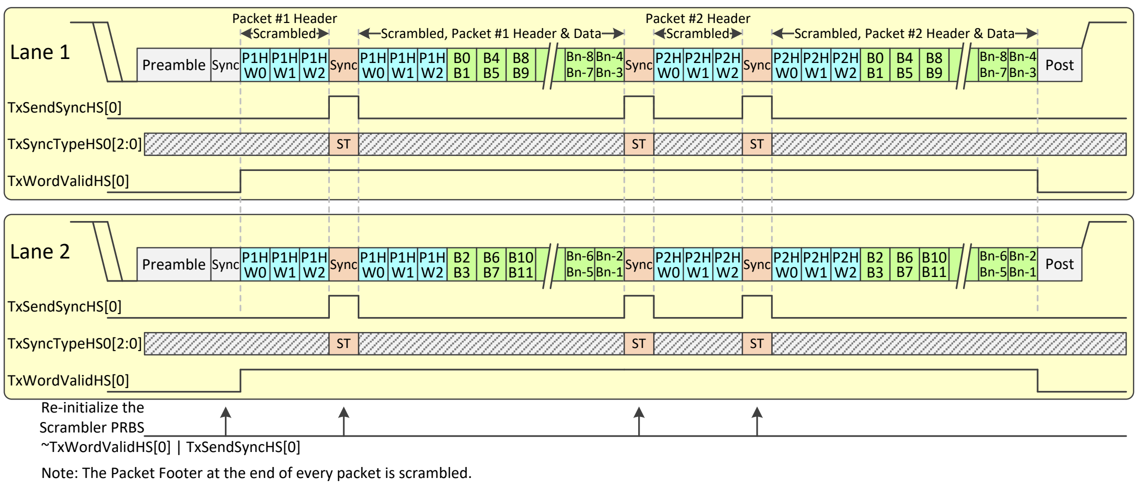


Figure 90 Example of Data Bursts in Two Lanes Using the C-PHY Physical Layer

In some cases, images may cause repetitive transmission of Long Packets having the same or similar Long Packet Header and the same pixel data (for example: all dark pixels, or all white pixels). If the scrambler is initialized with the same seed value at the beginning of every packet, coinciding with the beginning of every pixel row, then the scrambled pseudo-random sequence will repeat at the rate that rows of identical image data are transmitted. This can cause the emissions to be less random, and instead have peaks at frequencies equivalent to the rate at which the image data rows are transmitted.

To mitigate this issue, a different seed value is selected by the transmitter every time a Packet Header is transmitted. The Sync Word in the Packet Header encodes a small amount of data, so that the transmitter can inform the receiver which starting seed to use to descramble the packet. This small amount of data in the Sync Word is sent by transmitting a Sync Type that the CSI-2 protocol transmitter chooses. This Sync Type value is also used to select the starting seed in the scrambler and descrambler.

Table ~~17~~28 shows the five possible Sync Types that the C-PHY supports. The Sync Word values are normatively specified in the C-PHY Specification and duplicated in ***Table ~~17~~28*** for convenience. The CSI-2 protocol uses only the first four out of the five possible Sync Types, which simplifies the implementation.

Table 28 Symbol Sequence Values Per Sync Type

Sync Type	Sync Value	TxSyncTypeHS0[2:0], TxSyncTypeHS1[2:0]	Scrambler and Descrambler Seed Index
Type 0	3444440	0	0
Type 1	3444441	1	1
Type 2	3444442	2	2
Type 3	3444443	3	3
Type 4	3444444	4	N/A

Note:

When a single seed value is used, Sync Type 3 is the default Sync Word value.

Figure ~~85~~91 shows the architecture of the scrambling in a single Lane. The pseudo-random number generated by the PRBS shall be used as the seed index to select the initial seed value from the seed list prior to sending the packet. This seed index shall also be sent to the C-PHY using the PPI signals TxSyncTypeHS0[1:0]. TxSyncTypeHS0[2] is always zero. TxSyncTypeHS1 [2:0] is used similarly for a 32-bit data path. The C-PHY ensures that the very first packet in a burst begins with a Sync Word using Sync Type 3.

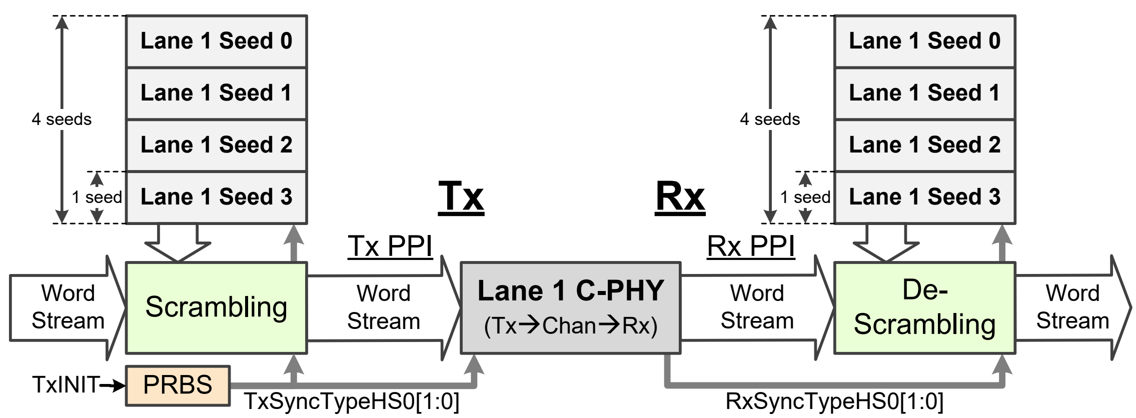


Figure 91 Generating Tx Sync Type as Seed Index (Single Lane View)

The seed list may contain either one or four initial seed values. Transmitters and receivers shall have the capability to select exactly one seed value from a list of seeds. When a single seed value is used, that seed shall be identified as Seed 3 and the transmitter shall always transmit Sync Type 3. Transmitters and receivers should also have the capability to select a seed value from a list of four seed values, as shown in ***Figure ~~85~~91***. When a list of four seed values is used then Sync Type 0 through Sync Type 3 shall be used to convey the seed index value from the transmitter to the receiver.

When the list of four seeds is used, the two-bit seed index shall be generated in the transmitter using a pseudo random generator (e.g., PRBS).

Slight differences in the implementation of the PRBS generator will not affect the interoperability of the transmitter and receiver, because the receiver responds to the seed index chosen in the transmitter and conveyed to the receiver using the Sync Type.

At the receiver, the C-PHY decodes the Sync Word and passes the 2-bit Sync Type value to the CSI-2 protocol logic. The CSI-2 protocol logic uses the two-bit value as a seed index to select one of four seed values to initialize the descrambler. This concept is shown in the single Lane diagram in ***Figure ~~85~~91***~~. *Figure 86*~~. ***Figure 88*** shows the use of the PPI signals to select which seed value was used to initialize the scrambler and descrambler. Since the seed selection field is transmitted via the Sync Word, no other mechanism is needed to coordinate the choice of specific descrambler initial seed values at the receiver.

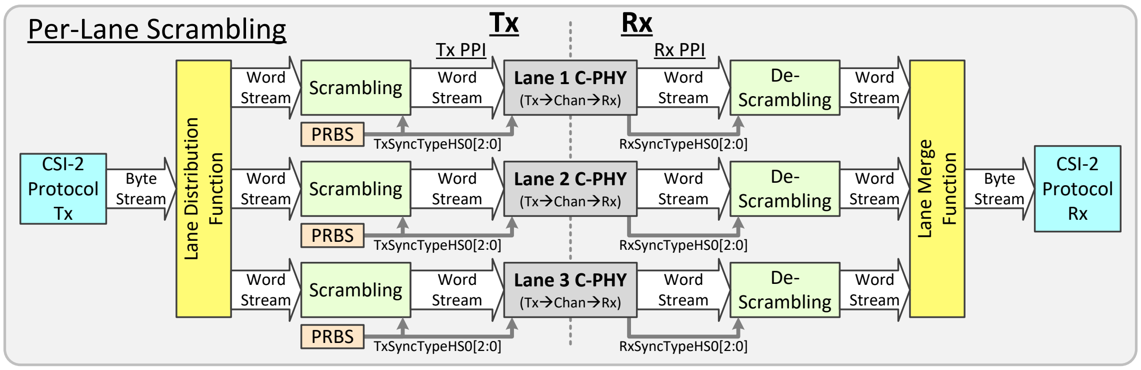


Figure 92 Generating Tx Sync Type Using the C-PHY Physical Layer

~~9.12.3~~9.13.3 Scrambling Details

The Long Packet Header, Data Payload, Long Packet Footer (which may include a Filler Byte), and Short Packets shall be scrambled. Special data fields generated by the PHY that are beyond the control of the CSI-2 protocol shall not be scrambled. For clarity, ***Table ~~18~~29*** lists all of the fields that are not scrambled.

Table 29 Fields That Are Not Scrambled

PHY	PHY-Generated	CSI-2-Protocol-Generated

D-PHY	• HS-Zero
	• Sync Word (aka Leader Sequence)
	• HS Trail
	• SoT
	• EoT
	• HS-Idle
	• All fields of the deskew sequence (aka deskew burst) including:
	  • HS-Zero
	  • Deskew sync pattern
	  • '01010101' data
	  • HS-Trail
		• LP Mode transactions for SoT, EoT and ULPS

C-PHY	• Preamble (including $t_{3\text{-PREBEGIN}}$ $t_{3\text{-PROGSEQ}}$ and $t_{3\text{-PREEND}}$) • Sync Word • Post • SoT • EoT	• Sync Word inserted via PPI command • LP Mode transactions for SoT, EoT and ULPS

The data scrambler and descrambler pseudo-random binary sequence (PRBS) shall be generated using the Galois form of an LFSR implementing the generator polynomial:

$$(x) = x^{16} + x^5 + x^4 + x^3 + 1$$

The initial D-PHY seed values in ***Table ~~19~~30*** should be used to initialize the D-PHY scrambler LFSR in Lanes 1 through 8.

Table 30 D-PHY Scrambler PRBS Initial Seed Values for Lanes 1 Through 8

Lane	Initial Seed Value
1	`0x0810`
2	`0x0990`
3	`0x0a51`
4	`0x0bd0`
5	`0x0c30`
6	`0x0db0`
7	`0x0e70`
8	`0x0ff0`

2036 The initial C-PHY seed values in ***Table ~~20~~31*** should be used to initialize the C-PHY scrambler LFSR in Lanes 1 through 8. The table provides initial seed values for each of the four possible Sync Type values per Lane number. If only a single Sync Type is used, then it shall default to Sync Type 3.

Table 31 C-PHY Scrambler PRBS Initial Seed Values for Lanes 1 Through 8

Lane	Initial Seed Value			
	Sync Type 0	Sync Type 1	Sync Type 2	Sync Type 3
1	0x0810	0x0001	0x1818	0x1008
2	0x0990	0x0180	0x1998	0x1188
3	0x0a51	0x0240	0x1a59	0x1248
4	0x0bd0	0x03c0	0x1bd8	0x13c8
5	0x0c30	0x0420	0x1c38	0x1428
6	0x0db0	0x05a0	0x1db8	0x15a8
7	0x0e70	0x0660	0x1e79	0x1668
8	0x0ff0	0x07e0	0x1ff8	0x17e8

For D-PHY and C-PHY systems requiring more than eight Lanes, ***Annex G*** provides 24 additional seed values for Lanes 9 through 32, as well as a mechanism for finding seed values for Lanes 33 and higher. For each seed value, the LSB corresponds to scrambler PRBS register bit Q0 and the MSB corresponds to bit Q15.

The LFSR shall generate an eight-bit sequence at G(x) for every byte of Payload data to be scrambled, starting from its initial seed value. The LFSR shall generate new bit sequences of G(x) by advancing eight bit cycles for each subsequent Payload data byte.

Scrambling shall be achieved by modulo-2 bit-wise addition (X-OR) of a sequence of eight bits G(x) with the CSI-2 Payload data to be scrambled.

Implementation Tip: the 8-bit value from the PRBS is the flip of bits Q15:Q8 of the PRBS LFSR register on every 8th bit clock. The designer might choose to implement the PRBS LFSR in parallel form to shift the equivalent of 8 places in a single byte clock, or the PRBS LFSR might even be configured to shift a multiple of 8 places in a single word clock.

For the example shown in ***Figure ~~87~~93***, Q[15:8] are captured in a temporary register, then the PRBS LFSR is shifted eight times before Q[15:8] are captured again. The scrambling is performed as follows:

- TxD[7] = PktD[7] ⊕ Q'[8];
- TxD[6] = PktD[6] ⊕ Q'[9];
- TxD[5] = PktD[5] ⊕ Q'[10];
- TxD[4] = PktD[4] ⊕ Q'[11];
- TxD[3] = PktD[3] ⊕ Q'[12];
- TxD[2] = PktD[2] ⊕ Q'[13];
- TxD[1] = PktD[1] ⊕ Q'[14];
- TxD[0] = PktD[0] ⊕ Q'[15];

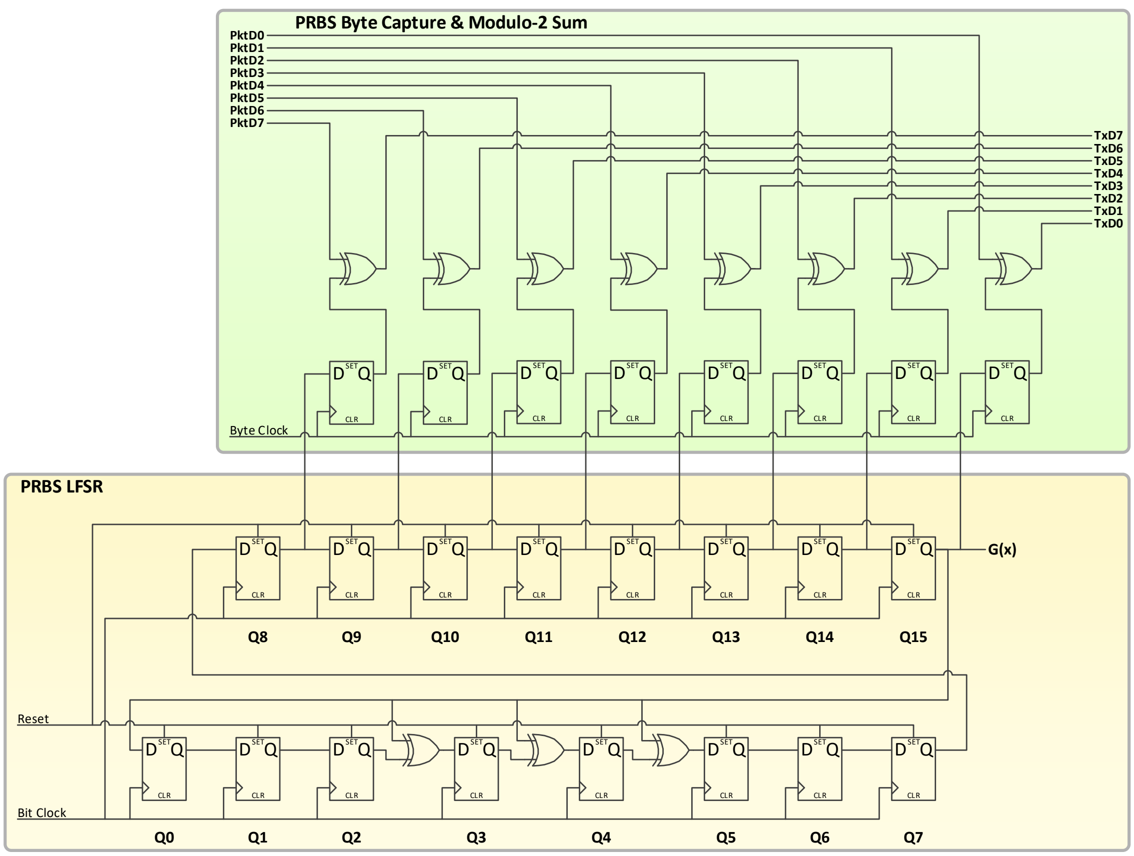


Figure 93 PRBS LFSR Serial Implementation Example

Table ~~***21***~~***32*** illustrates the sequence of the PRBS register one bit at a time, starting with the initial seed value for Lane 2. The data scrambling sequence is the output G(x). The first bit output from the scrambler is the value output from G(x) (also Q15 of the register in ***Figure*** ~~***87***~~***93***) when the register contains the initial seed value.

Table 32 Example of the PRBS Bit-at-a-Time Shift Sequence

t	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	LFSR
0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0x1188
1	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0x2310
2	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0x4620
3	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0x8C40
4	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	1	0x18B9
5	0	0	1	1	0	0	0	1	0	1	1	1	0	0	1	0	0x3172
6	0	1	1	0	0	0	1	0	1	1	1	0	0	1	0	0	0x62E4
7	1	1	0	0	0	1	0	1	1	1	0	0	1	0	0	0	0xC5C8
8	1	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	0x8BA9
9	0	0	0	1	0	1	1	1	0	1	1	0	1	0	1	1	0x176B
10	0	0	1	0	1	1	1	0	1	1	0	1	0	1	1	0	0x2ED6
11	0	1	0	1	1	1	0	1	1	0	1	0	1	1	0	0	0x5DAC
12	1	0	1	1	1	0	1	1	0	1	0	1	1	0	0	0	0xBB58
13	0	1	1	1	0	1	1	0	1	0	0	0	1	0	0	1	0x7689
14	1	1	1	0	1	1	0	1	0	0	0	1	0	0	1	0	0xED12
15	1	1	0	1	1	0	1	0	0	0	0	1	1	1	0	1	0xDA1D
16	1	0	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0xB403

Table ~~***22***~~***33*** shows the first ten PRBS Byte Outputs produced by the PRBS LFSR in Lane 2 when the D-PHY physical layer is being used.

Table 33 Example PRBS LFSR Byte Sequence for D-PHY Physical Layer

Scrambling Sequence	PRBS Register	PRBS Byte	Input Byte	Output Byte
Initial Seed, Byte 0	0x0990	0x90	0x2b	0xbb
Byte 1	0x91f1	0x89	0x0d	0x84
Byte 2	0xee29	0x77	0x63	0x14
Byte 3	0x3dbe	0xbc	0x00	0xbc
Byte 4	0xbba5	0xdd	0x00	0xdd
Byte 5	0xbcb3	0x3d	0x00	0x3d
Byte 6	0xaa1c	0x55	0x19	0x4c
Byte 7	0x061a	0x60	0x41	0x21
Byte 8	0x1a96	0x58	0x22	0x7a
Byte 9	0x942a	0x29	0x53	0x7a

Table ~~23~~34 shows an example of the PRBS Word Outputs at the beginning of a packet, that are produced by the PRBS LFSR in Lane 2 when the C-PHY physical layer is being used.

Table 34 Example PRBS LFSR Byte Sequence for C-PHY Physical Layer

Scrambling Sequence Word #	PRBS Register	PRBS Word	Input Word	Output Word
Initial Seed, Header[47:32]	0x0990	0x8990	0x2b00	0xa290
Header[31:16]	0xee29	0xbc77	0x13b0	0xafc7
Header[15:0]	0xbba5	0x3ddd	0x31c8	0x0c15
Sync Word	0xaa1c	0x6055	0xxxxx	0xxxxx
Re-initialized Seed, Header[47:32]	0x1188	0xd188	0x2b00	0xfa88
Header[31:16]	0xb403	0xd82d	0x13b0	0xcb9d
Header[15:0]	0xd613	0x406b	0x31c8	0x71a3
Word 0	0xc672	0x0663	0xd000	0xd663
Word 1	0x5f60	0x36fa	0x1360	0x259a
Word 2	0xbf4c	0xaafd	0x094c	0xa3b1
Word 3	0x5a0d	0x805a	0x100b	0x9051
Word 4	0x6a39	0x8c56	0x5fb8	0xd3ee
Word 5	0xde89	0x997b	0xd030	0x494b
Word 6	0x10e1	0x4708	0x0003	0x470b
Word 7	0x8592	0x71a1	0xd039	0xa198
Word 8	0x40de	0x0b02	0xa35b	0xa859
Word 9	0x5150	0xba8a	0x00ea	0xba60

9.14 Smart Region of Interest (SROI)

The Smart Region of Interest (SROI) feature supports the adaptive transfer of rectangular Regions of Interest (ROI). SROI can be used to reduce data bandwidth by selectively transmitting one or more smaller ROIs carved out from the original picture, such as a human face or a license plate. SROI has use cases in cameras for computer vision, and machine vision applications beyond mobile markets including industry, surveillance, and IoT.

In addition to reducing data bandwidth, SROI benefits include:

- **High Frame Rate / Low Latency:** Data reduction can increase the sensor frame rate and reduce processing workloads for application processors.
- **High Resolution:** A high-resolution image can be extracted by capturing the necessary information without increasing the amount of data transferred.
- **Low Power Dissipation:** Processing workload reductions can save system power.

9.14.1 Overview of SROI Frame Format

As shown in ***Figure 94***, each rectangular ROI is defined by position (X, Y coordinates of ROI rectangle upper left-hand corner pixel), size (Height and Width of ROI rectangle, in pixels), and other metadata (e.g., ADC bit depth; see ***Table 37***).

Each ROI has corresponding a ROI Information field with values for position, size, and other items (see ***Section 9.14.5***). ROI Information values either are determined by a detection function integrated into an AP or image sensor, or for some use cases such as factory automation are set in advance. The method of detecting an ROI is out of scope for this specification.

The maximum number of ROI is also out of scope for this specification, because it is implementation-specific. However, prior to the SROI transfer the application processor and the image sensor shall agree on the maximum number of ROI.

SROI Frames use three data packet types:

- **SROI Short Packet** is used for transmitting a Frame Start (FS) Packet and a Frame End (FE) Packet in an image frame with the SROI Long Packet.

  If Line synchronization packets are needed, then Line Start (LS) Packets and Line End (LE) Packets are also permitted as SROI Short Packets.
- **SROI Embedded Data Packet** is used for transmitting ROI Information, as detailed in ***Section 9.14.5***.

  If the SROI Embedded Data Packet is present in an image frame, it shall be located at the beginning of the image frame.
- **SROI Long Packet** (excludes the SROI Embedded Data Packet) is used for transmitting ROI image data for an image frame.

  The SROI Long Packet should use the same image Data Type used to transmit the image frame's normal, non-SROI image lines (e.g., RAW10), however a User-Defined Data Type is also permitted. For SROI transfers, it is not required for all SROI Long Packets within a given image frame to have equal length.

  When there are multiple ROIs within one line of original image data, all ROI data shall be merged together into a single SROI Long Packet, with no blanking between the regions. See example of A(0) and D(0) in ***Figure 94***.

  Any image region overlapped by multiple ROIs, for example A(n-2) and B(0) in ***Figure 94***, shall be transmitted only once (i.e., shall not be transmitted multiple times, one per ROI). As a result, each overlapped image region shall be counted only once when calculating the value of the SROI Long Packet Word Count field (i.e., shall not be counted multiple times, one per ROI).

The term **SROI Packet** means any SROI Short Packet, SROI Embedded Data Packet, or SROI Long Packet.

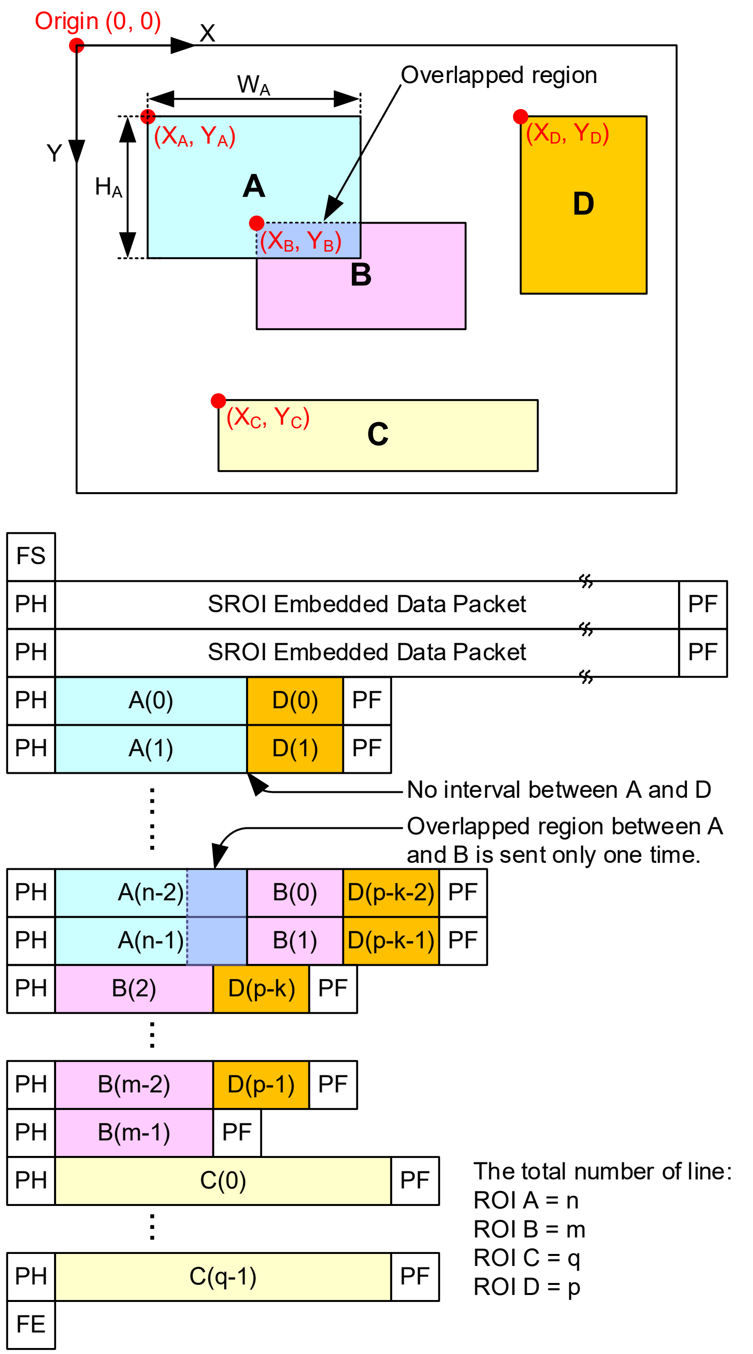


Figure 94 SROI Frame Format Example

9.14.2 Transmission of SROI Embedded Data Packet

This Section specifies when the image sensor is required to send the SROI Embedded Data Packet (SEDP) in the image frame.

This depends upon whether the application processor (AP) knows, vs. does not know, all required ROI Information (see ***Table 35***). When the image sensor does send the SEDP, the AP's method of detecting SROI Packets depends upon the SROI Packet Option (Option 1 vs. Option 2, see ***Section 9.14.3***) that the AP and image sensor have agreed to use.

- **If the application processor already knows all ROI information** required to receive an SROI Packet, then the image sensor is not required to transmit the SEDP. However, the image sensor may optionally transmit the SEDP.

  If SEDP is sent and SROI Packet Option 1 is used, then the AP can detect SROI Packets in the image frame by inspecting the Virtual Channel value (see ***Section 9.14.3.1***).

- **If the application processor does not already know all ROI information** required to receive an SROI Packet, then the image sensor shall transmit the SEDP.

  The method the AP uses to detect SROI Packets in an image frame depends upon which SROI Packet Option is in use: by Virtual Channel for Option 1 (see ***Section 9.14.3.1***), or by Data Type for Option 2 (see ***Section 9.14.3.2***).

Example use cases are shown in ***Section 9.14.4***.

Table 35 Transmission of SROI Embedded Data Packet

		AP Knowledge of All Required ROI Information	
		AP Knows (See ***Section 9.14.4.1***)	**AP Does Not Know** (See ***Section 9.14.4.2***)
SEDP Required		**No**	**Yes**
SROI Packet Option	**Option 1** (See ***Section 9.14.3.1***)	AP either knows SROI Packet, or can detect SROI Packet by Virtual Channel	AP can detect SROI Packet by Virtual Channel
	Option 2 (See ***Section 9.14.3.2***)	AP knows SROI Packet	AP can detect SROI Packet by Data Type

9.14.3 SROI Packet Detection Options

The following sub-sections detail the two options for distinguishing the SROI Packets in an image frame from the non-SROI Packets.

Prior to the SROI transfer, the application processor and the image sensor shall agree on which of the two options (i.e., Option 1 vs. Option 2) will be used.

9.14.3.1 SROI Packet Option 1

Option 1 distinguishes SROI Packets from non-SROI packets by using a different Virtual Channel value.

For Option 1, all SROI Packets for a given image frame shall use the same Virtual Channel, and this SROI Virtual Channel shall be different from the Virtual Channel used in the image frame's non-SROI Packets (see ***Figure 95***). Virtual Channel Interleaving may be used.

An image frame that includes SROI Packets may use Data Type Interleaving, but only if the Data Type used in the SROI Long Packet is different from the Data Type used in the non-SROI Long Packet (e.g., PDAF).

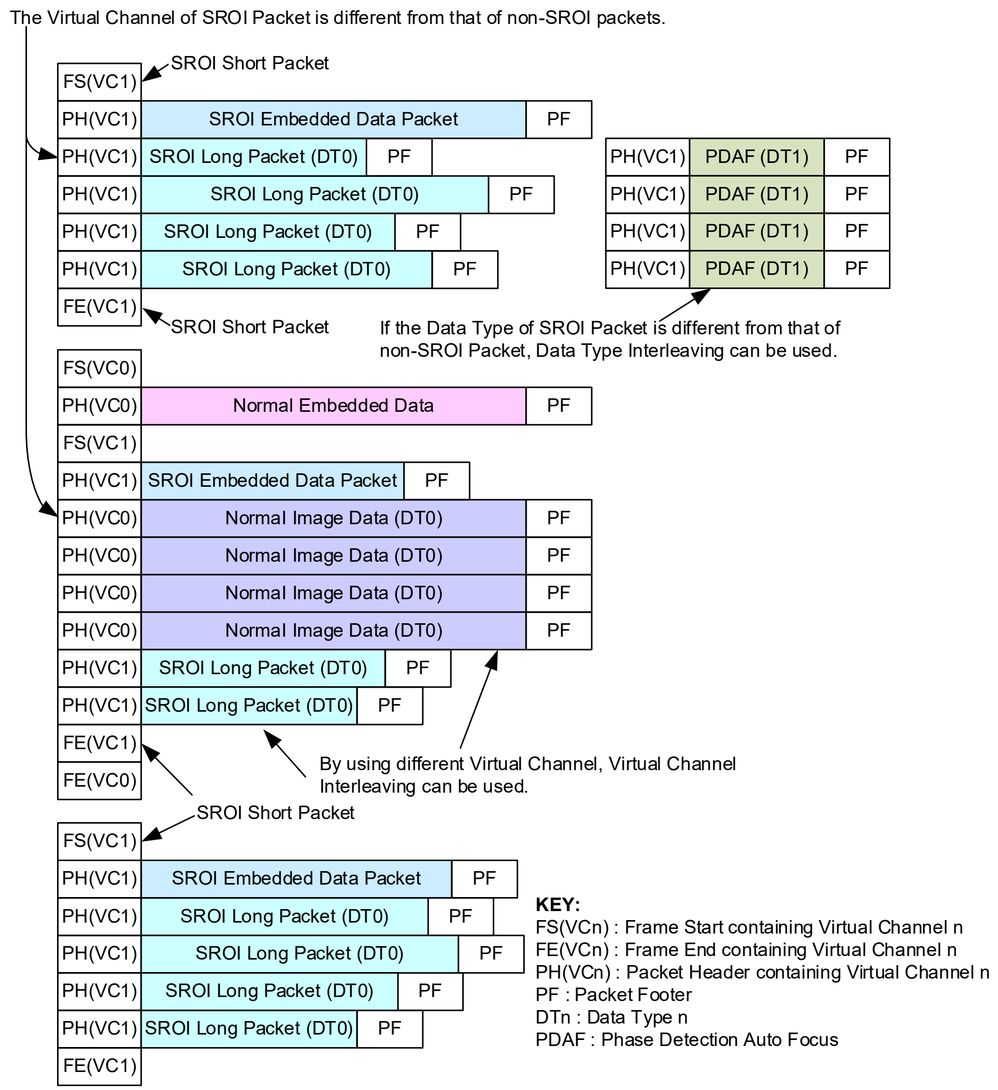


Figure 95 SROI Packet Option 1

9.14.3.2 SROI Packet Option 2

Option 2 distinguishes SROI Packets from non-SROI packets by Data Type; in particular, by detecting the presence of the SROI Embedded Data Packet in the image frame.

For Option 2, all SROI Packets for a given image frame shall use the same Virtual Channel that the non-SROI Packets use (see ***Figure 96***).

An image frame that includes SROI Packets may use Data Type Interleaving, but only if the Data Type used in the SROI Long Packet is different from the Data Type used in the non-SROI Long Packet (e.g., PDAF).

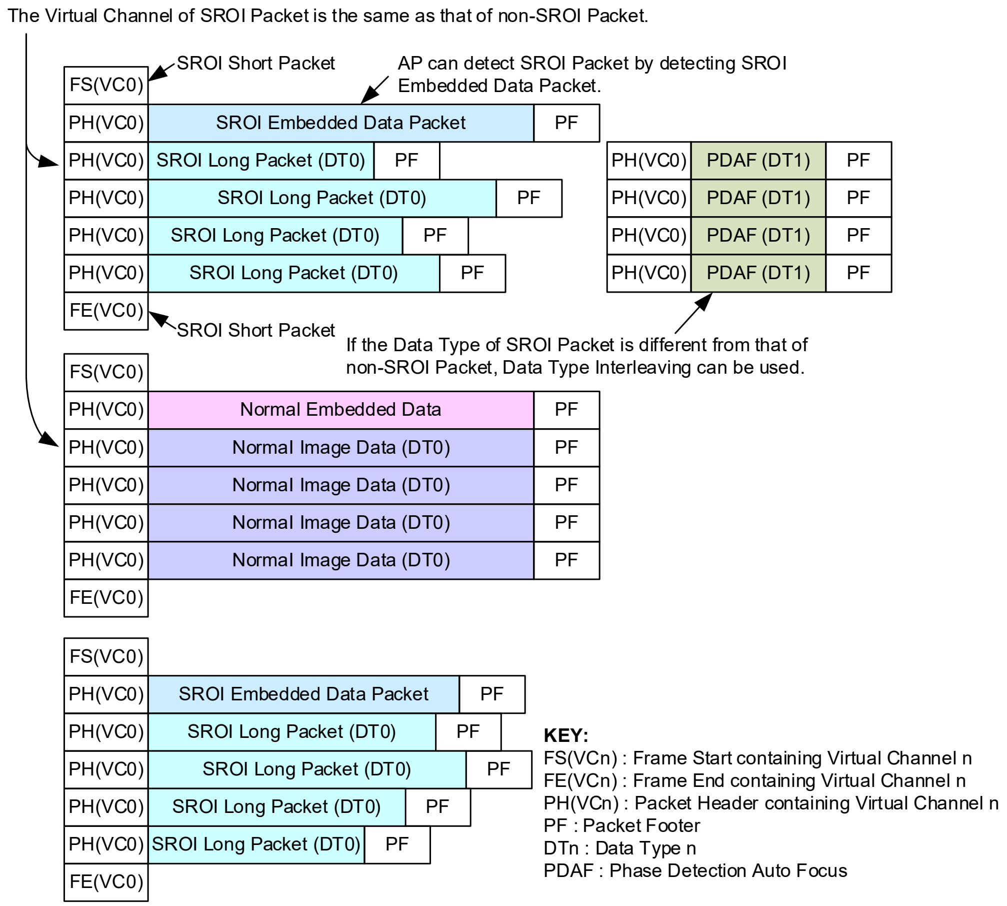


Figure 96 SROI Packet Option 2

9.14.4 SROI Use Cases (Informative)

This Section presents informative use cases illustrating ways in which the SROI feature can be used.

9.14.4.1 Use Case 1: ROI Detection by the Application Processor

If the AP is responsible for detecting an ROI, or has ROI information that is set in advance, then the image sensor is not required to transmit the SROI Embedded Data Packet. An example is shown in ***Figure 97***.

In this use case, the AP detects a ROI (e.g., a human face), and then sends the ROI's position and size to an image sensor through the CCI (see ***Section 6***). The image sensor then just carves out the ROI, based on the ordered position and size, and then keeps sending SROI Long Packets for the same image region.

In this case the SROI Embedded Data Packet is not transmitted, because it would be unnecessary: the application processor already knows all ROI information (e.g., the ROI position and size) required to receive the SROI Packets.

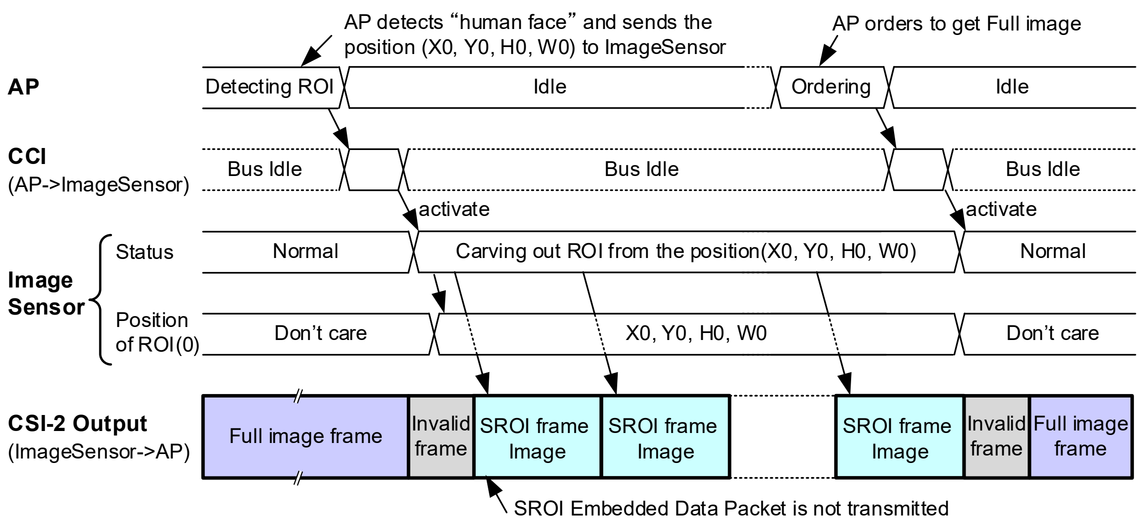


Figure 97 Use Case 1: SROI Embedded Data Packet Not Transmitted

9.14.4.2 Use Case 2: ROI Detection by the Image Sensor

If the image sensor is responsible for detecting an ROI, then the image sensor is required to transmit the SROI Embedded Data Packet as illustrated in ***Figure 98***.

The AP orders the image sensor to get an ROI (e.g., a human face). The image sensor detects the ROI and carves it out, and then keeps tracking the ROI.

In this case the SROI Embedded Data Packet is (and must be) transmitted, because the application processor doesn't know all of the ROI information (e.g., position and size) required to receive the SROI Packets.

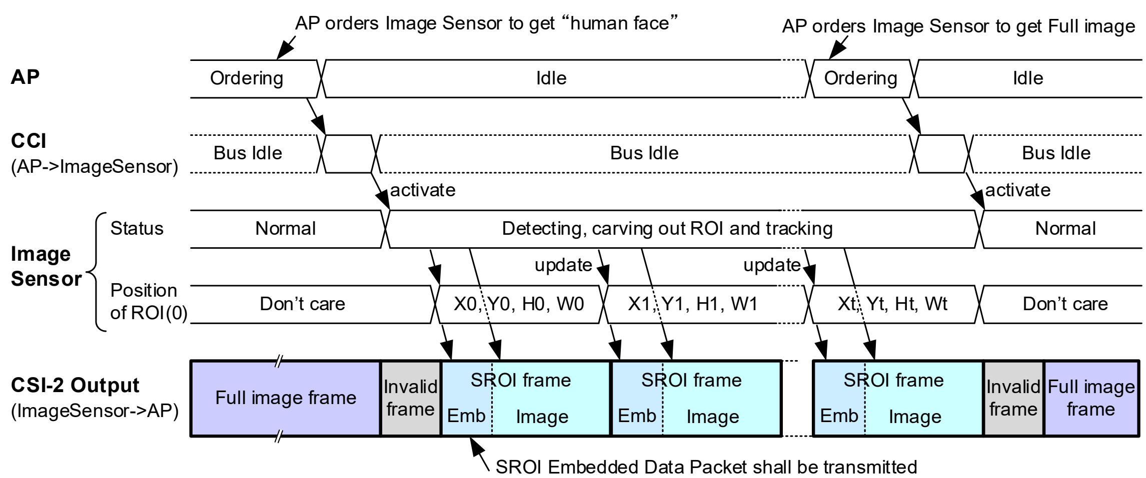


Figure 98 Use Case 2: SROI Embedded Data Packet Is Transmitted

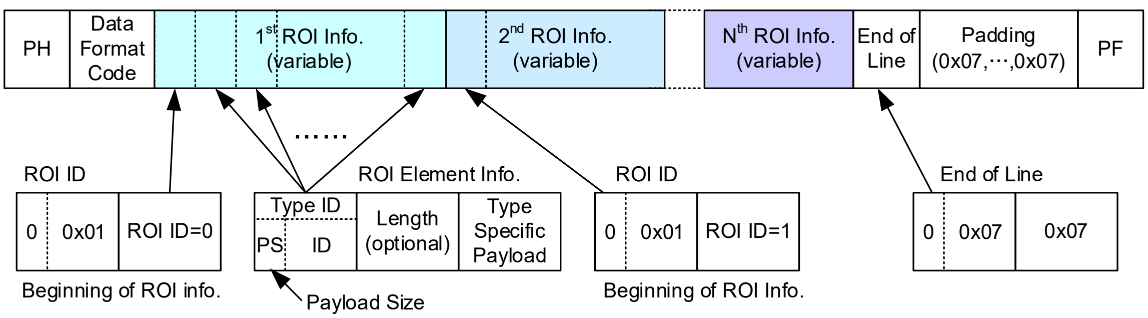
9.14.5 Format of SROI Embedded Data Packet (SEDP)

2173 For SROI transfers, the Embedded Data Format is based on the definition in the MIPI CCS specification
2174 ***[MIPI04]***. The Embedded Data Format Code for SROI frames is 0x0D (1 byte).

2175 The SROI Embedded Data Packet (see ***Figure 99***) is composed of multiple ROI Information fields, each
2176 containing ROI Information about one extracted image region. Every ROI Information field shall start with
2177 the ROI ID, followed by the ROI Element Information field defined by ***Table 36***. ***Table 37*** defines the
2178 allocation and assignment of values for the Type ID sub-field used in the ROI Element Information field.

2179 At the end of the embedded data line, the End of Line shall be inserted after the end of the last ROI
2180 Information field.

2181 The length of the SROI Embedded Data Packet line shall not exceed the length of the full-resolution image
2182 data line. After the End of Line, the remainder of the line should be padded with 0x07 characters if the SROI
2183 Embedded Data Packet line is shorter than the length of the full-resolution image data line.



2184

Figure 99 SROI Embedded Data Packet Format

2185 **Table 36 ROI Element Information Field Format**

Field Name		Size (bits)	Description	
Type ID	**Payload Size**	2	Size of the Type Specific Payload field: 0: 1 byte 1: 2 bytes 2: 4 bytes 3: Size is given by the Length field (below)	
	ID	6	Type Identifier (bottom bits of first byte):	
			0x00 – 0x1F	MIPI Defined ID
			0x20 – 0x3E	User Defined ID
			0x3F	MIPI Defined ID
Length (optional)		8	**If Payload Size is 3 (2'b11):** Number of 8-bit data bytes in the Type Specific Payload field *Example:* A value of 0x20 in the Length field indicates that the Type Specific Payload contains 32 bytes **If Payload size is 0, 1, or 2:** Length field is not included in the ROI Element Information field	

Type Specific Payload	Variable	The payload data is byte-based, i.e., the data size shall be divisible by 8 bits.

Table 37 ROI Element Type ID Definitions

Type ID	Name	Description
MIPI Defined IDs		
Payload Size = 1 Byte		
8'b00_0_00000	**Reserved**	Reserved for future use
8'b00_0_00001	**ROI ID**	Identification number (1 Byte) of each ROI. (Mandatory)
8'b00_0_00010	**ADC Bit Depth**	Bit depth of Analog Digital Converter of each ROI
8'b00_0_00011 through 8'b00_0_00110	**Reserved**	Reserved for future use
8'b00_0_00111	**End of Line**	The end of SROI Embedded Data line. The value of Type Specific Payload is 0x07.
8'b00_0_01000 through 8'b00_0_11111	**Reserved**	Reserved for future use
Payload Size = 2 Bytes		
8'b01_0_00000	**Reserved**	Reserved for future use
8'b01_0_00001	**ROI ID (2 Bytes)**	Identification number (2 Bytes) of each ROI. (Optional)
8'b01_0_00010 through 8'b01_0_00111	**Reserved**	Reserved for future use
8'b01_0_01000	**X**	X coordinate of upper left of region [pixel]
8'b01_0_01001	**Y**	Y coordinate of upper left of region [pixel]
8'b01_0_01010	**Height**	Height of region [pixels]
8'b01_0_01011	**Width**	Width of region [pixels]
8'b01_0_01100 through 8'b01_0_11111	**Reserved**	Reserved for future use
Payload Size = 4 Bytes		
8'b10_0_00000 through 8'b10_0_11111	**Reserved**	Reserved for future use

Type ID	Name	Description
Payload Size = Length		
8'b11_0_00000 through 8'b11_0_11111	**Reserved**	Reserved for future use
User Defined IDs		
Payload Size = 1 Byte		
8'b00_1_00000 through 8'b00_1_11111	**User Defined ID**	Reserved for user definition
Payload Size = 2 Bytes		
8'b01_1_00000 through 8'b01_1_11111	**User Defined ID**	Reserved for user definition
Payload Size = 4 Bytes		
8'b10_1_00000 through 8'b10_1_11111	**User Defined ID**	Reserved for user definition
Payload Size = Length		
8'b11_1_00000 through 8'b11_1_11110	**User Defined ID**	Reserved for user definition
MIPI Defined ID		
8'b11_1_11111	**Reserved**	Reserved for future use

~~9.13~~9.15 Packet Data Payload Size Rules

For YUV, RGB or RAW data types, one long packet shall contain one line of image data. Each long packet of the same Data Type shall have equal length when packets are within the same Virtual Channel and when packets are within the same frame. An exception to this rule is the YUV420 data type which is defined in ***Section 11.2.2***.

For User Defined Byte-based Data Types, the USL Data Type (code 0x38), and Data Types for SROI Long Packet, long packets can have arbitrary length. The spacing between packets can also vary.

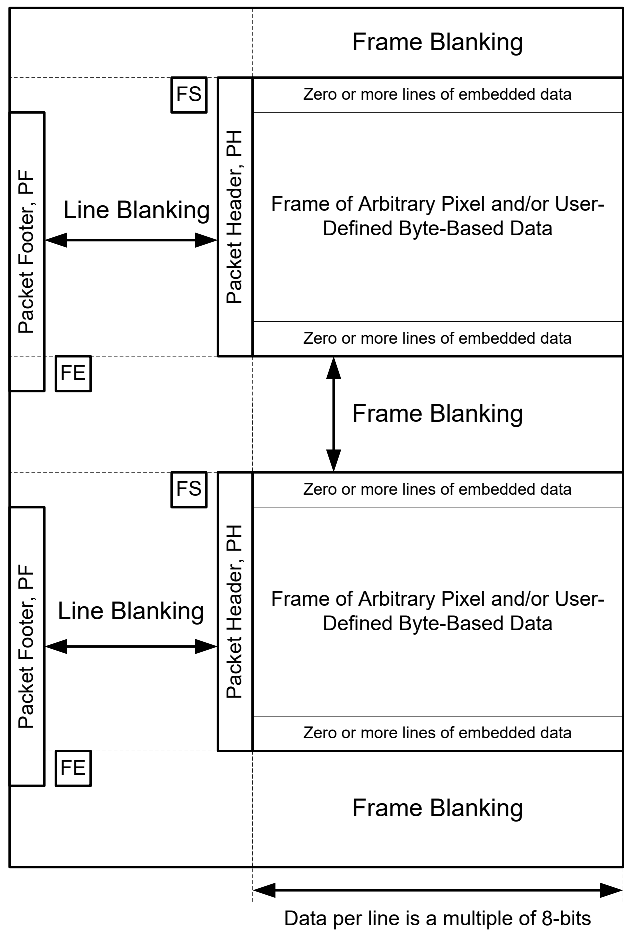
The total size of payload data within a long packet for all data types shall be a multiple of eight bits. However, it is also possible that a data types payload data transmission format, as defined elsewhere in this Specification, imposes additional constraints on payload size. In order to meet these constraints it may sometimes be necessary to add some number of "padding" pixels to the end of a payload e.g., when a packet with the RAW10 data type contains an image line whose length is not a multiple of four pixels as required by the RAW10 transmission format as described in ***Section 11.4.4***. The values of such padding pixels are not specified.

~~9.14~~9.16 Frame Format Examples

This is an informative section.

This section contains three examples to illustrate how the CSI-2 features can be used.

- General Frame Format Example, ***Figure*** ***~~88~~100***
- Digital Interlaced Video Example, ***Figure*** ***~~89~~101***
- Digital Interlaced Video with accurate synchronization timing information, ***Figure*** ***~~90~~102***

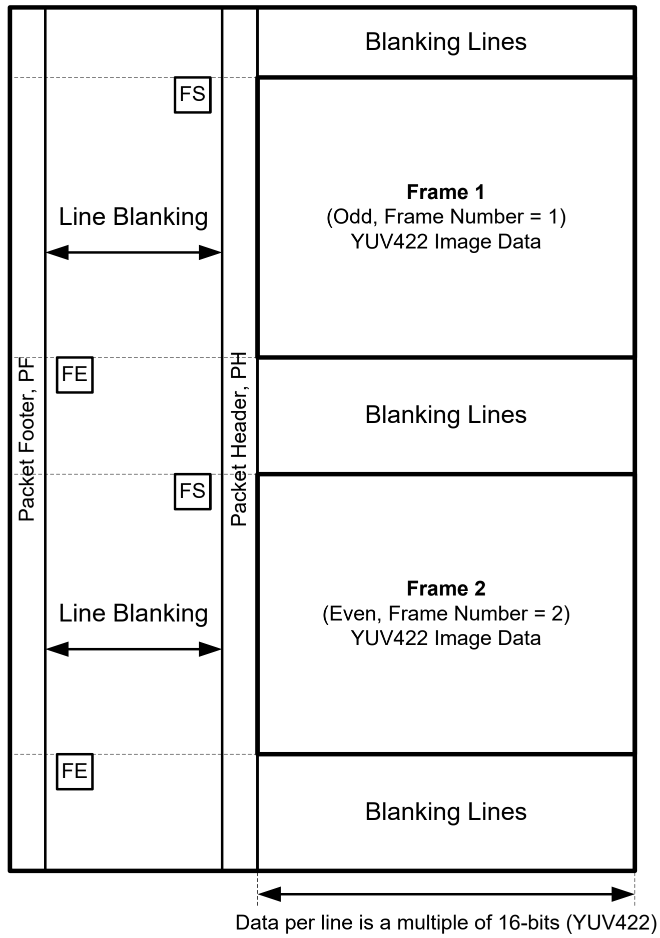


KEY:

PH – Packet Header
FS – Frame Start
LS – Line Start

PF – Packet Footer + Filler (if applicable)
FE – Frame End
LE – Line End

Figure 100 General Frame Format Example

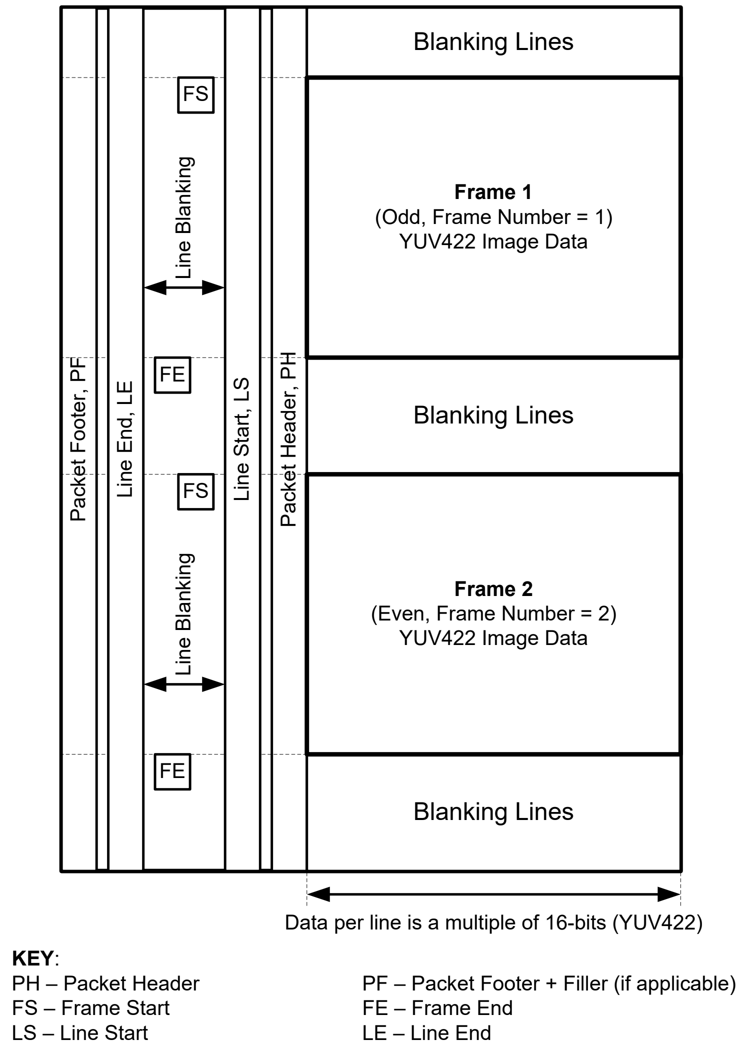


KEY:

PH – Packet Header
FS – Frame Start
LS – Line Start

PF – Packet Footer + Filler (if applicable)
FE – Frame End
LE – Line End

Figure 101 Digital Interlaced Video Example



2207

Figure 102 Digital Interlaced Video with Accurate Synchronization Timing Information

~~9.15~~9.17 Data Interleaving

The CSI-2 supports the interleaved transmission of different image data formats within the same video data stream.

There are two methods to interleave the transmission of different image data formats:

- Data Type
- Virtual Channel Identifier

The preceding methods of interleaved data transmission can be combined in any manner.

~~9.15.1~~9.17.1 Data Type Interleaving

The Data Type value uniquely defines the data format for that packet of data. The receiver uses the Data Type value in the packet header to de-multiplex data packets containing different data formats as illustrated in ***Figure ~~91~~103***. Note, in the figure the Virtual Channel Identifier is the same in each Packet Header.

The packet payload data format shall agree with the Data Type code in the Packet Header as follows:

- For defined image data types – any non-reserved codes in the range 0x18 to 0x3F – only the single corresponding MIPI-defined packet payload data format shall be considered correct
- Reserved image data types – any reserved codes in the range 0x18 to 0x3F – shall not be used. No packet payload data format shall be considered correct for reserved image data types
- For generic long packet data types (codes 0x10 thru 0x17) and user-defined, byte-based (codes 0x30 – 0x37), any packet payload data format shall be considered correct
- Generic long packet data types (codes 0x10 thru 0x17) and user-defined, byte-based (codes 0x30 – 0x37), should not be used with packet payloads that meet any MIPI image data format definition
- Synchronization short packet data types (codes 0x00 thru 0x07) shall consist of only the header and shall not include payload data bytes
- Generic short packet data types (codes 0x08 thru 0x0F) shall consist of only the header and shall not include payload data bytes

Data formats are defined further in ***Section 11***.

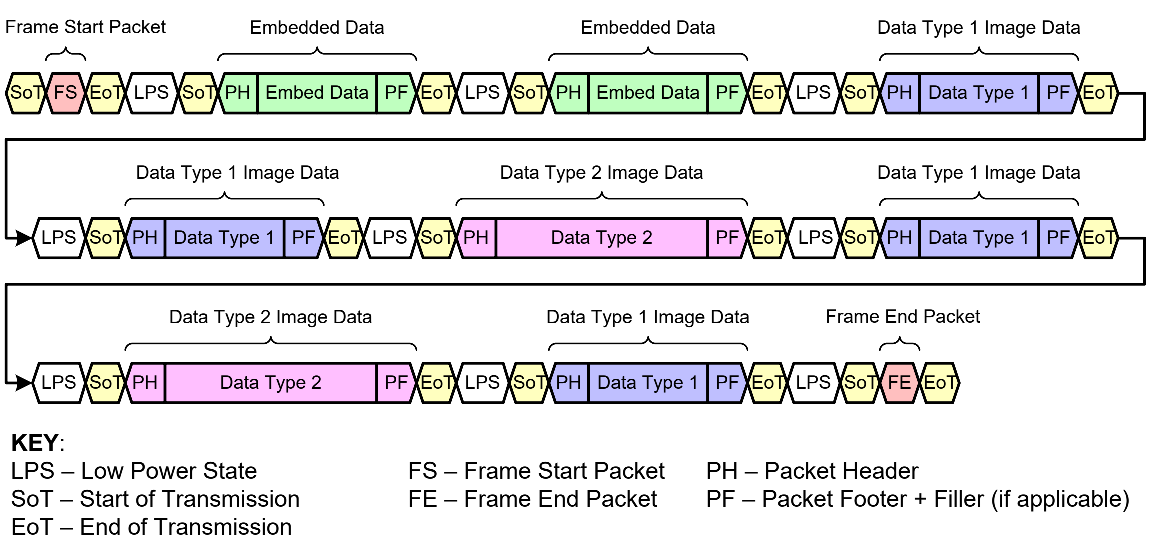
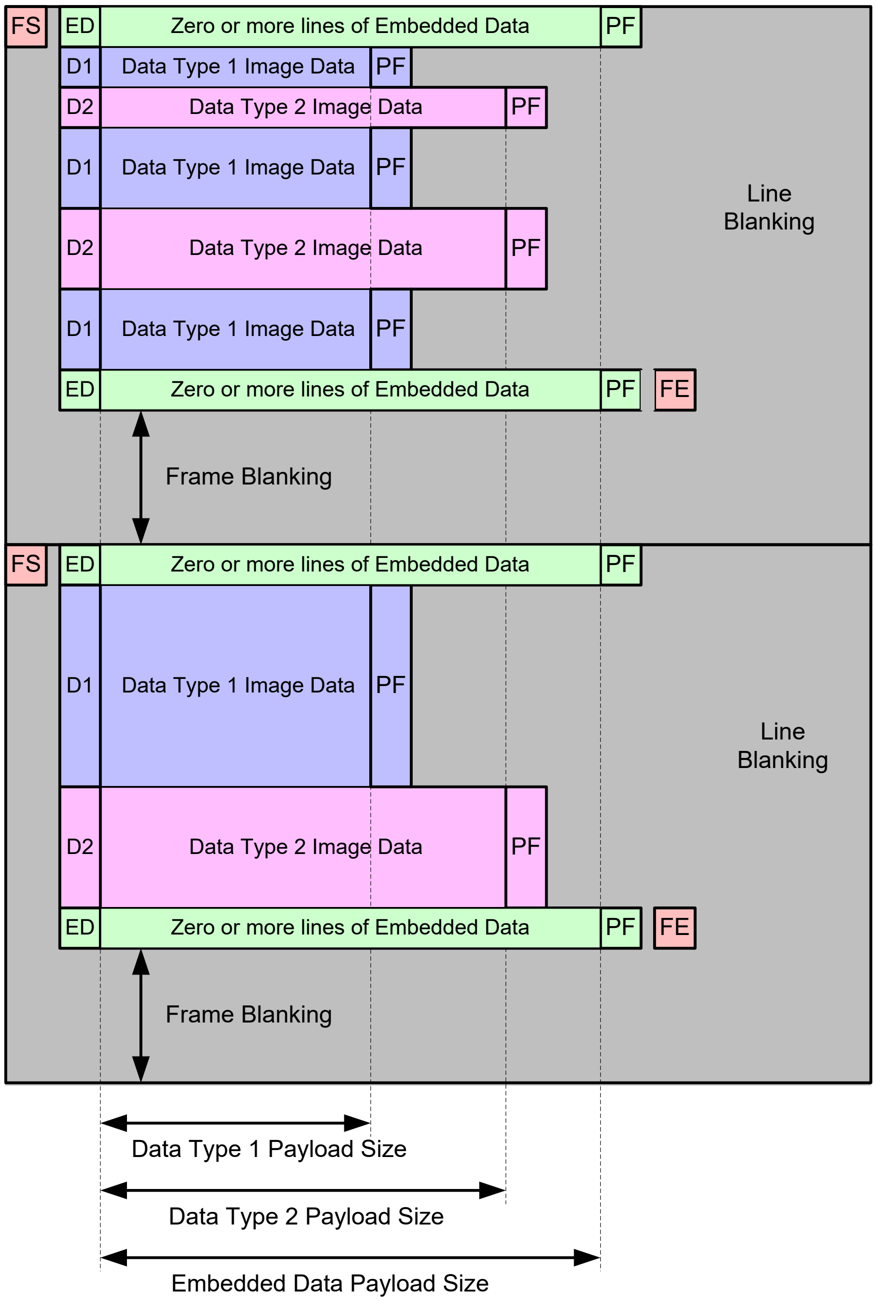


Figure 103 Interleaved Data Transmission using Data Type Value

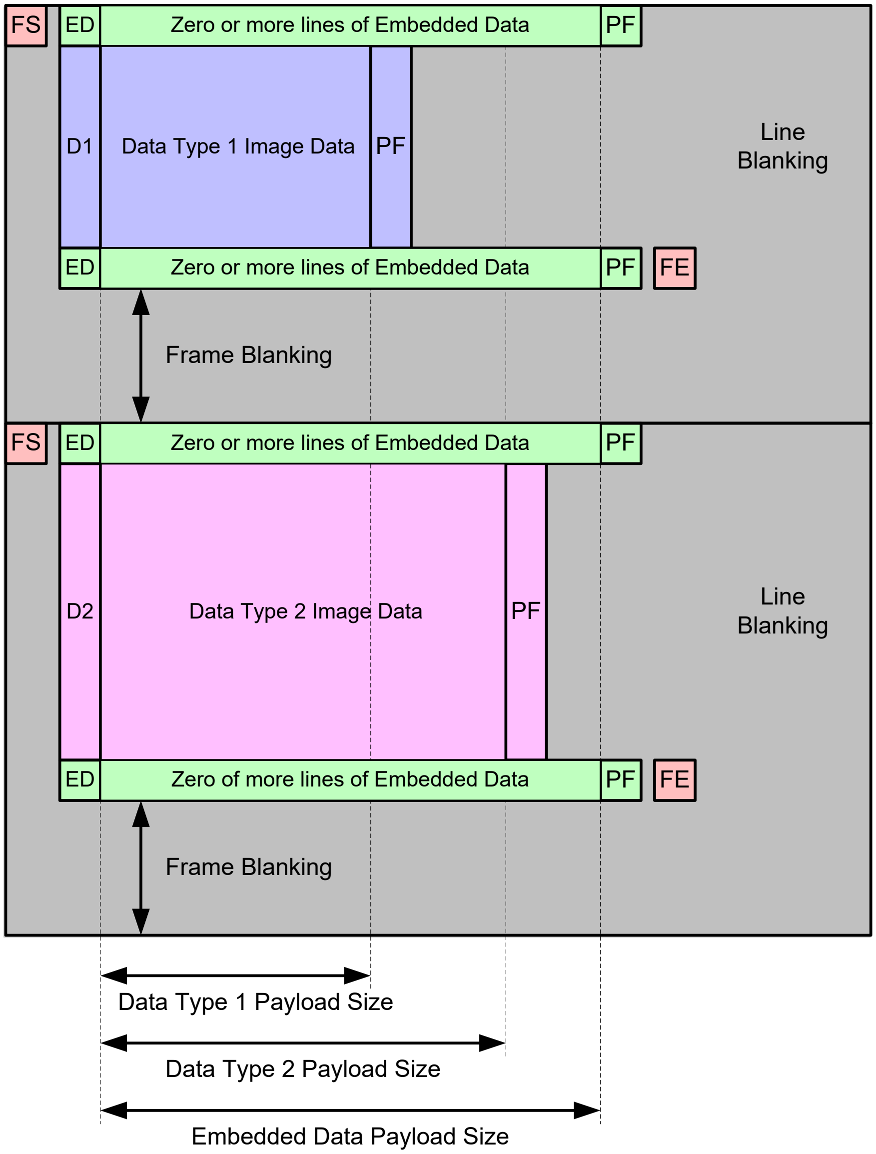
All of the packets within the same virtual channel, independent of the Data Type value, share the same frame start/end and line start/end synchronization information. By definition, all of the packets, independent of data type, between a Frame Start and a Frame End packet within the same virtual channel belong to the same frame.

Packets of different data types may be interleaved at either the packet level as illustrated in ***Figure ~~92~~104*** or the frame level as illustrated in ***Figure ~~93~~105***. Data formats are defined in ***Section 11***.



KEY:
LPS – Low Power State
FS – Frame Start
FE – Frame End
ED – Packet Header containing Embedded Data type code
D1 – Packet Header containing Data Type 1 Image Data Code
D2 – Packet Header containing Data Type 2 Image Data Code
PF – Packet Footer + Filler (if applicable)

2238 **Figure 104 Packet Level Interleaved Data Transmission**



KEY:

LPS – Low Power State	ED – Packet Header containing Embedded Data type code
FS – Frame Start	D1 – Packet Header containing Data Type 1 Image Data Code
FE – Frame End	D2 – Packet Header containing Data Type 2 Image Data Code
	PF – Packet Footer + Filler (if applicable)

Figure 105 Frame Level Interleaved Data Transmission

~~9.15.2~~9.17.2 Virtual Channel Identifier Interleaving

The Virtual Channel Identifier allows different data types within a single data stream to be logically separated from each other. ***Figure ~~94~~106*** illustrates data interleaving using the Virtual Channel Identifier.

Each virtual channel has its own Frame Start and Frame End packet~~.~~ (except for virtual channels used exclusively with USL Packets; see ***Section 9.12***). Therefore, it is possible for different virtual channels to have different frame rates, though the data rate for both channels would remain the same.

In addition, Data Type value Interleaving can be used for each virtual channel, allowing different data types within a virtual channel and a second level of data interleaving.

Therefore, receivers should be able to de-multiplex different data packets based on the combination of the Virtual Channel Identifier and the Data Type value. For example, data packets containing the same Data Type value but transmitted on different virtual channels are considered to belong to different frames (streams) of image data.

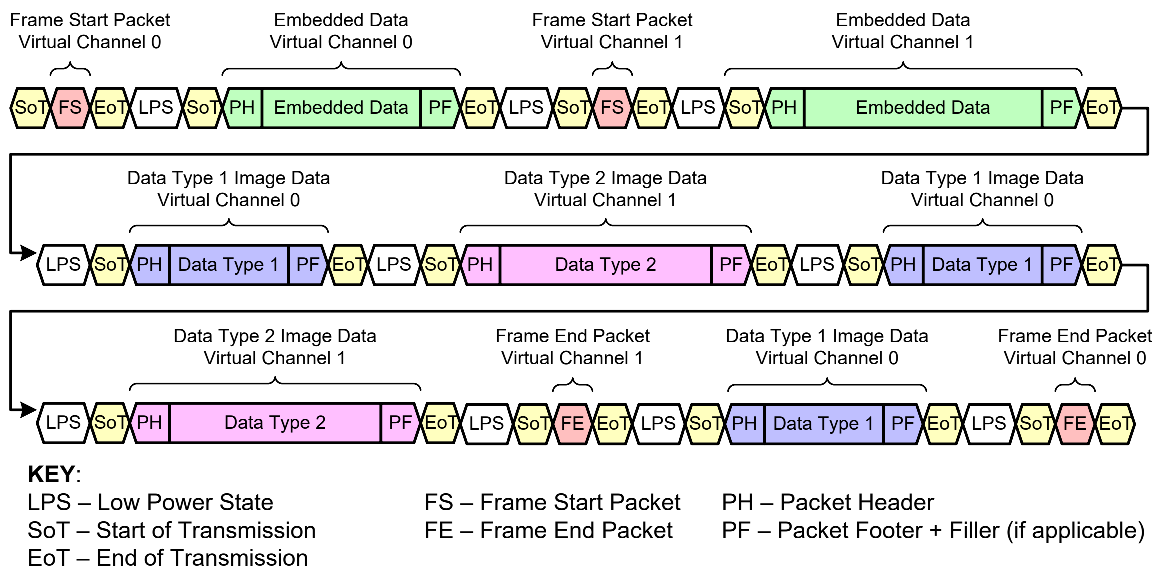


Figure 106 Interleaved Data Transmission using Virtual Channels

~~This page intentionally left blank~~

10 Color Spaces

The color space definitions in this section are simply references to other standards. The references are included only for informative purposes and not for compliance. The color space used is not limited to the references given.

10.1 RGB Color Space Definition

In this Specification, the abbreviation RGB means the nonlinear sRGB col or space in 8-bit representation based on the definition of sRGB in IEC 61966.

The 8-bit representation results as RGB888. The conversion to the more commonly used RGB565 format is achieved by scaling the 8-bit values to five bits (blue and red) and six bits (green). The scaling can be done either by simply dropping the LSBs or rounding.

10.2 YUV Color Space Definition

In this Specification, the abbreviation YUV refers to the 8-bit gamma corrected YCBCR color space defined in ITU-R BT601.4.

This page intentionally left blank.

11 Data Formats

The intent of this section is to provide a definitive reference for data formats typically used in CSI-2 applications. ***Table ~~24~~38*** summarizes the formats, followed by individual definitions for each format. Generic data types not shown in the table are described in ***Section 11.1***. For simplicity, all examples are single Lane configurations.

The formats most widely used in CSI-2 applications are distinguished by a "primary" designation in ***Table ~~24~~38***. Transmitter implementations of CSI-2 should support at least one of these primary formats. Receiver implementations of CSI-2 should support all of the primary formats.

The packet payload data format shall agree with the Data Type value in the Packet Header. See ***Section 9.4*** for a description of the Data Type values.

Table 38 Primary and Secondary Data Formats Definitions

Data Format	Primary	Secondary
YUV420 8-bit (legacy)		S
YUV420 8-bit		S
YUV420 10-bit		S
YUV420 8-bit (CSPS)		S
YUV420 10-bit (CSPS)		S
YUV422 8-bit	P	
YUV422 10-bit		S
RGB888	P	
RGB666		S
RGB565	P	
RGB555		S
RGB444		S
RAW6		S
RAW7		S
RAW8	P	
RAW10	P	
RAW12		S
RAW14		S
RAW16		S
RAW20		S
RAW24		S
Generic 8-bit Long Packet Data Types	P	
User Defined Byte-based Data (Note 1)	P	
USL Packet Data (See ***Section 9.12***)		S

Note:

1. *Compressed image data should use the user defined, byte-based data type codes*

For clarity the Start of Transmission and End of Transmission sequences in the figures in this section have been omitted.

The balance of this section details how sequences of pixels and other application data conforming to each of the data types listed in ***Table ~~24~~38*** are converted into equivalent byte sequences by the CSI-2 Pixel to Byte Packing Formats layer shown in ***Figure 3***.

Various figures in this section depict these byte sequences as shown at the top of ***Figure ~~95~~107***, where Byte n always precedes Byte m for n < m. Also note that even though each byte is shown in LSB-first order, this is not meant to imply that the bytes themselves are bit-reversed by the Pixel to Byte Packing Formats layer prior to output.

For the D-PHY physical layer option, each byte in the sequence is serially transmitted LSB-first, whereas for the C-PHY physical layer option, successive byte pairs in the sequence are encoded and then serially transmitted LSS-first. ***Figure ~~95~~107*** illustrates these options for a single-Lane system.

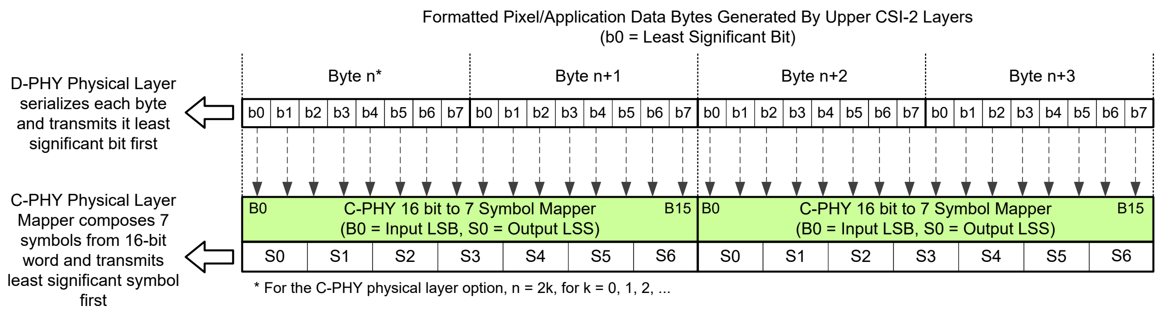


Figure 107 Byte Packing Pixel Data to C-PHY Symbol Illustration

11.1 Generic 8-bit Long Packet Data Types

Table ~~25~~39 defines the generic 8-bit Long packet data types.

Table 39 Generic 8-bit Long Packet Data Types

Data Type	Description	See Section
0x10	Null	***11.1.1***
0x11	Blanking Data	
0x12	Embedded 8-bit non Image Data	***11.1.2***
0x13	Generic long packet data type 1	***11.1.3***
0x14	Generic long packet data type 2	
0x15	Generic long packet data type 3	
0x16	Generic long packet data type 4	
0x17	Reserved	–

11.1.1 Null and Blanking Data

For both the null and blanking data types the receiver must ignore the content of the packet payload data.

A blanking packet differs from a null packet in terms of its significance within a video data stream. A null packet has no meaning whereas the blanking packet may be used, for example, as the blanking lines between frames in an ITU-R BT.656 style video stream.

11.1.2 Embedded Information

It is possible to embed extra lines containing additional information to the beginning and to the end of each picture frame as presented in the ***Figure*** ~~***96***~~***108***. If embedded information exists, then the lines containing the embedded data must use the embedded data code in the data identifier.

There may be zero or more lines of embedded data at the start of the frame. These lines are termed the frame header.

There may be zero or more line of embedded data at the end of the frame. These lines are termed the frame footer.

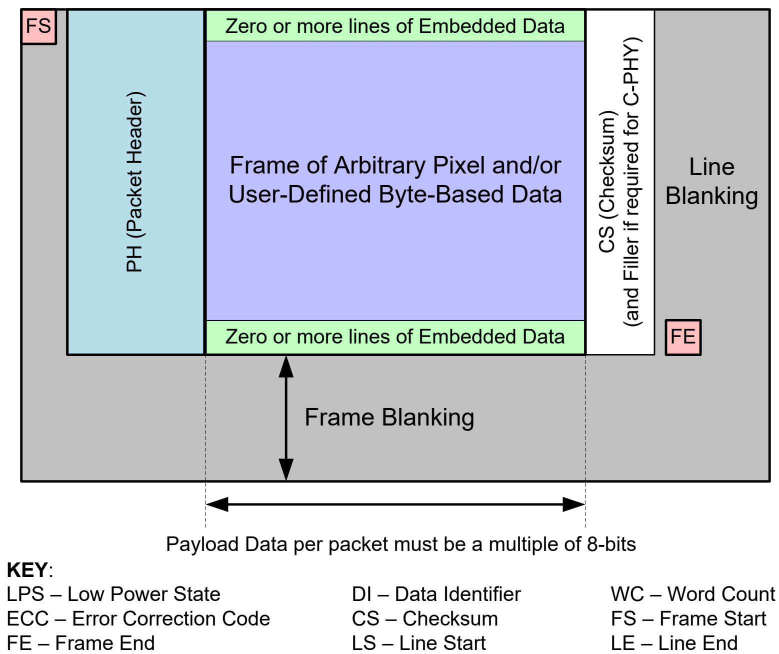


Figure 108 Frame Structure with Embedded Data at the Beginning and End of the Frame

11.1.3 Generic Long Packet Data Types 1 Through 4

These codes have no specific definitions and may be used, for example, to identify various types of vendor-specific metadata packets transmitted within an image frame.

11.2 YUV Image Data

Table ~~26~~40 defines the data type codes for YUV data formats described in this section. The number of lines transmitted for the YUV420 data type shall be even.

YUV420 data formats are divided into legacy and non-legacy data formats. The legacy YUV420 data format is for compatibility with existing systems. The non-legacy YUV420 data formats enable lower cost implementations.

Table 40 YUV Image Data Types

Data Type	Description
0x18	YUV420 8-bit
0x19	YUV420 10-bit
0x1A	Legacy YUV420 8-bit
0x1B	Reserved
0x1C	YUV420 8-bit (Chroma Shifted Pixel Sampling)
0x1D	YUV420 10-bit (Chroma Shifted Pixel Sampling)
0x1E	YUV422 8-bit
0x1F	YUV422 10-bit

11.2.1 Legacy YUV420 8-bit

Legacy YUV420 8-bit data transmission is performed by transmitting UYY… / VYY… sequences in odd / even lines. U component is transferred in odd lines (1, 3, 5 …) and V component is transferred in even lines (2, 4, 6 …). This sequence is illustrated in ***Figure ~~97~~109***.

Table ~~27~~41 specifies the packet size constraints for YUV420 8-bit packets. Each packet must be a multiple of the values in the table.

Table 41 Legacy YUV420 8-bit Packet Data Size Constraints

Pixels	Bytes	Bits
2	3	24

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in ***Figure ~~98~~110***.

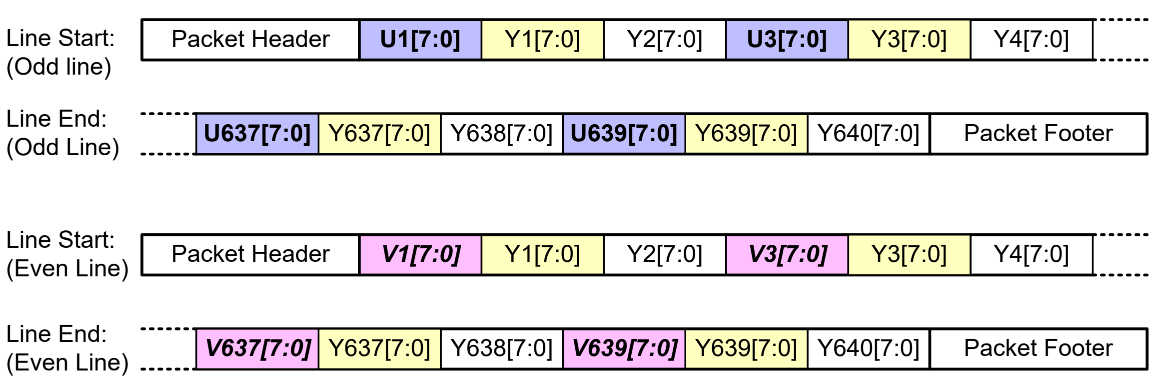


Figure 109 Legacy YUV420 8-bit Transmission

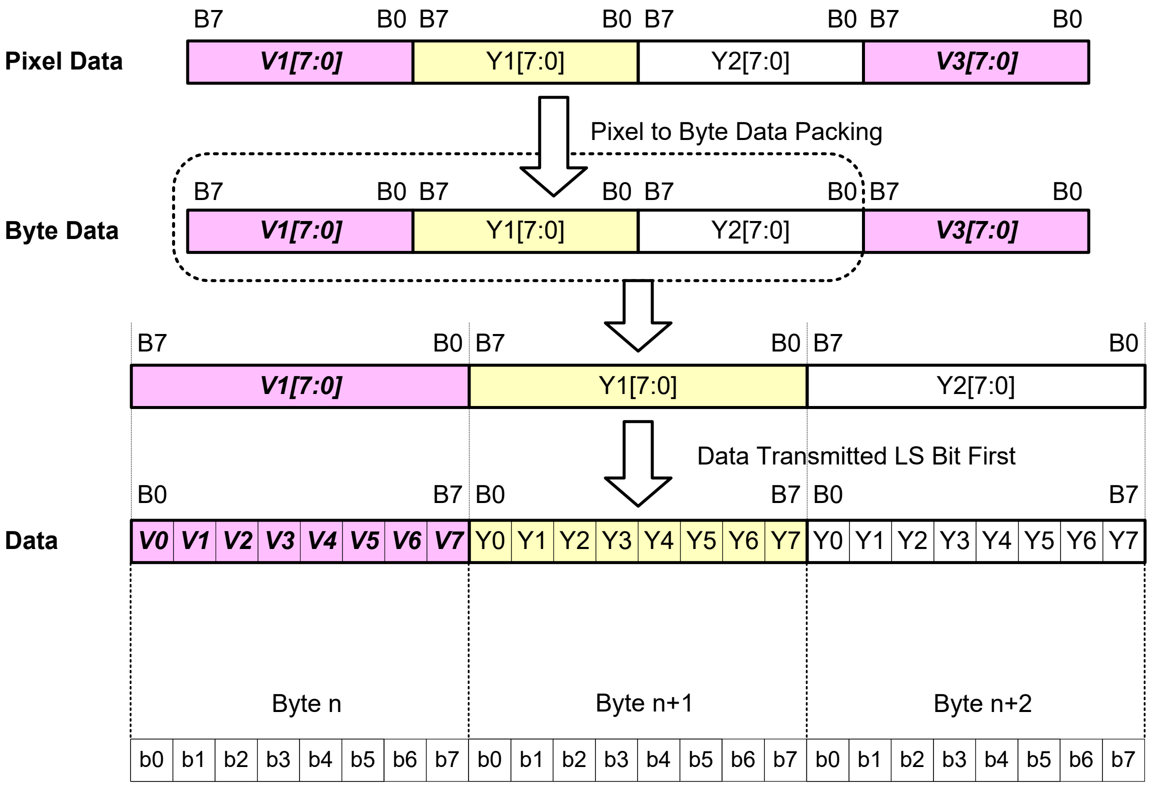


Figure 110 Legacy YUV420 8-bit Pixel to Byte Packing Bitwise Illustration

There is one spatial sampling option

- H.261, H.263 and MPEG1 Spatial Sampling (***Figure*** ~~99~~111).

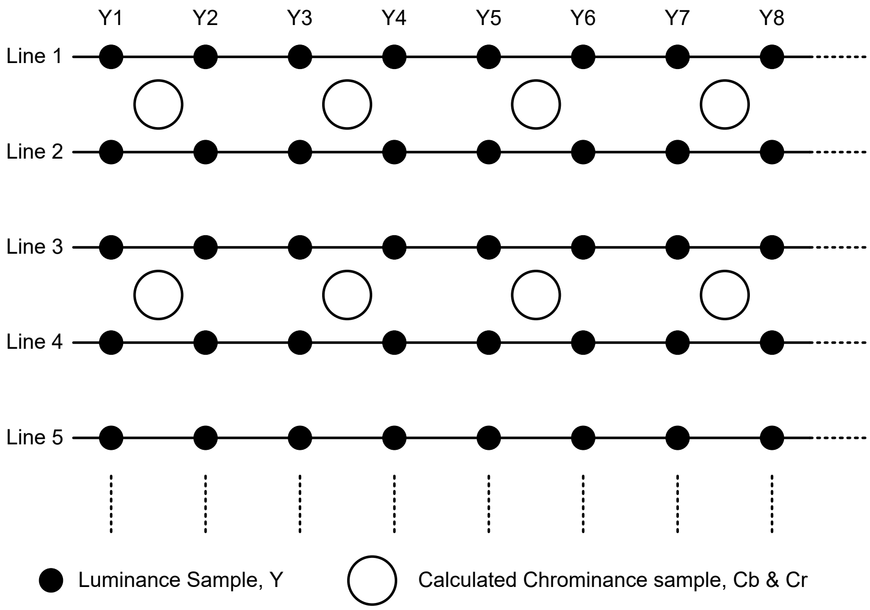


Figure 111 Legacy YUV420 Spatial Sampling for H.261, H.263 and MPEG 1

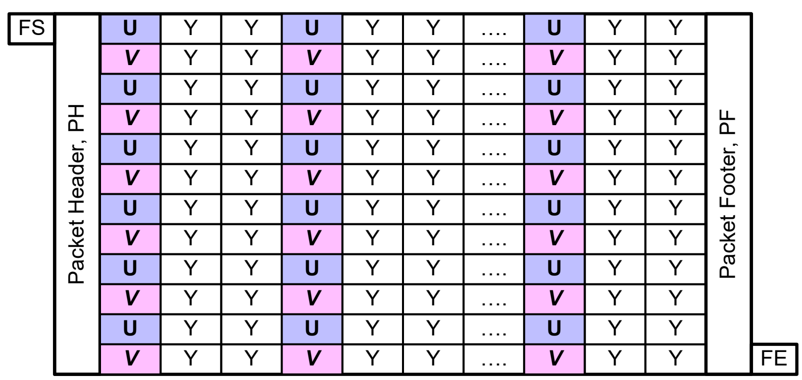


Figure 112 Legacy YUV420 8-bit Frame Format

11.2.2 YUV420 8-bit

YUV420 8-bit data transmission is performed by transmitting YYYY… / UYVYUYVY… sequences in odd / even lines. Only the luminance component (Y) is transferred for odd lines (1, 3, 5…) and both luminance (Y) and chrominance (U and V) components are transferred for even lines (2, 4, 6…). The format for the even lines (UYVY) is identical to the YUV422 8-bit data format. The data transmission sequence is illustrated in ***Figure*** ~~***101***~~***113***.

The payload data size, in bytes, for even lines (UYVY) is double the payload data size for odd lines (Y). This is exception to the general CSI-2 rule that each line shall have an equal length.

Table ~~***28***~~***42*** specifies the packet size constraints for YUV420 8-bit packets. Each packet must be a multiple of the values in the table.

Table 42 YUV420 8-bit Packet Data Size Constraints

Odd Lines (1, 3, 5...) Luminance Only, Y			Even Lines (2, 4, 6…) Luminance and Chrominance, UYVY		
Pixels	**Bytes**	**Bits**	**Pixels**	**Bytes**	**Bits**
2	2	16	2	4	32

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in ***Figure*** ~~***102***~~***114***.

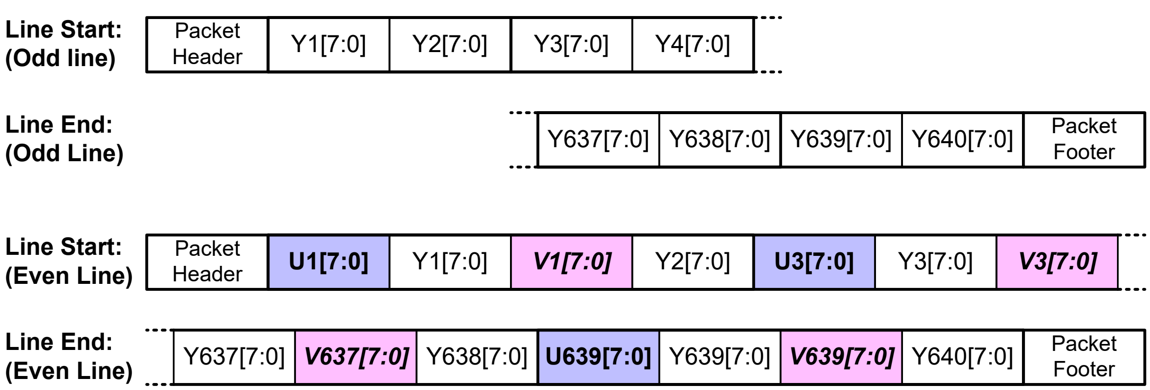


Figure 113 YUV420 8-bit Data Transmission Sequence

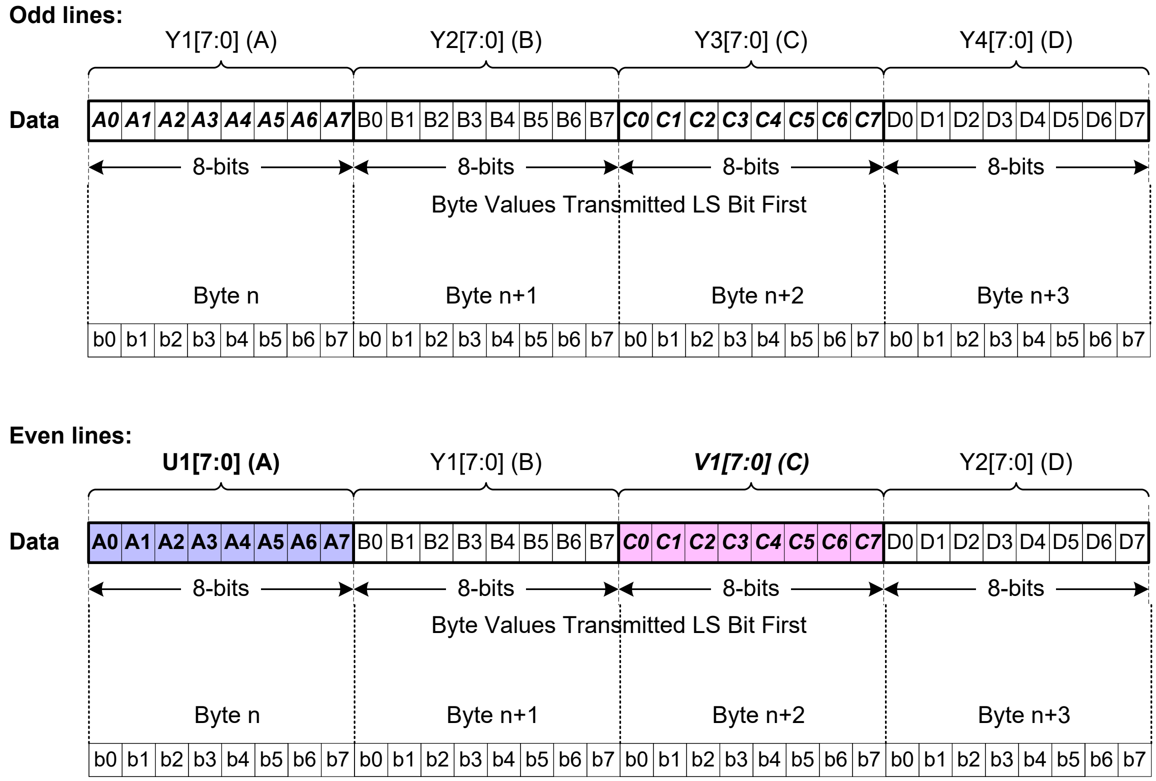
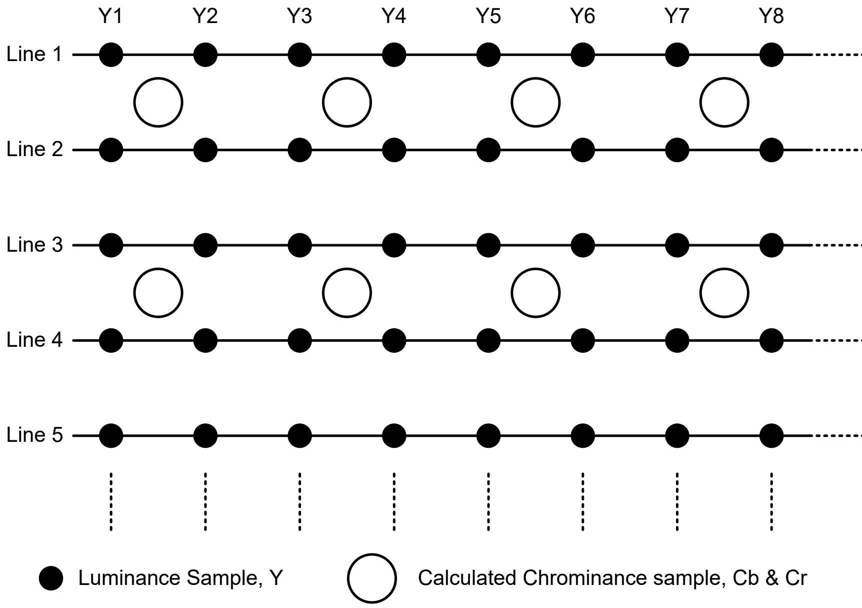


Figure 114 YUV420 8-bit Pixel to Byte Packing Bitwise Illustration

There are two spatial sampling options

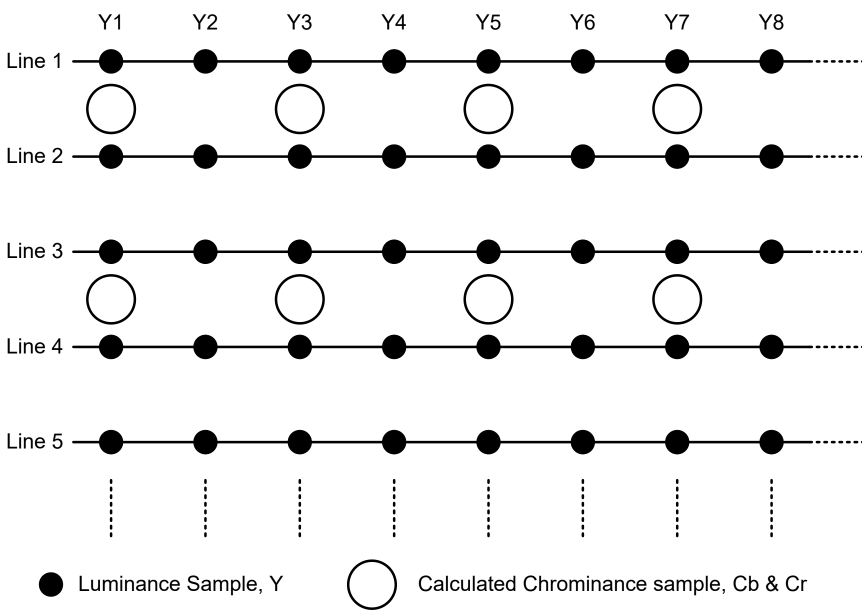
- H.261, H.263 and MPEG1 Spatial Sampling (***Figure ~~103~~115***).
- Chroma Shifted Pixel Sampling (CSPS) for MPEG2, MPEG4 (***Figure ~~104~~116***).

Figure ~~105~~117 shows the YUV420 frame format.



2339

Figure 115 YUV420 Spatial Sampling for H.261, H.263 and MPEG 1



2340

Figure 116 YUV420 Spatial Sampling for MPEG 2 and MPEG 4

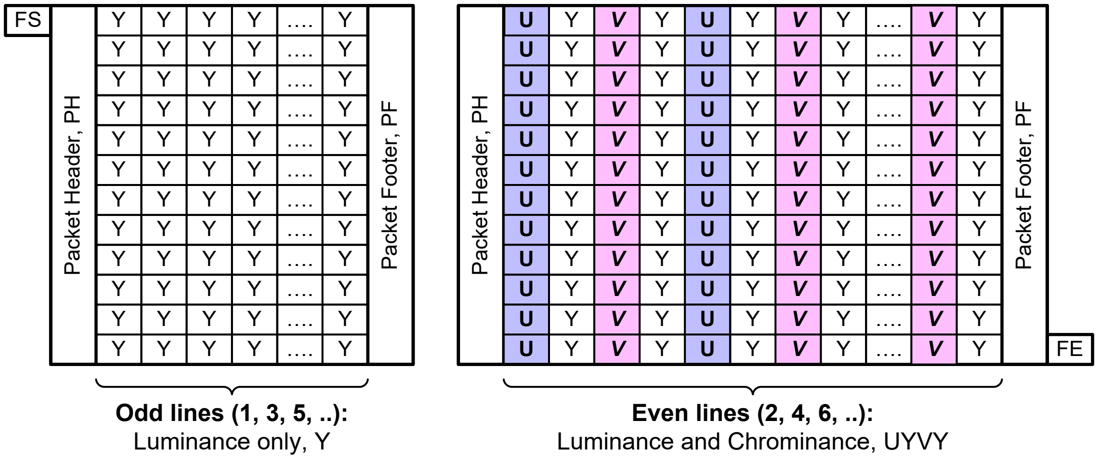


Figure 117 YUV420 8-bit Frame Format

11.2.3 YUV420 10-bit

YUV420 10-bit data transmission is performed by transmitting YYYY… / UYVYUYVY… sequences in odd / even lines. Only the luminance component (Y) is transferred in odd lines (1, 3, 5…) and both luminance (Y) and chrominance (U and V) components transferred in even lines (2, 4, 6…). The format for the even lines (UYVY) is identical to the YUV422 –10-bit data format. The sequence is illustrated in ***Figure ~~106~~118***.

The payload data size, in bytes, for even lines (UYVY) is double the payload data size for odd lines (Y). This is exception to the general CSI-2 rule that each line shall have an equal length.

Table ~~29~~43 specifies the packet size constraints for YUV420 10-bit packets. The length of each packet must be a multiple of the values in the table.

Table 43 YUV420 10-bit Packet Data Size Constraints

Odd Lines (1, 3, 5...) Luminance Only, Y			Even Lines (2, 4, 6…) Luminance and Chrominance, UYVY		
Pixels	**Bytes**	**Bits**	**Pixels**	**Bytes**	**Bits**
4	5	40	4	10	80

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel-to-byte mapping is illustrated in ***Figure ~~107~~119***.

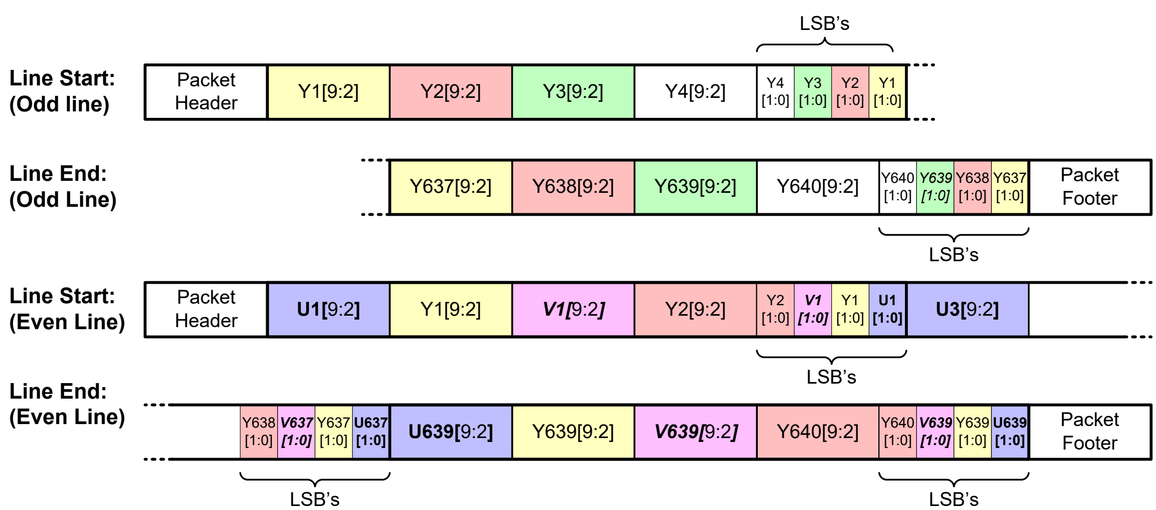
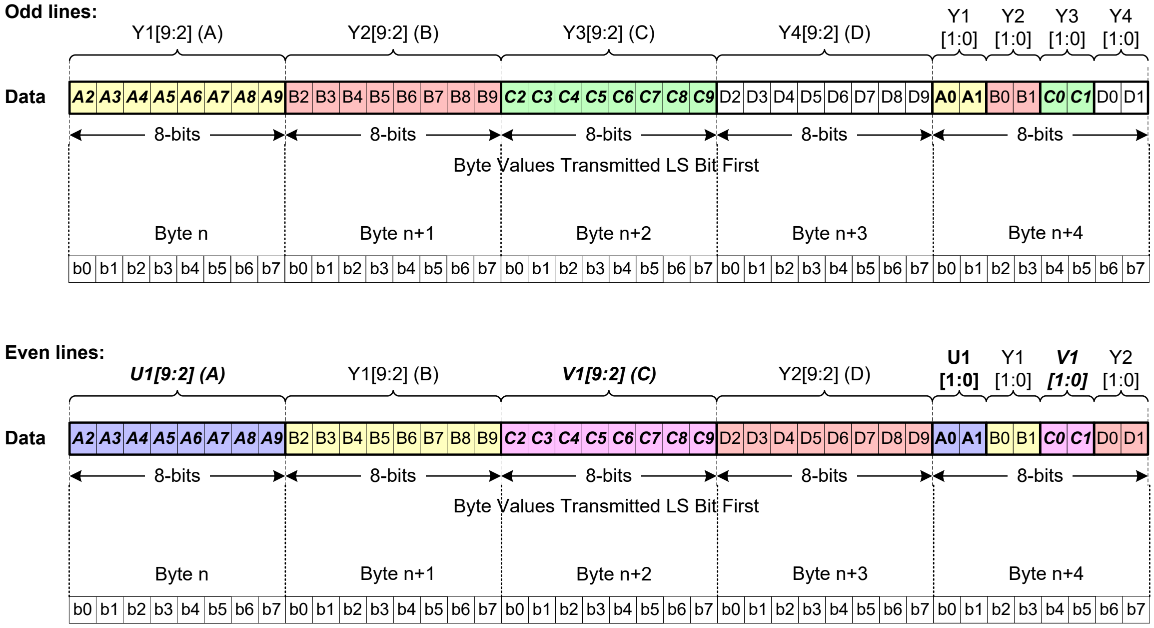


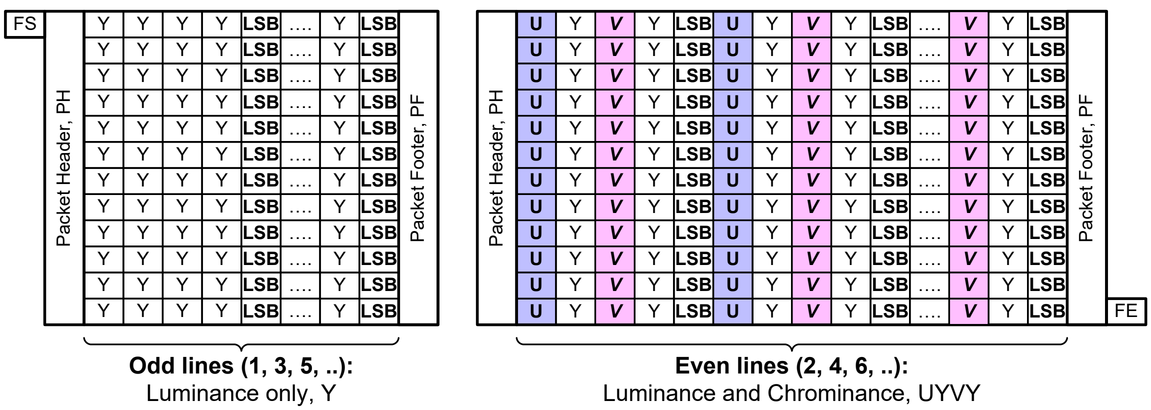
Figure 118 YUV420 10-bit Transmission



2354

Figure 119 YUV420 10-bit Pixel to Byte Packing Bitwise Illustration

2355 The pixel spatial sampling options are the same as for the YUV420 8-bit data format.



2356

Figure 120 YUV420 10-bit Frame Format

11.2.4 YUV422 8-bit

YUV422 8-bit data transmission is performed by transmitting a UYVY sequence. This sequence is illustrated in ***Figure ~~109~~121***.

Table ~~30~~44 specifies the packet size constraints for YUV422 8-bit packet. The length of each packet must be a multiple of the values in the table.

Table 44 YUV422 8-bit Packet Data Size Constraints

Pixels	Bytes	Bits
2	4	32

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in ***Figure ~~110~~122***.

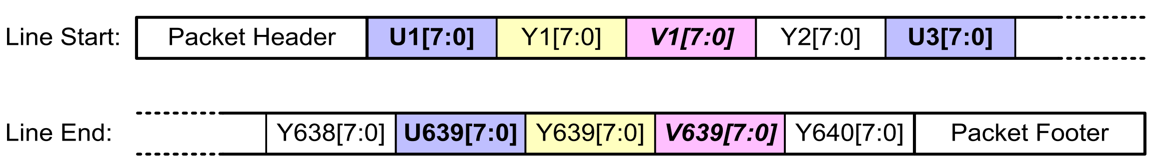


Figure 121 YUV422 8-bit Transmission

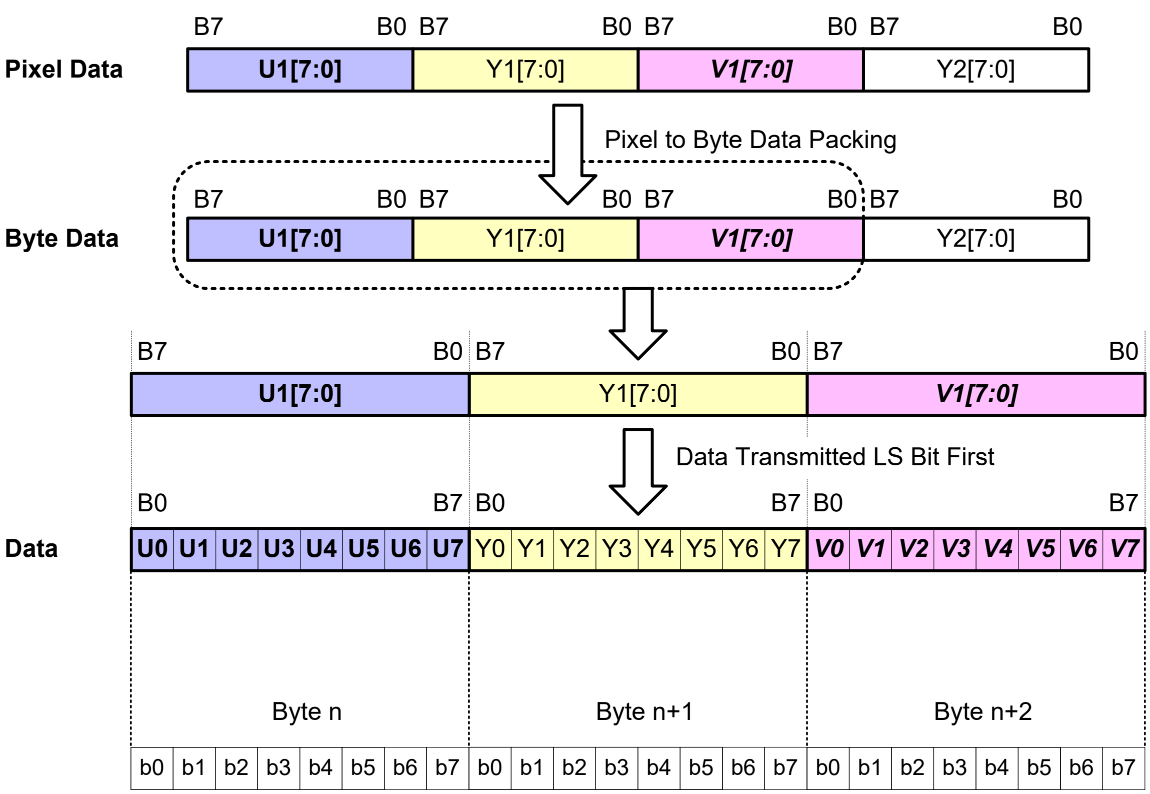


Figure 122 YUV422 8-bit Pixel to Byte Packing Bitwise Illustration

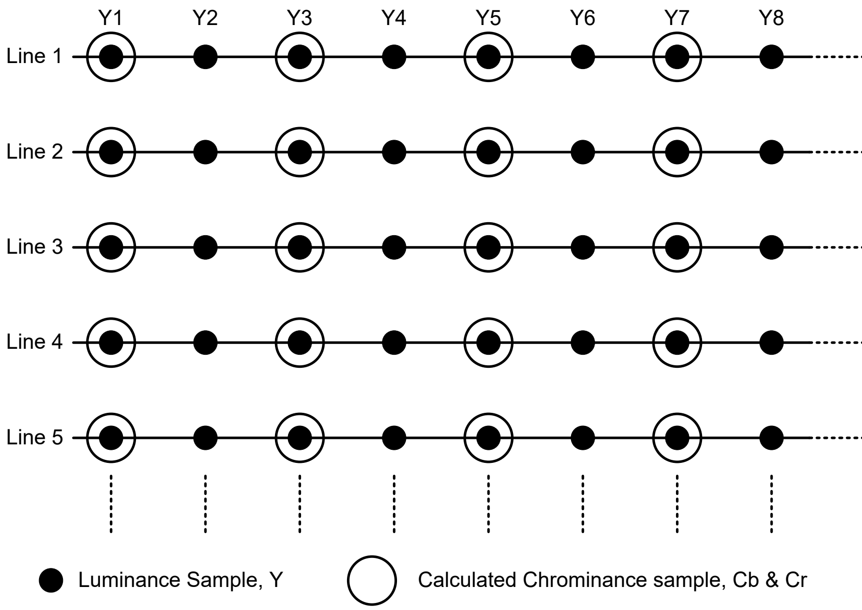


Figure 123 YUV422 Co-sited Spatial Sampling

The pixel spatial alignment is the same as in CCIR-656 standard. The frame format for YUV422 is presented in ***Figure*** ~~*112*~~*124*.

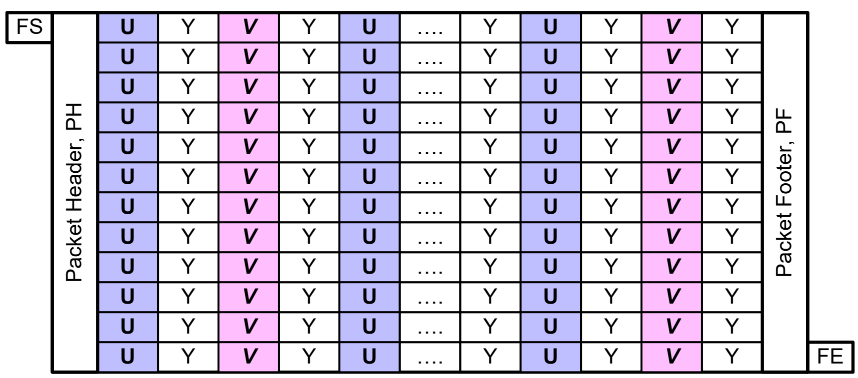


Figure 124 YUV422 8-bit Frame Format

11.2.5 YUV422 10-bit

YUV422 10-bit data transmission is performed by transmitting a UYVY sequence. This sequence is illustrated in ***Figure*** ~~***113***~~***125***.

Table ~~***31***~~***45*** specifies the packet size constraints for YUV422 10-bit packet. The length of each packet must be a multiple of the values in the table.

Table 45 YUV422 10-bit Packet Data Size Constraints

Pixels	Bytes	Bits
2	5	40

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in ***Figure*** ~~***114***~~***126***.

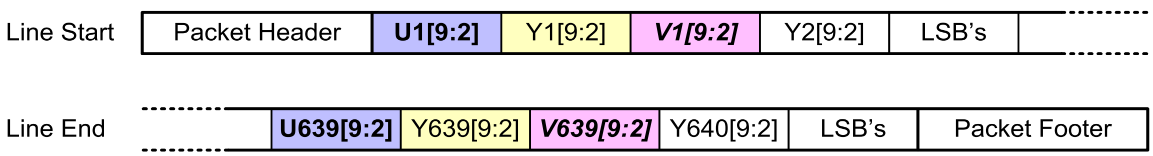


Figure 125 YUV422 10-bit Transmitted Bytes

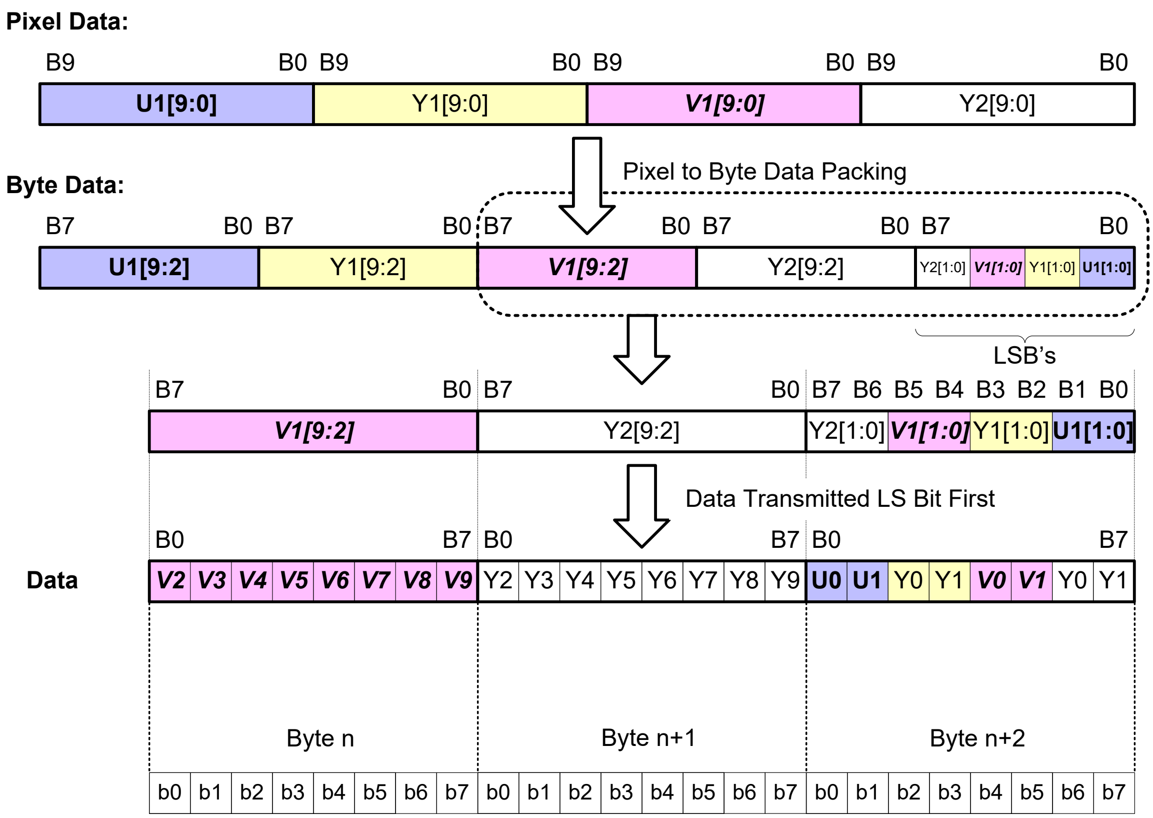


Figure 126 YUV422 10-bit Pixel to Byte Packing Bitwise Illustration

The pixel spatial alignment is the same as in the YUV422 8-bit data case. The frame format for YUV422 is presented in the ***Figure ~~115~~127***.

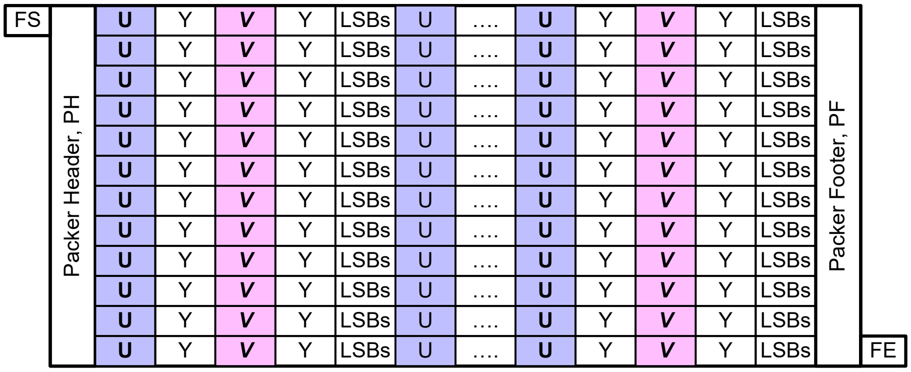


Figure 127 YUV422 10-bit Frame Format

11.3 RGB Image Data

2382 ***Table*** ~~*32*~~***46*** defines the data type codes for RGB data formats described in this section.

2383 **Table 46 RGB Image Data Types**

Data Type	Description
0x20	RGB444
0x21	RGB555
0x22	RGB565
0x23	RGB666
0x24	RGB888
0x25	Reserved
0x26	Reserved
~~0x27~~	~~Reserved~~

11.3.1 RGB888

RGB888 data transmission is performed by transmitting a BGR byte sequence. This sequence is illustrated in ***Figure*** ***~~116~~128***. The RGB888 frame format is illustrated in ***Figure*** ***~~118~~130***.

Table ***~~33~~47*** specifies the packet size constraints for RGB888 packets. The length of each packet must be a multiple of the values in the table.

Table 47 RGB888 Packet Data Size Constraints

Pixels	Bytes	Bits
1	3	24

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in ***Figure*** ***~~117~~129***.

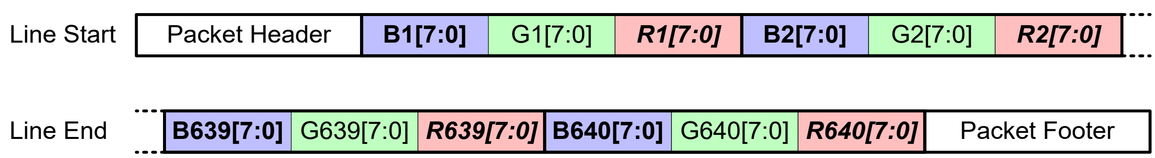


Figure 128 RGB888 Transmission

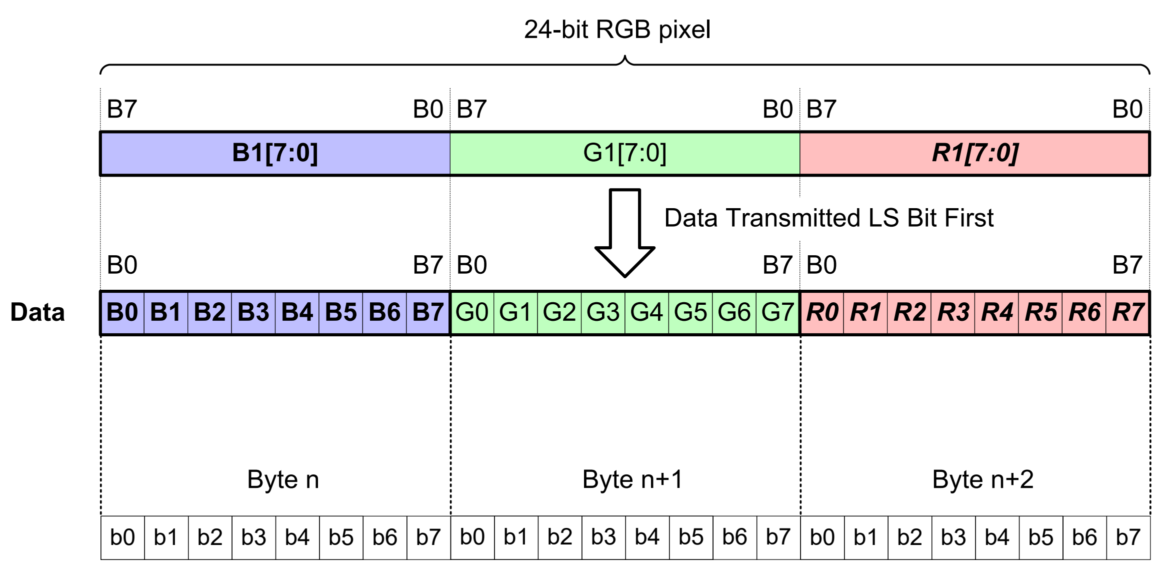


Figure 129 RGB888 Transmission in CSI-2 Bus Bitwise Illustration

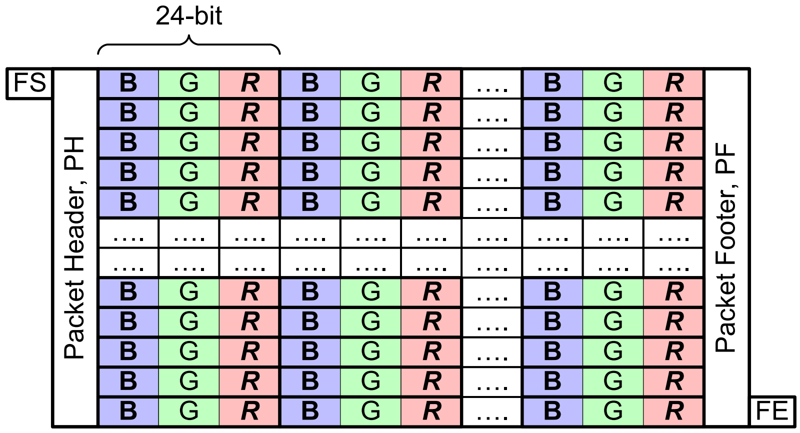


Figure 130 RGB888 Frame Format

11.3.2 RGB666

RGB666 data transmission is performed by transmitting a B0…5, G0…5, and R0…5 (18-bit) sequence. This sequence is illustrated in ***Figure ~~119~~131***. The frame format for RGB666 is presented in the ***Figure ~~121~~133***.

Table ~~34~~48 specifies the packet size constraints for RGB666 packets. The length of each packet must be a multiple of the values in the table.

Table 48 RGB666 Packet Data Size Constraints

Pixels	Bytes	Bits
4	9	72

Bit order in transmission follows the general CSI-2 rule, LSB first. In RGB666 case the length of one data word is 18-bits, not eight bits. The word-wise flip is done for 18-bit BGR words; i.e. instead of flipping each byte (8-bits), each 18-bits pixel value is flipped. This is illustrated in ***Figure ~~120~~132***.

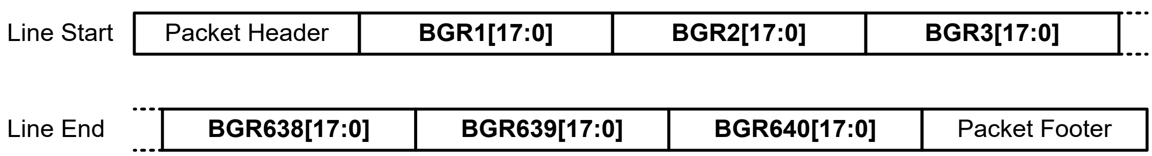


Figure 131 RGB666 Transmission with 18-bit BGR Words

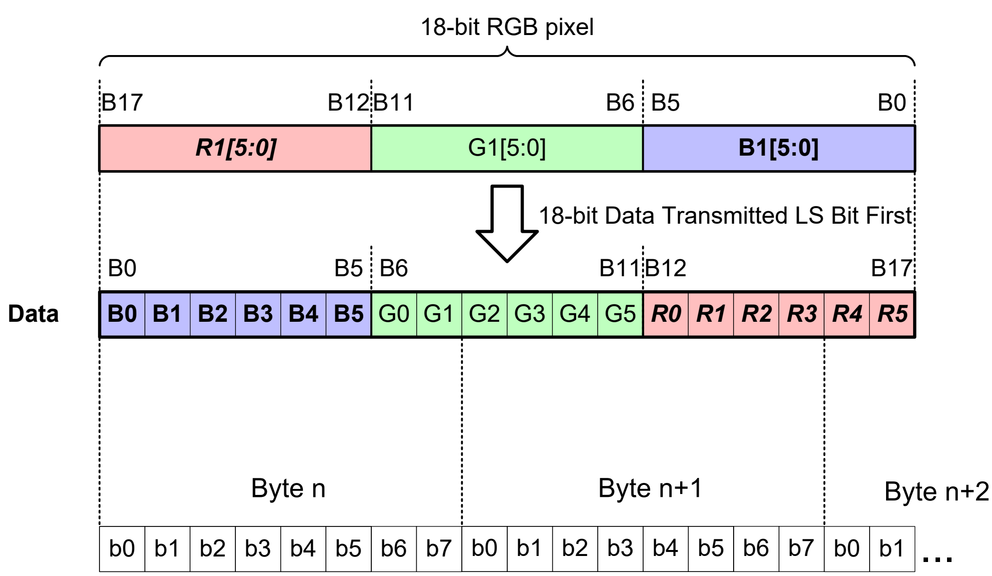


Figure 132 RGB666 Transmission on CSI-2 Bus Bitwise Illustration

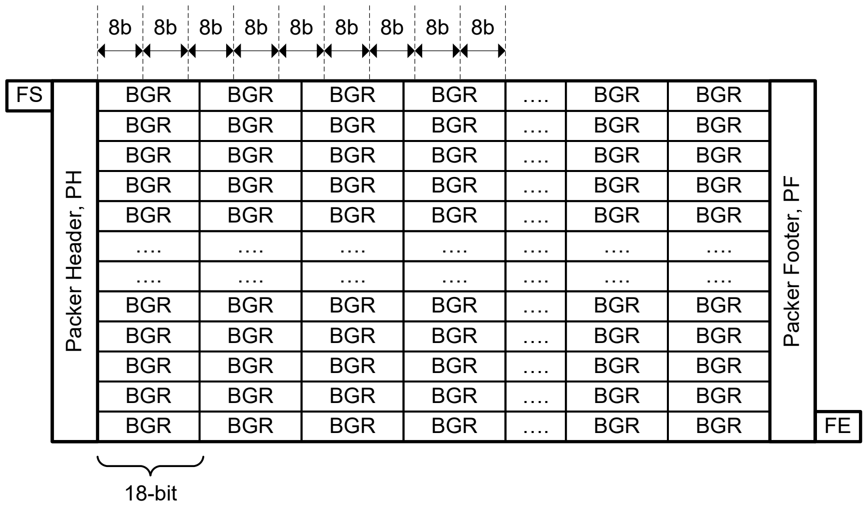


Figure 133 RGB666 Frame Format

11.3.3 RGB565

RGB565 data transmission is performed by transmitting B0…B4, G0…G5, R0…R4 in a 16-bit sequence. This sequence is illustrated in ***Figure ~~122~~134***. The frame format for RGB565 is presented in the ***Figure ~~124~~136***.

Table ~~35~~49 specifies the packet size constraints for RGB565 packets. The length of each packet must be a multiple of the values in the table.

Table 49 RGB565 Packet Data Size Constraints

Pixels	Bytes	Bits
1	2	16

Bit order in transmission follows the general CSI-2 rule, LSB first. In RGB565 case the length of one data word is 16-bits, not eight bits. The word-wise flip is done for 16-bit BGR words; i.e. instead of flipping each byte (8-bits), each two bytes (16-bits) are flipped. This is illustrated in ***Figure ~~123~~135***.

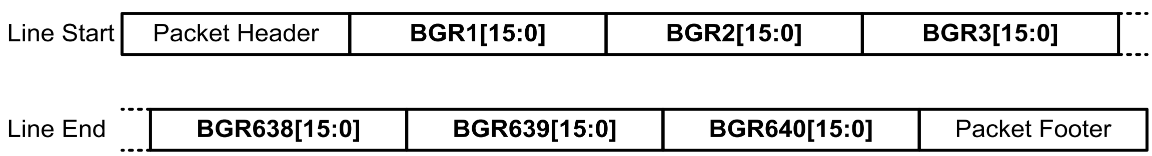


Figure 134 RGB565 Transmission with 16-bit BGR Words

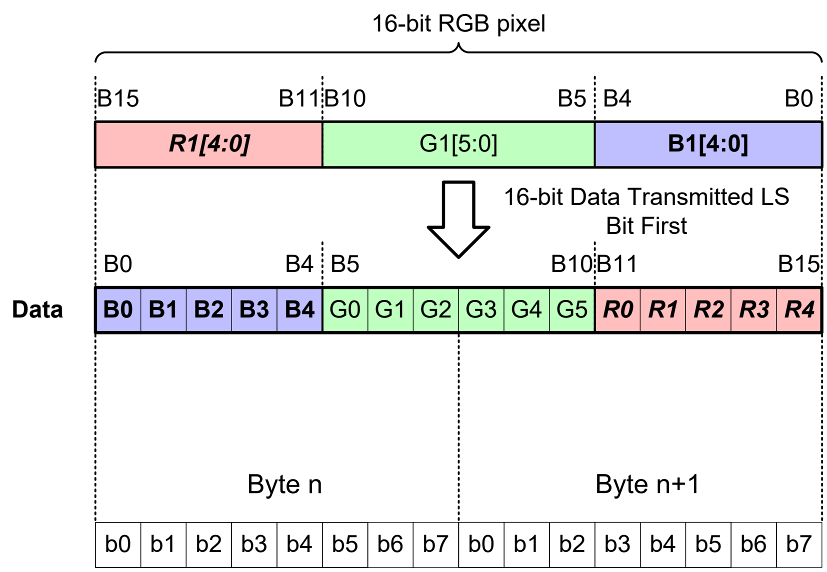


Figure 135 RGB565 Transmission on CSI-2 Bus Bitwise Illustration

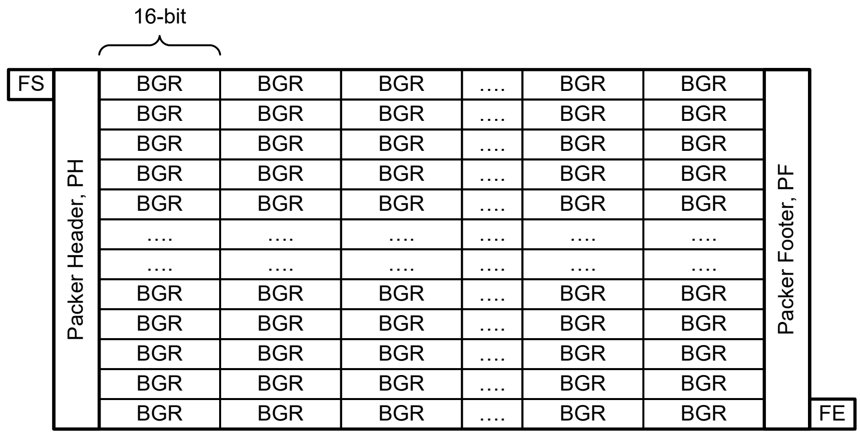


Figure 136 RGB565 Frame Format

11.3.4 RGB555

RGB555 data can be transmitted over a CSI-2 bus with some special arrangements. The RGB555 data should be made to look like RGB565 data. This can be accomplished by inserting padding bits to the LSBs of the green color component as illustrated in ***Figure ~~125~~137***.

Both the frame format and the package size constraints are the same as the RGB565 case.

Bit order in transmission follows the general CSI-2 rule, LSB first. In RGB555 case the length of one data word is 16-bits, not eight bits. The word-wise flip is done for 16-bit BGR words; i.e. instead of flipping each byte (8-bits), each two bytes (16-bits) are flipped. This is illustrated in ***Figure ~~125~~137***.

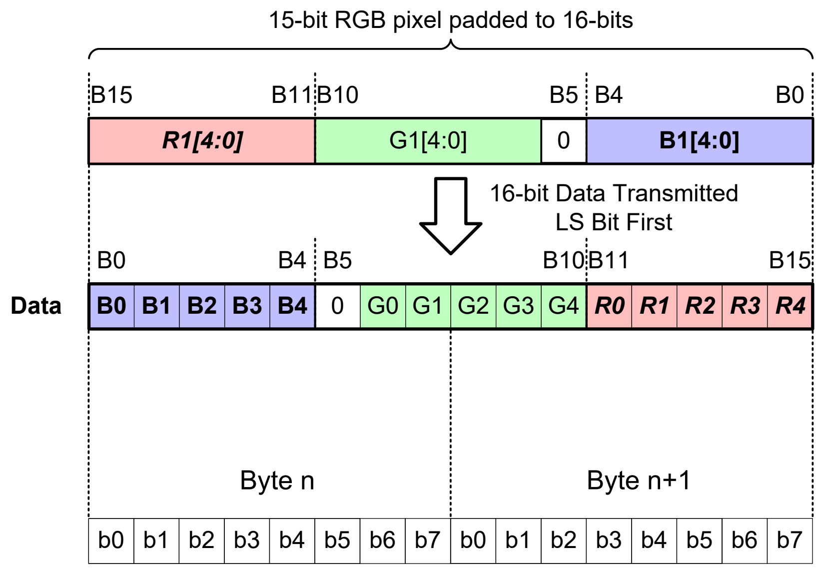


Figure 137 RGB555 Transmission on CSI-2 Bus Bitwise Illustration

11.3.5 RGB444

RGB444 data can be transmitted over a CSI-2 bus with some special arrangements. The RGB444 data should be made to look like RGB565 data. This can be accomplished by inserting padding bits to the LSBs of each color component as illustrated in ***Figure*** ~~***126***~~***138***.

Both the frame format and the package size constraints are the same as the RGB565 case.

Bit order in transmission follows the general CSI-2 rule, LSB first. In RGB444 case the length of one data word is 16-bits, not eight bits. The word-wise flip is done for 16-bit BGR words; i.e. instead of flipping each byte (8-bits), each two bytes (16-bits) are flipped. This is illustrated in ***Figure*** ~~***126***~~***138***.

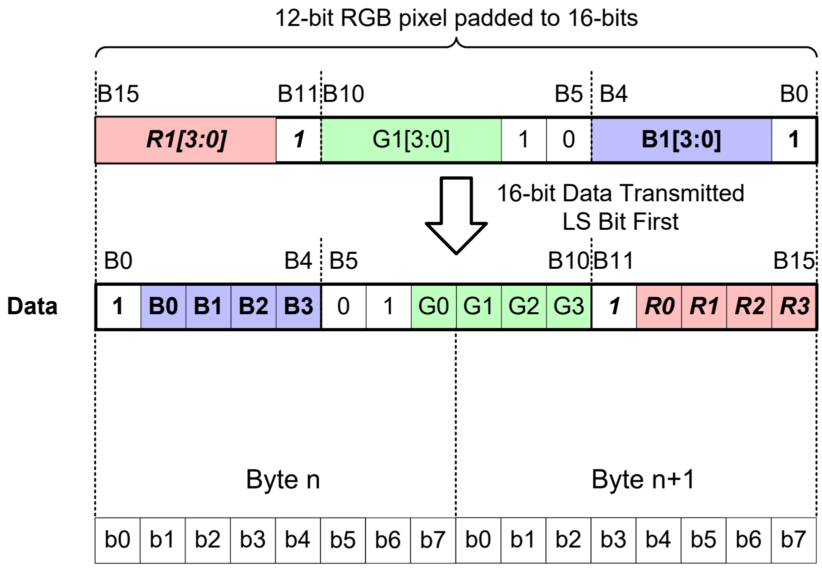


Figure 138 RGB444 Transmission on CSI-2 Bus Bitwise Illustration

11.4 RAW Image Data

The RAW 6/7/8/10/12/14/16/20/24 modes are used for transmitting Raw image data from the image sensor.

The intent is that Raw image data is unprocessed image data (i.e. Raw Bayer data) or complementary color data, but RAW image data is not limited to these data types.

It is possible to transmit e.g. light shielded pixels in addition to effective pixels. This leads to a situation where the line length is longer than sum of effective pixels per line. The line length, if not specified otherwise, has to be a multiple of word (32 bits).

Table ~~36~~50 defines the data type codes for RAW data formats described in this section.

Table 50 RAW Image Data Types

Data Type	Description
0x27	RAW24
0x28	RAW6
0x29	RAW7
0x2A	RAW8
0x2B	RAW10
0x2C	RAW12
0x2D	RAW14
0x2E	RAW16
0x2F	RAW20

11.4.1 RAW6

The 6-bit Raw data transmission is done by transmitting the pixel data over CSI-2 bus. ~~Each line is separated by line start / end synchronization codes.~~ This sequence is illustrated in ***Figure ~~127~~139*** (VGA case). ***Table ~~37~~51*** specifies the packet size constraints for RAW6 packets. The length of each packet must be a multiple of the values in the table.

Table 51 RAW6 Packet Data Size Constraints

Pixels	Bytes	Bits
4	3	24

Each 6-bit pixel is sent LSB first. This is an exception to general CSI-2 rule byte wise LSB first.

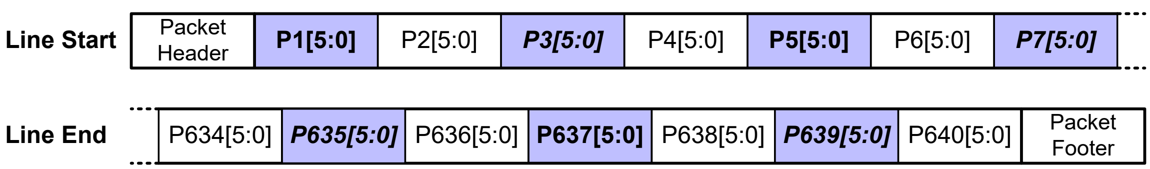


Figure 139 RAW6 Transmission

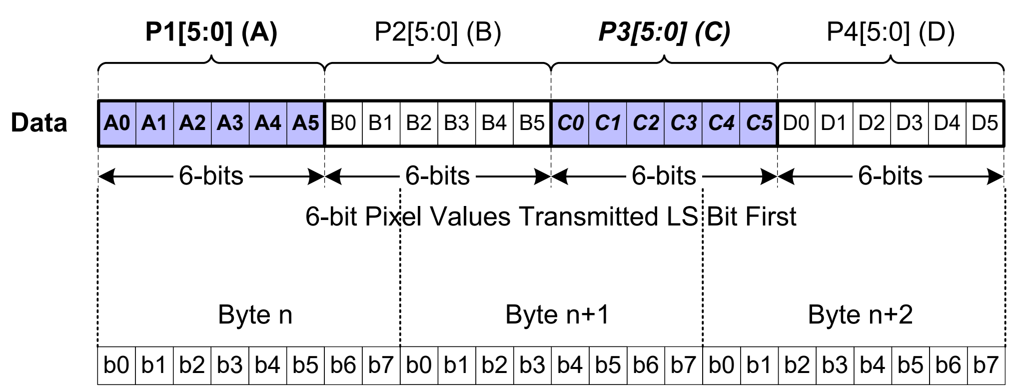


Figure 140 RAW6 Data Transmission on CSI-2 Bus Bitwise Illustration

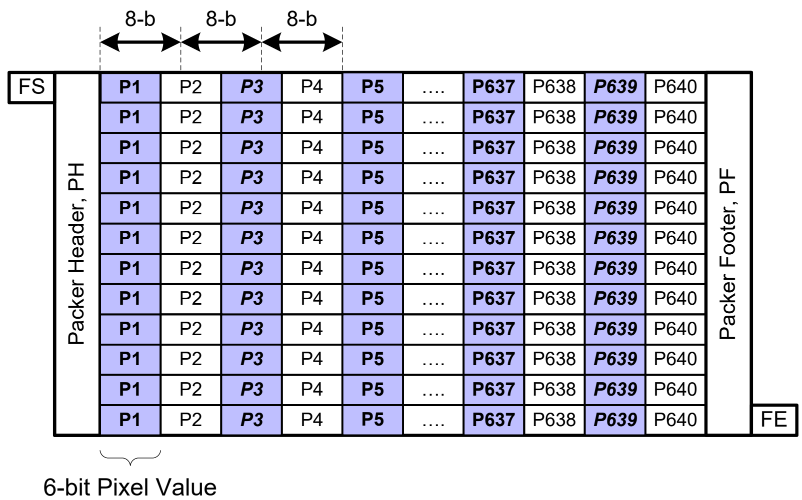


Figure 141 RAW6 Frame Format

11.4.2 RAW7

The 7-bit Raw data transmission is done by transmitting the pixel data over CSI-2 bus. ~~Each line is separated by line start / end synchronization codes.~~ This sequence is illustrated in ***Figure ~~130~~142*** (VGA case). ***Table ~~38~~52*** specifies the packet size constraints for RAW7 packets. The length of each packet must be a multiple of the values in the table.

Table 52 RAW7 Packet Data Size Constraints

Pixels	Bytes	Bits
8	7	56

Each 7-bit pixel is sent LSB first. This is an exception to general CSI-2 rule byte-wise LSB first.

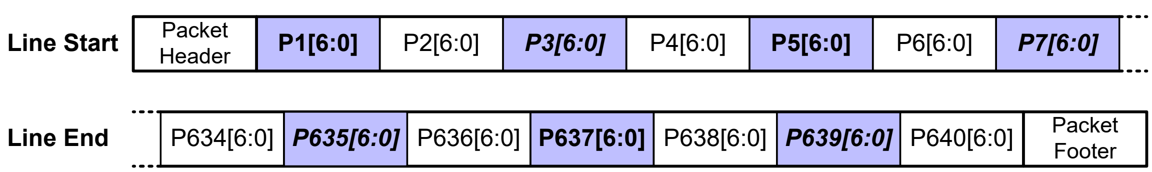


Figure 142 RAW7 Transmission

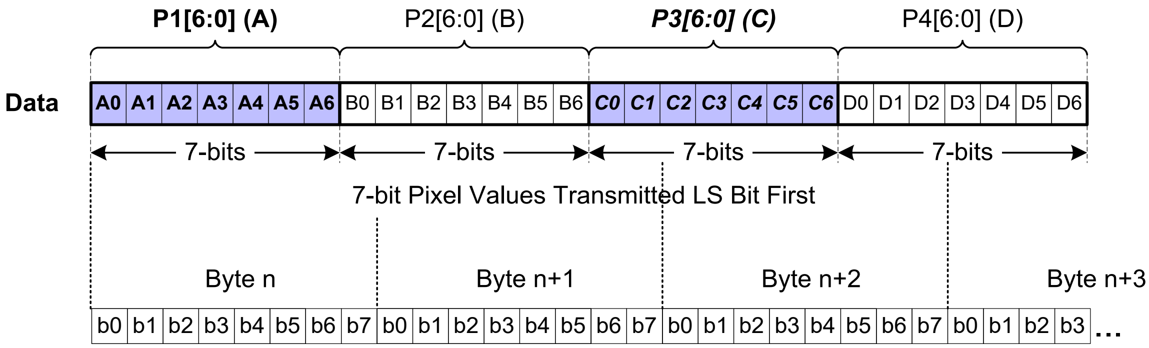


Figure 143 RAW7 Data Transmission on CSI-2 Bus Bitwise Illustration

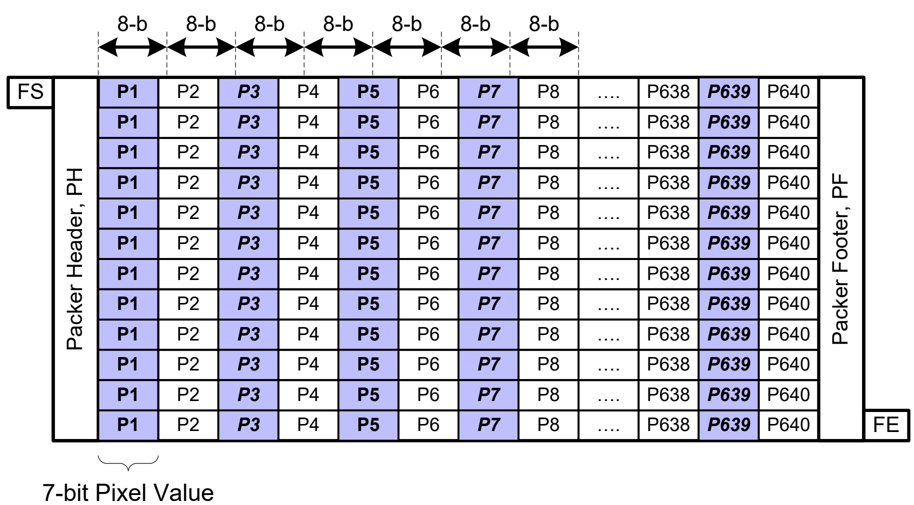


Figure 144 RAW7 Frame Format

11.4.3 RAW8

The 8-bit Raw data transmission is done by transmitting the pixel data over a CSI-2 bus. ***Table ~~39~~53*** specifies the packet size constraints for RAW8 packets. The length of each packet must be a multiple of the values in the table.

Table 53 RAW8 Packet Data Size Constraints

Pixels	Bytes	Bits
1	1	8

This sequence is illustrated in ***Figure ~~133~~145*** (VGA case).

Bit order in transmission follows the general CSI-2 rule, LSB first.

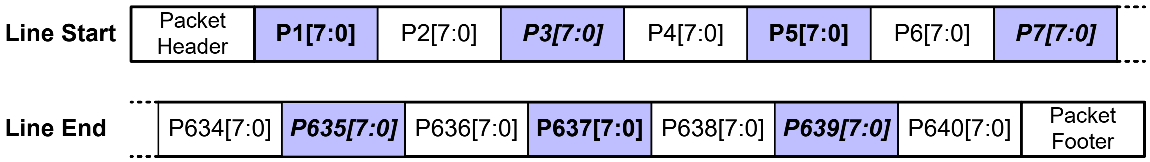


Figure 145 RAW8 Transmission

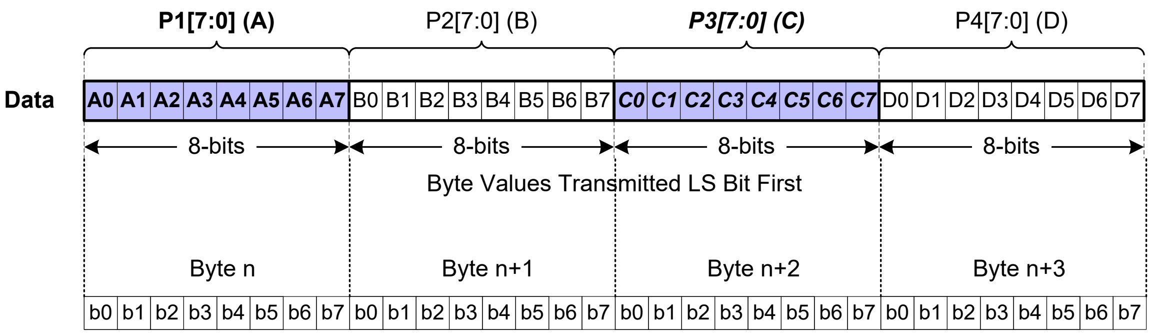


Figure 146 RAW8 Data Transmission on CSI-2 Bus Bitwise Illustration

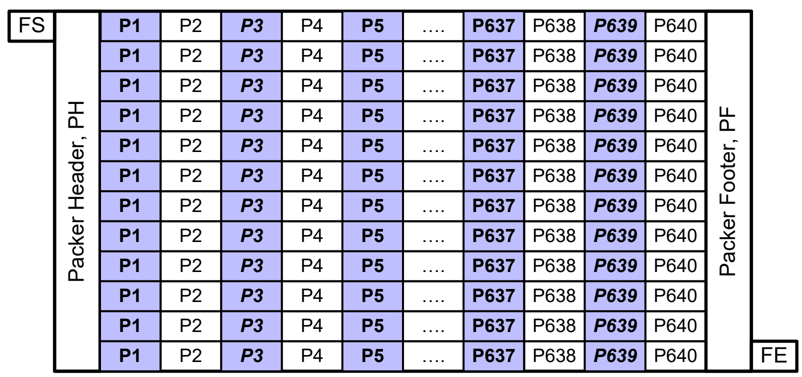


Figure 147 RAW8 Frame Format

11.4.4 RAW10

The transmission of 10-bit Raw data is done by packing the 10-bit pixel data to look like 8-bit data format. ***Table*** ~~***40***~~***54*** specifies the packet size constraints for RAW10 packets. The length of each packet must be a multiple of the values in the table.

Table 54 RAW10 Packet Data Size Constraints

Pixels	Bytes	Bits
4	5	40

This sequence is illustrated in ***Figure*** ~~***136***~~***148*** (VGA case).

Bit order in transmission follows the general CSI-2 rule: LSB first.

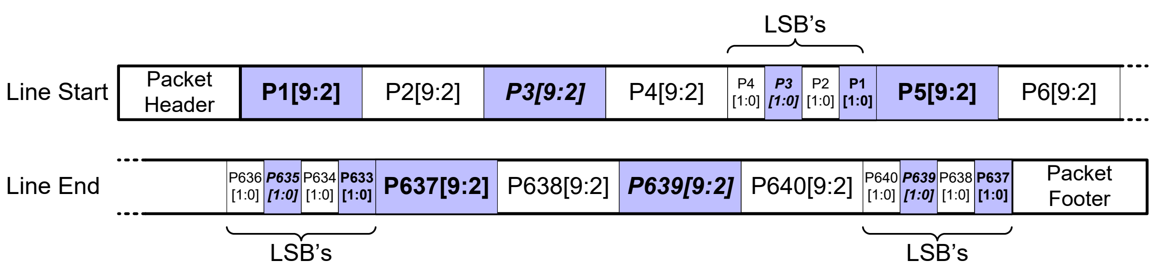


Figure 148 RAW10 Transmission

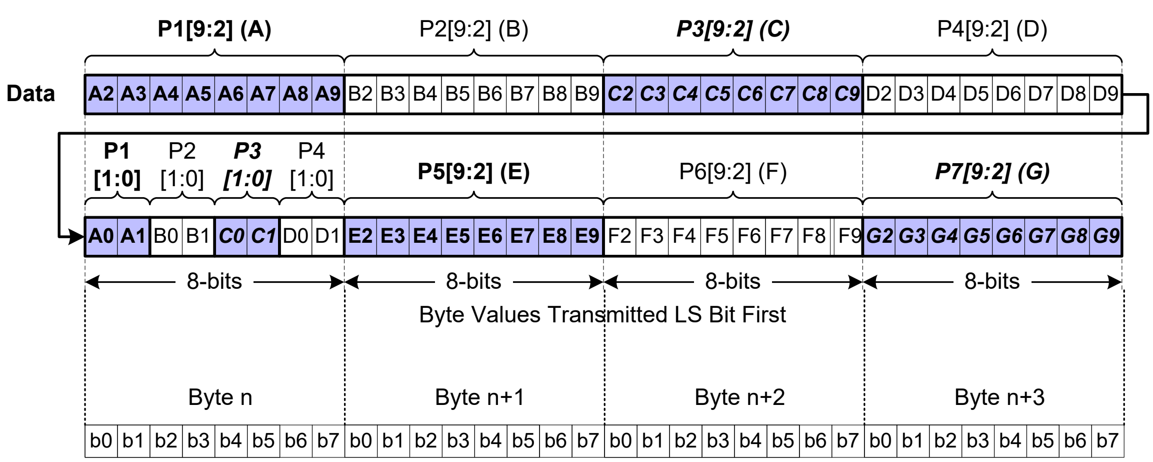


Figure 149 RAW10 Data Transmission on CSI-2 Bus Bitwise Illustration

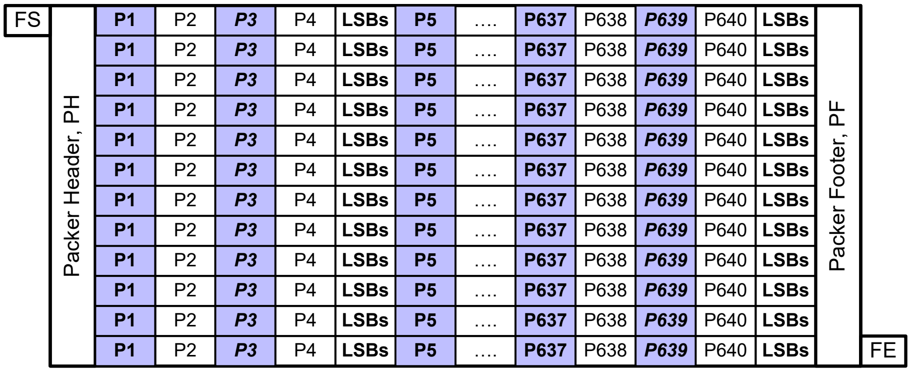


Figure 150 RAW10 Frame Format

11.4.5 RAW12

The transmission of 12-bit Raw data is done by packing the 12-bit pixel data to look like 8-bit data format. ***Table*** ~~*41*~~*55* specifies the packet size constraints for RAW12 packets. The length of each packet must be a multiple of the values in the table.

Table 55 RAW12 Packet Data Size Constraints

Pixels	Bytes	Bits
2	3	24

This sequence is illustrated in ***Figure*** ~~*139*~~*151* (VGA case).

Bit order in transmission follows the general CSI-2 rule: LSB first.

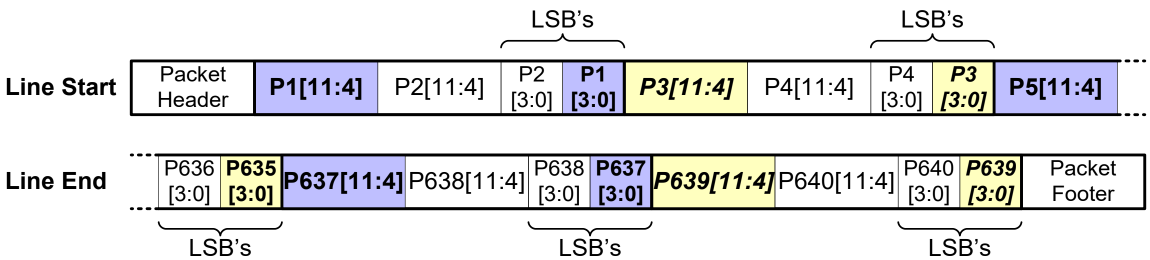


Figure 151 RAW12 Transmission

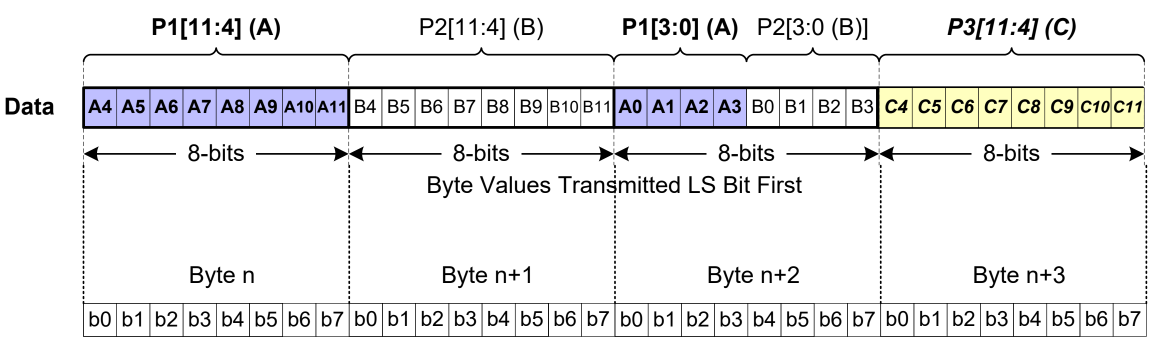


Figure 152 RAW12 Transmission on CSI-2 Bus Bitwise Illustration

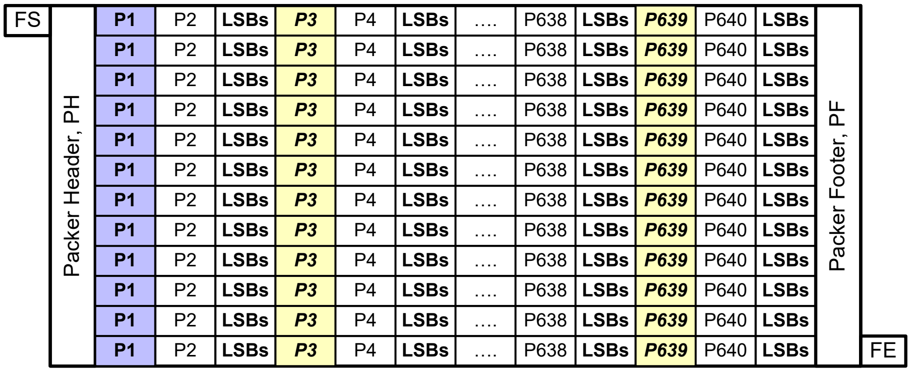


Figure 153 RAW12 Frame Format

11.4.6 RAW14

The transmission of 14-bit Raw data is done by packing the 14-bit pixel data in 8-bit slices. For every four pixels, seven bytes of data is generated. ***Table ~~42~~56*** specifies the packet size constraints for RAW14 packets. The length of each packet must be a multiple of the values in the table.

Table 56 RAW14 Packet Data Size Constraints

Pixels	Bytes	Bits
4	7	56

The sequence is illustrated in ***Figure ~~142~~154*** (VGA case).

The LS bits for P1, P2, P3, and P4 are distributed in three bytes as shown in ***Figure ~~142~~154*** and ***Figure ~~143~~155***. The same is true for the LS bits for P637, P638, P639, and P640. The bit order during byte transmission follows the general CSI-2 rule, i.e. LSB first.

Note:

> ***Figure ~~142~~154*** *has been modified relative to the figures shown in the CSI-2 Specification version 2.0 and earlier, in order to more clearly correspond with* ***Figure ~~143~~155****. The RAW14 byte packing and transmission formats themselves have not changed relative to earlier CSI-2 Specification versions.*

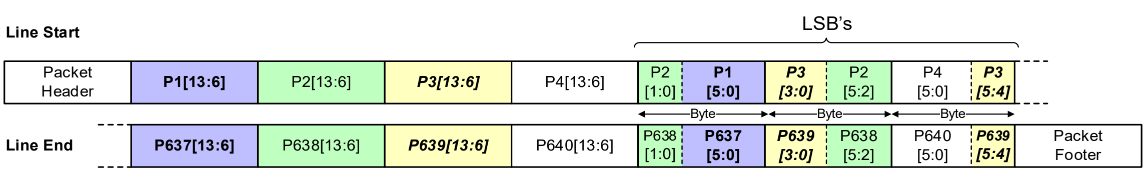


Figure 154 RAW14 Transmission

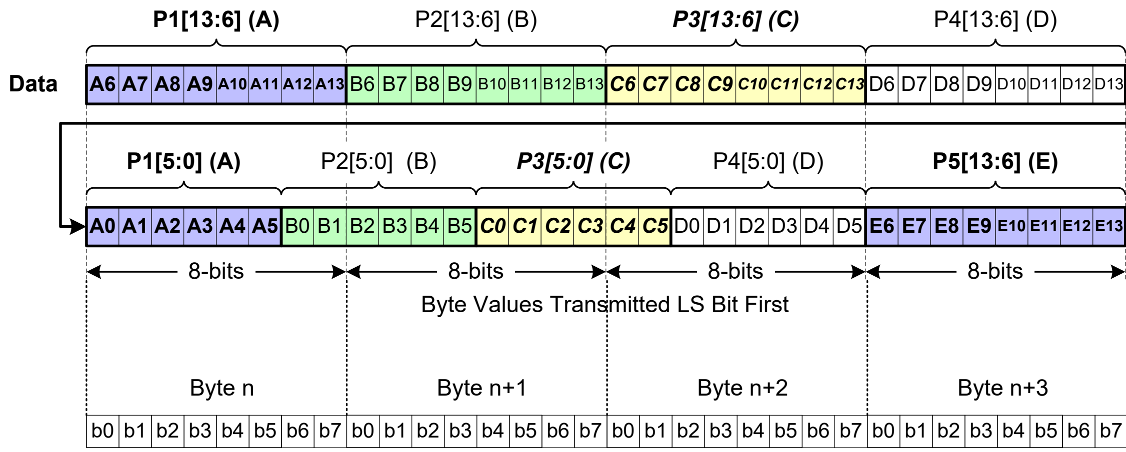


Figure 155 RAW14 Transmission on CSI-2 Bus Bitwise Illustration

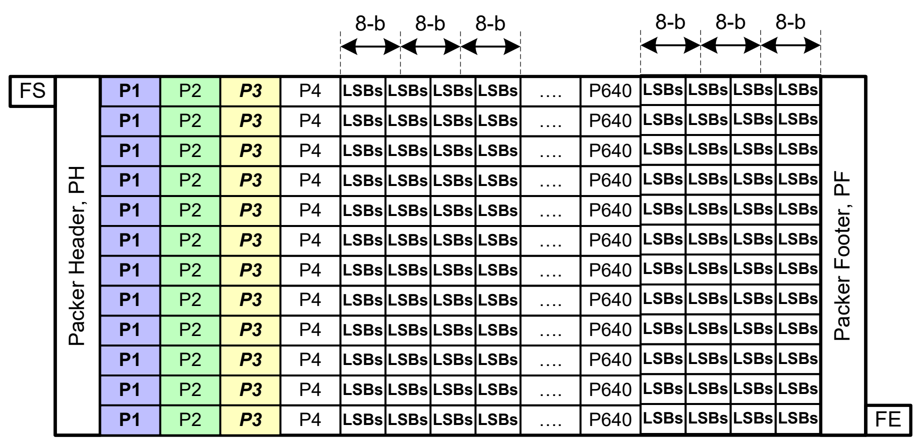


Figure 156 RAW14 Frame Format

11.4.7 RAW16

The transmission of 16-bit Raw data is done by packing the 16-bit pixel data to look like the 8-bit data format. ***Table*** ~~***43***~~***57*** specifies the packet size constraints for RAW16 packets. The length of each packet must be a multiple of the values in the table.

Table 57 RAW16 Packet Data Size Constraints

Pixels	Bytes	Bits
1	2	16

This sequence is illustrated in ***Figure*** ~~***145***~~***157*** (VGA case).

Bit order in transmission follows the general CSI-2 rule: LSB first.

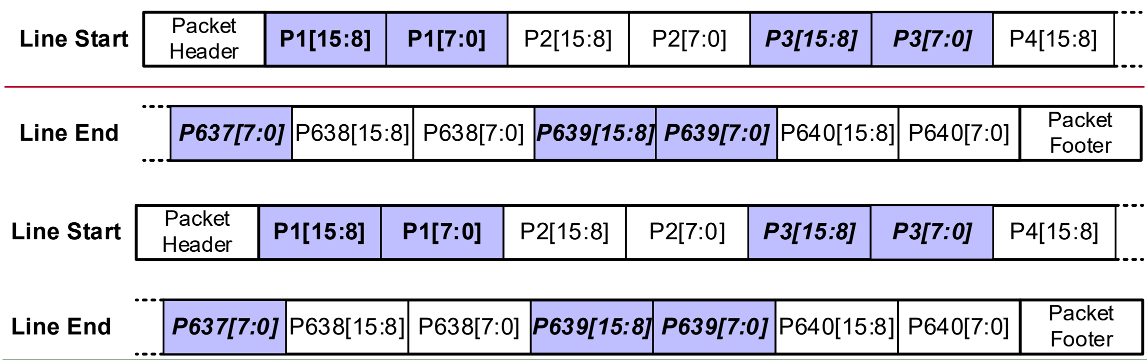


Figure 157 RAW16 Transmission

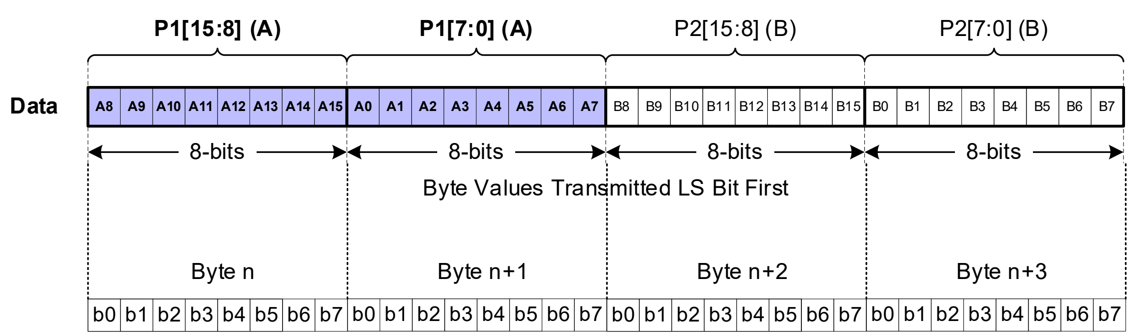
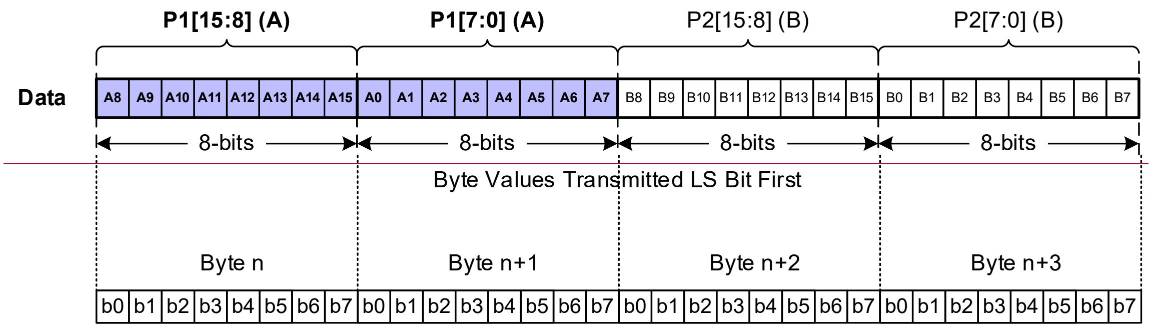
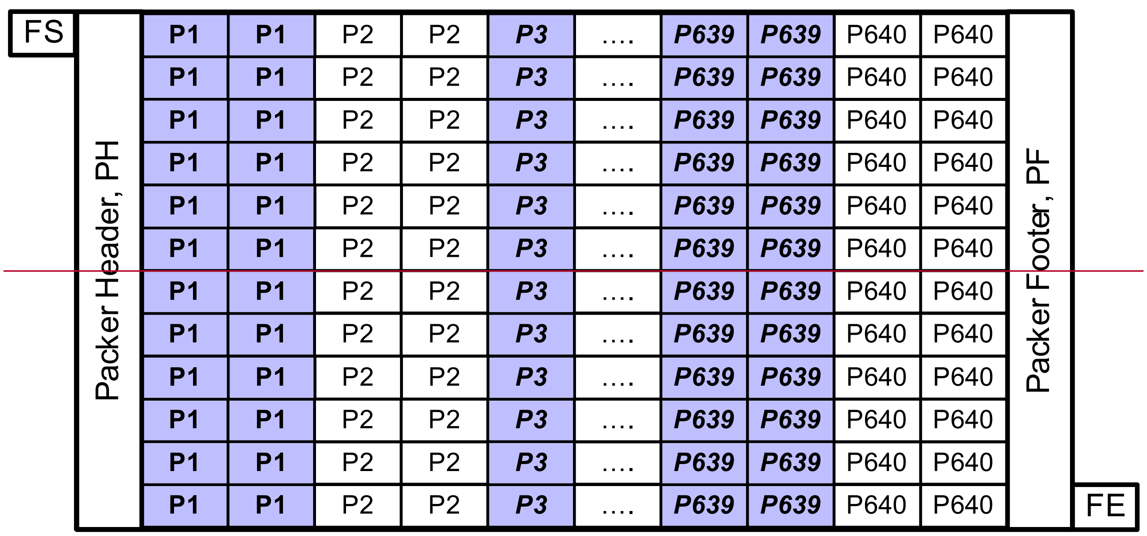


Figure 158 RAW16 Transmission on CSI-2 Bus Bitwise Illustration

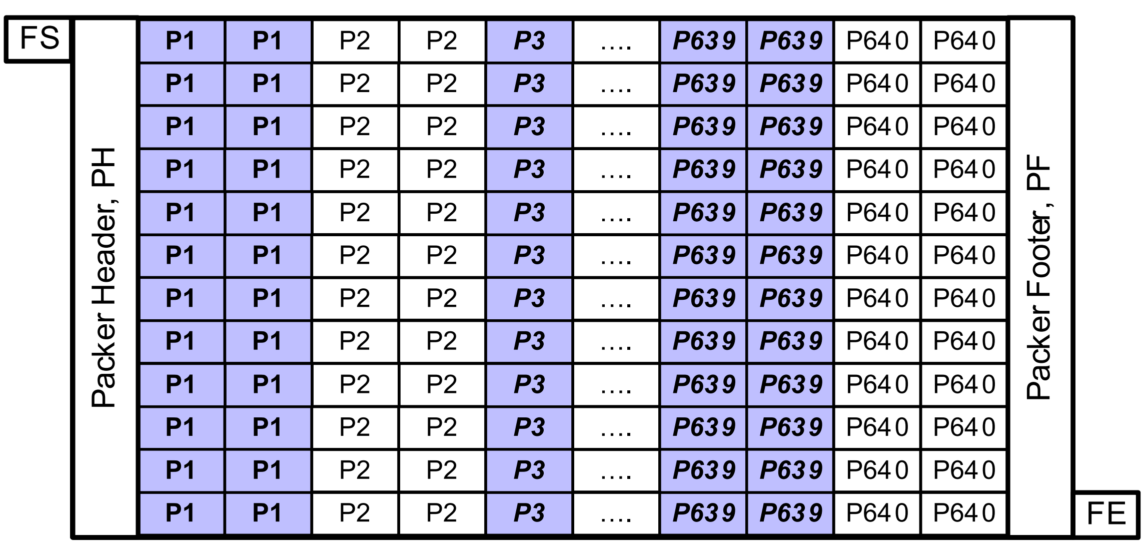


2510

~~**Figure 146 RAW16 Transmission on CSI-2 Bus Bitwise Illustration**~~



2511



2512

Figure 159 RAW16 Frame Format

11.4.8 RAW20

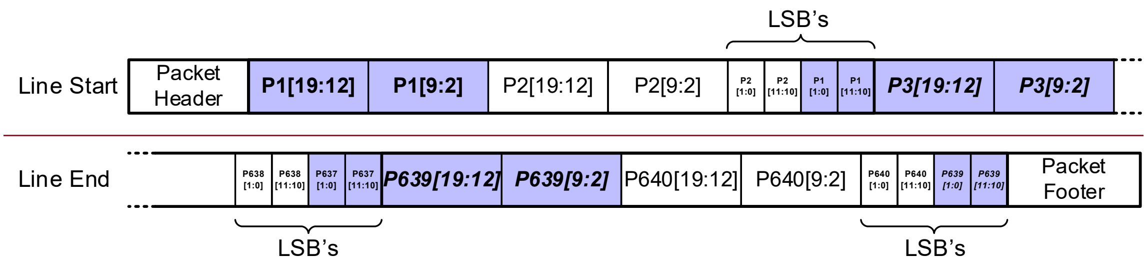
The transmission of 20-bit Raw data is done by packing the 20-bit pixel data to look like the 10-bit data format. ***Table ~~44~~58*** specifies the packet size constraints for RAW20 packets. The length of each packet must be a multiple of the values in the table.

Table 58 RAW20 Packet Data Size Constraints

Pixels	Bytes	Bits
2	5	40

This sequence is illustrated in ***Figure ~~148~~160*** (VGA case).

Bit order in transmission follows the general CSI-2 rule: LSB first.



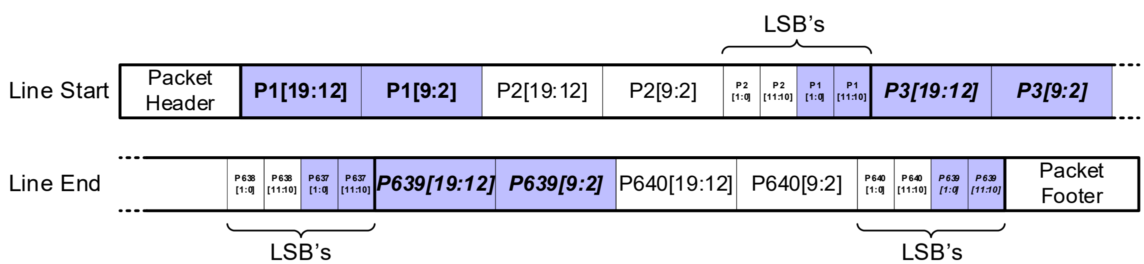


Figure 160 RAW20 Transmission

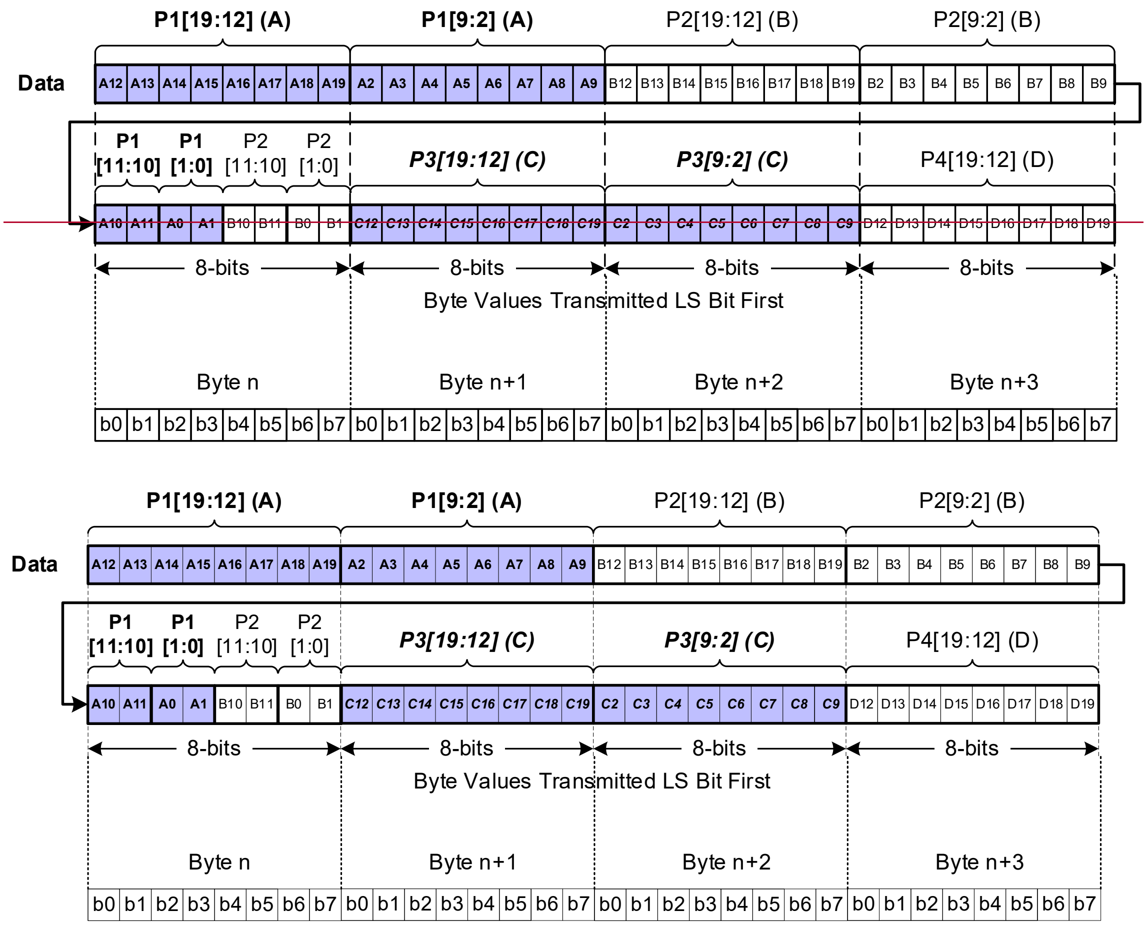


Figure 161 RAW20 Transmission on CSI-2 Bus Bitwise Illustration

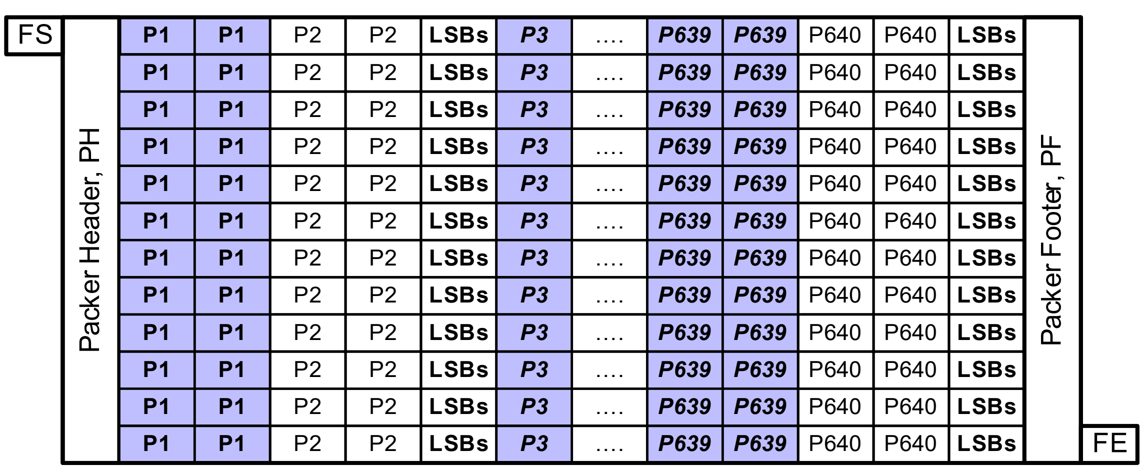


Figure 162 RAW20 Frame Format

11.4.9 RAW24

2524 The transmission of 24-bit Raw data is done by packing the 24-bit pixel data to look like the 12-bit data
2525 format. ***Table 59*** specifies the packet size constraints for RAW24 packets. The length of each packet must be
2526 a multiple of the values in the table.

2527 **Table 59 RAW24 Packet Data Size Constraints**

Pixels	Bytes	Bits
1	3	24

2528 This sequence is illustrated in ***Figure 163*** (VGA case).

2529 Bit order in transmission follows the general CSI-2 rule: LSB first.

2530

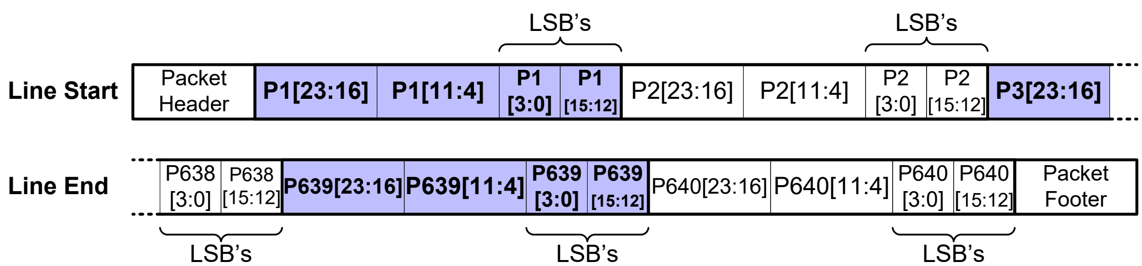


Figure 163 RAW24 Transmission

2531

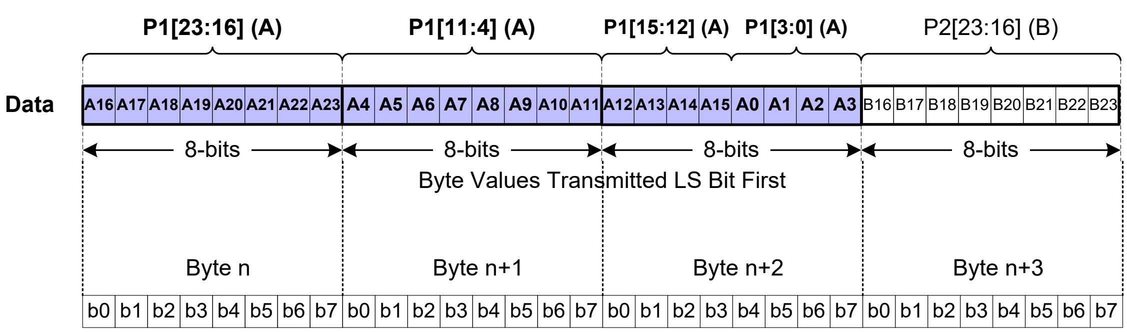


Figure 164 RAW24 Transmission on CSI-2 Bus Bitwise Illustration

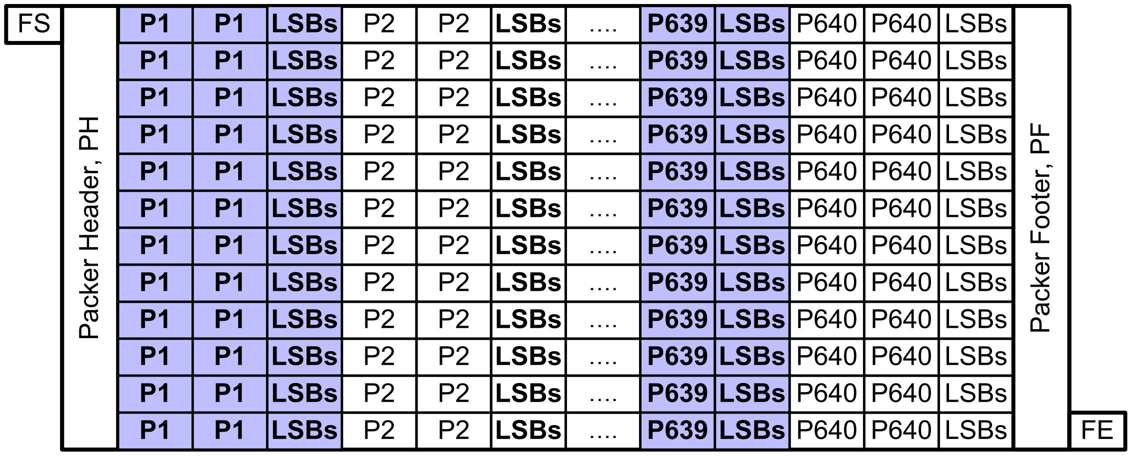


Figure 165 RAW24 Frame Format

11.5 User Defined Data Formats

The User Defined Data Type values shall be used to transmit arbitrary data, such as JPEG and MPEG4 data, over the CSI-2 bus. Data shall be packed so that the data length is divisible by eight bits. If data padding is required, the padding shall be added before data is presented to the CSI-2 protocol interface.

Bit order in transmission follows the general CSI-2 rule, LSB first.

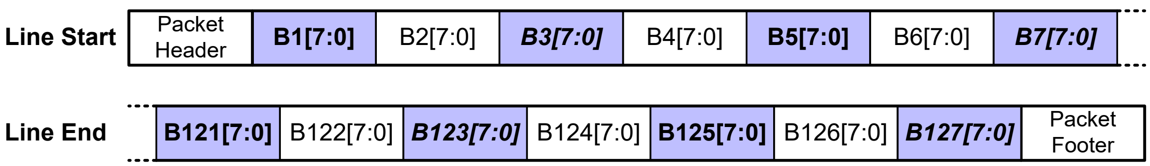


Figure 166 User Defined 8-bit Data (128 Byte Packet)

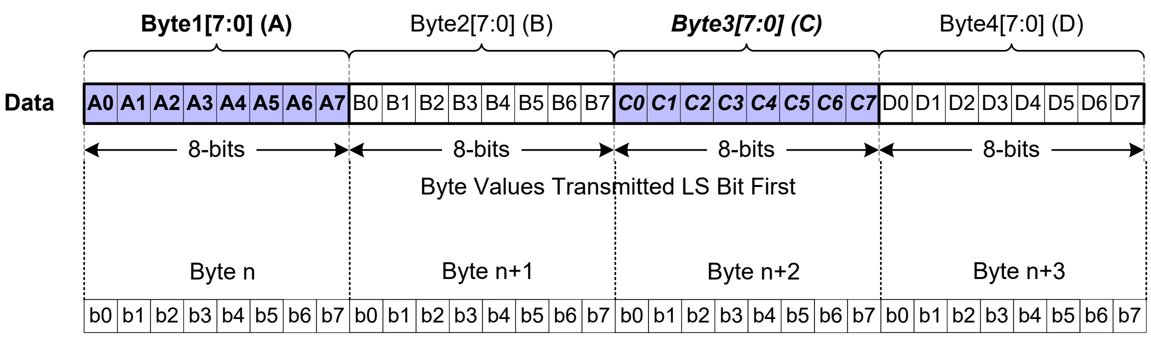
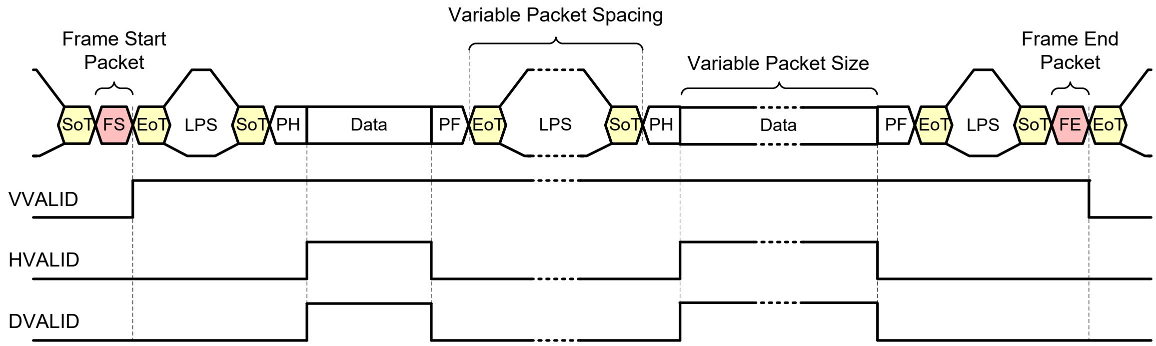


Figure 167 User Defined 8-bit Data Transmission on CSI-2 Bus Bitwise Illustration

The packet data size in bits shall be divisible by eight, i.e. a whole number of bytes shall be transmitted.

For User Defined data:

- The frame is transmitted as a sequence of arbitrary sized packets.
- The packet size may vary from packet to packet.
- The packet spacing may vary between packets.



KEY:

SoT – Start of Transmission
PH – Packet Header
FS – Frame Start

EoT – End of Transmission
PF – Packet Footer
FE – Frame End
LE – Line End

LPS – Low Power State

Figure 168 Transmission of User Defined 8-bit Data

2545 Eight different User Defined data type codes are available as shown in ***Table ~~45~~60***.

2546 **Table 60 User Defined 8-bit Data Types**

Data Type	Description
0x30	User Defined 8-bit Data Type 1
0x31	User Defined 8-bit Data Type 2
0x32	User Defined 8-bit Data Type 3
0x33	User Defined 8-bit Data Type 4
0x34	User Defined 8-bit Data Type 5
0x35	User Defined 8-bit Data Type 6
0x36	User Defined 8-bit Data Type 7
0x37	User Defined 8-bit Data Type 8

This page intentionally left blank.

12 Recommended Memory Storage

This section is informative.

The CSI-2 data protocol requires certain behavior from the receiver connected to the CSI transmitter. The following sections describe how different data formats should be stored inside the receiver. While informative, this section is provided to ease application software development by suggesting a common data storage format among different receivers.

12.1 General/Arbitrary Data Reception

In the generic case and for arbitrary data the first byte of payload data transmitted maps the LS byte of the 32-bit memory word and the fourth byte of payload data transmitted maps to the MS byte of the 32-bit memory word.

Figure ~~*154*~~*169* shows the generic CSI-2 byte to 32-bit memory word mapping rule.

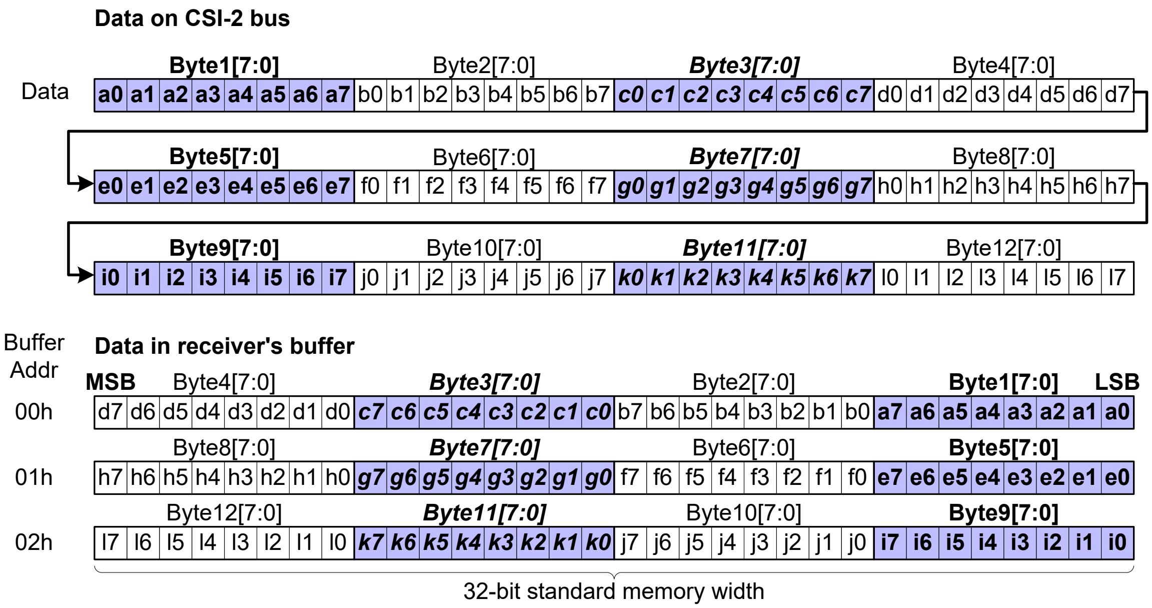


Figure 169 General/Arbitrary Data Reception

12.2 RGB888 Data Reception

The RGB888 data format byte to 32-bit memory word mapping follows the generic CSI-2 rule.

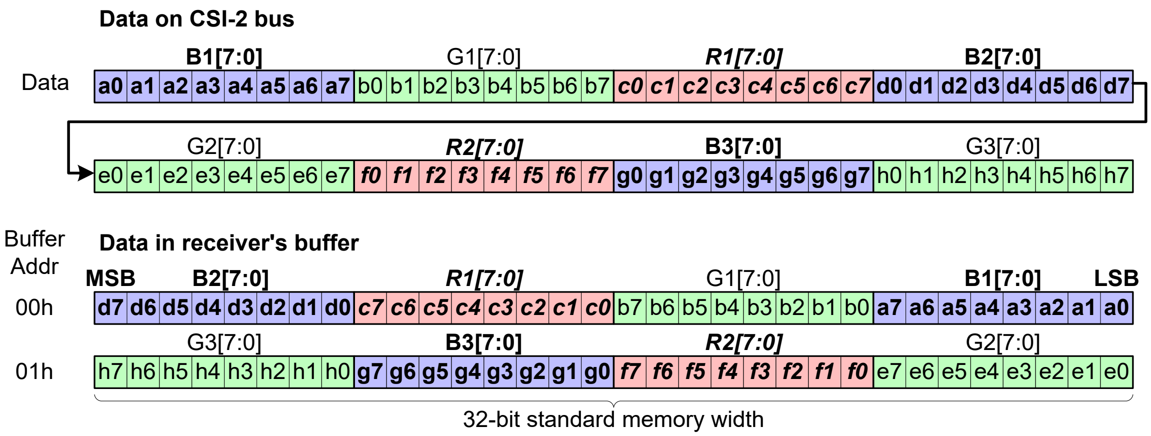


Figure 170 RGB888 Data Format Reception

12.3 RGB666 Data Reception

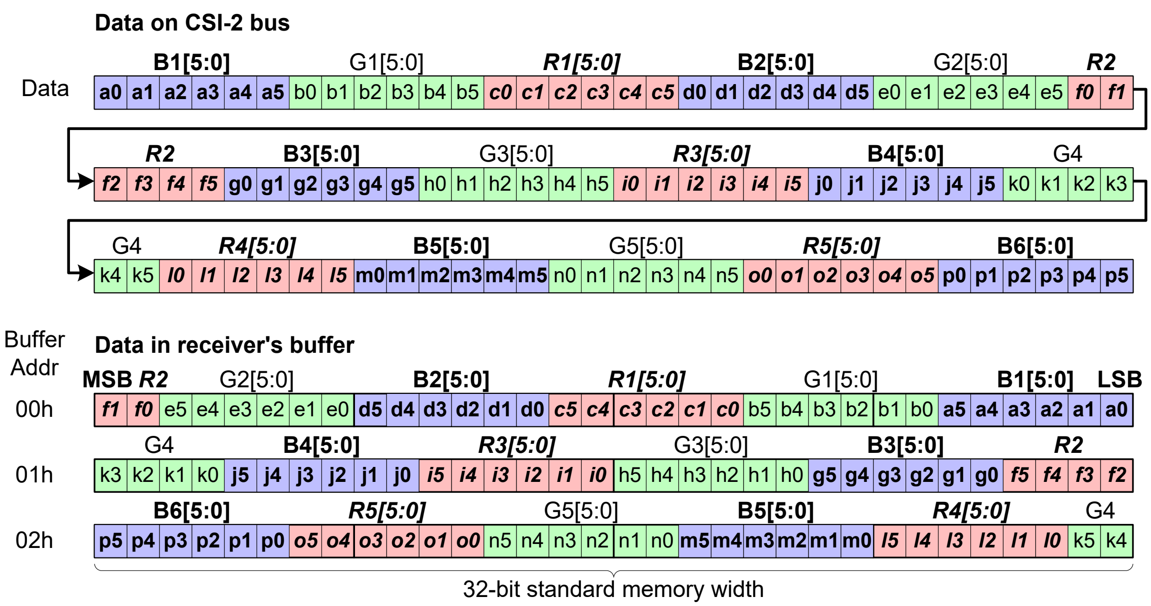


Figure 171 RGB666 Data Format Reception

12.4 RGB565 Data Reception

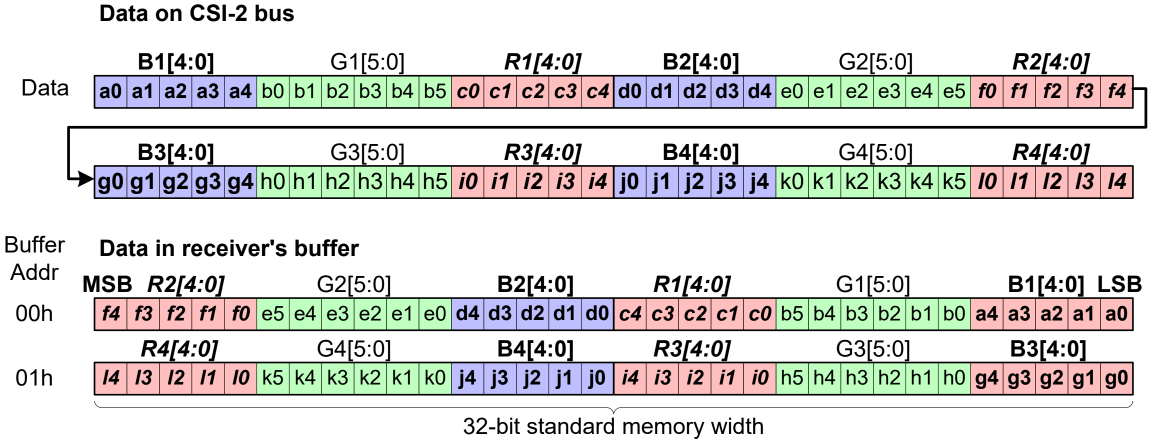
2560 

Figure 172 RGB565 Data Format Reception

12.5 RGB555 Data Reception

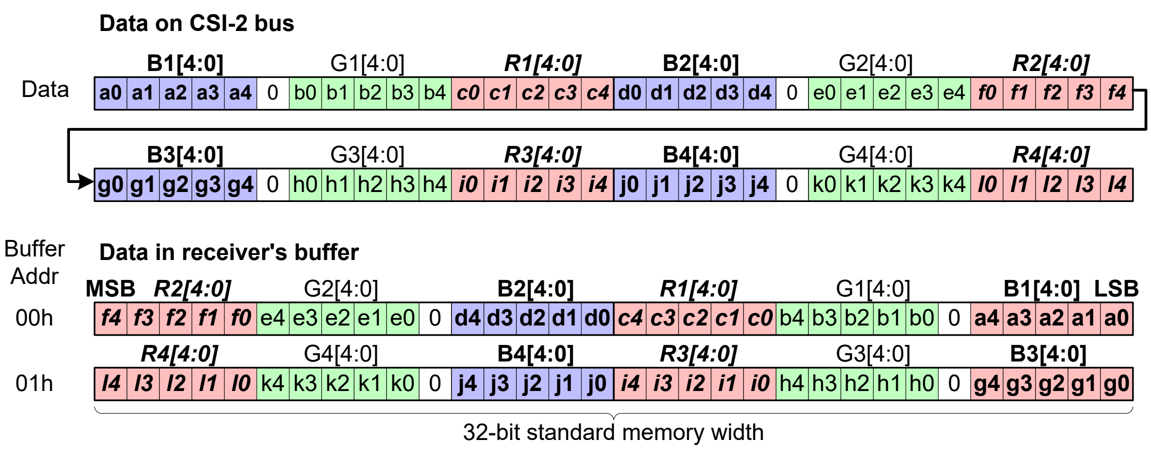
2561 

Figure 173 RGB555 Data Format Reception

12.6 RGB444 Data Reception

The RGB444 data format byte to 32-bit memory word mapping has a special transform as shown in ***Figure*** ~~*159*~~*174*.

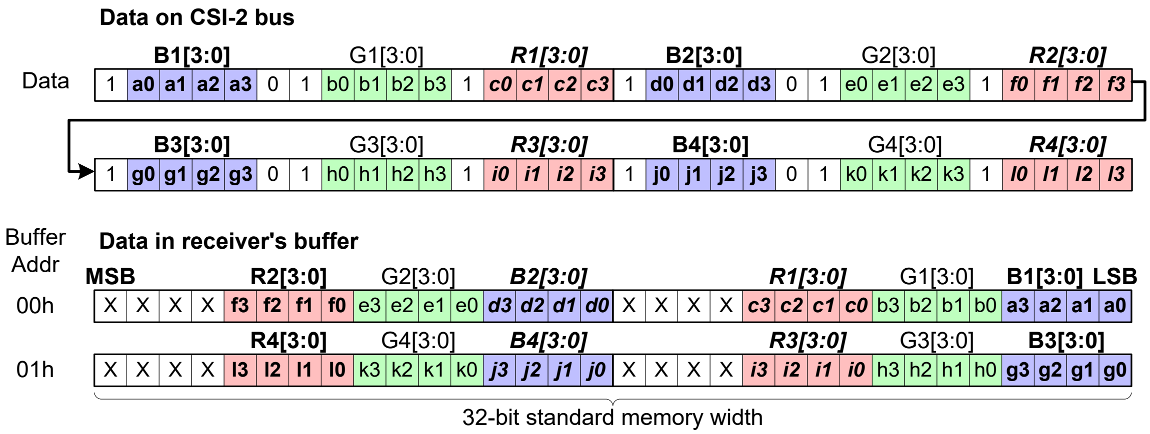


Figure 174 RGB444 Data Format Reception

12.7 YUV422 8-bit Data Reception

The YUV422 8-bit data format the byte to 32-bit memory word mapping does not follow the generic CSI-2 rule.

For YUV422 8-bit data format the first byte of payload data transmitted maps the MS byte of the 32-bit memory word and the fourth byte of payload data transmitted maps to the LS byte of the 32-bit memory word.

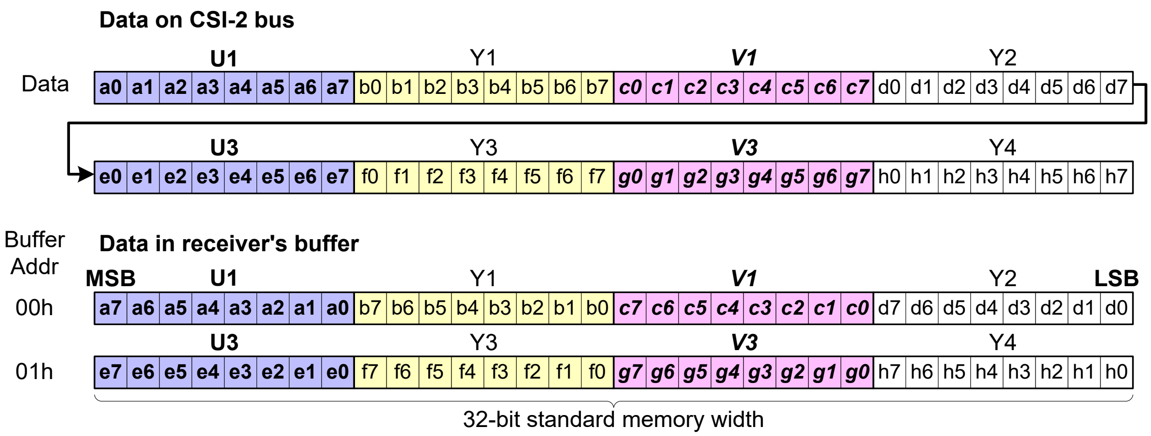


Figure 175 YUV422 8-bit Data Format Reception

12.8 YUV422 10-bit Data Reception

The YUV422 10-bit data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

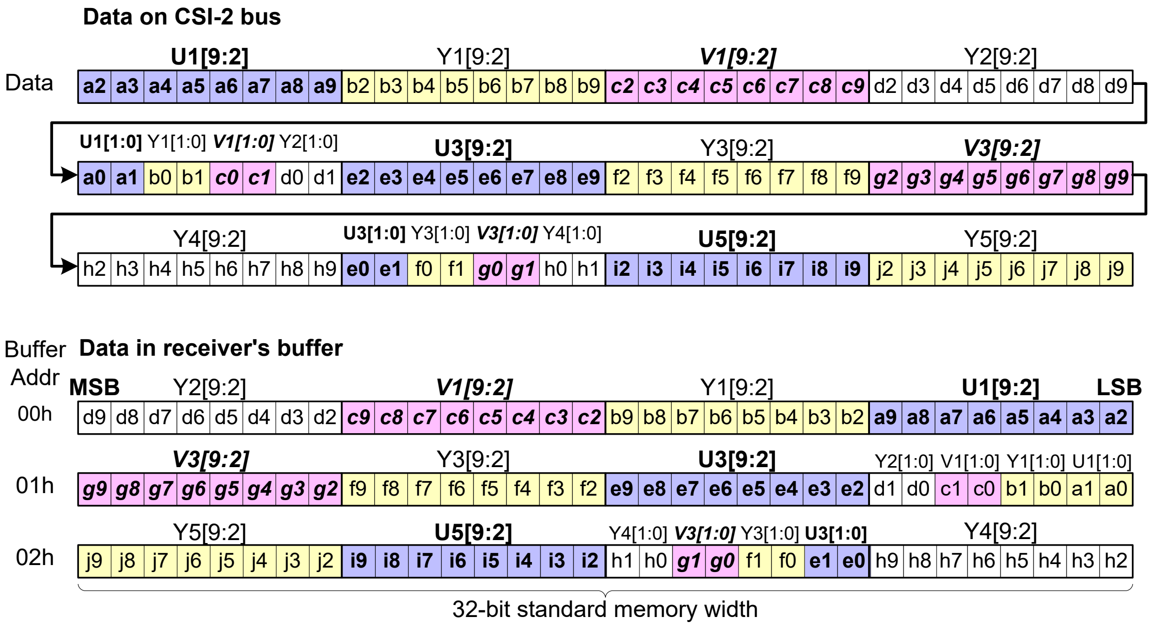


Figure 176 YUV422 10-bit Data Format Reception

12.9 YUV420 8-bit (Legacy) Data Reception

The YUV420 8-bit (legacy) data format the byte to 32-bit memory word mapping does not follow the generic CSI-2 rule.

For YUV422 8-bit (legacy) data format the first byte of payload data transmitted maps the MS byte of the 32-bit memory word and the fourth byte of payload data transmitted maps to the LS byte of the 32-bit memory word.

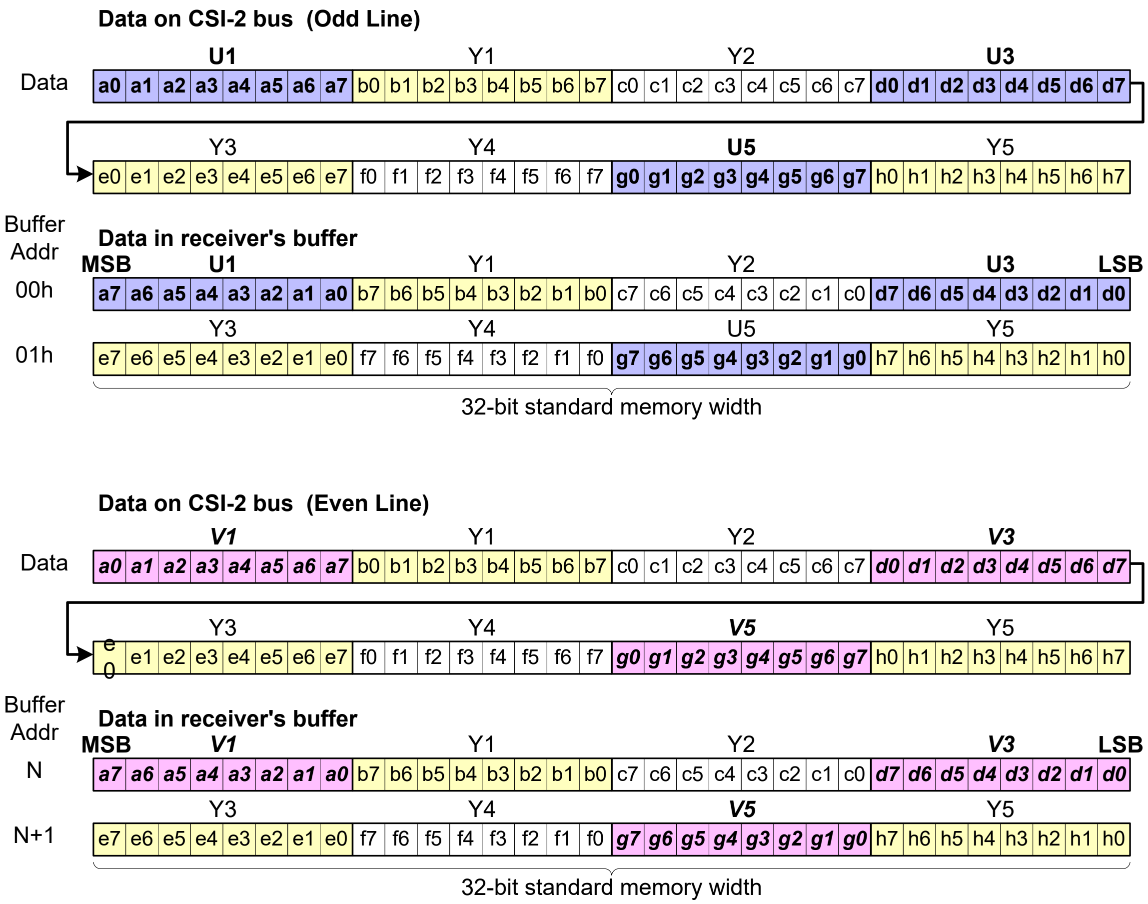


Figure 177 YUV420 8-bit Legacy Data Format Reception

12.10 YUV420 8-bit Data Reception

The YUV420 8-bit data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

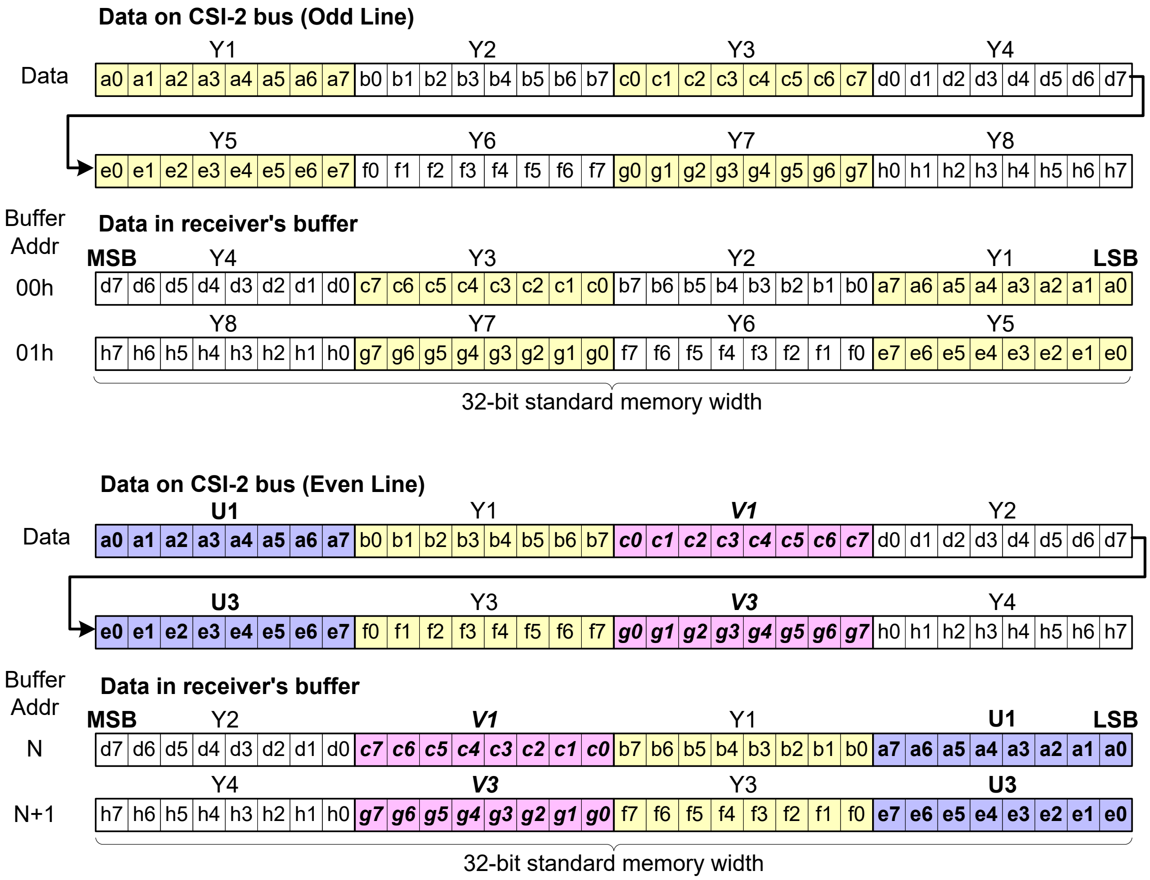


Figure 178 YUV420 8-bit Data Format Reception

12.11 YUV420 10-bit Data Reception

The YUV420 10-bit data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

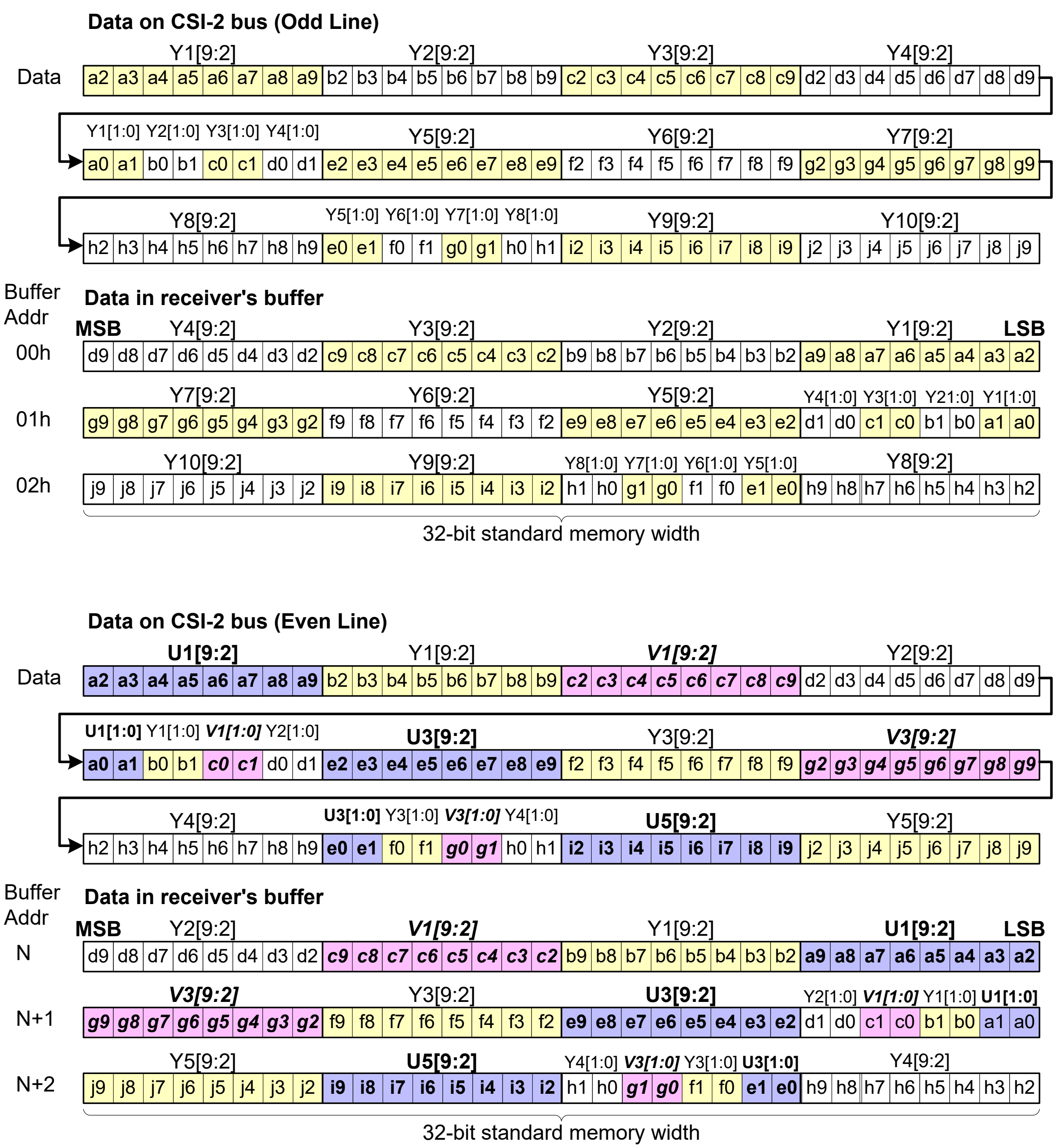


Figure 179 YUV420 10-bit Data Format Reception

12.12 RAW6 Data Reception

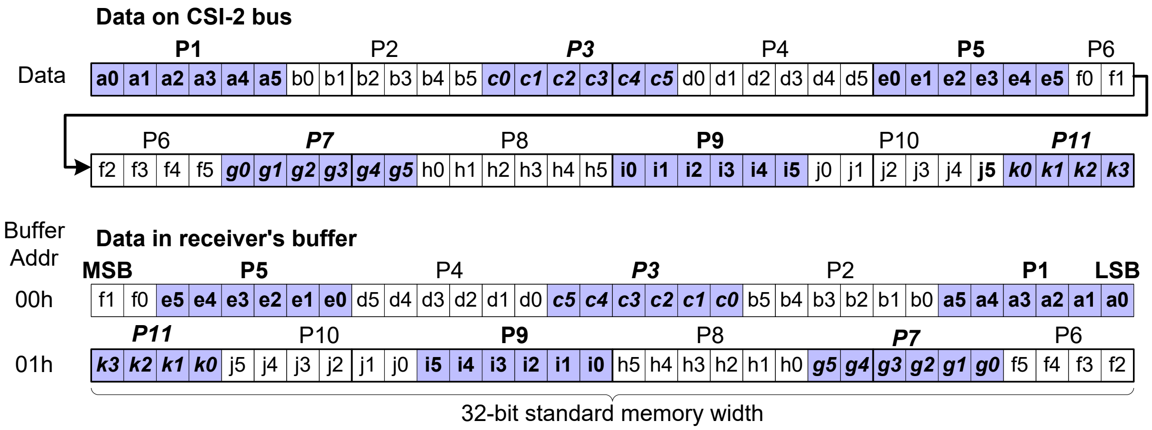


Figure 180 RAW6 Data Format Reception

12.13 RAW7 Data Reception

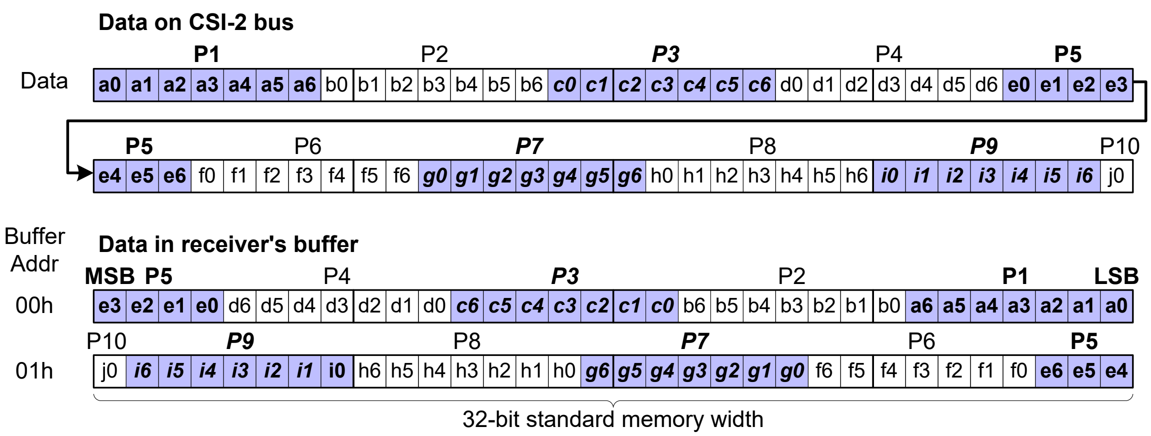


Figure 181 RAW7 Data Format Reception

12.14 RAW8 Data Reception

2585 The RAW8 data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

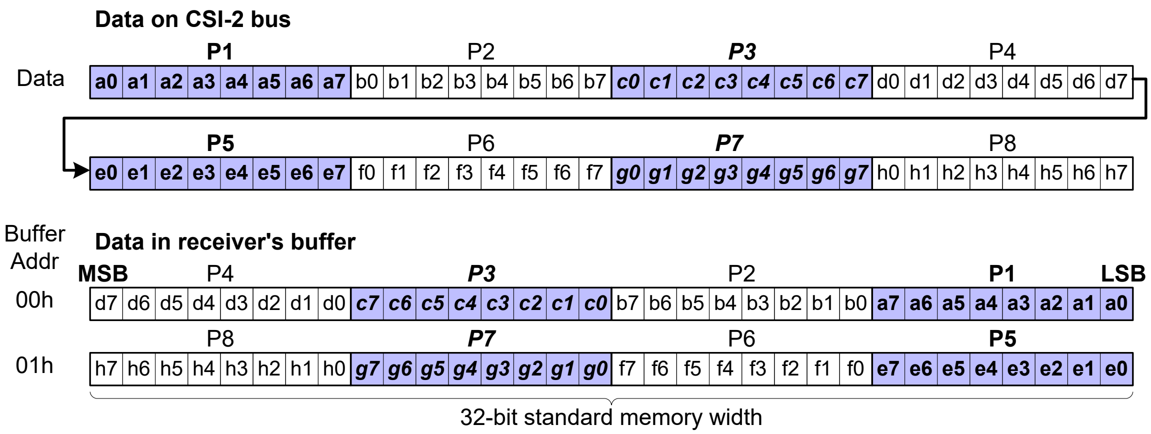
2586 

Figure 182 RAW8 Data Format Reception

12.15 RAW10 Data Reception

2587 The RAW10 data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

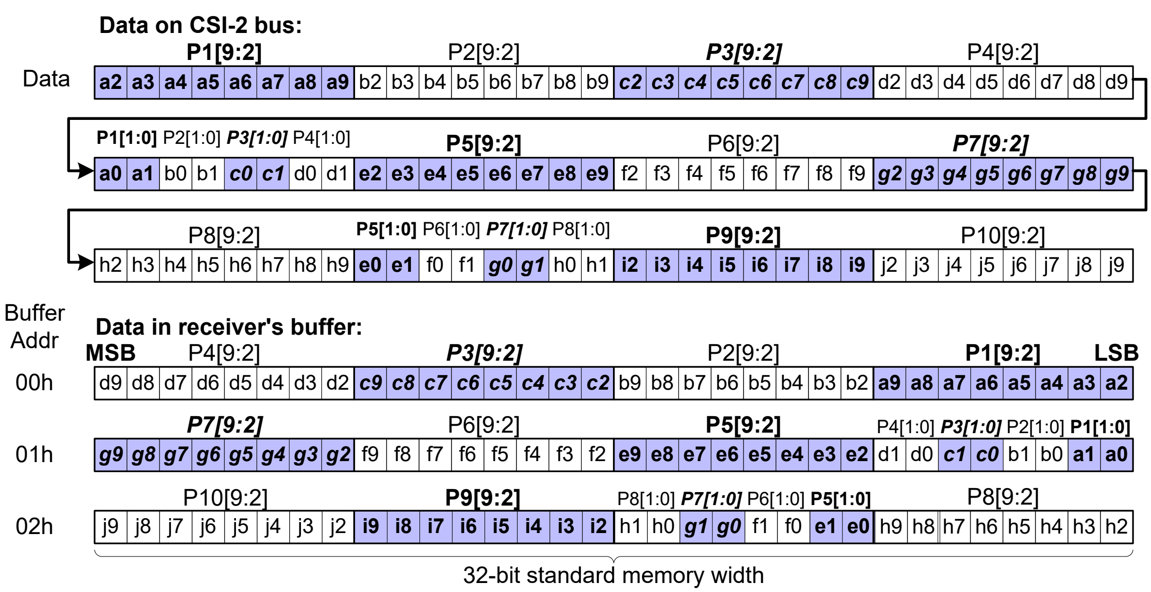
2588 

Figure 183 RAW10 Data Format Reception

12.16 RAW12 Data Reception

The RAW12 data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

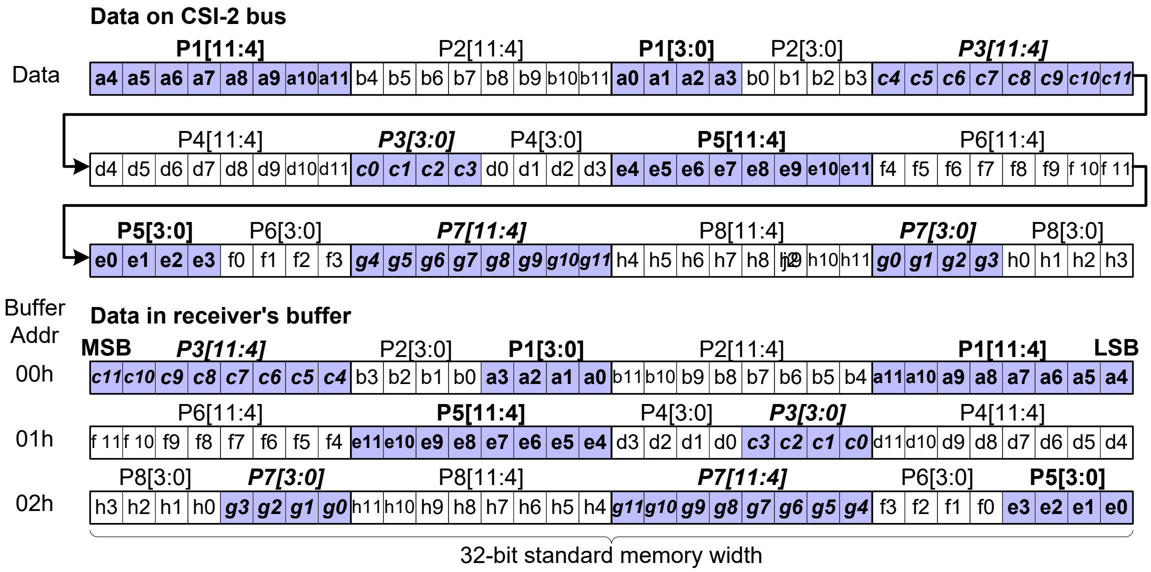


Figure 184 RAW12 Data Format Reception

12.17 RAW14 Data Reception

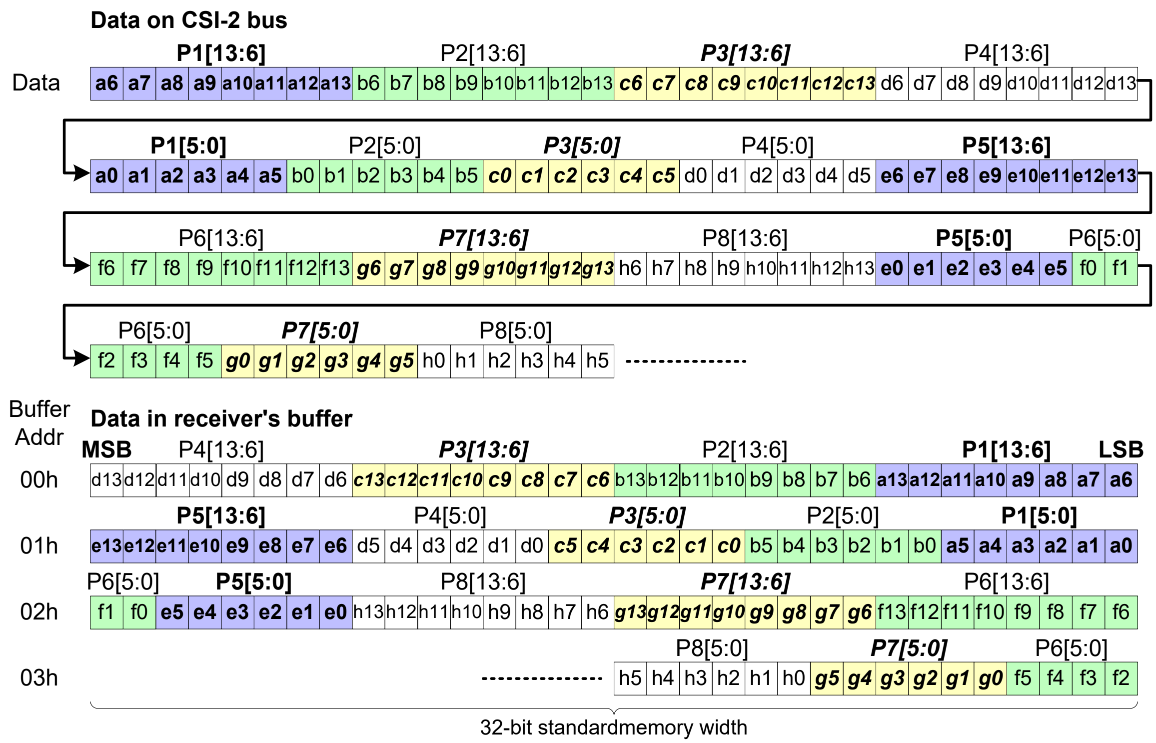


Figure 185 RAW 14 Data Format Reception

12.18 RAW16 Data Reception

The RAW16 data format byte to 32-bit memory word mapping follows the generic CSI-2 rule.

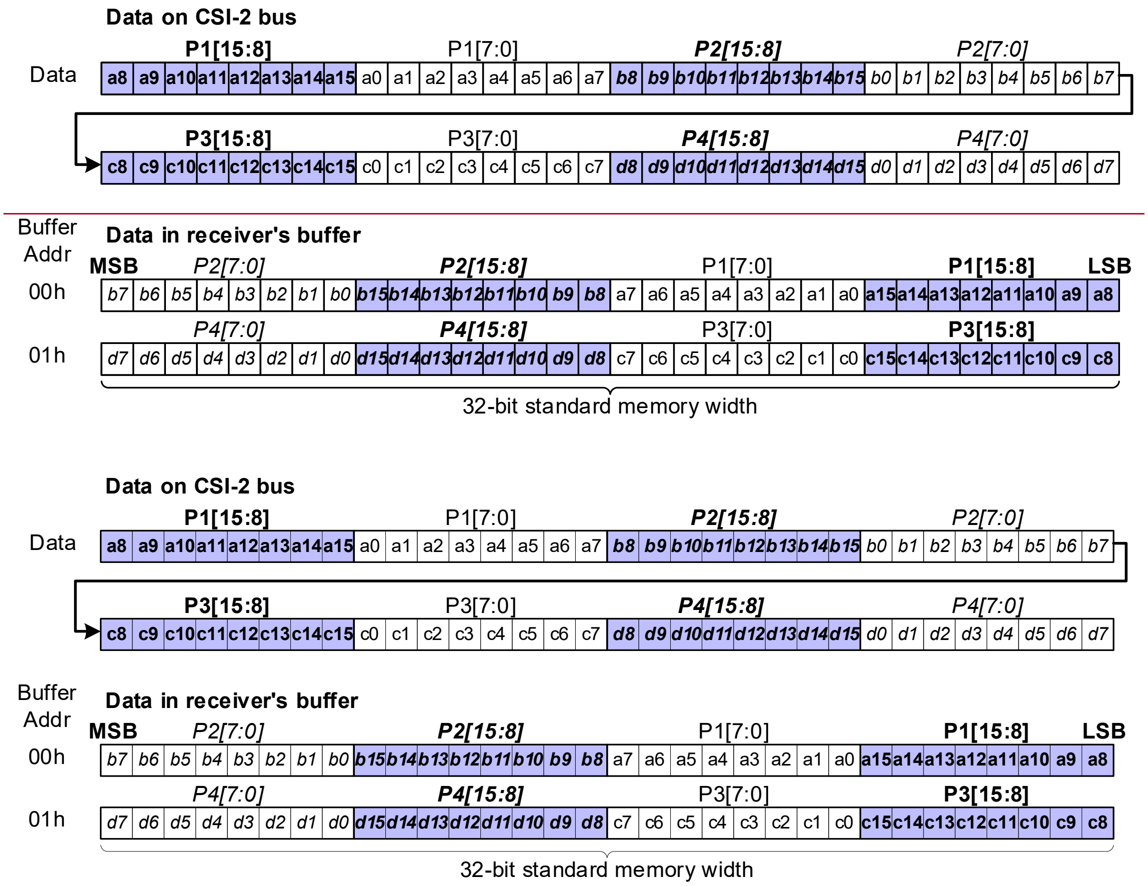
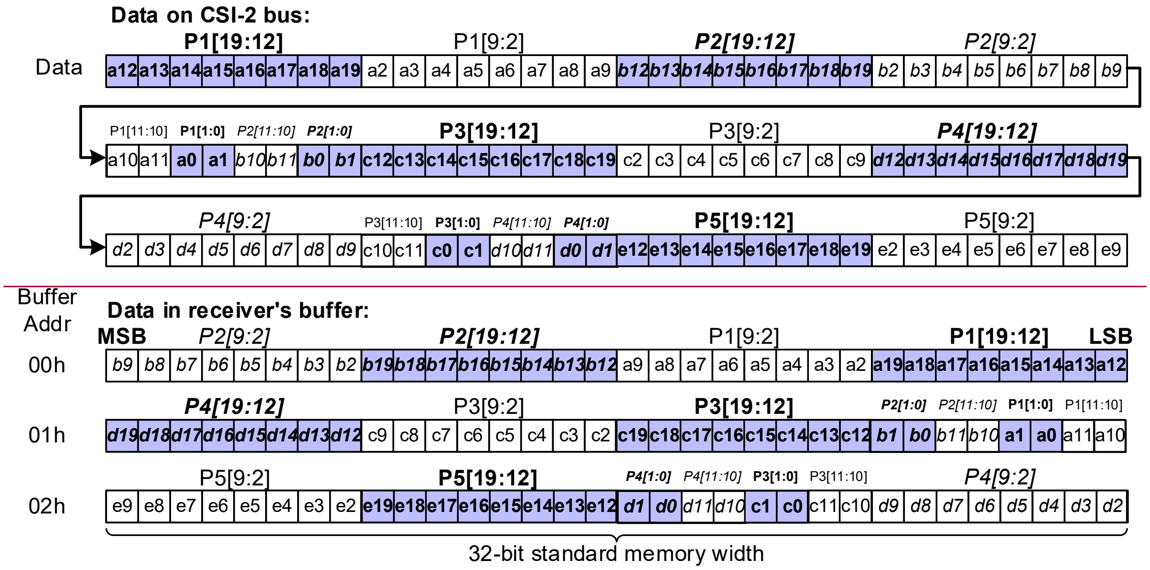


Figure 186 RAW16 Data Format Reception

12.19 RAW20 Data Reception

The RAW20 data format byte to 32-bit memory word mapping follows the generic CSI-2 rule.



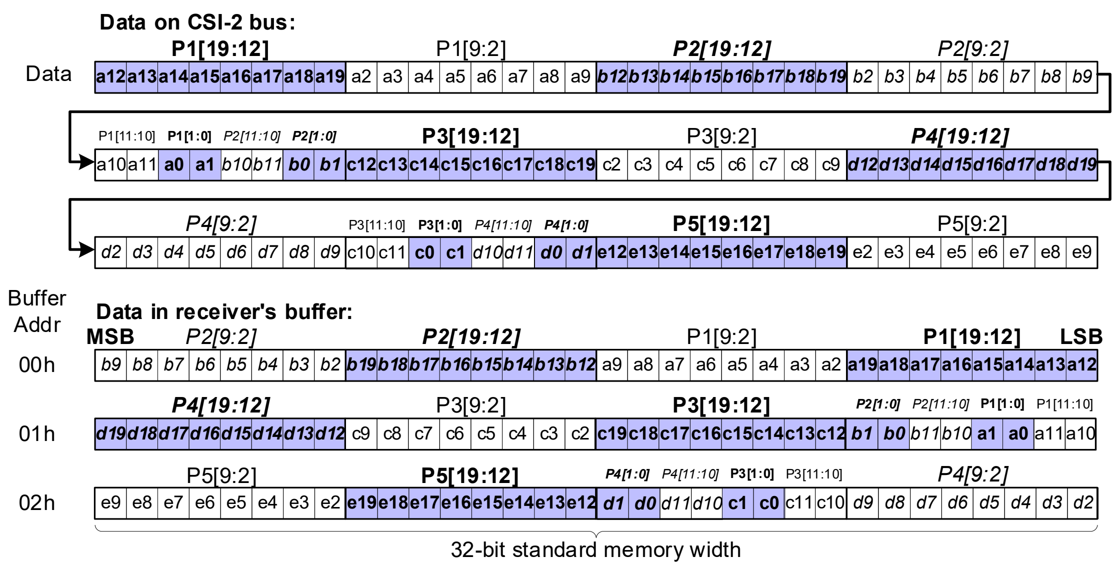


Figure 187 RAW20 Data Format Reception

12.20 RAW24 Data Reception

The RAW24 data format byte to 32-bit memory word mapping follows the generic CSI-2 rule.

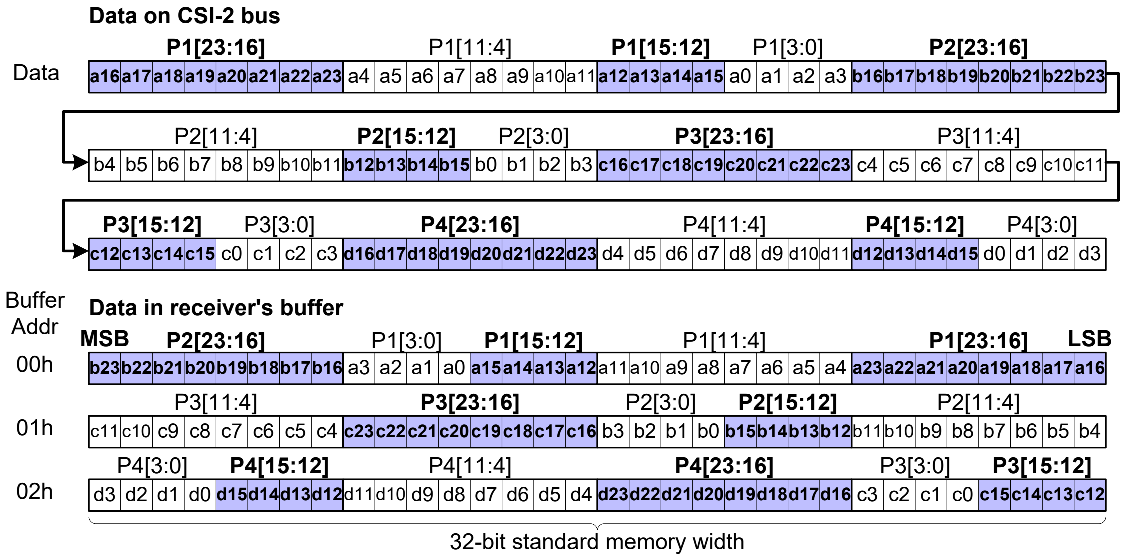


Figure 188 RAW24 Data Format Reception

This page intentionally left blank.

Annex A JPEG8 Data Format (informative)

A.1 Introduction

This Annex contains an informative example of the transmission of compressed image data format using the arbitrary Data Type values.

JPEG8 has two non-standard extensions:

- Status information (mandatory)
- Embedded Image information e.g. a thumbnail image (optional)

Any non-standard or additional data inside the baseline JPEG data structure has to be removed from JPEG8 data before it is compliant with e.g. standard JPEG image viewers in e.g. a personal computer.

The JPEG8 data flow is illustrated in ***Figure ~~173~~189*** and ***Figure ~~174~~190***.

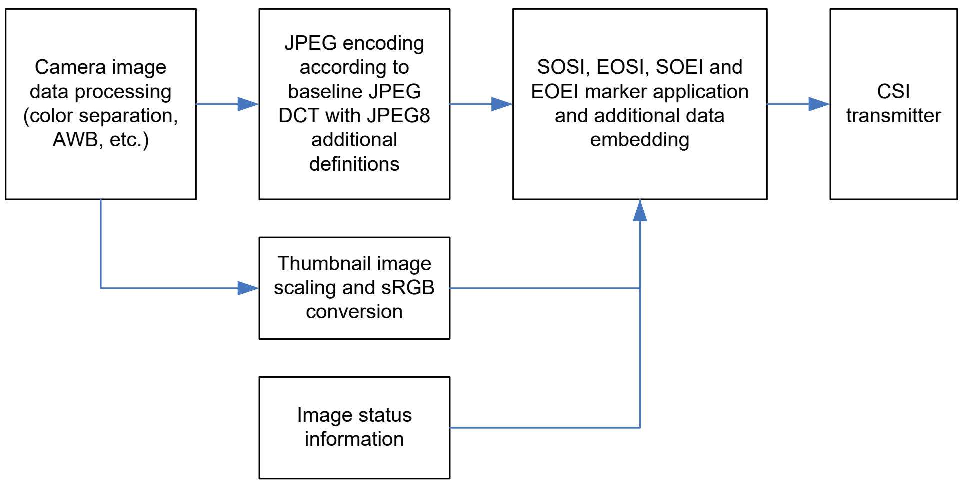


Figure 189 JPEG8 Data Flow in the Encoder

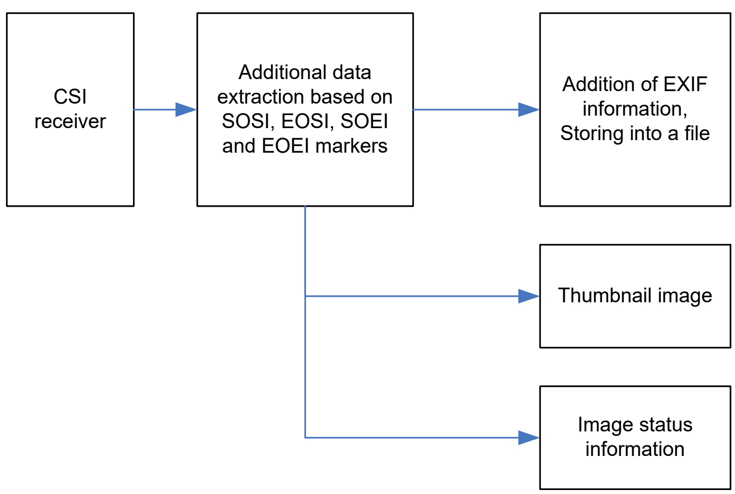


Figure 190 JPEG8 Data Flow in the Decoder

A.2 JPEG Data Definition

The JPEG data generated in camera module is baseline JPEG DCT format defined in ISO/IEC 10918-1, with following additional definitions or modifications:

- sRGB color space shall be used. The JPEG is generated from YCbCr format after sRGB to YCbCr conversion.
- The JPEG metadata has to be EXIF compatible, i.e. metadata within application segments has to be placed in beginning of file, in the order illustrated in ***Figure*** ***~~175~~191***.
- A status line is added in the end of JPEG data as defined in ***Section A.3***.
- If needed, an embedded image is interlaced in order which is free of choice as defined in ***Section A.4***.
- Prior to storing into a file, the CSI-2 JPEG data is processed by the data separation process described in ***Section A.1***.

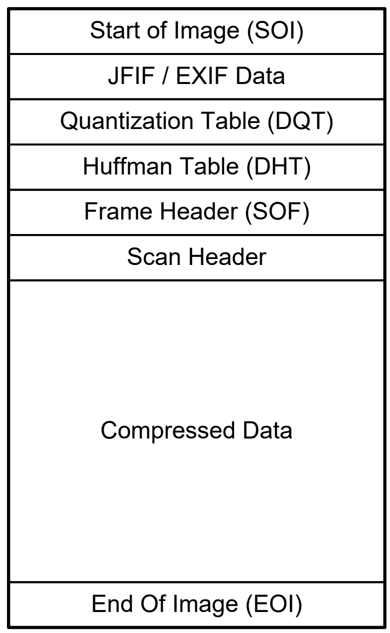


Figure 191 EXIF Compatible Baseline JPEG DCT Format

A.3 Image Status Information

Information of at least the following items has to be stored in the end of the JPEG sequence as illustrated in ***Figure ~~176~~192***:

- Image exposure time
- Analog & digital gains used
- White balancing gains for each color component
- Camera version number
- Camera register settings
- Image resolution and possible thumbnail resolution

The camera register settings may include a subset of camera's registers. The essential information needed for JPEG8 image is the information needed for converting the image back to linear space. This is necessary e.g. for printing service. An example of register settings is following:

- Sample frequency
- Exposure
- Analog and digital gain
- Gamma
- Color gamut conversion matrix
- Contrast
- Brightness
- Pre-gain

The status information content has to be defined in the product specification of each camera module containing the JPEG8 feature. The format and content is manufacturer specific.

The image status data should be arranged so that each byte is split into two 4-bit nibbles and "1010" padding sequence is added to MSB, as presented in ***Table ~~46~~61***. This ensures that no JPEG escape sequences (0xFF 0x00) are present in the status data.

The SOSI and EOSI markers are defined in ***Section A.5***.

Table 61 Status Data Padding

Data Word	After Padding
D7D6D5D4 D3D2D1D0	1010D7D6D5D4 1010D3D2D1D0

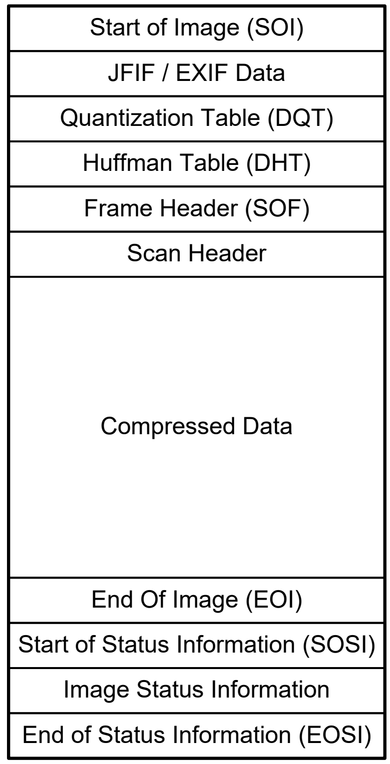


Figure 192 Status Information Field in the End of Baseline JPEG Frame

A.4 Embedded Images

An image may be embedded inside the JPEG data, if needed. The embedded image feature is not compulsory for each camera module containing the JPEG8 feature. An example of embedded data is a 24-bit RGB thumbnail image.

The philosophy of embedded / interleaved thumbnail additions is to minimize the needed frame memory. The EI (Embedded Image) data can be included in any part of the compressed image data segment and in as many pieces as needed. See ***Figure ~~177~~193***.

Embedded Image data is separated from compressed data by SOEI (Start Of Embedded Image) and EOEI (End Of Embedded Image) non-standard markers, which are defined in ***Section A.5***. The amount of fields separated by SOEI and EOEI is not limited.

The pixel to byte packing for image data within an EI data field should be as specified for the equivalent CSI-2 data format. However there is an additional restriction; the embedded image data must not generate any false JPEG marker sequences (0xFFXX).

The suggested method of preventing false JPEG marker codes from occurring within the embedded image data it to limit the data range for the pixel values. For example

- For RGB888 data the suggested way to solve the false synchronization code issue is to constrain the numerical range of R, G and B values from 1 to 254.
- For RGB565 data the suggested way to solve the false synchronization code issue is to constrain the numerical range of G component from 1-62 and R component from 1-30.

Each EI data field is separated by the SOEI / EOEI markers, and has to contain an equal amount bytes and a complete number of pixels. An EI data field may contain multiple lines or a full frame of image data.

The embedded image data is decoded and removed apart from the JPEG compressed data prior to writing the JPEG into a file. In the process, EI data fields are appended one after each other, in order of occurrence in the received JPEG data.

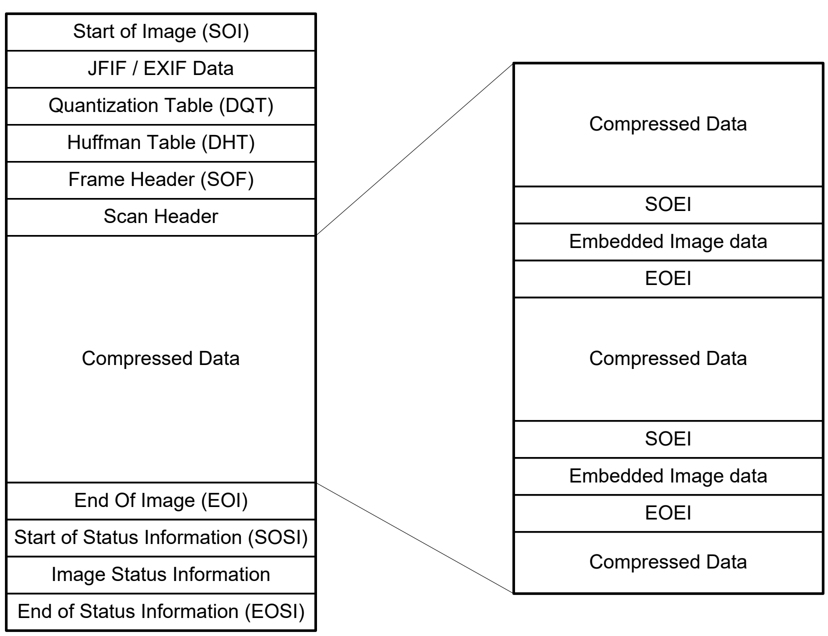


Figure 193 Example of TN Image Embedding Inside the Compressed JPEG Data Block

A.5 JPEG8 Non-standard Markers

JPEG8 uses the reserved JPEG data markers for special purposes, marking the additional segments inside the data file. These segments are not part of the JPEG, JFIF [0], EXIF [0] or any other specifications; instead their use is specified in this document in ***Section A.3*** and ***Section A.4***.

The use of the non-standard markers is always internal to a product containing the JPEG8 camera module, and these markers are always removed from the JPEG data before storing it into a file.

Table 62 JPEG8 Additional Marker Codes Listing

Non-standard Marker Symbol	Marker Data Code
SOSI	0xFF 0xBC
EOSI	0xFF 0xBD
SOEI	0xFF 0xBE
EOEI	0xFF 0xBF

A.6 JPEG8 Data Reception

The compressed data format the byte to 32-bit memory word mapping follows the generic CSI-2 rule.

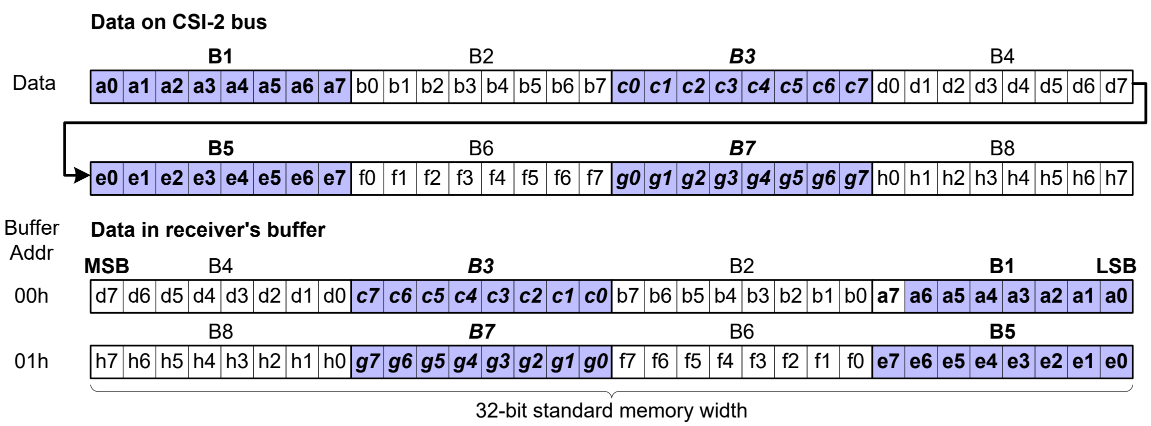


Figure 194 JPEG8 Data Format Reception

Annex B CSI-2 Implementation Example (informative)

B.1 Overview

The CSI-2 implementation example assumes that the interface comprises of D-PHY unidirectional Clock and Data, with forward ~~escape mode~~Escape Mode and optional deskew functionality. The scope in this implementation example refers only to the unidirectional data link without any references to the CCI interface, as it can be seen in ***Figure ~~179~~195***. This implementation example varies from the informative PPI example in ***[MIPI01]***.

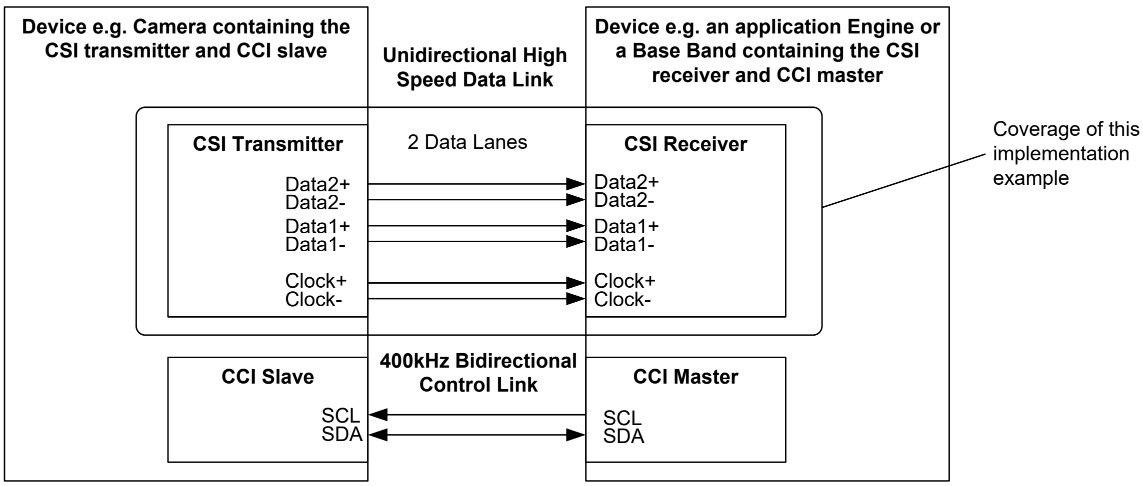


Figure 195 Implementation Example Block Diagram and Coverage

For this implementation example a layered structure is described with the following parts:

- D-PHY implementation details
- Multi lane merger details
- Protocol layer details

This implementation example refers to a RAW8 data type only; hence no packing/unpacking or byte clock/pixel clock timing will be referenced as for this type of implementation they are not needed.

No error recovery mechanism or error processing details will be presented, as the intent of the document is to present an implementation from the data flow perspective.

B.2 CSI-2 Transmitter Detailed Block Diagram

Using the layered structure described in the overview the CSI-2 transmitter could have the block diagram in ***Figure ~~180~~196***.

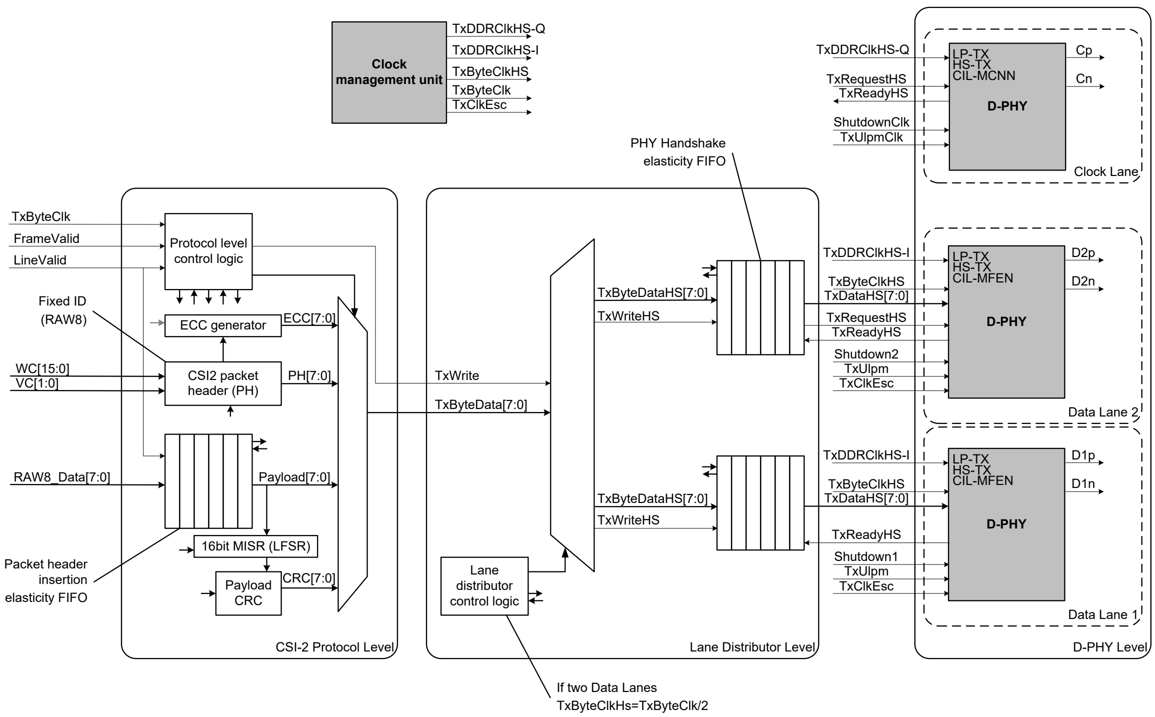


Figure 196 CSI-2 Transmitter Block Diagram

B.3 CSI-2 Receiver Detailed Block Diagram

Using the layered structure described in the overview, the CSI-2 receiver could have the block diagram in ***Figure ~~181~~197***.

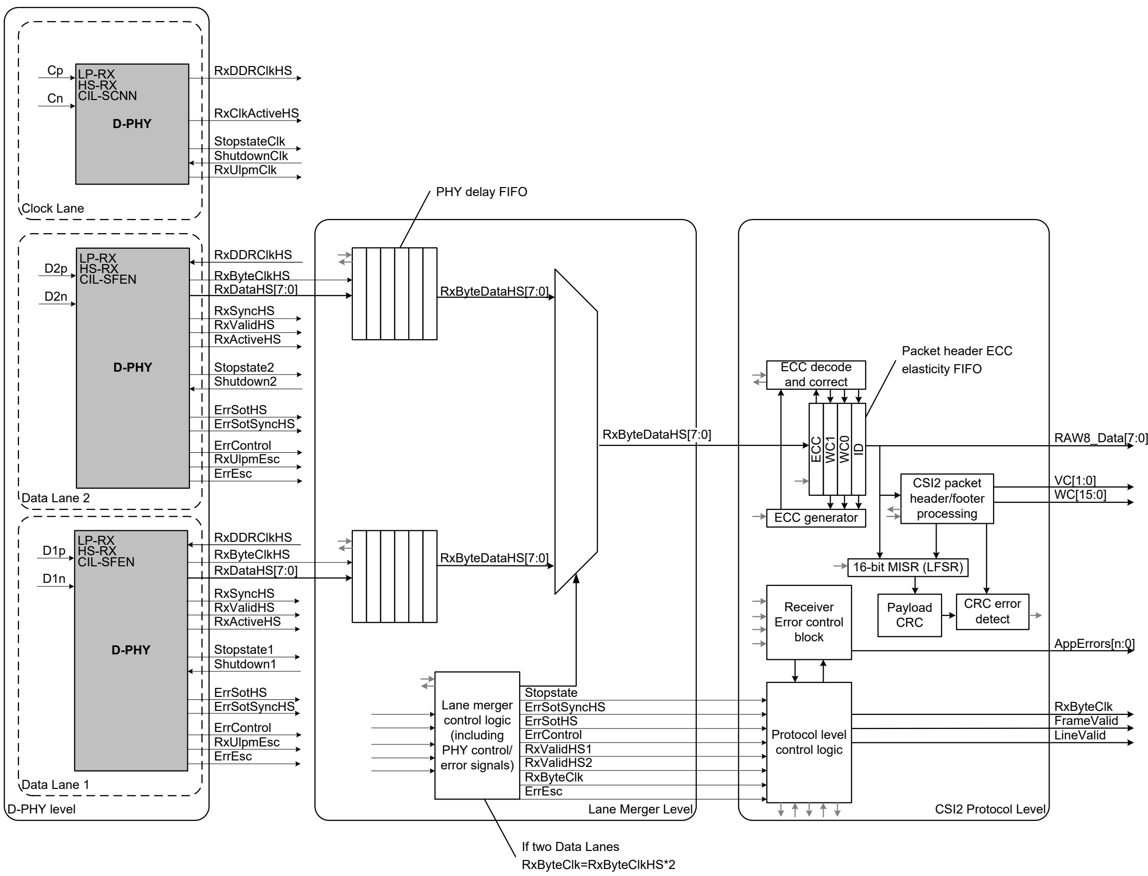


Figure 197 CSI-2 Receiver Block Diagram

B.4 Details on the D-PHY Implementation

The PHY level of implementation has the top level structure as seen in ***Figure ~~182~~198***.

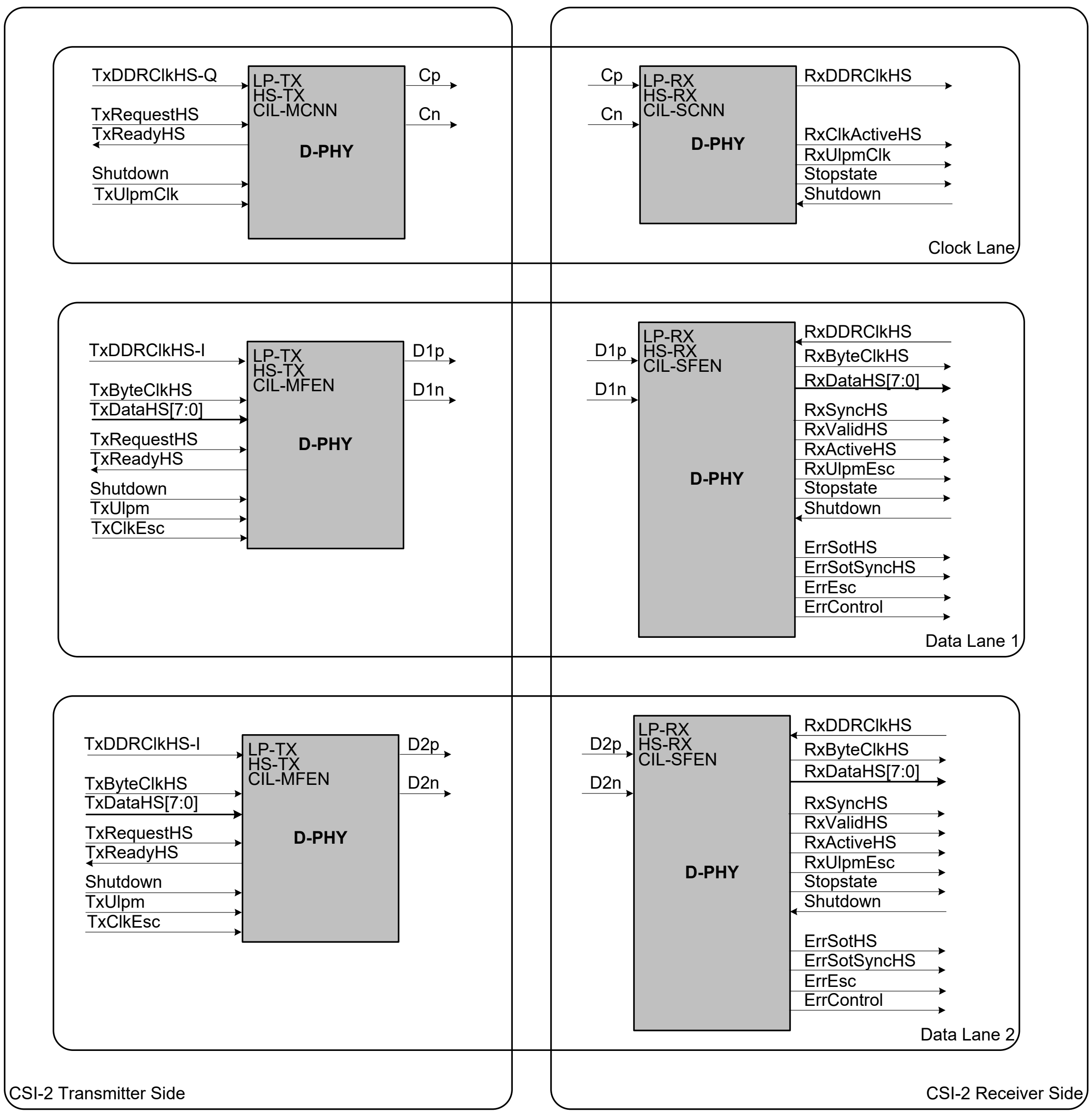


Figure 198 D-PHY Level Block Diagram

The components can be categorized as:

- CSI-2 Transmitter side:
  - Clock lane (Transmitter)
  - Data1 lane (Transmitter)
  - Data2 lane (Transmitter)

- CSI-2 Receiver side:
  - Clock lane (Receiver)
  - Data1 lane (Receiver)
  - Data2 lane (Receiver)

B.4.1 CSI-2 Clock Lane Transmitter

The suggested implementation can be seen in ***Figure ~~183~~199***.

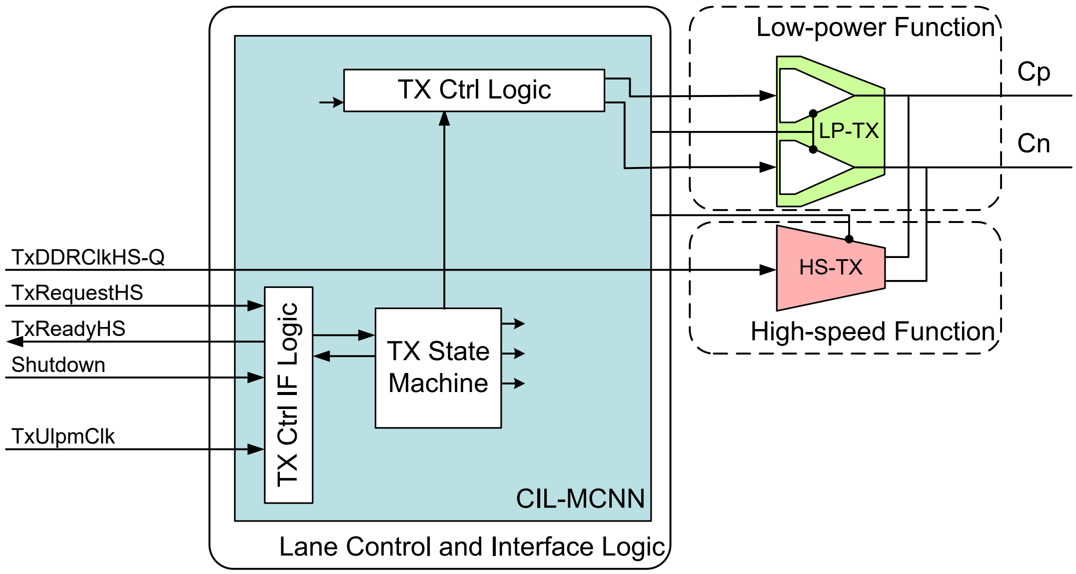


Figure 199 CSI-2 Clock Lane Transmitter

The modular D-PHY components used to build a CSI-2 clock lane transmitter are:

- **LP-TX** for the Low-power function
- **HS-TX** for the High-speed function
- **CIL-MCNN** for the Lane control and interface logic

The PPI interface signals to the CSI-2 clock lane transmitter are:

- **TxDDRClkHS-Q** (Input): High-Speed Transmit DDR Clock (Quadrature).
- **TxRequestHS** (Input): High-Speed Transmit Request. This active high signal causes the lane module to begin transmitting a high-speed clock.
- **TxReadyHS** (Output): High-Speed Transmit Ready. This active high signal indicates that the clock lane is transmitting HS clock.
- **Shutdown** (Input): Shutdown Lane Module. This active high signal forces the lane module into “shutdown”, disabling all activity. All line drivers, including terminators, are turned off when Shutdown is asserted. When Shutdown is high, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Shutdown is a level sensitive signal and does not depend on any clock.
- **TxUlpmClk** (Input): Transmit Ultra Low-Power mode on Clock Lane This active high signal is asserted to cause a Clock Lane module to enter the Ultra Low-Power mode. The lane module remains in this mode until TxUlpmClk is de-asserted.

B.4.2 CSI-2 Clock Lane Receiver

The suggested implementation can be seen in ***Figure ~~184~~200***.

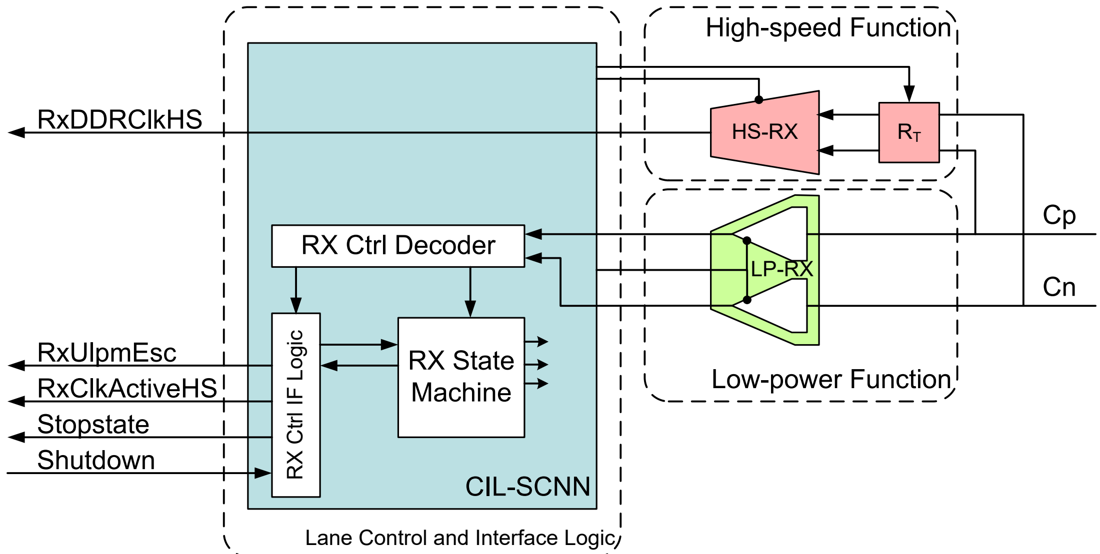


Figure 200 CSI-2 Clock Lane Receiver

The modular D-PHY components used to build a CSI-2 clock lane receiver are:

- **LP-RX** for the Low-power function
- **HS-RX** for the High-speed function
- **CIL-SCNN** for the Lane control and interface logic

The PPI interface signals to the CSI-2 clock lane receiver are:

- **RxDDRClkHS** (Output): High-Speed Receive DDR Clock used to sample the data in all data lanes.
- **RxClkActiveHS** (Output): High-Speed Reception Active. This active high signal indicates that the clock lane is receiving valid clock. This signal is asynchronous.
- **Stopstate** (Output): Lane is in Stop state. This active high signal indicates that the lane module is currently in Stop state. This signal is asynchronous.
- **Shutdown** (Input): Shutdown Lane Module. This active high signal forces the lane module into "shutdown", disabling all activity. All line drivers, including terminators, are turned off when Shutdown is asserted. When Shutdown is high, all PPI outputs are driven to the default inactive state. Shutdown is a level sensitive signal and does not depend on any clock.
- **RxUlpmEsc** (Output): Escape Ultra Low Power (Receive) mode. This active high signal is asserted to indicate that the lane module has entered the Ultra Low-Power mode. The lane module remains in this mode with RxUlpmEsc asserted until a Stop state is detected on the lane interconnect.

B.4.3 CSI-2 Data Lane Transmitter

The suggested implementation can be seen in ***Figure ~~185~~201***.

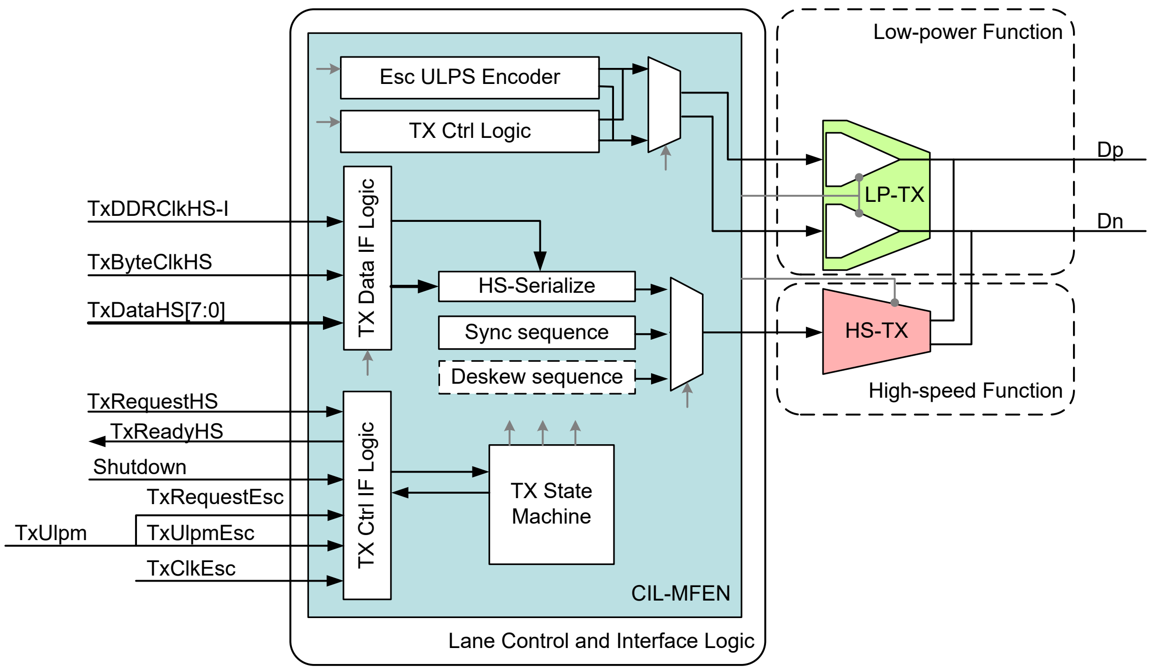


Figure 201 CSI-2 Data Lane Transmitter

The modular D-PHY components used to build a CSI-2 data lane transmitter are:

- **LP-TX** for the Low-power function
- **HS-TX** for the High-speed function
- **CIL-MFEN** for the Lane control and interface logic. For optional deskew calibration support, the data lane transmitter transmits a deskew sequence. The deskew sequence transmission is enabled by a mechanism out of the scope of this specification.

The PPI interface signals to the CSI-2 data lane transmitter are:

- **TxDDRClkHS-I** (Input): High-Speed Transmit DDR Clock (in-phase).
- **TxByteClkHS** (Input): High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that both transmitting data lane modules share one TxByteClkHS signal. The frequency of TxByteClkHS must be exactly 1/8 the high-speed bit rate.
- **TxDataHS[7:0]** (Input): High-Speed Transmit Data. Eight bit high-speed data to be transmitted. The signal connected to TxDataHS[0] is transmitted first. Data is registered on rising edges of TxByteClkHS.
- **TxRequestHS** (Input): High-Speed Transmit Request. A low-to-high transition on TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the lane module to initiate an End-of-Transmission sequence. This active high signal also indicates that the protocol is driving valid data on TxByteDataHS to be transmitted. The lane module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when

TxRequestHS is active. Once asserted, TxRequestHS should remain high until the all the data has been accepted.

- **TxReadyHS** (Output): High-Speed Transmit Ready. This active high signal indicates that TxDataHS is accepted by the lane module to be serially transmitted. TxReadyHS is valid on rising edges of TxByteClkHS. Valid data has to be provided for the whole duration of active TxReadyHS.
- **Shutdown** (Input): Shutdown Lane Module. This active high signal forces the lane module into “shutdown”, disabling all activity. All line drivers, including terminators, are turned off when Shutdown is asserted. When Shutdown is high, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Shutdown is a level sensitive signal and does not depend on any clock.
- **TxUlpmEsc** (Input): Escape ~~mode~~Mode Transmit Ultra Low Power. This active high signal is asserted with TxRequestEsc to cause the lane module to enter the Ultra Low-Power mode. The lane module remains in this mode until TxRequestEsc is de-asserted.
- **TxRequestEsc** (Input): This active high signal, asserted together with TxUlpmEsc is used to request entry into ~~escape mode~~Escape Mode. Once in ~~escape mode~~Escape Mode, the lane stays in ~~escape mode~~Escape Mode until TxRequestEsc is de-asserted. TxRequestEsc is only asserted by the protocol while TxRequestHS is low.
- **TxClkEsc** (Input): Escape ~~mode~~Mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. It is therefore constrained by the normative part of the ***[MIPI01]***.

B.4.4 CSI-2 Data Lane Receiver

The suggested implementation can be seen in ***Figure ~~186~~202***.

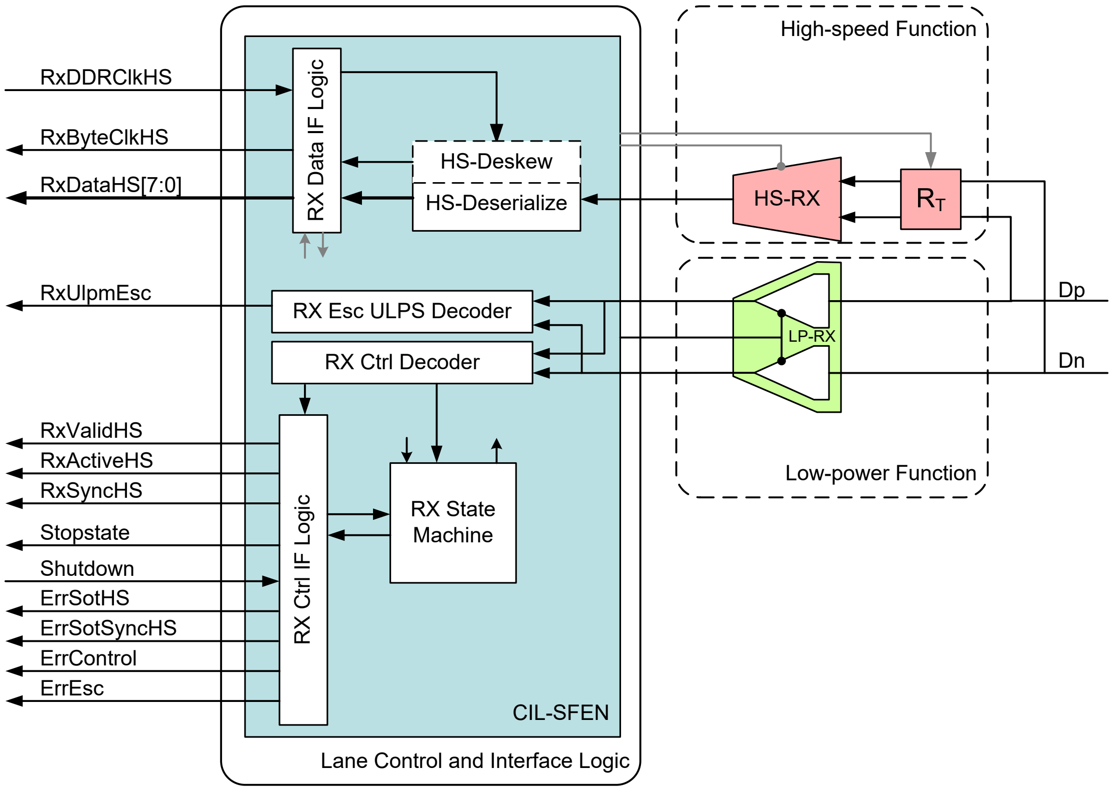


Figure 202 CSI-2 Data Lane Receiver

The modular D-PHY components used to build a CSI-2 data lane receiver are:

- **LP-RX** for the Low-power function
- **HS-RX** for the High-speed function
- **CIL-SFEN** for the Lane control and interface logic. For optional deskew calibration support the data lane receiver detects a transmitted deskew calibration pattern and performs optimum deskew of the Data with respect to the RxDDRClkHS Clock.

The PPI interface signals to the CSI-2 data lane receiver are:

- **RxDDRClkHS** (Input): High-Speed Receive DDR Clock used to sample the date in all data lanes. This signal is supplied by the CSI-2 clock lane receiver.
- **RxByteClkHS** (Output): High-Speed Receive Byte Clock. This signal is used to synchronize signals in the high-speed receive clock domain. The RxByteClkHS is generated by dividing the received RxDDRClkHS.
- **RXDataHS[7:0]** (Output): High-Speed Receive Data. Eight bit high-speed data received by the lane module. The signal connected to RxDataHS[0] was received first. Data is transferred on rising edges of RxByteClkHS.
- **RxValidHS** (Output): High-Speed Receive Data Valid. This active high signal indicates that the lane module is driving valid data to the protocol on the RxDataHS output. There is no "RxReadyHS" signal, and the protocol is expected to capture RxDataHS on every rising edge of

RxByteClkHS where RxValidHS is asserted. There is no provision for the protocol to slow down ("throttle") the receive data.

- **RxActiveHS** (Output): High-Speed Reception Active. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.
- **RxSyncHS** (Output): Receiver Synchronization Observed. This active high signal indicates that the lane module has seen an appropriate synchronization event. In a typical high-speed transmission, RxSyncHS is high for one cycle of RxByteClkHS at the beginning of a high-speed transmission when RxActiveHS is first asserted. This signal missing is signaled using ErrSotSyncHS.
- **RxUlpmEsc** (Output): Escape Ultra Low Power (Receive) mode. This active high signal is asserted to indicate that the lane module has entered the Ultra Low-Power mode. The lane module remains in this mode with RxUlpmEsc asserted until a Stop state is detected on the lane interconnect.
- **Stopstate** (Output): Lane is in Stop state. This active high signal indicates that the lane module is currently in Stop state. This signal is asynchronous.
- **Shutdown** (Input): Shutdown Lane Module. This active high signal forces the lane module into "shutdown", disabling all activity. All line drivers, including terminators, are turned off when Shutdown is asserted. When Shutdown is high, all PPI outputs are driven to the default inactive state. Shutdown is a level sensitive signal and does not depend on any clock.
- **ErrSotHS** (Output): Start-of-Transmission (SoT) Error. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxByteClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
- **ErrSotSyncHS** (Output): Start-of-Transmission Synchronization Error. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error is asserted for one cycle of RxByteClkHS.
- **ErrControl** (Output): Control Error. This signal is asserted when an incorrect line state sequence is detected.
- **ErrEsc** (Output): Escape Entry Error. If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state. The only escape entry command supported by the receiver is the ULPS.

Annex C CSI-2 Recommended Receiver Error Behavior (informative)

C.1 Overview

This section proposes one approach to handling error conditions at the receiving side of a CSI-2 Link. Although the section is informative and therefore does not affect compliance for CSI-2, the approach is offered by the MIPI Camera Working Group as a recommended approach. The CSI-2 receiver assumes the case of a CSI-2 Link comprised of unidirectional Lanes for D-PHY Clock and Data Lanes with Escape Mode functionality on the Data Lanes and a continuously running clock. This Annex does not discuss other cases, including those that differ widely in implementation, where the implementer should consider other potential error situations.

Because of the layered structure of a compliant CSI-2 receiver implementation, the error behavior is described in a similar way with several "levels" where errors could occur, each requiring some implementation at the appropriate functional layer of the design:

- *D-PHY Level errors*
  Refers to any PHY related transmission error and is unrelated to the transmission's contents:
  - Start of Transmission (SoT) errors, which can be:
    - Recoverable, if the PHY successfully identifies the Sync code but an error was detected.
    - Unrecoverable, if the PHY does not successfully identify the sync code but does detect a HS transmission.
  - *Control Error,* which signals that the PHY has detected a control sequence that should not be present in this implementation of the Link.
- *Packet Level errors*
  This type of error refers strictly to data integrity of the received Packet Header and payload data:
  - *Packet Header errors*, signaled through the ECC code, that result in:
    - A single bit-error, which can be detected and corrected by the ECC code
    - Two bit-errors in the header, which can be detected but not corrected by the ECC code, resulting in a corrupt header
  - *Packet payload errors*, signaled through the CRC code
- *Protocol Decoding Level errors*
  This type of error refers to errors present in the decoded Packet Header or errors resulting from an incomplete sequence of events:
  - *Frame Sync Error*, caused when a FS could not be successfully paired with a FE on a given virtual channel
  - *Unrecognized ID,* caused by the presence of an unimplemented or unrecognized ID in the header

The proposed methodology for handling errors is signal based, since it offers an easy path to a viable CSI-2 implementation that handles all three error levels. Even so, error handling at the Protocol Decoding Level should implement sequential behavior using a state machine for proper operation.

C.2 D-PHY Level Error

The recommended behavior for handling this error level covers only those errors generated by the Data Lane(s), since an implementation can assume that the Clock Lane is running reliably as provided by the expected BER of the Link, as discussed in ***[MIPI01]***. Note that this error handling behavior assumes unidirectional Data Lanes without ~~escape mode~~Escape Mode functionality. Considering this, and using the signal names and descriptions from the ***[MIPI01]***, PPI Annex, signal errors at the PHY-Protocol Interface (PPI) level consist of the following:

- **ErrSotHS:** Start-of-Transmission (SoT) Error. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxByteClkHS. This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced.
- **ErrSotSyncHS:** Start-of-Transmission Synchronization Error. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of RxByteClkHS.
- **ErrControl:** Control Error. This signal is asserted when an incorrect line state sequence is detected. For example, if a Turn-around request or Escape Mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains high until the next change in line state.

The recommended receiver error behavior for this level is:

- **ErrSotHS** should be passed to the Application Layer. Even though the error was detected and corrected and the Sync mechanism was unaffected, confidence in the data integrity is reduced and the application should be informed. This signal should be referenced to the corresponding data packet.
- **ErrSotSyncHS** should be passed to the Protocol Decoding Level, since this is an unrecoverable error. An unrecoverable type of error should also be signaled to the Application Layer, since the whole transmission until the first D-PHY Stop state should be ignored if this type of error occurs.
- **ErrControl** should be passed to the Application Layer, since this type of error doesn’t normally occur if the interface is configured to be unidirectional. Even so, the application should be aware of the error and configure the interface accordingly through other, implementation specific-means that are out of scope for this specification.

Also, it is recommended that the PPI StopState signal for each implemented Lane should be propagated to the Application Layer during configuration or initialization to indicate the Lane is ready.

C.3 Packet Level Error

The recommended behavior for this error level covers only errors recognized by decoding the Packet Header's ECC field and computing the CRC of the data payload.

Decoding and applying the ECC field of the Packet Header should signal the following errors:

- **ErrEccDouble:** Asserted when an ECC syndrome was computed and two bit-errors are detected in the received Packet Header.
- **ErrEccCorrected:** Asserted when an ECC syndrome was computed and a single bit-error in the Packet Header was detected and corrected.
- **ErrEccNoError:** Asserted when an ECC syndrome was computed and the result is zero indicating a Packet Header that is considered to be without errors or has more than two bit-errors. CSI-2's ECC mechanism cannot detect this type of error.

Also, computing the CRC code over the whole payload of the received packet could generate the following errors:

- **ErrCrc:** Asserted when the computed CRC code is different than the received CRC code.
- **ErrID:** Asserted when a Packet Header is decoded with an unrecognized or unimplemented data ID.

The recommended receiver error behavior for this level is:

- **ErrEccDouble** should be passed to the Application Layer since assertion of this signal proves that the Packet Header information is corrupt, and therefore the WC is not usable, and thus the packet end cannot be estimated. Commonly, this type of error will be accompanied with an ErrCrc. This type of error should also be passed to the Protocol Decoding Level, since the whole transmission until D-PHY Stop state should be ignored.
- **ErrEccCorrected** should be passed to the Application Layer since the application should be informed that an error had occurred but was corrected, so the received Packet Header was unaffected, although the confidence in the data integrity is reduced.
- **ErrEccNoError** can be passed to the Protocol Decoding Level to signal the validity of the current Packet Header.
- **ErrCrc** should be passed to the Protocol Decoding Level to indicate that the packet's payload data might be corrupt.
- **ErrID** should be passed to the Application Layer to indicate that the data packet is unidentified and cannot be unpacked by the receiver. This signal should be asserted after the ID has been identified and de-asserted on the first Frame End (FE) on same virtual channel.

C.4 Protocol Decoding Level Error

The recommended behavior for this error level covers errors caused by decoding the Packet Header information and detecting a sequence that is not allowed by the CSI-2 protocol or a sequence of detected errors by the previous layers. CSI-2 implementers will commonly choose to implement this level of error handling using a state machine that should be paired with the corresponding virtual channel. The state machine should generate at least the following error signals:

- **ErrFrameSync:** Asserted when a Frame End (FE) is not paired with a Frame Start (FS) on the same virtual channel. An ErrSotSyncHS should also generate this error signal.
- **ErrFrameData:** Asserted after a FE when the data payload received between FS and FE contains errors.

The recommended receiver error behavior for this level is:

- **ErrFrameSync** should be passed to the Application Layer with the corresponding virtual channel, since the frame could not be successfully identified. Several error cases on the same virtual channel can be identified for this type of error.
  - If a FS is followed by a second FS on the same virtual channel, the frame corresponding to the first FS is considered in error.
  - If a Packet Level ErrEccDouble was signaled from the Protocol Layer, the whole transmission until the first D-PHY Stop-state should be ignored since it contains no information that can be safely decoded and cannot be qualified with a data valid signal.
  - If a FE is followed by a second FE on the same virtual channel, the frame corresponding to the second FE is considered in error.
  - If an ErrSotSyncHS was signaled from the PHY Layer, the whole transmission until the first D-PHY Stop state should be ignored since it contains no information that can be safely decoded and cannot be qualified with a data valid signal.
- **ErrFrameData**: should be passed to the Application Layer to indicate that the frame contains data errors. This signal should be asserted on any ErrCrc and de-asserted on the first FE.

Annex D CSI-2 Sleep Mode (informative)

D.1 Overview

Since a camera in a mobile terminal spends most of its time in an inactive state, implementers need a way to put the CSI-2 Link into a low power mode that approaches, or may be as low as, the leakage level. This section proposes one approach for putting a CSI-2 Link in a "Sleep Mode" (SLM). Although the section is informative and therefore does not affect compliance for CSI-2, the approach is offered by the MIPI Camera Working Group as a recommended approach.

This approach relies on an aspect of a D-PHY or C-PHY transmitter's behavior that permits regulators to be disabled safely when LP-00 (Space state) is on the Link. Accordingly, this will be the output state for a CSI-2 camera transmitter in SLM.

SLM can be thought of as a three-phase process:

1. SLM Command Phase. The 'ENTER SLM' command is issued to the TX side only, or to both sides of the Link.
2. SLM Entry Phase. The CSI-2 Link has entered, or is entering, the SLM in a controlled or synchronized manner. This phase is also part of the power-down process.
3. SLM Exit Phase. The CSI-2 Link has exited the SLM and the interface/device is operational. This phase is also part of the power-up process.

In general, when in SLM, both sides of the interface will be in ULPS, as defined in ***[MIPI01]*** or ***[MIPI02]***.

D.2 SLM Command Phase

For the first phase, initiation of SLM occurs by a mechanism outside the scope of CSI-2. Of the many mechanisms available, two examples would be:

1. An External SLEEP signal input to the CSI-2 transmitter and optionally also to the CSI-2 Receiver. When at logic 0, the CSI-2 Transmitter and the CSI Receiver (if connected) will enter Sleep mode. When at logic 1, normal operation will take place.
2. A CCI control command, provided on the I^2C control Link, is used to trigger ULPS.

D.3 SLM Entry Phase

For the second phase, consider one option:

Only the TX side enters SLM and propagates the ULPS to the RX side by sending a D-PHY or C-PHY 'ULPS' command on each Lane. In ***Figure ~~187~~203***, only the Data Lane 'ULPS' command is used as an example. The D-PHY Dp, Dn, and C-PHY Data_A, Data_C are logical signal names and do not imply specific multiplexing on dual mode (combined D-PHY and C-PHY) implementations.

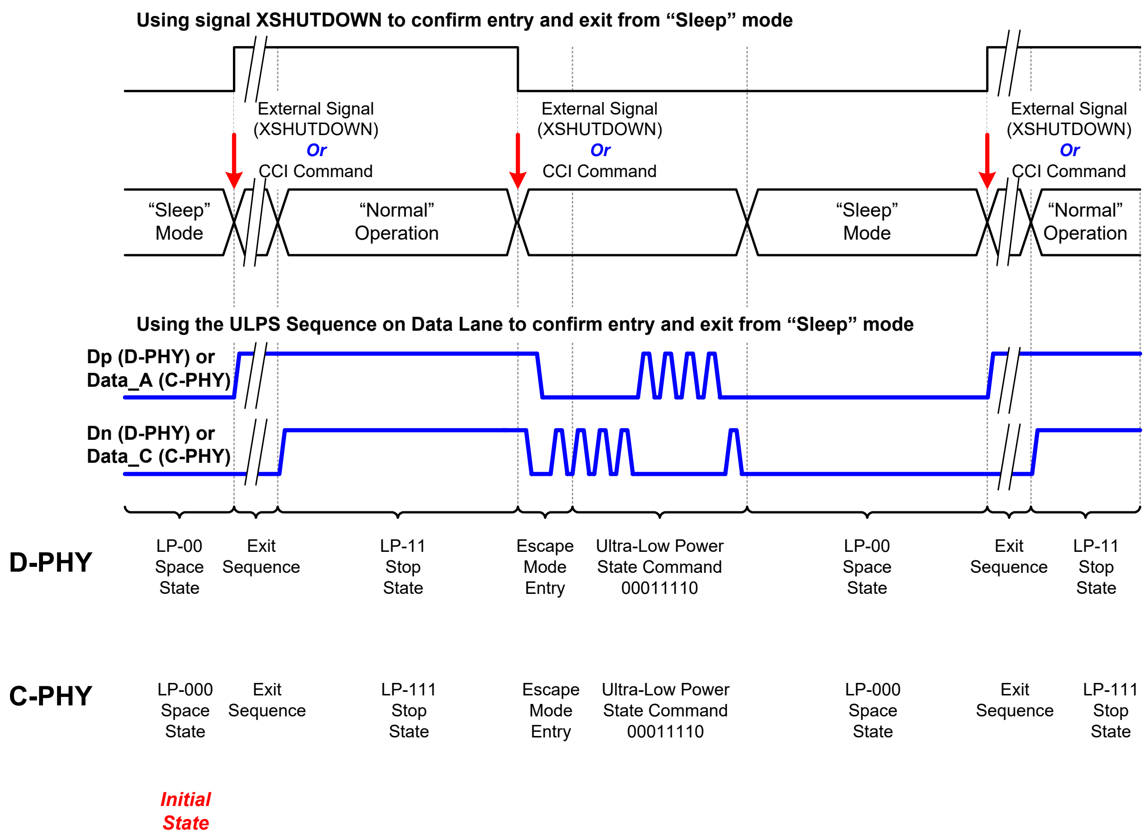


Figure 203 SLM Synchronization

D.4 SLM Exit Phase

For the third phase, three options are presented and assume the camera peripheral is in ULPS or Sleep mode at power-up:

1. Use a SLEEP signal to power-up both sides of the interface.
2. Detect any CCI activity on the I^2C control Link, which was in the 00 state ({SCL, SDA}), after receiving the I^2C instruction to enter ULPS command as per ***Section D.2***, option 2. Any change on those lines should wake up the camera peripheral. The drawback of this method is that I^2C lines are used exclusively for control of the camera.
3. Detect a wake-up sequence on the I^2C lines. This sequence, which may vary by implementation, shall not disturb the I^2C interface so that it can be used by other devices. One example sequence is: StopI2C-StartI2C-StopI2C. See ***Section 6*** for details on CCI.

A handshake using the ‘ULPS’ mechanism as described in ***[MIPI01]*** or ***[MIPI02]***, as appropriate, should be used for powering up the interface.

Annex E Data Compression for RAW Data Types (normative)

A CSI-2 implementation using RAW data types may support compression on the interface to reduce the data bandwidth requirements between the host processor and a camera module. Data compression is not mandated by this Specification. However, if data compression is used, it shall be implemented as described in this annex.

Data compression schemes use an X–Y–Z naming convention where X is the number of bits per pixel in the original image, Y is the encoded (compressed) bits per pixel and Z is the decoded (uncompressed) bits per pixel.

The following data compression schemes are defined:

- 12-10-12
- 12–8–12
- 12–7–12
- 12–6–12
- 10–8–10
- 10–7–10
- 10–6–10

To identify the type of data on the CSI-2 interface, packets with compressed data shall have a User Defined Data Type value as indicated in ***Table ~~45~~60***. Note that User Defined data type codes are not reserved for compressed data types. Therefore, a CSI-2 device shall be able to communicate over the CCI the data compression scheme represented by a particular User Defined data type code for each scheme supported by the device. Note that the method to communicate the data compression scheme to Data Type code mapping is beyond the scope of this document.

The number of bits in a packet shall be a multiple of eight. Therefore, implementations with data compression schemes that result in each pixel having other than eight encoded bits per pixel shall transfer the encoded data in a packed pixel format. For example, the 12–7–12 data compression scheme uses a packed pixel format as described in ***Section 11.4.2*** except the Data Type value in the Packet Header is a User Defined data type code.

The data compression schemes in this annex are lossy and designed to encode each line independent of the other lines in the image.

The following definitions are used in the description of the data compression schemes:

- **Xorig** is the original pixel value
- **Xpred** is the predicted pixel value
- **Xdiff** is the difference value (**Xorig** - **Xpred**)
- **Xenco** is the encoded value
- **Xdeco** is the decoded pixel value

The data compression system consists of encoder, decoder and predictor blocks as shown in ***Figure ~~188~~204***.

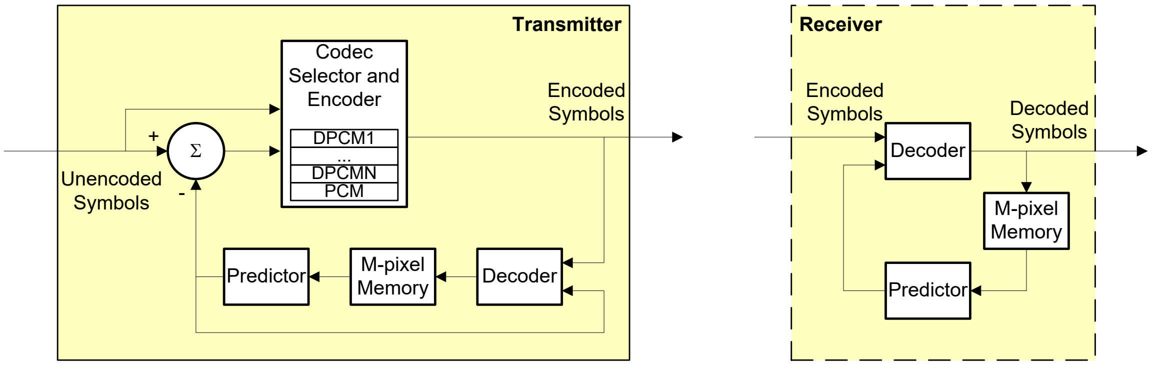


Figure 204 Data Compression System Block Diagram

The encoder uses a simple algorithm to encode the pixel values. A fixed number of pixel values at the beginning of each line are encoded without using prediction. These first few values are used to initialize the predictor block. The remaining pixel values on the line are encoded using prediction.

If the predicted value of the pixel (**Xpred)** is close enough to the original value of the pixel (**Xorig**) (abs(**Xorig - Xpred**) < difference limit), its difference value (**Xdiff**) is quantized using a DPCM codec. Otherwise, **Xorig** is quantized using a PCM codec. The quantized value is combined with a code word describing the codec used to quantize the pixel and the sign bit, if applicable, to create the encoded value (**Xenco**).

E.1 Predictors

In order to have meaningful data transfer, both the transmitter and the receiver need to use the same predictor block.

The order of pixels in a raw image is shown in ***Figure ~~189~~205***.

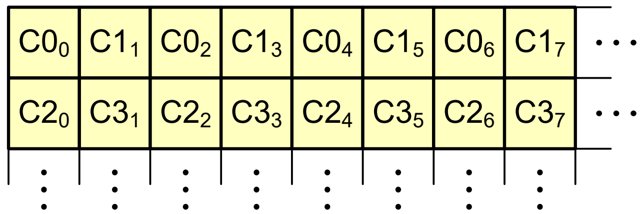


Figure 205 Pixel Order of the Original Image

Figure ~~190~~206 shows an example of the pixel order with RGB data.

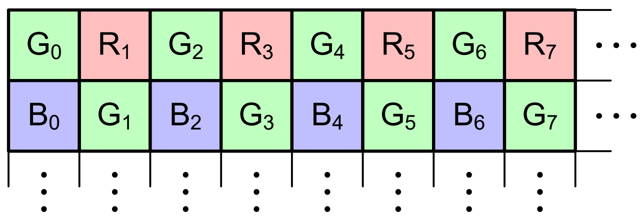


Figure 206 Example Pixel Order of the Original Image

Two predictors are defined for use in the data compression schemes.

Predictor1 uses a very simple algorithm and is intended to minimize processing power and memory size requirements. Typically, this predictor is used when the compression requirements are modest and the original image quality is high. Predictor1 should be used with 10–8–10, 10–7–10, 12-10-12, and 12–8–12 data compression schemes.

The second predictor, Predictor2, is more complex than Predictor1. This predictor provides slightly better prediction than Predictor1 and therefore the decoded image quality can be improved compared to Predictor1. Predictor2 should be used with 10–6–10, 12–7–12, and 12–6–12 data compression schemes.

Both receiver and transmitter shall support Predictor1 for all data compression schemes.

E.1.1 Predictor1

Predictor1 uses only the previous same color component value as the prediction value. Therefore, only a two-pixel deep memory is required.

The first two pixels ($C0_0$, $C1_1$ / $C2_0$, $C3_1$ or as in example G_0, R_1 / B_0, G_1) in a line are encoded without prediction.

The prediction values for the remaining pixels in the line are calculated using the previous same color decoded value, **Xdeco**. Therefore, the predictor equation can be written as follows:

```
Xpred( n ) = Xdeco( n-2 )
```

E.1.2 Predictor2

Predictor2 uses the four previous pixel values, when the prediction value is evaluated. This means that also the other color component values are used, when the prediction value has been defined. The predictor equations can be written as shown in the following formulas.

Predictor2 uses all color components of the four previous pixel values to create the prediction value. Therefore, a four-pixel deep memory is required.

The first pixel ($C0_0$ / $C2_0$, or as in example G_0 / B_0) in a line is coded without prediction.

The second pixel ($C1_1$ / $C3_1$ or as in example R_1 / G_1) in a line is predicted using the previous decoded different color value as a prediction value. The second pixel is predicted with the following equation:

```
Xpred( n ) = Xdeco( n-1 )
```

The third pixel ($C0_2$ / $C2_2$ or as in example G_2 / B_2) in a line is predicted using the previous decoded same color value as a prediction value. The third pixel is predicted with the following equation:

```
Xpred( n ) = Xdeco( n-2 )
```

The fourth pixel ($C1_3$ / $C3_3$ or as in example R_3 / G_3) in a line is predicted using the following equation:

```
if ((Xdeco( n-1 ) <= Xdeco( n-2 ) AND Xdeco( n-2 ) <= Xdeco( n-3 )) OR
   (Xdeco( n-1 ) >= Xdeco( n-2 ) AND Xdeco( n-2 ) >= Xdeco( n-3 ))) then
      Xpred( n ) = Xdeco( n-1 )
else
   Xpred( n ) = Xdeco( n-2 )
endif
```

Other pixels in all lines are predicted using the equation:

```
if ((Xdeco( n-1 ) <= Xdeco( n-2 ) AND Xdeco( n-2 ) <= Xdeco( n-3 )) OR
   (Xdeco( n-1 ) >= Xdeco( n-2 ) AND Xdeco( n-2 ) >= Xdeco( n-3 ))) then
      Xpred( n ) = Xdeco( n-1 )
else if ((Xdeco( n-1 ) <= Xdeco( n-3 ) AND Xdeco( n-2 ) <= Xdeco( n-4 )) OR
   (Xdeco( n-1 ) >= Xdeco( n-3 ) AND Xdeco( n-2 ) >= Xdeco( n-4 ))) then
      Xpred( n ) = Xdeco( n-2 )
else
   Xpred( n ) = (Xdeco( n-2 ) + Xdeco( n-4 ) + 1) / 2
endif
```

E.2 Encoders

There are seven different encoders available, one for each data compression scheme.

For all encoders, the formula used for non-predicted pixels (beginning of lines) is different than the formula for predicted pixels.

E.2.1 Coder for 10–8–10 Data Compression

The 10–8–10 coder offers a 20% bit rate reduction with very high image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 4
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 32) then
    use DPCM1
else if (abs(Xdiff( n )) < 64) then
    use DPCM2
else if (abs(Xdiff( n )) < 128) then
    use DPCM3
else
    use PCM
endif
```

E.2.1.1 DPCM1 for 10–8–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "00 s xxxxx"
```

where,

```
"00" is the code word
"s" is the sign bit
"xxxxx" is the five bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note: Zero code has been avoided (0 is sent as -0).

E.2.1.2 DPCM2 for 10–8–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 32) / 2
```

E.2.1.3 DPCM3 for 10–8–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 64) / 4
```

E.2.1.4 PCM for 10–8–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxx" is the seven bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 8
```


E.2.2 Coder for 10–7–10 Data Compression

The 10–7–10 coder offers 30% bit rate reduction with high image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 8
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 8) then
    use DPCM1
else if (abs(Xdiff( n )) < 16) then
    use DPCM2
else if (abs(Xdiff( n )) < 32) then
    use DPCM3
else if (abs(Xdiff( n )) < 160) then
    use DPCM4
else
    use PCM
endif
```

E.2.2.1 DPCM1 for 10–7–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "000 s xxx"
```

where,

```
"000" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note: Zero code has been avoided (0 is sent as -0).

E.2.2.2 DPCM2 for 10–7–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0010 s xx"
```

where,

```
"0010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 8) / 2
```

E.2.2.3 DPCM3 for 10–7–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s xx"
```

where,

```
"0011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 16) / 4
```

E.2.2.4 DPCM4 for 10–7–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "01 s xxxx"
```

where,

```
"01" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 32) / 8
```

E.2.2.5 PCM for 10–7–10 Coder

Xenco(**n**) has the following format:

```
Xenco( n ) = "1 xxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxx" is the six bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 16
```

E.2.3 Coder for 10–6–10 Data Compression

The 10–6–10 coder offers 40% bit rate reduction with acceptable image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 16
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 1) then
    use DPCM1
else if (abs(Xdiff( n )) < 3) then
    use DPCM2
else if (abs(Xdiff( n )) < 11) then
    use DPCM3
else if (abs(Xdiff( n )) < 43) then
    use DPCM4
else if (abs(Xdiff( n )) < 171) then
    use DPCM5
else
    use PCM
endif
```

E.2.3.1 DPCM1 for 10–6–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "00000 s"
```

where,

```
"00000" is the code word
"s" is the sign bit
the value field is not used
```

The coder equation is described as follows:

```
sign = 1
Note: Zero code has been avoided (0 is sent as -0).
```

E.2.3.2 DPCM2 for 10–6–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "00001 s"
```

where,

```
"00001" is the code word
"s" is the sign bit
the value field is not used
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
```

E.2.3.3 DPCM3 for 10–6–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s x"
```

where,

```
"0001" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
value = (abs(Xdiff( n )) - 3) / 4
endif
```

E.2.3.4 DPCM4 for 10–6–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "001 s xx"
```

where,

```
"001" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 11) / 8
```

E.2.3.5 DPCM5 for 10–6–10 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "01 s xxx"
```

where,

```
"01" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 43) / 16
```

E.2.3.6 PCM for 10–6–10 Coder

Xenco(**n**) has the following format:

```
Xenco( n ) = "1 xxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxx" is the five bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 32
```

E.2.4 Coder for 12-10-12 Data Compression

The 12–10–12 coder offers a 16.7% bit rate reduction with very high image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 4
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 128) then
    use DPCM1
else if (abs(Xdiff( n )) < 256) then
    use DPCM2
else if (abs(Xdiff( n )) < 512) then
    use DPCM3
else
    use PCM
endif
```

E.2.4.1 DPCM1 for 12–10–12 Coder

Xenco(**n**) has the following format:

```
Xenco( n ) = "00 s xxxxxxx"
```

where,

```
"00" is the code word
"s" is the sign bit
"xxxxxxx" is the seven bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note:

Zero code has been avoided (0 is sent as -0).

E.2.4.2 DPCM2 for 12–10–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxxxx" is the six bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 128) / 2
```

E.2.4.3 DPCM3 for 12–10–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxxxx" is the six bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 256) / 4
```

E.2.4.4 PCM for 12–10–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxxxx" is the nine bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 8
```

E.2.5 Coder for 12–8–12 Data Compression

The 12–8–12 coder offers 33% bit rate reduction with very high image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 16
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 8) then
    use DPCM1
else if (abs(Xdiff( n )) < 40) then
    use DPCM2
else if (abs(Xdiff( n )) < 104) then
    use DPCM3
else if (abs(Xdiff( n )) < 232) then
    use DPCM4
else if (abs(Xdiff( n )) < 360) then
    use DPCM5
else
    use PCM
```

E.2.5.1 DPCM1 for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s xxx"
```

where,

```
"0000" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note: Zero code has been avoided (0 is sent as -0).

E.2.5.2 DPCM2 for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 8) / 2
```

E.2.5.3 DPCM3 for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 40) / 4
```

E.2.5.4 DPCM4 for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "001 s xxxx"
```

where,

```
"001" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
    sign = 1
else
    sign = 0
endif
value = (abs(Xdiff( n )) - 104) / 8
```

E.2.5.5 DPCM5 for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s xxx"
```

where,

```
"0001" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 232) / 16
```

E.2.5.6 PCM for 12–8–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxx" is the seven bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 32
```

E.2.6 Coder for 12–7–12 Data Compression

The 12–7–12 coder offers 42% bit rate reduction with high image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 32
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 4) then
    use DPCM1
else if (abs(Xdiff( n )) < 12) then
    use DPCM2
else if (abs(Xdiff( n )) < 28) then
    use DPCM3
else if (abs(Xdiff( n )) < 92) then
    use DPCM4
else if (abs(Xdiff( n )) < 220) then
    use DPCM5
else if (abs(Xdiff( n )) < 348) then
    use DPCM6
else
    use PCM
endif
```

E.2.6.1 DPCM1 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s xx"
```

where,

```
"0000" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note: Zero code has been avoided (0 is sent as -0).

E.2.6.2 DPCM2 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s xx"
```

where,

```
"0001" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 4) / 2
```

E.2.6.3 DPCM3 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0010 s xx"
```

where,

```
"0010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 12) / 4
```

E.2.6.4 DPCM4 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 28) / 8
```

E.2.6.5 DPCM5 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 92) / 16
```

E.2.6.6 DPCM6 for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s xx"
```

where,

```
"0011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 220) / 32
```

E.2.6.7 PCM for 12–7–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxx" is the six bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 64
```

E.2.7 Coder for 12–6–12 Data Compression

The 12–6–12 coder offers 50% bit rate reduction with acceptable image quality.

Pixels without prediction are encoded using the following formula:

```
Xenco( n ) = Xorig( n ) / 64
```

To avoid a full-zero encoded value, the following check is performed:

```
if (Xenco( n ) == 0) then
    Xenco( n ) = 1
endif
```

Pixels with prediction are encoded using the following formula:

```
if (abs(Xdiff( n )) < 2) then
    use DPCM1
else if (abs(Xdiff( n )) < 10) then
    use DPCM3
else if (abs(Xdiff( n )) < 42) then
    use DPCM4
else if (abs(Xdiff( n )) < 74) then
    use DPCM5
else if (abs(Xdiff( n )) < 202) then
    use DPCM6
else if (abs(Xdiff( n )) < 330) then
    use DPCM7
else
    use PCM
endif
```

*Note: **DPCM2** is not used.*

E.2.7.1 DPCM1 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s x"
```

where,

```
"0000" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) <= 0) then
    sign = 1
else
    sign = 0
endif
value = abs(Xdiff( n ))
```

Note: Zero code has been avoided (0 is sent as -0).

E.2.7.2 DPCM3 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s x"
```

where,

```
"0001" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 2) / 4
```

E.2.7.3 DPCM4 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 10) / 8
```

E.2.7.4 DPCM5 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0010 s x"
```

where,

```
"0010" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 42) / 16
```

E.2.7.5 DPCM6 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 74) / 32
```

E.2.7.6 DPCM7 for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s x"
```

where,

```
"0011" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The coder equation is described as follows:

```
if (Xdiff( n ) < 0) then
   sign = 1
else
   sign = 0
endif
value = (abs(Xdiff( n )) - 202) / 64
```

E.2.7.7 PCM for 12–6–12 Coder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxx" is the five bit value field
```

The coder equation is described as follows:

```
value = Xorig( n ) / 128
```

E.3 Decoders

There are six different decoders available, one for each data compression scheme.

For all decoders, the formula used for non-predicted pixels (beginning of lines) is different than the formula for predicted pixels.

E.3.1 Decoder for 10–8–10 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 4 * Xenco( n ) + 2
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0xc0 == 0x00) then
    use DPCM1
else if (Xenco( n ) & 0xe0 == 0x40) then
    use DPCM2
else if (Xenco( n ) & 0xe0 == 0x60) then
    use DPCM3
else
    use PCM
endif
```

E.3.1.1 DPCM1 for 10–8–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "00 s xxxxx"
```

where,

```
"00" is the code word
"s" is the sign bit
"xxxxx" is the five bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x20
value = Xenco( n ) & 0x1f
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.1.2 DPCM2 for 10–8–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 2 * (Xenco( n ) & 0xf) + 32
if (sign > 0) then
   Xdeco( n ) = Xpred( n ) - value
else
   Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.1.3 DPCM3 for 10–8–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 4 * (Xenco( n ) & 0xf) + 64 + 1
if (sign > 0) then
   Xdeco( n ) = Xpred( n ) - value
   if (Xdeco( n ) < 0) then
      Xdeco( n ) = 0
   endif
else
   Xdeco( n ) = Xpred( n ) + value
   if (Xdeco( n ) > 1023) then
      Xdeco( n ) = 1023
   endif
endif
```

E.3.1.4 PCM for 10–8–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxx" is the seven bit value field
```

The codec equation is described as follows:

```
value = 8 * (Xenco( n ) & 0x7f)
if (value > Xpred( n )) then
   Xdeco( n ) = value + 3
endif
else
   Xdeco( n ) = value + 4
endif
```

E.3.2 Decoder for 10–7–10 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 8 * Xenco( n ) + 4
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0x70 == 0x00) then
    use DPCM1
else if (Xenco( n ) & 0x78 == 0x10) then
    use DPCM2
else if (Xenco( n ) & 0x78 == 0x18) then
    use DPCM3
else if (Xenco( n ) & 0x60 == 0x20) then
    use DPCM4
else
    use PCM
endif
```

E.3.2.1 DPCM1 for 10–7–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "000 s xxx"
```

where,

```
"000" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = Xenco( n ) & 0x7
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.2.2 DPCM2 for 10–7–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0010 s xx"
```

where,

```
"0010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 2 * (Xenco( n ) & 0x3) + 8
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.2.3 DPCM3 for 10–7–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s xx"
```

where,

```
"0011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 4 * (Xenco( n ) & 0x3) + 16 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 1023) then
        Xdeco( n ) = 1023
    endif
endif
```

E.3.2.4 DPCM4 for 10–7–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "01 s xxxx"
```

where,

```
"01" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 8 * (Xenco( n ) & 0xf) + 32 + 3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 1023) then
        Xdeco( n ) = 1023
    endif
endif
```


E.3.2.5 PCM for 10–7–10 Decoder

Xenco(**n**) has the following format:

```
Xenco( n ) = "1 xxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxx" is the six bit value field
```

The codec equation is described as follows:

```
value = 16 * (Xenco( n ) & 0x3f)
if (value > Xpred( n )) then
   Xdeco( n ) = value + 7
else
   Xdeco( n ) = value + 8
endif
```

E.3.3 Decoder for 10–6–10 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 16 * Xenco( n ) + 8
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0x3e == 0x00) then
    use DPCM1
else if (Xenco( n ) & 0x3e == 0x02) then
    use DPCM2
else if (Xenco( n ) & 0x3c == 0x04) then
    use DPCM3
else if (Xenco( n ) & 0x38 == 0x08) then
    use DPCM4
else if (Xenco( n ) & 0x30 == 0x10) then
    use DPCM5
else
    use PCM
endif
```

E.3.3.1 DPCM1 for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "00000 s"
```

where,

```
"00000" is the code word
"s" is the sign bit
the value field is not used
```

The codec equation is described as follows:

```
Xdeco( n ) = Xpred( n )
```

E.3.3.2 DPCM2 for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "00001 s"
```

where,

```
"00001" is the code word
"s" is the sign bit
the value field is not used
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x1
value = 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.3.3 DPCM3 for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s x"
```

where,

```
"0001" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x2
value = 4 * (Xenco( n ) & 0x1) + 3 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 1023) then
        Xdeco( n ) = 1023
    endif
endif
```

E.3.3.4 DPCM4 for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "001 s xx"
```

where,

```
"001" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 8 * (Xenco( n ) & 0x3) + 11 + 3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 1023) then
        Xdeco( n ) = 1023
    endif
endif
```

E.3.3.5 DPCM5 for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "01 s xxx"
```

where,

```
"01" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = 16 * (Xenco( n ) & 0x7) + 43 + 7
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 1023) then
        Xdeco( n ) = 1023
    endif
endif
```

E.3.3.6 PCM for 10–6–10 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxx" is the five bit value field
```

The codec equation is described as follows:

```
value = 32 * (Xenco( n ) & 0x1f)
if (value > Xpred( n )) then
    Xdeco( n ) = value + 15
else
    Xdeco( n ) = value + 16
endif
```

E.3.4 Decoder for 12–10–12 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 4 * Xenco( n ) + 2
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0x300 == 0x000) then
    use DPCM1
else if (Xenco( n ) & 0x380 == 0x100) then
    use DPCM2
else if (Xenco( n ) & 0x380 == 0x180) then
    use DPCM3
else
    use PCM
endif
```

E.3.4.1 DPCM1 for 12–10–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "00 s xxxxxxx"
```

where,

```
"00" is the code word
"s" is the sign bit
"xxxxxxx" is the seven bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x80
value = Xenco( n ) & 0x7f
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.4.2 DPCM2 for 12–10–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxxxx" is the six bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x40
value = 2 * (Xenco( n ) & 0x3f) + 128
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.4.3 DPCM3 for 12–10–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxxxx" is the six bit value field
```

The decoder equation is described as follows:

```
sign = Xenco( n ) & 0x40
value = 4 * (Xenco( n ) & 0x3f) + 256 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.4.4 PCM for 12–10–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxxxx" is the nine bit value field
```

The codec equation is described as follows:

```
value = 8 * (Xenco( n ) & 0x1ff)
if (value > Xpred( n )) then
   Xdeco( n ) = value + 3
endif
else
   Xdeco( n ) = value + 4
endif
```

E.3.5 Decoder for 12–8–12 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 16 * Xenco( n ) + 8
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0xf0 == 0x00) then
   use DPCM1
else if (Xenco( n ) & 0xe0 == 0x60) then
   use DPCM2
else if (Xenco( n ) & 0xe0 == 0x40) then
   use DPCM3
else if (Xenco( n ) & 0xe0 == 0x20) then
   use DPCM4
else if (Xenco( n ) & 0xf0 == 0x10) then
   use DPCM5
else
   use PCM
endif
```

E.3.5.1 DPCM1 for 12–8–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s xxx"
```

where,

```
"0000" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = Xenco( n ) & 0x7
if (sign > 0) then
   Xdeco( n ) = Xpred( n ) - value
else
   Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.5.2 DPCM2 for 12–8–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 2 * (Xenco( n ) & 0xf) + 8
if (sign > 0) then
   Xdeco( n ) = Xpred( n ) - value
else
   Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.5.3 DPCM3 for 12–8–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 4 * (Xenco( n ) & 0xf) + 40 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.5.4 DPCM4 for 12–8–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "001 s xxxx"
```

where,

```
"001" is the code word
"s" is the sign bit
"xxxx" is the four bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x10
value = 8 * (Xenco( n ) & 0xf) + 104 + 3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095)
        Xdeco( n ) = 4095
    endif
endif
```

E.3.5.5 DPCM5 for 12–8–12 Decoder

Xenco(**n**) has the following format:

```
Xenco( n ) = "0001 s xxx"
```

where,

```
"0001" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = 16 * (Xenco( n ) & 0x7) + 232 + 7
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.5.6 PCM for 12–8–12 Decoder

Xenco(**n**) has the following format:

```
Xenco( n ) = "1 xxxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxxx" is the seven bit value field
```

The codec equation is described as follows:

```
value = 32 * (Xenco( n ) & 0x7f)
if (value > Xpred( n )) then
    Xdeco( n ) = value + 15
else
    Xdeco( n ) = value + 16
endif
```

E.3.6 Decoder for 12–7–12 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 32 * Xenco( n ) + 16
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0x78 == 0x00) then
    use DPCM1
else if (Xenco( n ) & 0x78 == 0x08) then
    use DPCM2
else if (Xenco( n ) & 0x78 == 0x10) then
    use DPCM3
else if (Xenco( n ) & 0x70 == 0x20) then
    use DPCM4
else if (Xenco( n ) & 0x70 == 0x30) then
    use DPCM5
else if (Xenco( n ) & 0x78 == 0x18) then
    use DPCM6
else
    use PCM
endif
```

E.3.6.1 DPCM1 for 12–7–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s xx"
```

where,

```
"0000" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = Xenco( n ) & 0x3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.6.2 DPCM2 for 12–7–12 Decoder

Xenco(**n**) has the following format:

```
Xenco( n ) = "0001 s xx"
```

where,

```
"0001" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 2 * (Xenco( n ) & 0x3) + 4
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.6.3 DPCM3 for 12–7–12 Decoder

Xenco(**n**) has the following format:

```
Xenco( n ) = "0010 s xx"
```

where,

```
"0010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 4 * (Xenco( n ) & 0x3) + 12 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.6.4 DPCM4 for 12–7–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xxx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = 8 * (Xenco( n ) & 0x7) + 28 + 3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.6.5 DPCM5 for 12–7–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xxx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xxx" is the three bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x8
value = 16 * (Xenco( n ) & 0x7) + 92 + 7
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.6.6 DPCM6 for 12–7–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s xx"
```

where,

```
"0011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 32 * (Xenco( n ) & 0x3) + 220 + 15
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.6.7 PCM for 12–7–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxxx" is the six bit value field
```

The codec equation is described as follows:

```
value = 64 * (Xenco( n ) & 0x3f)
if (value > Xpred( n )) then
    Xdeco( n ) = value + 31
else
    Xdeco( n ) = value + 32
endif
```

E.3.7 Decoder for 12–6–12 Data Compression

Pixels without prediction are decoded using the following formula:

```
Xdeco( n ) = 64 * Xenco( n ) + 32
```

Pixels with prediction are decoded using the following formula:

```
if (Xenco( n ) & 0x3c == 0x00) then
    use DPCM1
else if (Xenco( n ) & 0x3c == 0x04) then
    use DPCM3
else if (Xenco( n ) & 0x38 == 0x10) then
    use DPCM4
else if (Xenco( n ) & 0x3c == 0x08) then
    use DPCM5
else if (Xenco( n ) & 0x38 == 0x18) then
    use DPCM6
else if (Xenco( n ) & 0x3c == 0x0c) then
    use DPCM7
else
    use PCM
endif
```

*Note: **DPCM2** is not used.*

E.3.7.1 DPCM1 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0000 s x"
```

where,

```
"0000" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x2
value = Xenco( n ) & 0x1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
else
    Xdeco( n ) = Xpred( n ) + value
endif
```

E.3.7.2 DPCM3 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0001 s x"
```

where,

```
"0001" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x2
value = 4 * (Xenco( n ) & 0x1) + 2 + 1
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.7.3 DPCM4 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "010 s xx"
```

where,

```
"010" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 8 * (Xenco( n ) & 0x3) + 10 + 3
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.7.4 DPCM5 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0010 s x"
```

where,

```
"0010" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x2
value = 16 * (Xenco( n ) & 0x1) + 42 + 7
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.7.5 DPCM6 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "011 s xx"
```

where,

```
"011" is the code word
"s" is the sign bit
"xx" is the two bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x4
value = 32 * (Xenco( n ) & 0x3) + 74 + 15
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.7.6 DPCM7 for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "0011 s x"
```

where,

```
"0011" is the code word
"s" is the sign bit
"x" is the one bit value field
```

The codec equation is described as follows:

```
sign = Xenco( n ) & 0x2
value = 64 * (Xenco( n ) & 0x1) + 202 + 31
if (sign > 0) then
    Xdeco( n ) = Xpred( n ) - value
    if (Xdeco( n ) < 0) then
        Xdeco( n ) = 0
    endif
else
    Xdeco( n ) = Xpred( n ) + value
    if (Xdeco( n ) > 4095) then
        Xdeco( n ) = 4095
    endif
endif
```

E.3.7.7 PCM for 12–6–12 Decoder

Xenco(n) has the following format:

```
Xenco( n ) = "1 xxxxx"
```

where,

```
"1" is the code word
the sign bit is not used
"xxxxx" is the five bit value field
```

The codec equation is described as follows:

```
value = 128 * (Xenco( n ) & 0x1f)
if (value > Xpred( n )) then
    Xdeco( n ) = value + 63
else
    Xdeco( n ) = value + 64
endif
```

Annex F JPEG Interleaving (informative)

This annex illustrates how the standard features of the CSI-2 protocol should be used to interleave (multiplex) JPEG image data with other types of image data, e.g. RGB565 or YUV422, without requiring a custom JPEG format such as JPEG8.

The Virtual Channel Identifier and Data Type value in the CSI-2 Packet Header provide simple methods of interleaving multiple data streams or image data types at the packet level. Interleaving at the packet level minimizes the amount of buffering required in the system.

The Data Type value in the CSI-2 Packet Header should be used to multiplex different image data types at the CSI-2 transmitter and de-multiplex the data types at the CSI-2 receiver.

The Virtual Channel Identifier in the CSI-2 Packet Header should be used to multiplex different data streams (channels) at the CSI-2 transmitter and de-multiplex the streams at the CSI-2 receiver.

The main difference between the two interleaving methods is that images with different Data Type values within the same Virtual Channel use the same frame and line synchronization information, whereas multiple Virtual Channels (data streams) each have their own independent frame and line synchronization information and thus potentially each channel may have different frame rates.

Since the predefined Data Type values represent only YUV, RGB and RAW data types, one of the User Defined Data Type values should be used to represent JPEG image data.

Figure ~~191~~207 illustrates interleaving JPEG image data with YUV422 image data using Data Type values.

Figure ~~192~~208 illustrates interleaving JPEG image data with YUV422 image data using both Data Type values and Virtual Channel Identifiers.

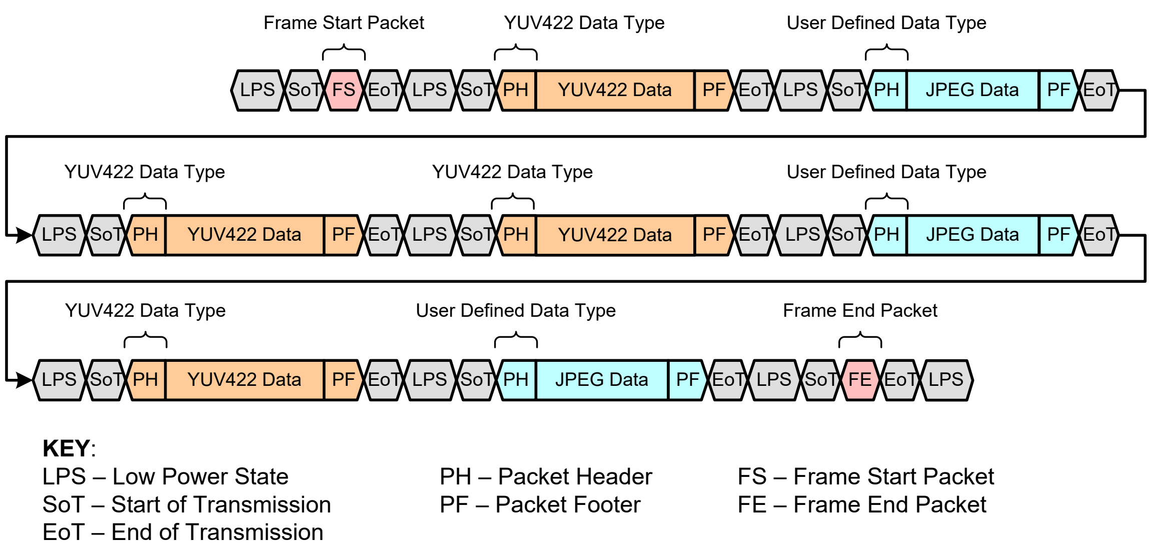


Figure 207 Data Type Interleaving: Concurrent JPEG and YUV Image Data

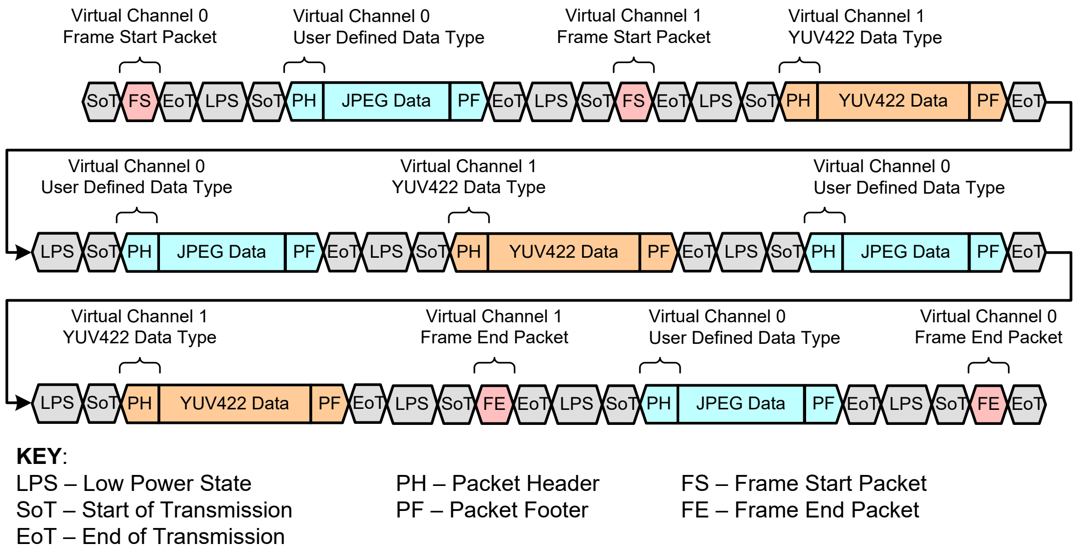


Figure 208 Virtual Channel Interleaving: Concurrent JPEG and YUV Image Data

Both ***Figure ~~191~~207*** and ***Figure ~~192~~208*** can be similarly extended to the interleaving of JPEG image data with any other type of image data, e.g. RGB565.

Figure ~~193~~209 illustrates the use of Virtual Channels to support three different JPEG interleaving usage cases:

- Concurrent JPEG and YUV422 image data.
- Alternating JPEG and YUV422 output - one frame JPEG, then one frame YUV
- Streaming YUV22 with occasional JPEG for still capture

Again, these examples could also represent interleaving JPEG data with any other image data type.

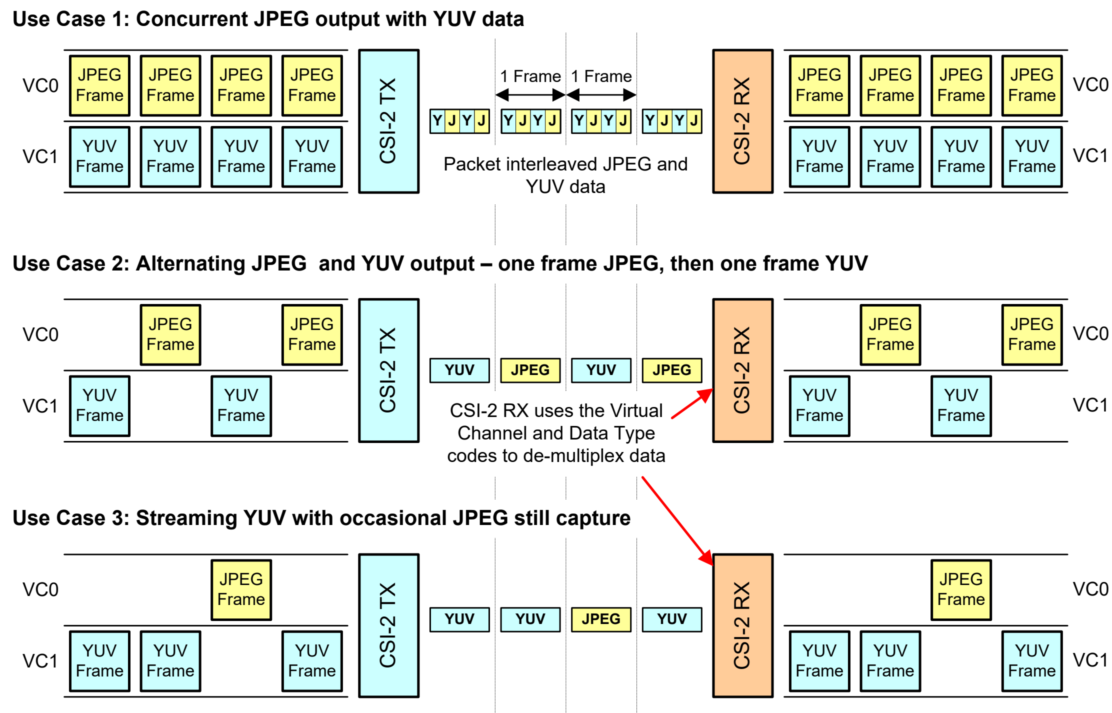


Figure 209 Example JPEG and YUV Interleaving Use Cases

~~This page intentionally left blank~~

Annex G Scrambler Seeds for Lanes 9 and Above

(See also: ***Section 9.12***).

For Links of 9 to 32 Lanes, the Scrambler PRBS registers of Lanes 9 through 32 should be initialized with the initial seed values as listed in ***Table ~~48~~63***.

For Links of more than 32 Lanes, the Scrambler PRBS registers of Lanes 33 and higher shall use the same initial seed value that is used for the Lane number modulo 32. (See ***Section 9.12*** and ***Table ~~48~~63***.)

Examples:

- Lane 33 shall use the same initial seed value as Lane 1
- Lane 34 shall use the same initial seed value as Lane 2
- Lane 64 shall use the same initial seed value as Lane 32
- Lane 65 shall use the same initial seed value as Lane 1

Table 63 Initial Seed Values for Lanes 9 through 32

Lane	Initial Seed Value
9	0x1818
10	0x1998
11	0x1a59
12	0x1bd8
13	0x1c38
14	0x1db8
15	0x1e78
16	0x1ff8
17	0x0001
18	0x0180
19	0x0240
20	0x03c0
21	0x0420
22	0x05a0
23	0x0660
24	0x07e0
25	0x0810
26	0x0990
27	0x0a51
28	0x0bd0
29	0x0c30
30	0x0db0
31	0x0e70
32	0x0ff0

Note that the binary representation of each initial seed value is symmetrical with respect to the forwards and backwards directions, with the exceptions of Lanes 11, 17, and 27. The initial seed values can be created easily using a Lane index value (i.e., Lane number minus one).

This page intentionally left blank.

Annex H Guidance on CSI-2 Over C-PHY ALP and PPI

H.1 CSI-2 with C-PHY ALP Mode

C-PHY Alternate Low Power (ALP) Mode is an alternative to the legacy LP mode of C-PHY. ALP Mode uses solely High-Speed signaling with a special state where the signals can cease toggling and collapse to zero. The legacy LP Mode signaling and escape sequences have equivalent ALP Mode functions so that the high-voltage low power signaling can be replaced by ALP Mode signaling if that is beneficial in specific systems. ALP Mode replaces the legacy LP Mode line levels by the transmission of unique code words that are used only for Lane signaling events. These unique codes are never produced by the 3-Phase mapping function, so there is never ambiguity in the interpretation of these codes at the receiver.

Reasons to replace the legacy LP mode with equivalent ALP Mode functions are to begin a transitionary path to the future so that legacy LP mode might someday be eliminated in some devices. Another reason to choose ALP Mode over Legacy LP mode is to support systems that have long interconnect between the Master and Slave devices.

H.1.1 Concepts of ALP Mode and Legacy LP Mode

In ALP mode, the conventional LP receivers are not used to detect signaling states. Instead, all communication is performed using High-Speed signaling levels. The system level functions performed by ALP signaling are quite similar to the functional behavior of legacy LP mode. The intent of this is to cause the least amount of disruption to systems that support both ALP Mode and legacy LP mode. ***Figure*** ***~~194~~210*** shows a comparison of a High-Speed data burst with LP Mode versus ALP Mode. The purpose of this diagram is to show that each of the intervals in the High-Speed data burst with LP mode correspond to similar intervals in the High-Speed data burst with ALP mode.

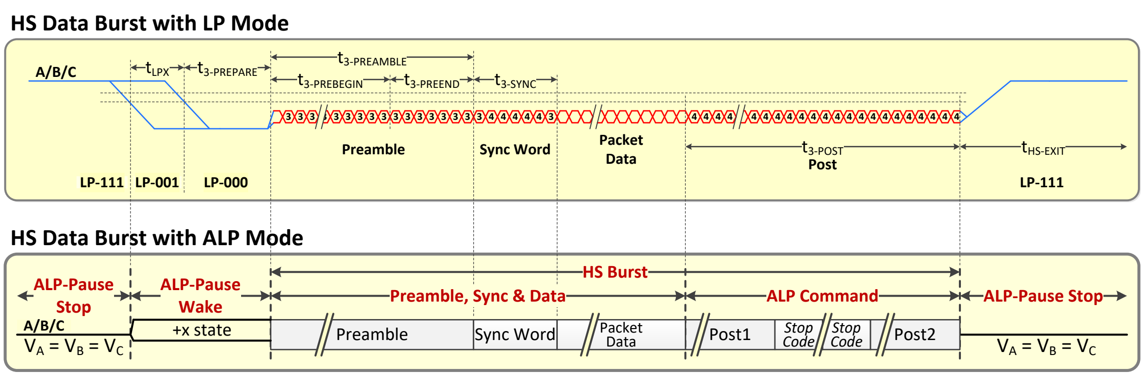


Figure 210 Comparing Data Burst Timing of Legacy LP mode versus ALP Mode

ALP Mode supports the transmission of High-Speed data bursts as well as the transmission of control sequences that are traditionally transmitted using legacy LP mode Escape Mode sequences. The format of all ALP mode bursts is like the timing diagram in ***Figure*** ***~~195~~211***.

The burst begins and ends in an ALP-Pause state. There are two types of ALP-Pause: ALP-Pause Stop and ALP-Pause ULPS. ALP-Pause Stop is analogous to the legacy LP mode Stop state; ALP-Pause ULPS is analogous to the legacy LP mode ULPS state. The only difference between these two types of ALP-Pause states is the time allowed to wake up from each, which is the duration of the ALP-Pause Wake interval. The nominal time allowed to ~~wave~~wake from ALP-Pause Stop is 100 ns, which is about the same time as the duration of the LP-001 and LP-000 states at the beginning of a HS Data Burst using legacy LP mode. The nominal time to wake from the ALP-Pause ULPS state is 1 msec, which is approximately the time allowed in legacy LP mode for t_{WAKEUP}. (The time that a transmitter drives a Mark-1 state prior to a Stop state to initiate an exit from ULPS.) The longer wake-up time from ALP-Pause ULPS compared to ALP-Pause Stop allows a lower power consumption while in the ALP-Pause ULPS state.

The ALP-Pause Stop and ALP-Pause ULPS line states are defined by the following relationships of the Line levels: $V_A = V_B = V_C$, and $V_{OD\_AB} = V_{OD\_BC} = V_{OD\_CA} = 0$. Examples of the ALP-Pause and the ALP-Pause Wake states are illustrated at the beginning and end of the waveform in ***Figure ~~195~~211***. The ALP-Pause Wake state, which is very long compared to a High-Speed Unit Interval, is detected by the low-power wake-up receiver. This causes the system to leave one of the ALP-Pause states and to begin receiving a High-Speed signal.

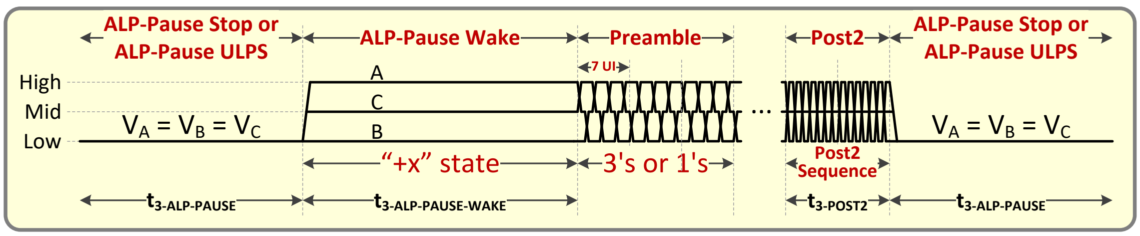


Figure 211 ALP Mode General Burst Format

To minimize power consumption while Lane activity has ceased during one of the ALP-Pause states, a special low-speed and low-power differential receiver circuit is present, in addition to the three High-Speed differential receivers for A-B, B-C and C-A. This special low-speed and low-power differential receiver has a nominal +80 mV offset input threshold voltage that detects the difference in differential levels between the ALP-Pause state ($V_{OD} = 0$) and ALP-Pause Wake state ($V_{OD} = |V_{OD}|$ Strong). This allows the line signals to collapse to zero with the 100Ω Z_{ID} termination still connected, and still have a well-defined method to detect the difference between the ALP-Pause and ALP-Pause Wake line conditions. Collapsing to zero with the terminations still connected makes it possible for implementations to have very low power consumption during the ALP-Pause states. The ALP-Pause Wake pulse is very long compared to a High-Speed Unit Interval so that the wake receiver can be slow and consume very little power compared to the High-Speed differential receivers.

An example of the differential receiver circuit to support ALP mode is shown in ***Figure ~~196~~212***. Two different offset receivers are shown for wake from stop versus wake from ULPS, because the power consumption in the ALP-Pause ULPS state is expected to be lower than in ALP-Pause Stop state. The ALP-Pause Wake pulse from the ULPS state can be longer than waking from ALP-Pause Stop, so the ALP ULPS receiver can be slower and consume less power compared to the ALP Stop receiver.

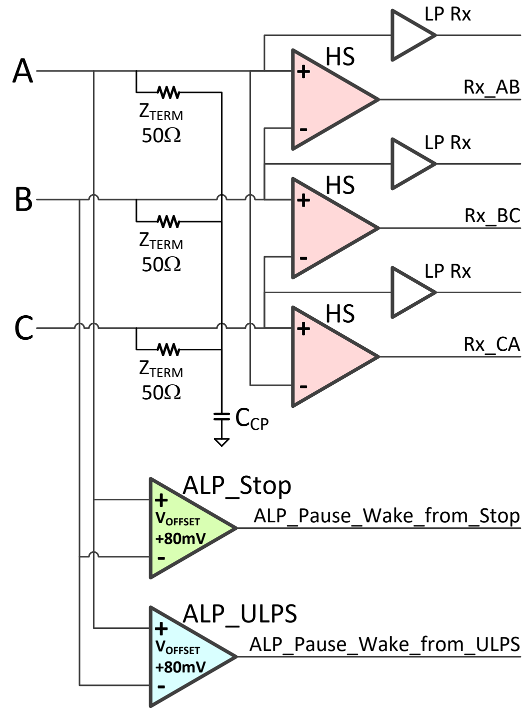


Figure 212 High-Speed and ALP-Pause Wake Receiver Example

The C-PHY specification defines ~~twelve~~thirteen unique 7-symbol ALP Code Words that are the functional equivalent of the LP pulse sequences of legacy LP mode. In some cases, a single 7-symbol ALP Code Word can replace the transmission of a long sequence of legacy LP mode pulses, such as for the transmission of Escape Mode triggers or low-power data transmission. The CSI-2 specification needs only three of these LP mode pulse sequences to emulate the functionality of legacy LP mode: Stop Code, ULPS Code, and Post. A fourth code, the TAC Code, is used for Fast Bus Turnaround.

Exit from and entry into the ALP-Pause state, which is the functional equivalent of the legacy LP mode Stop state, requires a special ALP Mode sequence consisting of one or more Stop Codes or ULPS codes followed by a string of Post codes followed by setting the voltage of all three Lines of a Lane to the same value.

As illustrated in ***Figure ~~194~~210***, the burst starting sequence of the legacy LP mode consisting of: LP-111, LP-001, and LP-000 followed by preamble, has a functional equivalent sequence in ALP Mode consisting of: ALP-Pause Stop followed by ALP Pause Wake followed by preamble. Similarly, the burst ending sequence of legacy LP mode consisting of Post sequence followed by LP-111, has a functional equivalent sequence in ALP Mode consisting of: the Post1 field by two or more Stop Codes followed by the Post2 field followed by ALP-Pause Stop.

H.1.2 Burst Examples Using ALP Mode

Figure ~~197~~213 shows examples of the three types of High-Speed bursts that can be sent in ALP mode. Many combinations of ALP code sequences are possible, but ***Figure ~~197~~213*** shows three sequences that adequately perform the functions necessary to support CSI-2 that are currently performed using legacy LP mode. The ALP state machine from the C-PHY Specification has been highlighted in ***Figure ~~198~~214***, ***Figure ~~199~~215***, and ***Figure ~~200~~216*** to show how transmission of these three sequences should occur.

For interop sake, only these three types of sequences are required to support CSI-2. Note that all bursts begin in the same manner with the assertion of ALP-Pause Wake followed by a Preamble. The words that follow the Preamble determine the type of burst that is being transmitted. All bursts end in the same manner with multiple Stop Codes followed by the Post2 field, or multiple ULPS Codes followed by the Post2 field. The Post 1 and Post2 fields are the same as Post (4444444), described in the C-PHY specification for burst transmission using legacy LP mode. The only difference is that the Post1 and Post2 fields are transmitted as a result of signaling over the PPI from the CSI-2 Tx to the C-PHY Tx.

The last ALP code sent in the burst determines whether the system enters the ALP-Pause Stop or the ALP-Pause ULPS state.

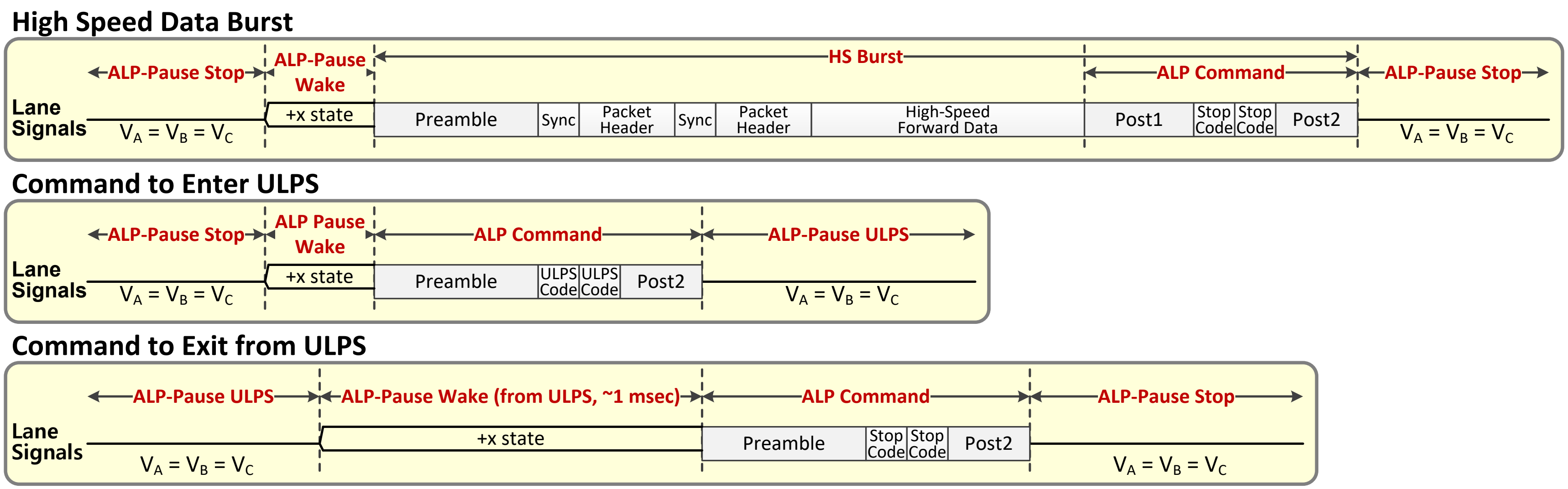


Figure 213 Examples of Bursts to Send High-Speed Data and ALP Commands

Figure ~~***198***~~***214*** shows the ALP state machine transitions (highlighted in red) necessary to transmit a High-Speed data burst in ALP mode. States and state transitions that are not used by CSI-2 for any type of burst are shown using dashed lines. The red highlighted states and transitions indicate the path required to transmit and receive the High-Speed Data Burst example in ***Figure*** ~~***197***~~***213***.

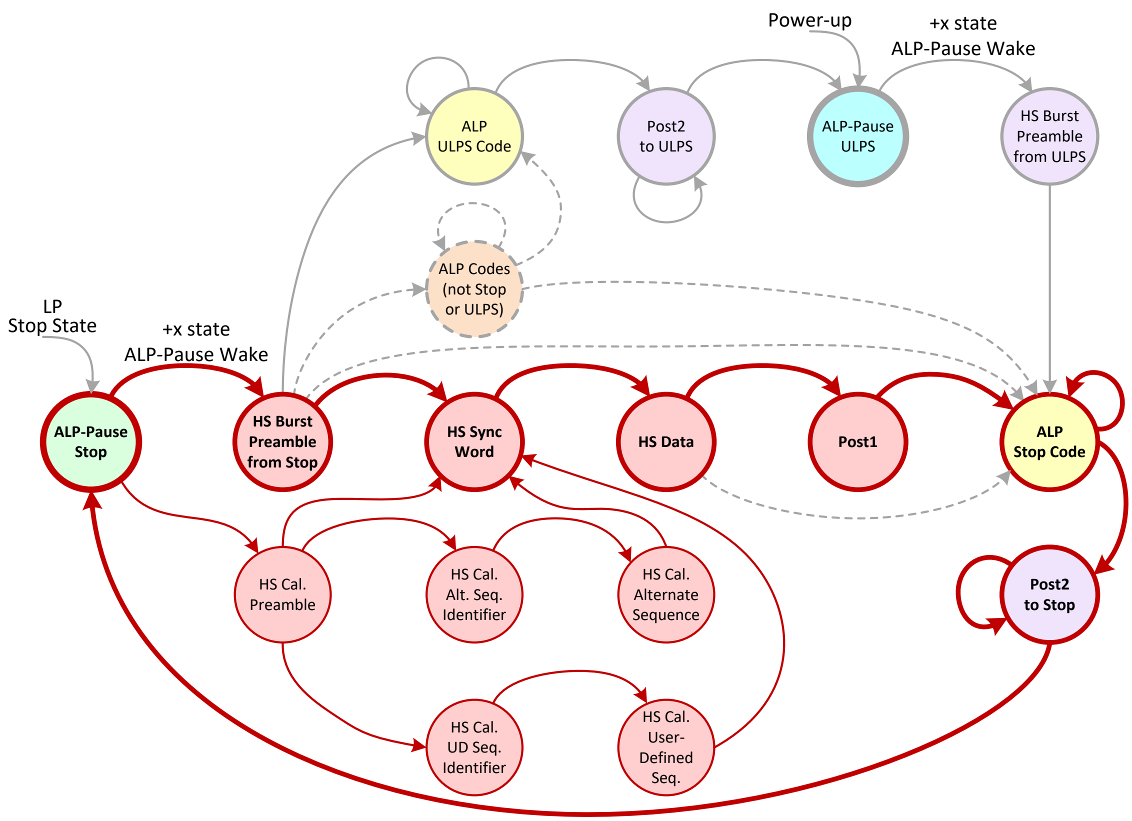
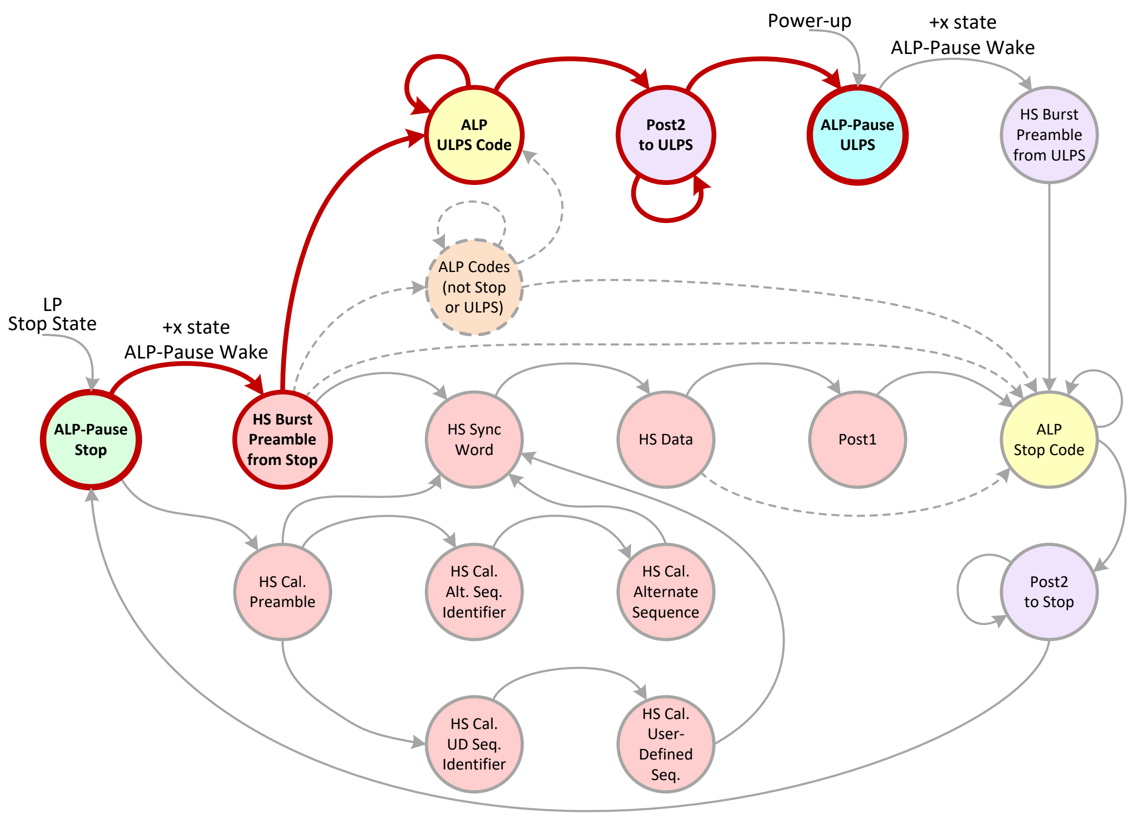


Figure 214 State Transitions for an HS Data Burst

4618 *Figure ~~199~~215* shows the ALP state machine transitions (highlighted in red) necessary to enter the ALP-
4619 Pause ULPS state.



4620

Figure 215 State Transitions to Enter the ULPS State

Figure ~~*200*~~*216* shows the ALP state machine transitions (highlighted in red) necessary to enter the ALP-Pause Stop state.

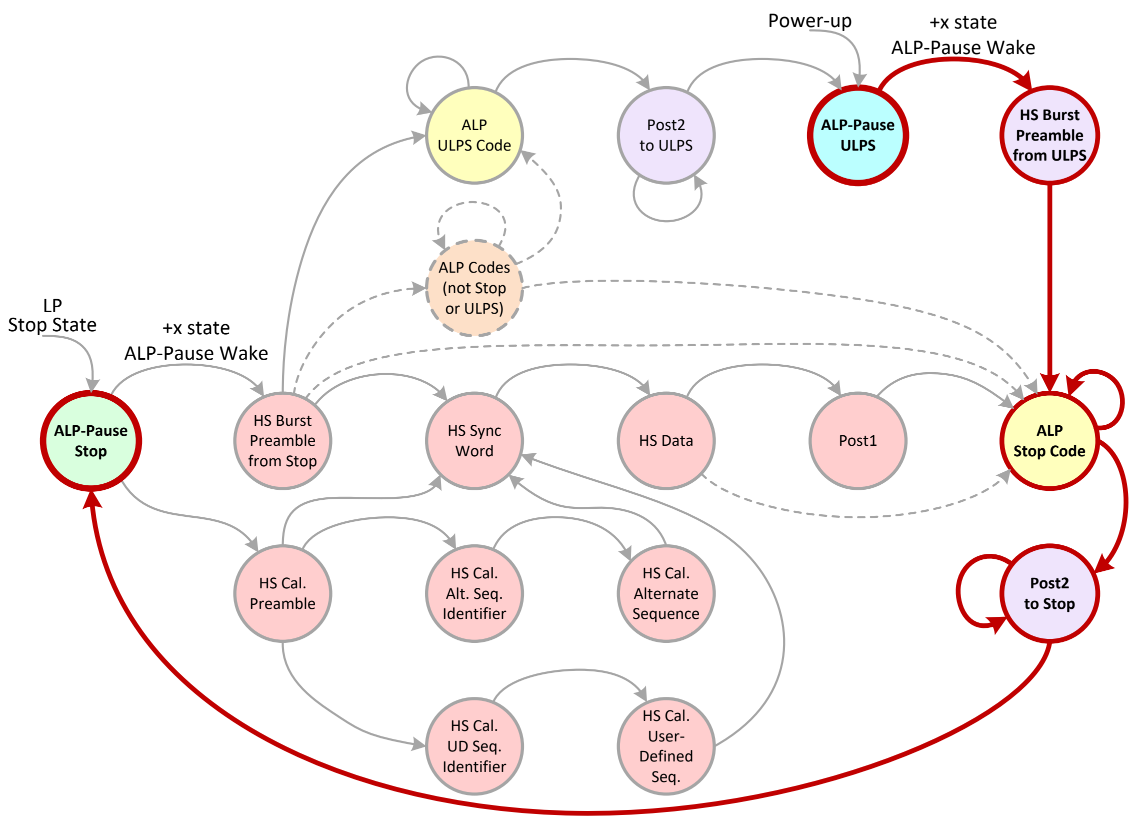


Figure 216 State Transitions to Exit from the ULPS State

Table ~~*49*~~*64* describes the 7-symbol codes transmitted in ALP mode. The corresponding LP mode or Escape mode function is described, where applicable.

Table 64 ALP Code Definitions used by CSI-2

ALP Code	Symbol Sequence	PPI ALP Code	Corresponding LP State or Escape Mode Sequence
Stop Code	0244440	0b0000	LP-111 (End of Transmission, or EoT)
ULPS Code	0244441	0b0001	Escape Mode Entry + Ultra-Low Power State (ULPS)
Post1	4444444	0b1011	No equivalent legacy LP mode sequence exists. The CSI-2 TX can cause the Post sequence to be transmitted by sending this code.
Post2			
Turnaround Code (TAC)	2144441	0b1100	No equivalent legacy LP mode sequence exists, although TAC triggers a Fast Lane Turnaround that is functionally similar to Control Mode Turnaround.

H.1.3 Transmission and Reception of ALP Commands Through the PPI

In ALP mode there are three types of code words transmitted by the PHY:

- **Data:** Data words received from the CSI-2 Tx are mapped through the C-PHY mapper, encoded, and transmitted over the Lane.
- **Sync Words:** The CSI-2 Tx can cause the C-PHY Tx to transmit a Sync Word in place of a data word created by the C-PHY mapper. Sync Words can have one of five different values which are defined as Sync Types.
- **ALP Codes**: The CSI-2 Tx can cause the C-PHY Tx to transmit a specific ALP code which is one of the 7-symbol sequences defined in ***Table ~~49~~64***.

These three different types of code words comprise a high speed burst while in ALP mode. ***Figure ~~201~~217*** highlights the control signals that facilitate the transmission of each of these three different types of code words.

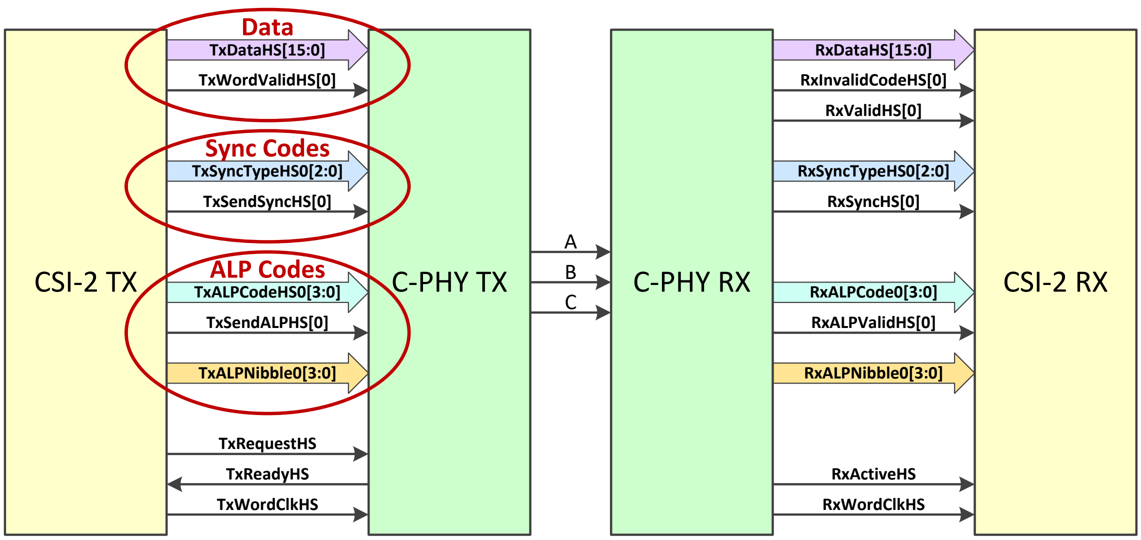


Figure 217 PPI Example: HS Signals for Transmission of Data, Sync and ALP Commands

Figure ~~202~~218 and ***Figure ~~203~~219*** show examples of PPI signals and the corresponding PHY data for transmission and reception of high speed data in ALP mode. These figures show additional detail of the High-Speed Data Burst waveform in ***Figure ~~197~~213***.

The signal TxRequestHS is asserted simultaneously with TxWordValidHS to request that a high speed burst be transmitted. The PHY will know to send a data burst because TxWordValidHS is asserted early in the burst timing. This will cause the C-PHY Tx to transmit the first Sync Word at the end of the Preamble. Note that the first Sync Word is transmitted autonomously by the C-PHY Tx, and has the default Sync Type value of 3. Subsequent Sync Words transmitted in a burst are sent as a result of asserting the TxSendSyncHS[0] signal, and the associated Sync Type is defined by the TxSyncTypeHS0[2:0] signals.

The end of burst in the Transmitter functions differently for ALP mode compared to the non-ALP high-speed mode. In the non-ALP high-speed mode, the end of burst is signaled to the PHY by pulling TxRequestHS low, as described in Annex A of the C-PHY specification. After TxRequestHS goes low, the C-PHY Tx will generate the Post sequence of length determined by a PHY configuration parameter that sets the length of Post.

In ALP mode, the protocol transmit unit generates all fields of the burst after the first sync word, including the packet headers, data burst, Stop Code, ULPS Code, Post1, and Post2. The burst is ended by pulling TxRequestHS low, and no additional data is transmitted on the Lane after this time.

4656

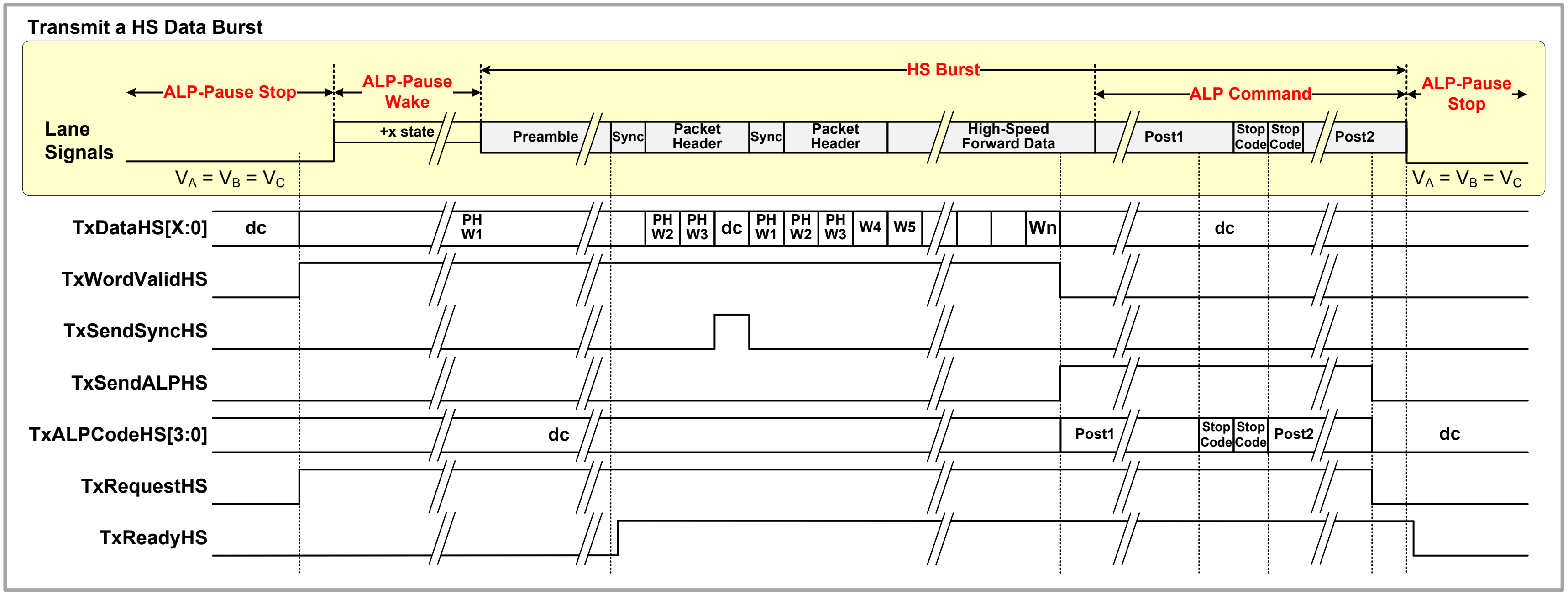
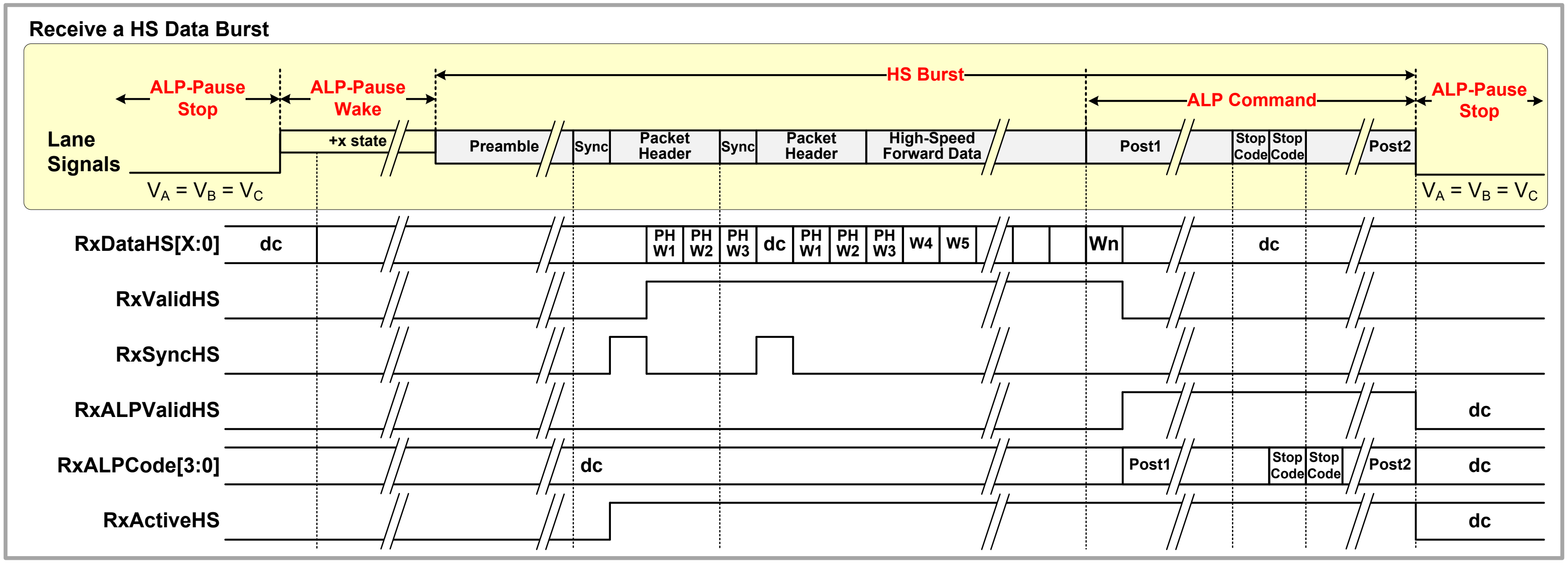


Figure 218 PPI Example Transmit Side Timing for an HS Data Burst



4657

Figure 219 PPI Example Receive Side Timing for an HS Data Burst

Figure ~~204~~220, ***Figure ~~205~~221***, ***Figure ~~206~~222***, and ***Figure ~~207~~223*** show examples of PPI signals and the corresponding PHY data for transmission and reception ALP Commands to enter into and exit from the ALP-Pause ULPS state in ALP mode. These figures show additional detail of the Command to Enter ULPS and the Command to Exit from ULPS waveforms in ***Figure ~~197~~213***.

The signal TxRequestHS is asserted simultaneously with TxSendALPHS to request that a high speed burst be transmitted. The PHY will know to send a ALP commands in the burst rather than the Sync Word because TxSendALPHS is asserted early in the burst timing, and TxWordValidHS is not asserted.

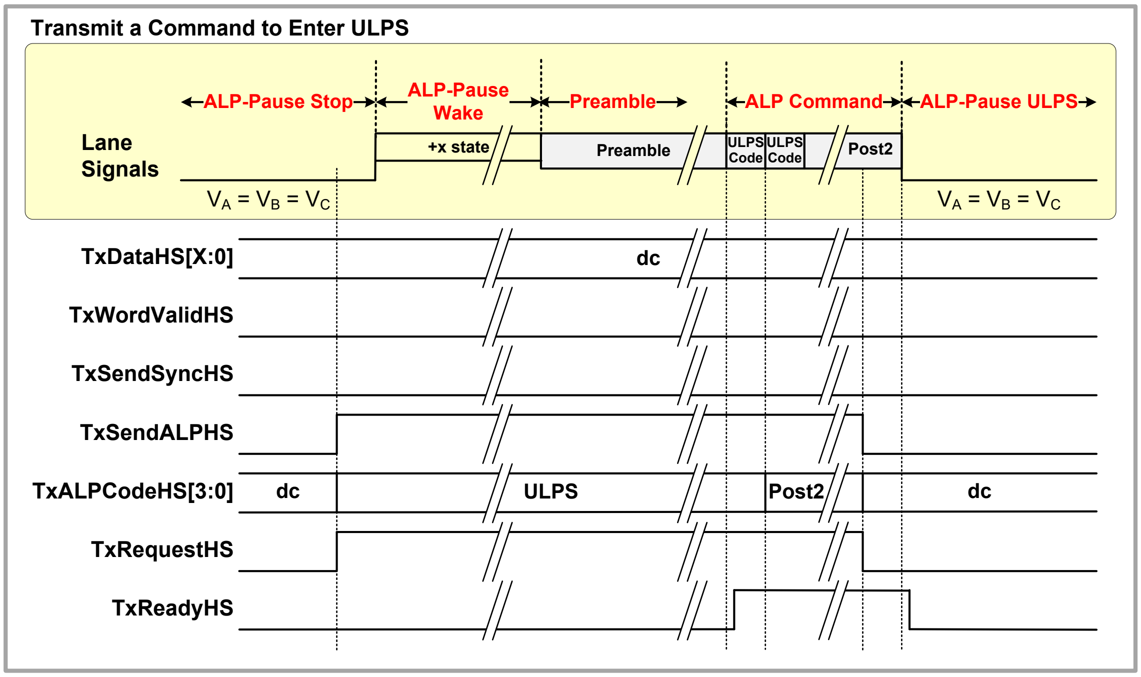


Figure 220 PPI Example Transmit Side Timing to Enter the ULPS State

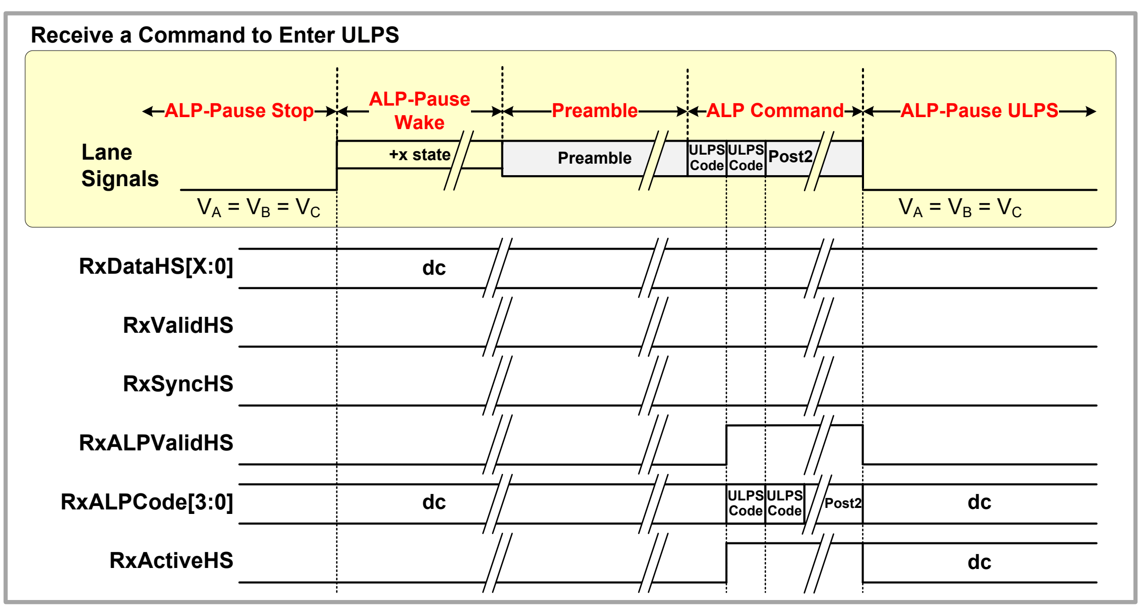


Figure 221 PPI Example Receive Side Timing to Enter the ULPS State

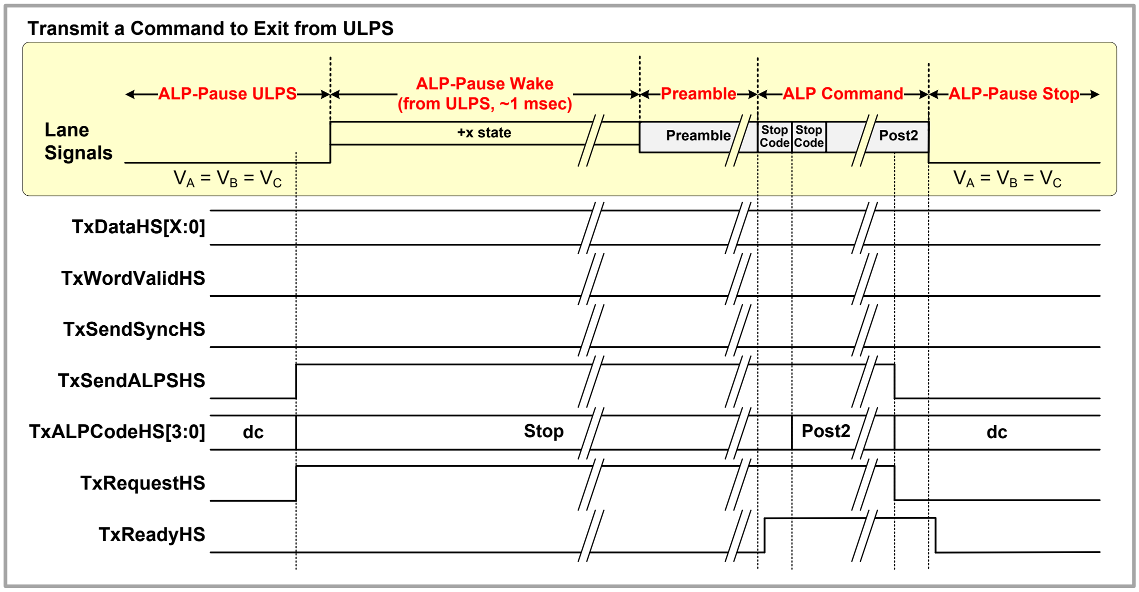
4667 

Figure 222 PPI Example Transmit Side Timing to Exit from the ULPS State

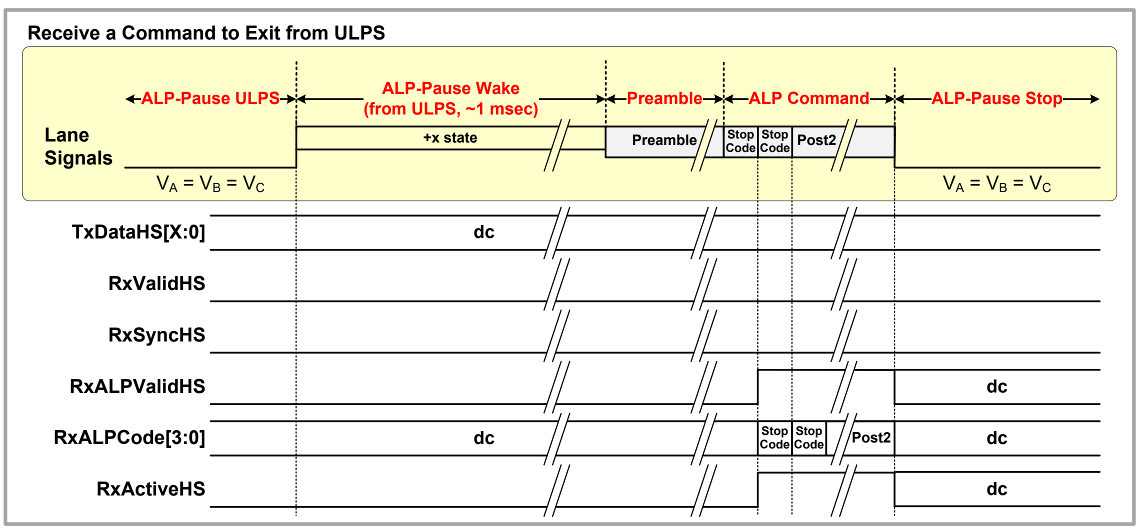
4668 

Figure 223 PPI Example Receive Side Timing to Exit from the ULPS State

H.1.4 Multi-Lane Operation Using ALP Mode

Figure ~~***208***~~***224*** and ***Figure*** ~~***209***~~***225*** show examples of three Lanes operating together in a Link in ALP mode. The High-Speed data burst in ***Figure*** ~~***208***~~***224*** begins with identical packet headers (consisting of PH W0, PH W1, and PH W2) transmitted twice on each of the three Lanes. The Packet Headers are followed by packet data (consisting of DW 0 through DW n-1) striped across the three Lanes by the CSI-2 Lane Distribution Function. The burst starts and ends in the manner described in Section H.1.2 above. The example of ***Figure*** ~~***209***~~***225*** showing the command to enter ULPS has identical data on each of the three Lanes.

The example also shows that the assertion of the +x state for ALP-Pause Wake can be staggered in time on each of the lanes. This is shown to highlight a particular implementation where the system designer might prefer to enable the high speed drivers for each of the Lanes at a slightly different time.

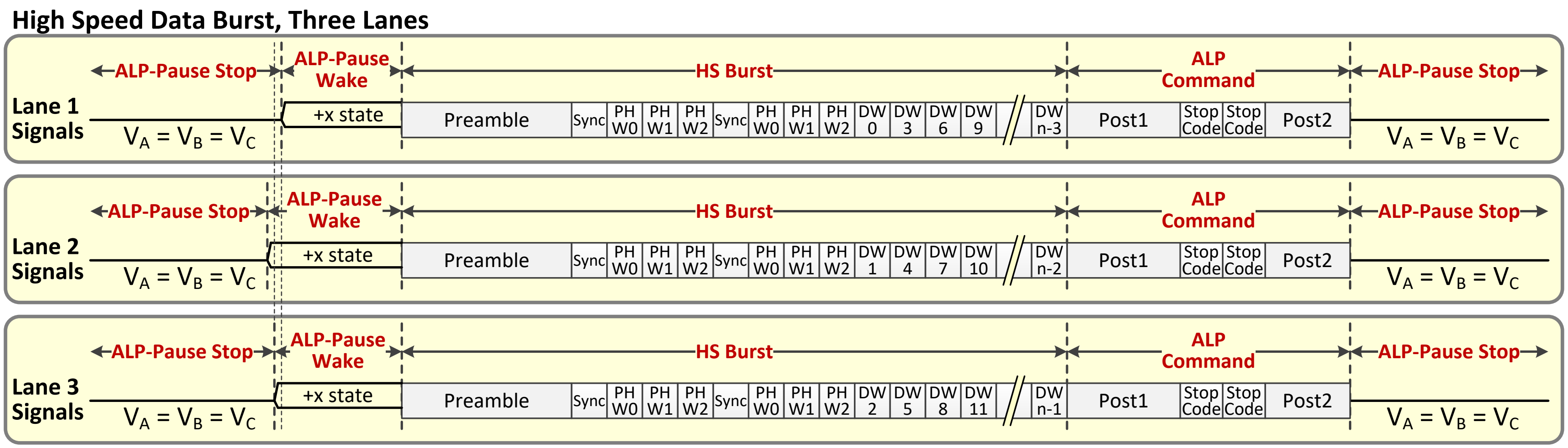


Figure 224 Example Showing a Data Transmission Burst using Three Lanes

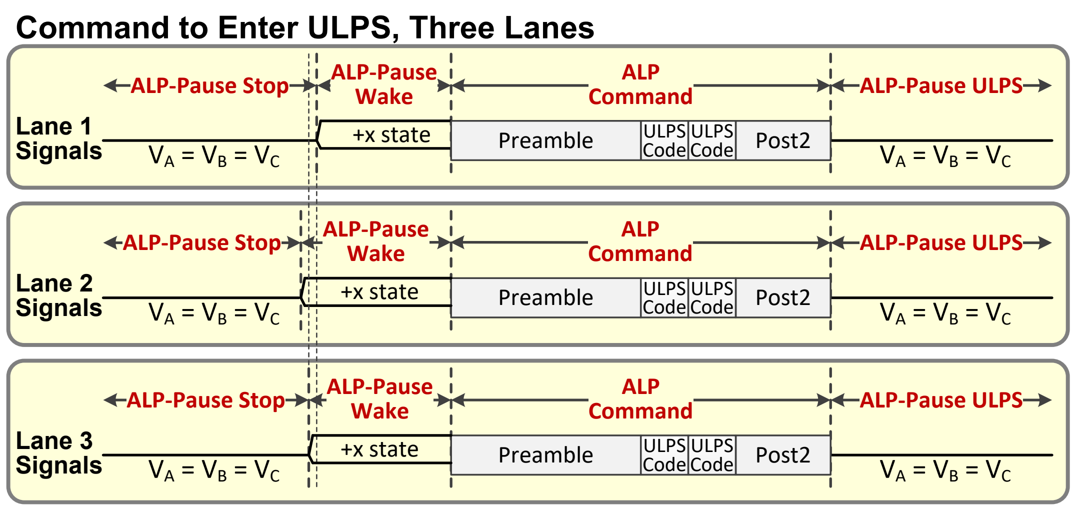


Figure 225 Example Showing an ALP Command Burst using Three Lanes

H.1.5 ~~Concurrent~~ LP and ALP Operation

Section 6.4.5.8 of ~~*[MIPI02]*~~*[MIPI02]* describes ~~the concurrent~~ support of LP and ALP operation. The ~~system is configured for LP operation at power-up. During initialization, the system~~ transmitter and receiver can be configured for LP-only operation, or ALP-only operation ~~or concurrent LP-ALP operation. It is anticipated that most systems will~~ using the PPI signals TxALP-LPSelect and RxALP-LPSelect, respectively. Devices can use a ~~mode bit or configuration option that causes the system~~variety of means such as a register, an I/O pin, or a non-volatile storage element to ~~operate in either LP-only or ALP-only operation. However, it is also possible to implement the capability for concurrent operation. A burst can begin as LP and end as ALP, or vice-versa.~~ determine the initial state of these two PPI signals

H.1.6 Bi-Directional Lane Turnaround

The ~~method of ending the burst, whether via the~~ transmission ~~of ALP codes or transmission of LP-111, determines whether~~direction of a Bi-Directional Lane can be swapped by performing a Lane Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward Direction to Reverse Direction, or a change from Reverse Direction to Forward Direction. Notice that the roles of Master and Slave are not changed as a result of performing the ~~system is~~ Turnaround procedure.

The Turnaround procedure can be performed in ~~ALP operation or LP operation.~~two ways: one is via a Control Mode Lane Turnaround that uses LP Mode signaling, and the other is via a Fast Lane Turnaround.

Control Mode Lane Turnaround occurs by going to the Exit state (Control Mode) where LP Mode signaling is used to perform the Control Mode Turnaround procedure, as shown in ***Figure 226***.

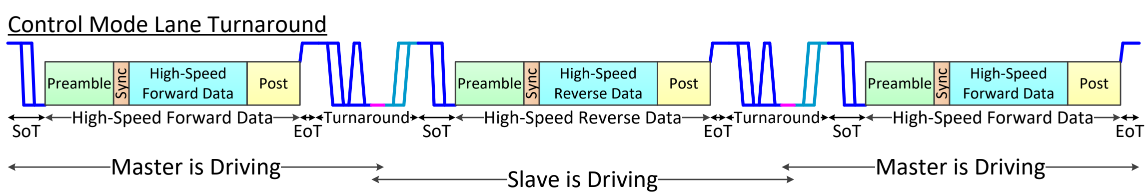


Figure 226 High-Level View of the Control Mode Lane Turnaround Procedure

A somewhat less likely configuration is to combine ALP mode and Control Mode Lane Turnaround if optional Dynamic LP and ALP operation is supported by the C-PHY, and if the electrical specifications can be met with the transmission channel being used in the system. An example is shown in ***Figure 227***.

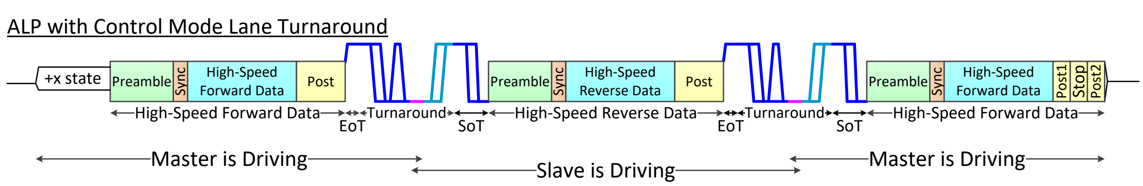


Figure 227 High-Level View of ALP Mode with the Control Mode Lane Turnaround Procedure

Fast Lane Turnaround is the most likely method to be used with the CSI-2 USL feature. Fast Lane Turnaround is performed without having to return to LP mode. This reduces the latency to change the transmission direction of a Bi-directional lane. Fast Lane Turnaround is handled completely in High-Speed mode. One or more Turnaround Codes (TAC) is transmitted near the end of the burst (between Post1 and Post 2) to inform the receiver that the Lane is about to change the transmission direction. A small Turnaround Gap (TGAP) exists between Post2 from the First Transmitting Device and the Preamble from the Second Transmitting Device to allow the Master and Slave to swap roles as transmitter and receiver. ***Figure 228*** shows a high-level view of the Fast Lane Turnaround Procedure with ALP Mode. It is anticipated that the Fast Lane Turnaround will most often be used with ALP Mode, and infrequently with Control Mode.

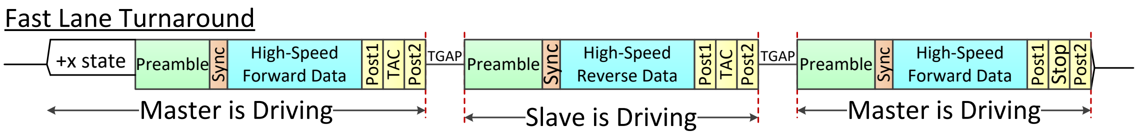


Figure 228 High-Level View of the Fast Lane Turnaround Procedure with ALP Mode

Figure 229 is a comparison of events that occur in the Fast Lane Turnaround Procedure versus the Control Mode Lane Turnaround Procedure. Fields that are the same color are either the same field in the two waveforms, or have comparable durations. Post1 + TAC + Post2 in the Fast Lane Turnaround is like Post in the Control Mode Lane Turnaround. The Preambles are the same duration and Syncs are the same duration. Fields that cause the durations of the two Turnaround methods to be different are highlighted with "Time difference between Fast Lane Turnaround and Control Mode Lane Turnaround" in the figure. In this case, the TGAP (nominally 14 UI) in the Fast Lane Turnaround waveform is usually much shorter in duration compared to the LP signaling (EoT + Turnaround + SoT, in the Control Mode Lane Turnaround waveform).

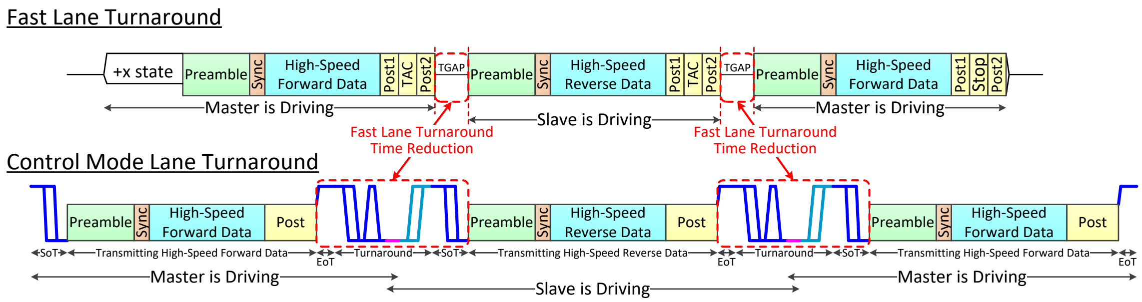


Figure 229 High-Level View, Comparing Lane Turnaround Procedures

The Fast Lane Turnaround Procedure is triggered by the transmission of a sequence of ALP codes at the end of a burst.

Figure 230 shows the detailed sequence of events that occur during the Fast Lane Turnaround Procedure. The transmitting C-PHY ends the data burst by sending Post1, followed by the TAC symbol sequence, followed by Post2. TAC is the symbol sequence "2144441", which is an unmapped sequence of seven symbols. The least significant symbol of TAC ("1") is transmitted first and the most significant symbol ("2") is transmitted last, which is the same convention used for transmitting any ALP code word. TAC may be transmitted multiple times for improved system reliability, to increase the probability that TAC will be detected by the receiver. The Post1 + TAC + Post2 is somewhat similar to the end of a burst in ALP mode, except that the TAC Code is sent instead of the Stop Code. The protocol receiver can easily identify the end of Packet Data when it detects Post1. The duration of the TAC and Post2 are programmable in the transmitter, and this duration is determined by the protocol layer. The protocol layer enables the transmission of Post1, TAC, and Post2 via the PPI signals TxSendALPHS[1:0], TxALPCodeHS0[3:0], and TxALPCodeHS1[3:0].

The purpose of Post1 is to indicate the end of the burst and provide a sufficient number of word clock intervals so the protocol layer can gracefully stop transmitting and receiving packet data that is sent prior to Post1. Post2 exists so the C-PHY transmitter and receiver has a sufficient number of clock intervals following TAC to be able to shut down transmitter and receiver circuitry and change the direction of transmission.

A Turnaround Gap (TGAP) exists to allow one transmitter to be disabled before the other is enabled. This avoids contention between the two drivers. The First Transmitting Device that sent the TAC disables its output by placing the driver into a high-impedance state just after the last symbol of Post2. The C-PHY ensures that the transmitter in the First Transmitting Device is completely disabled at the end of TGAP. The Second Transmitting Device begins to enable its output after TGAP at the beginning of the Preamble.

When the Second Transmitting Device receives TAC, it starts a timer that is used to determine when the end of TGAP, and the beginning of Preamble, should occur. It is necessary for the Second Transmitting Device to identify this interval using a timer, because there are no transmissions during TGAP to identify when the Second Transmitting Device needs to begin transmitting the Preamble. The number of words of TAC and duration of Post2 can be stored in registers in both the First Transmitting Device and Second Transmitting Device, so the C-PHY can determine the proper $t_{3\text{-TAC\_TO\_TX}}$ time. This is so the Second Transmitting Device starts transmitting Preamble at the proper time at the end of TGAP. The number of words of TAC and duration of Post2 can be different when transmission changes from Master to Slave, versus from Slave to Master. Therefore, it is necessary for the Master and Slave to have registers related to the TAC duration and Post2 duration for both types of turnaround (Master-to-Slave and Slave-to-Master).

An interval $t_{3\text{-TA-SETTLE}}$ exists to allow the driver transmitting the Preamble to have sufficient time to stabilize before it is used by the receiver for symbol clock recovery. The $t_{3\text{-TA-SETTLE}}$ interval is a time during which the HS receiver in the C-PHY will ignore any HS transitions on the Lane. This concept is ~~illustrated in by the~~ very similar to the $t_{3\text{-SETTLE}}$ time at the beginning of a HS burst from LP mode.

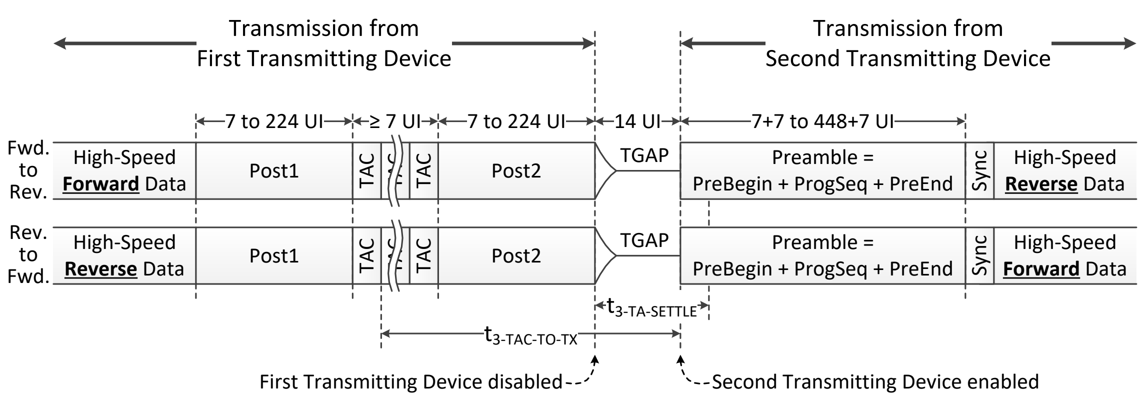
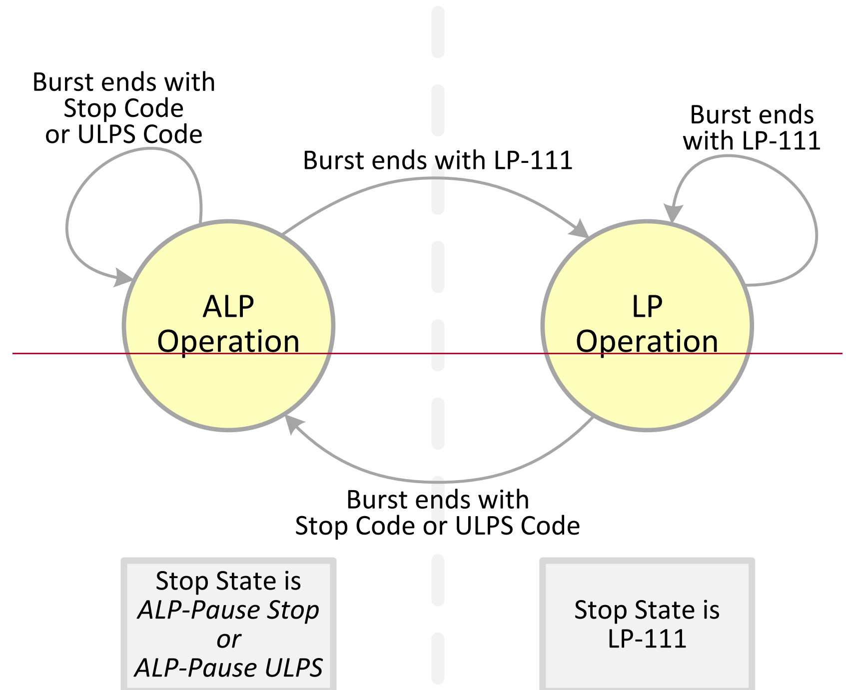


Figure 230 Detailed View of the Fast Lane Turnaround Procedure

Figure 231 shows an example of ALP state machine ~~in *Figure 210*.~~transitions (highlighted in red) that occur when a burst begins in the conventional manner with an ALP-Pause Wake pulse and finishes by performing a Fast Lane Turnaround Procedure. This is the sequence of events that occur during the first “Master is Driving” interval shown in ***Figure 228***. The highlighted sequence begins from the ALP-Pause Stop state, and ends when the turnaround event occurs during the HS-BTA Rx Wait state. This state diagram presents a high-level view of events. It can be interpreted to illustrate states that occur in the transmitter as well as the receiver.



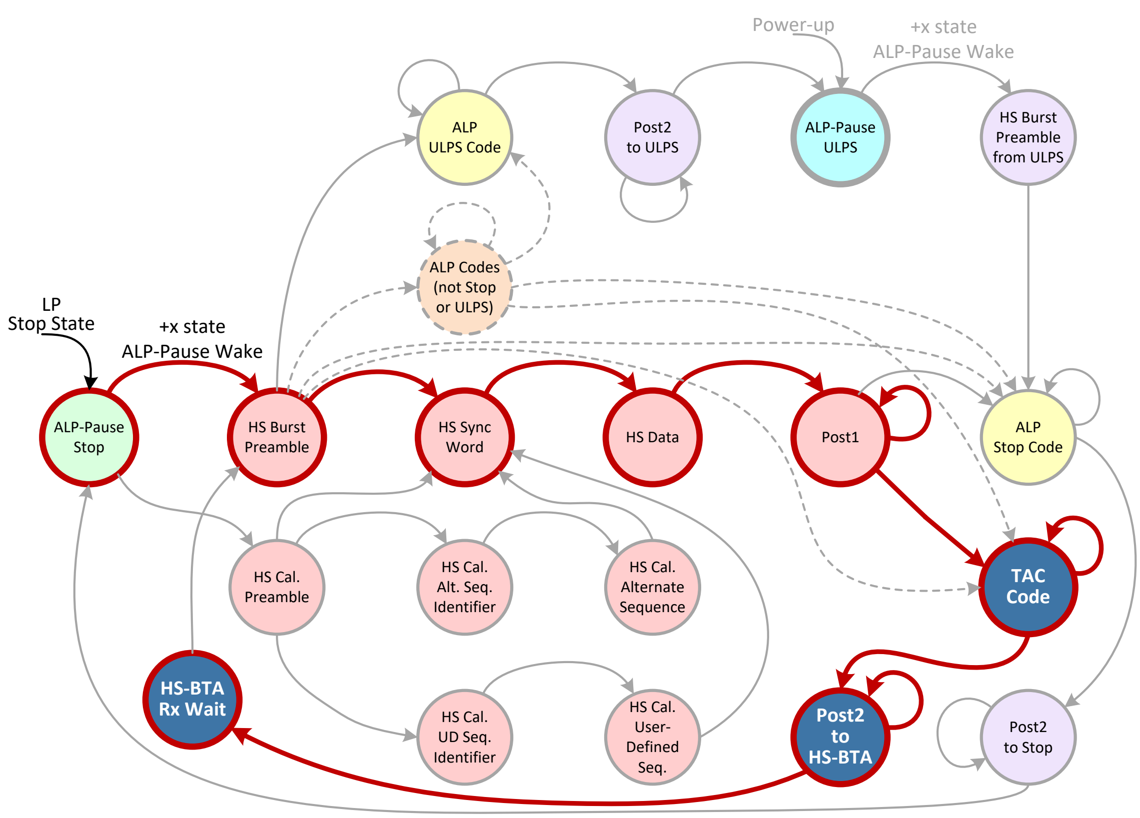


Figure 231 ~~Automatic Selection~~ State Transitions from ALP-Pause Stop to Turnaround

Figure 232 shows an example of ALP ~~Operation or LP Operation~~state machine transitions (highlighted in red) that occur between two Fast Lane Turnaround events. This is the sequence of events that occur during the "Slave is Driving" interval shown in ***Figure 228***.

~~This page intentionally left blank.~~

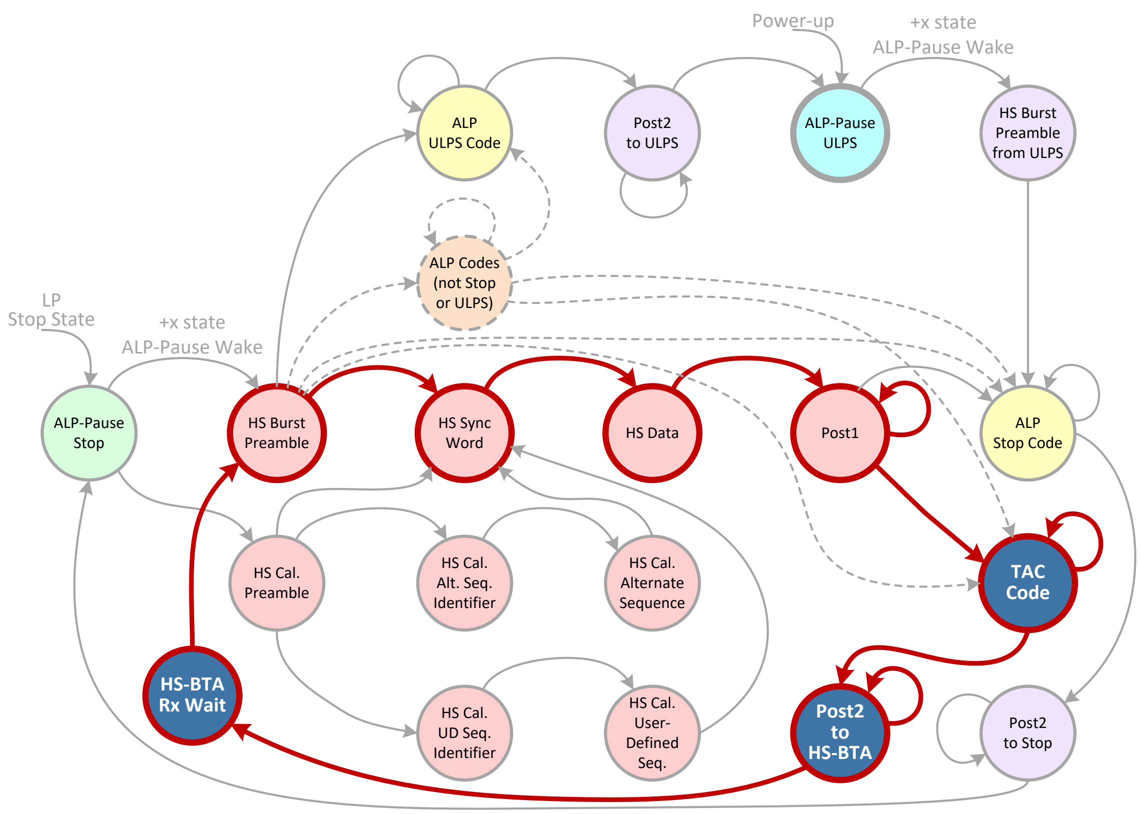


Figure 232 State Transitions from Turnaround to Turnaround

Figure 233 shows an example of ALP state machine transitions (highlighted in red) that occur, starting from a Fast Lane Turnaround Procedure (the HS-BTA Rx Wait state) and finishing when the burst ends and there is a transition to the ALP-Pause Stop state. This is the sequence of events that occur during the second "Master is Driving" interval shown in ***Figure 228***.

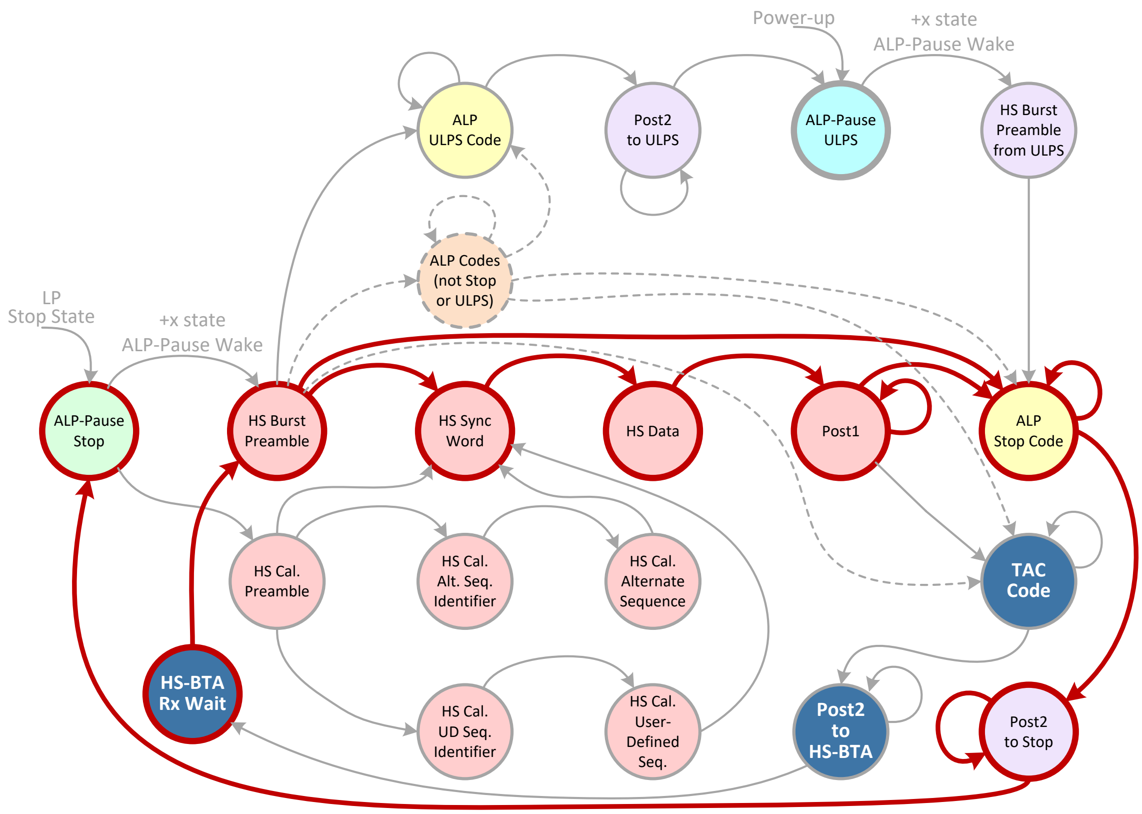


Figure 233 State Transitions from Turnaround to ALP-Pause Stop

The PPI signals that support ALP functions are used to perform a Fast Lane Turnaround. The first transmitting device stops transmission in much the same way as a transmitter signals the end of an ALP burst, except that a TAC code is sent instead of a Stop code. The first transmitting device becomes a receiver after it ceases transmission, so it can immediately switch to receive mode. In this case, the device that becomes a receiver does not need to be triggered by a long ALP Pause Wake pulse prior to the preamble. Instead, the trigger for assuming the role of a receiver is the transmission of the TAC code prior to the TGAP interval.

4782 *Figure 234* shows an example of the of the transmitter and receiver PPI signaling in the first transmitting
4783 device when a Fast Lane Turnaround occurs.

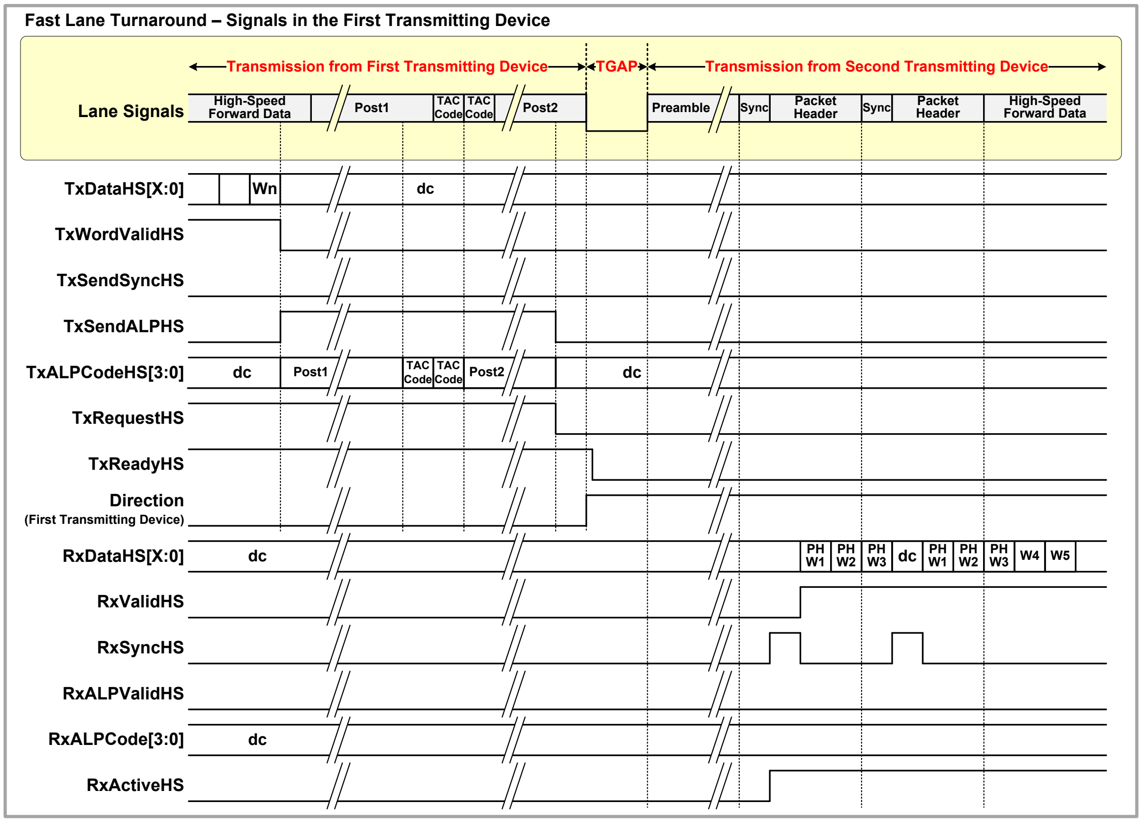
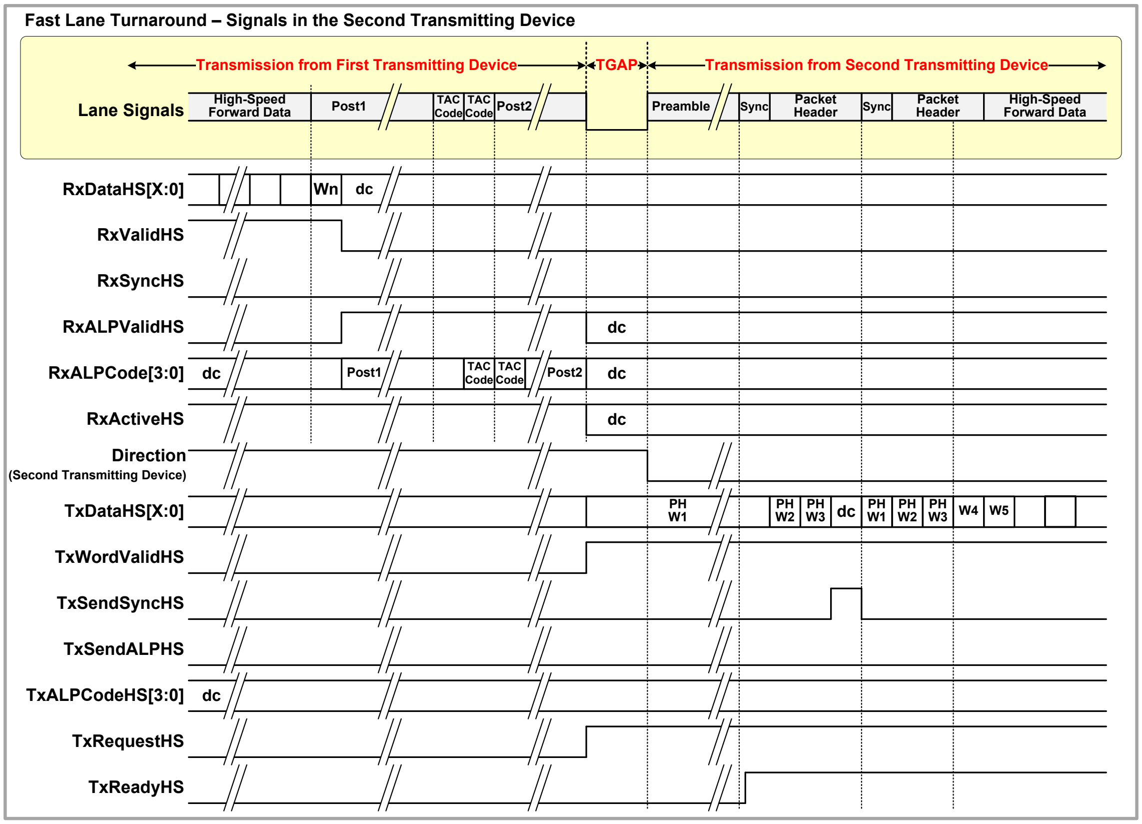
4784 

Figure 234 Example Fast Lane Turnaround at the First Transmitting Device

4785 *Figure 235* shows an example of the of the receiver and transmitter PPI signaling in the second transmitting
4786 device when a Fast Lane Turnaround occurs.



4787

Figure 235 Example Fast Lane Turnaround at the Second Transmitting Device