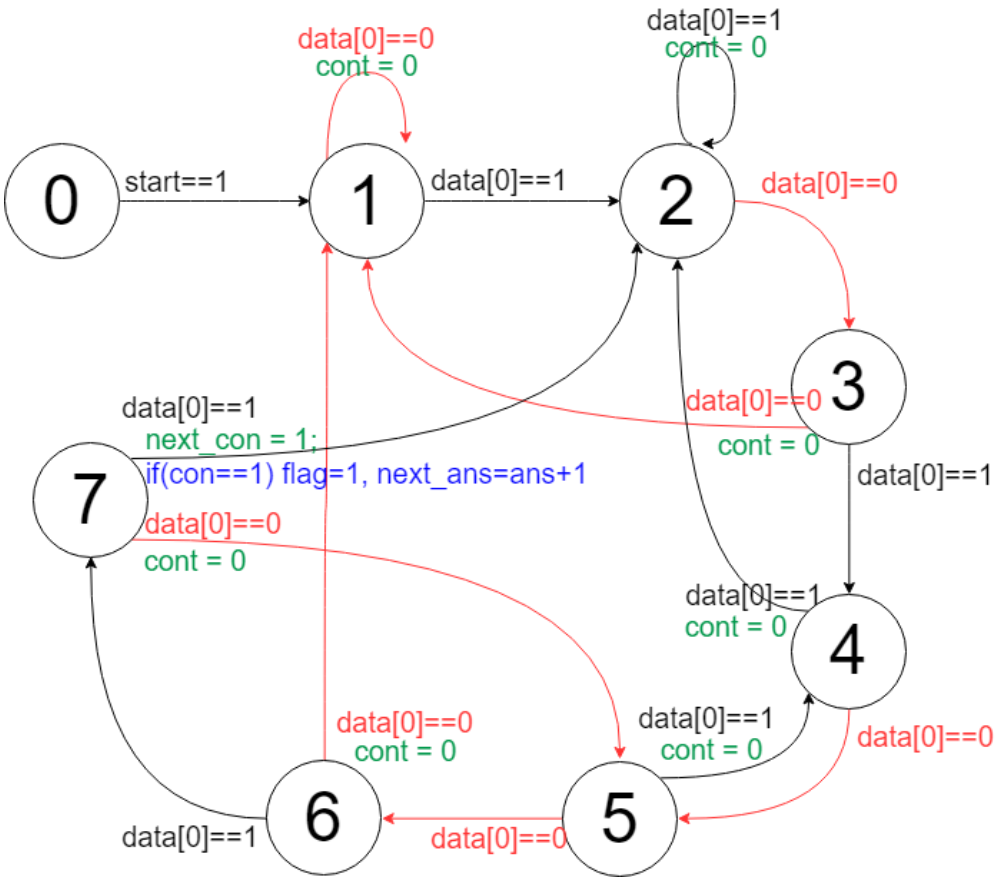
Lab3: PTM (Bonus)

1) State Transition Graph



Reason

cont 的用途：判斷之前是否出現過 10(100)+11 的字串，且與目前的 data 連續。

0-1：0 是初始值。Start 跳到 1 之後，state 從 1 開始。

1-6：每當分別符合 101001 中相應的數字，就往上個 state。

1 2 3 4 5 6

如果不符合，就按以下方式判斷，並且因為連續中斷，將 cont 歸零：

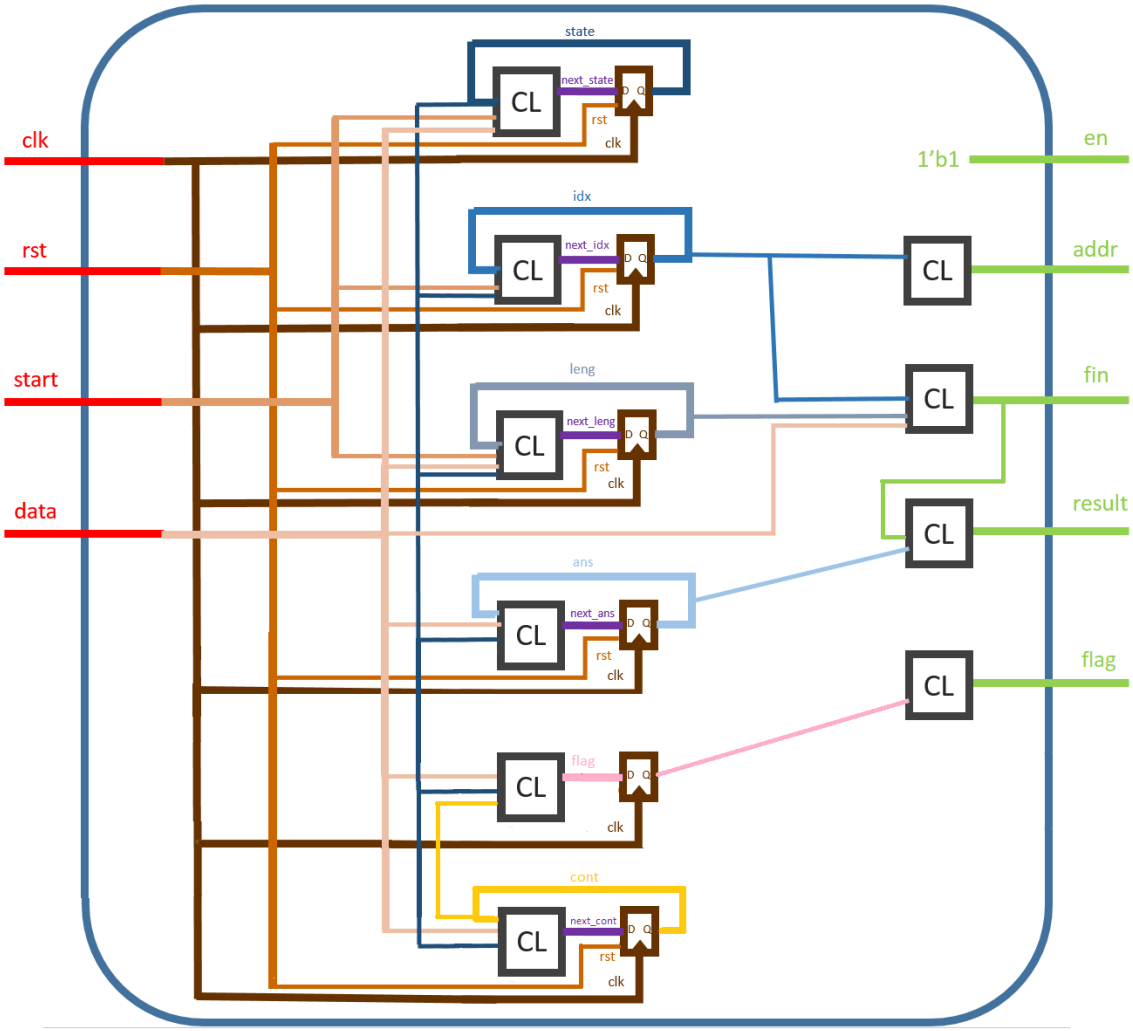
state	不符合的結果	1010011	match	next state
1	0	1010011	0	0+1=1
2	11	1010011	1	1+1=2
3	100	1010011	0	0+1=1
4	1011	1010011	1	1+1=2
5	10101	1010011	3	3+4=4
6	101000	1010011	0	0+1=1

7：如果是 0 -> 回到 (100)+ 的循環。

5 6 7

如果是 1 表示偵測到符合的字串，把 next_cont 設為 1。同時 1 可以作為下個字串的開頭，回到 state 2。如果 cont 為 1，表示 10(100)+11 出現 2 次或以上，把 flag 設為 1，ans 也 +1。

2) Block Diagram



BON

3) ncverilog simulation (sim)

```
rcfile = /users/course/2018S/cs210201/dld0119/lab3/novas.rc
guiConfFile = /users/course/2018S/cs210201/dld0119/lab3/novas.conf
[dld0119@ic26 ~/lab3]$ ncverilog BON_tb.v BON_v2.v +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Recompiling... reason: file './BON_v2.v' is newer than expected.
        expected: Fri Apr 20 23:13:15 2018
        actual:   Fri Apr 20 23:30:04 2018
file: BON_v2.v
        module worklib.BON:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.BON:v <0x0d4f86e1>
                        streams:   7, words:  5763
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                2       2
                Registers:             19      19
                Scalar wires:           6       -
                Vectored wires:         3       -
                Always blocks:          3       3
                Initial blocks:         3       3
                Cont. assignments:      3       5
                Pseudo assignments:     2       2
        Writing initial simulation snapshot: worklib.BON_tb:v
Loading snapshot worklib.BON_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the prog
rams that are using this file.
*Verdi3* : Create FSDB file 'BON.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

GET ! addr =   18 , your_flag = 1 , ans_flag = 1
GET ! addr =   49 , your_flag = 1 , ans_flag = 1
GET ! addr =   71 , your_flag = 1 , ans_flag = 1
GET ! addr =   89 , your_flag = 1 , ans_flag = 1
GET ! addr =   95 , your_flag = 1 , ans_flag = 1
GET ! addr =  123 , your_flag = 1 , ans_flag = 1
GET ! addr =  151 , your_flag = 1 , ans_flag = 1
GET ! addr =  197 , your_flag = 1 , ans_flag = 1

Result =    8 , Answer =    8
!!!!! ACCEPTED !!!!!

Simulation complete via $finish(1) at time 6120 NS + 0
./BON_tb.v:97           $finish;
```

4) ncverilog simulation (syn)

```
[dld0119@ic22 bonus]$ make syn
ncverilog header.v BON_syn.v BON_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/t
smc13.v +define+SDF +access+r


ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: BON_syn.v
        module worklib.BON:v
                errors: 0, warnings: 0
file: BON_tb.v
        module worklib.BON_tb:v
                errors: 0, warnings: 0
                Caching library 'tsmc13' ....... Done
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
  DFFRX1 \leng_reg[9]  ( .D(n85), .CK(clk), .RN(n216), .QN(n63) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,78|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[8]  ( .D(n84), .CK(clk), .RN(n216), .QN(n62) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,79|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[7]  ( .D(n83), .CK(clk), .RN(n216), .QN(n61) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,80|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[1]  ( .D(n77), .CK(clk), .RN(n216), .QN(n55) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,81|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[6]  ( .D(n82), .CK(clk), .RN(n216), .QN(n60) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,82|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[5]  ( .D(n81), .CK(clk), .RN(n216), .QN(n59) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,83|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[4]  ( .D(n80), .CK(clk), .RN(n216), .QN(n58) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,84|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[3]  ( .D(n79), .CK(clk), .RN(n216), .QN(n57) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,85|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[2]  ( .D(n78), .CK(clk), .RN(n216), .QN(n56) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,86|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 \leng_reg[0]  ( .D(n76), .CK(clk), .RN(n216), .QN(n54) );
                       |
ncelab: *W,CUVWSP (./BON_syn.v,87|21): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q

  DFFRX1 cont_reg ( .D(n96), .CK(clk), .RN(n216), .QN(n74) );
                  |
ncelab: *W,CUVWSP (./BON_syn.v,120|16): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,18240): Q
```

```
        Reading SDF file from location "./BON.sdf"
        Annotating SDF timing data:
                Compiled SDF file:     BON.sdf.X
                Log file:
                Backannotation scope:  BON_tb.BON
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of Pathdelays = 747  Annotated = 100.00% -- No. of Tc
hecks = 315  Annotated = 100.00%
                                      Total      Annotated      Percentage
                  Path Delays           747            747          100.00
                       $width           105            105          100.00
                   $setuphold           210            210          100.00
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.BON:v <0x5ad13c7c>
                        streams:   1, words:   115
                worklib.BON_tb:v <0x031d64f6>
                        streams:   6, words:  8850
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                 Instances  Unique
                Modules:               224      40
                UDPs:                   35       1
                Primitives:            517       8
                Timing outputs:        271      15
                Registers:              43      10
                Scalar wires:          311       -
                Expanded wires:         10       1
                Always blocks:           1       1
                Initial blocks:          3       3
                Cont. assignments:       1       1
                Pseudo assignments:      2       2
                Timing checks:         315      38
                Interconnect:          614       -
                Delayed tcheck signals:  105      36
                Simulation timescale:    1ps
        Writing initial simulation snapshot: worklib.BON_tb:v
Loading snapshot worklib.BON_tb:v .................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file ma
y crash the programs that are using this file.
*Verdi3* : Create FSDB file 'BON_syn.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

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GET ! addr =  151 , your_flag = 1 , ans_flag = 1
GET ! addr =  197 , your_flag = 1 , ans_flag = 1

Result =    8 , Answer =    8
!!!!! ACCEPTED !!!!!

Simulation complete via $finish(1) at time 6120 NS + 0
./BON_tb.v:97           $finish;
ncsim> exit
```