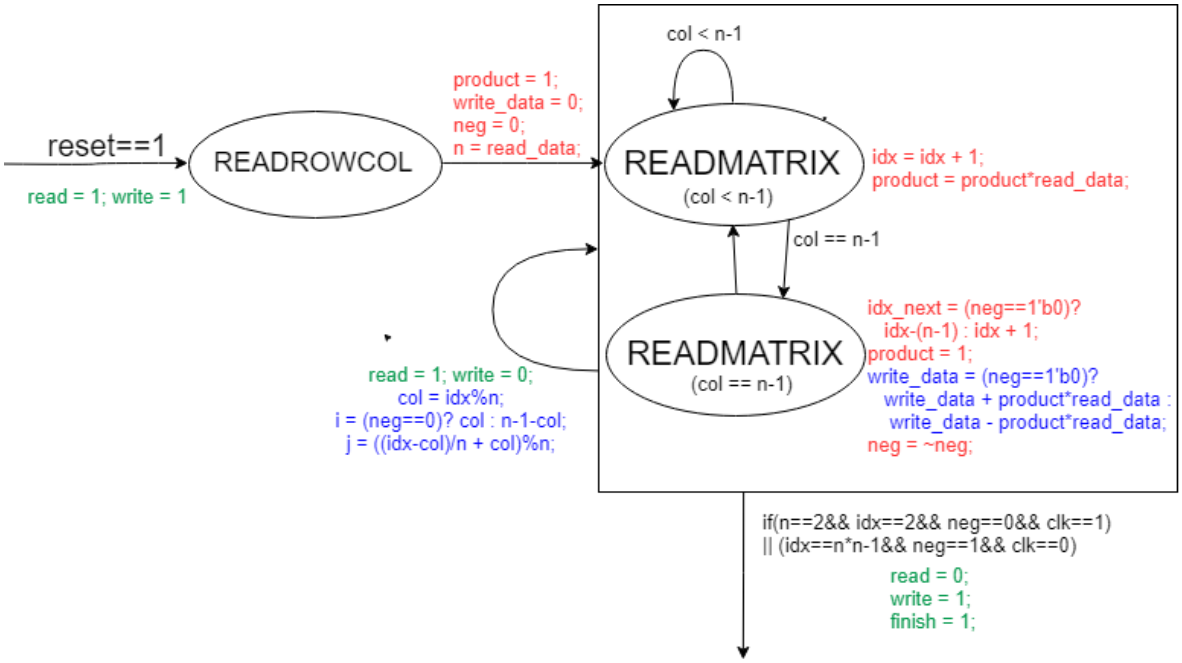
Lab4 Bonus: Determinant

1) State Transition Graph



Reason

有兩個 state：READROWCOL 和 READMATRIX，但是 READMATRIX 中分為 col < n-1 和 col == n-1 的情況。

READROWCOL：將 read、write 都設為 1，得到矩陣的行列數，記錄在 n。到下一個 state（READMATRIX），初始化 product = 1， write_data = 0，neg = 0。

READMATIRX：read 為 1，write 為 0，讀取矩陣。

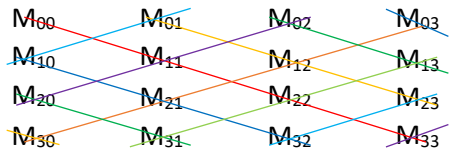
- idx 為目前累計讀取了幾次，通過 idx 可推算 i 與 j（下面有說明）。
- product 是目前這個 cycle 中得到的總積數，read_data 後與 product 相乘，更新 product_next。當 col == n-1 即完成 1 個 cycle，write_data 就根據 neg 選擇加上或減掉這個 cycle 的積數。然後 product 歸零
- neg = ~neg：如果是加，拿下一個 cycle 就是減，反之亦然。

當 idx==n*n-1，neg = 1 的時候輸出答案，立起 finish。考慮到 2×2 矩陣的特殊情況：

```
(n==2'd2 && idx==2 && neg==1'b0 && clk==1'b1)
```

col、idx、i、j、neg 之間的關係

例如在 4×4 矩陣，計算過程如下（矩陣 M_{ij}，括號內為 idx）：



+	M_{00} (0)	*	M_{11} (1)	*	M_{22} (2)	*	M_{33} (3)	Cycle 0
-	M_{30} (0)	*	M_{21} (1)	*	M_{12} (2)	*	M_{03} (3)	Cycle 1
+	M_{01} (4)	*	M_{12} (5)	*	M_{23} (6)	*	M_{30} (7)	Cycle 2
-	M_{31} (4)	*	M_{22} (5)	*	M_{13} (6)	*	M_{00} (7)	Cycle 3
+	M_{02} (8)	*	M_{13} (9)	*	M_{20} (10)	*	M_{31} (11)	Cycle 4
-	M_{32} (8)	*	M_{23} (9)	*	M_{10} (10)	*	M_{01} (11)	Cycle 5
+	M_{03} (12)	*	M_{10} (13)	*	M_{21} (14)	*	M_{32} (15)	Cycle 6
-	M_{33} (12)	*	M_{20} (13)	*	M_{11} (14)	*	M_{02} (15)	Cycle 7

col、idx、i、j、neg 關係如下表：

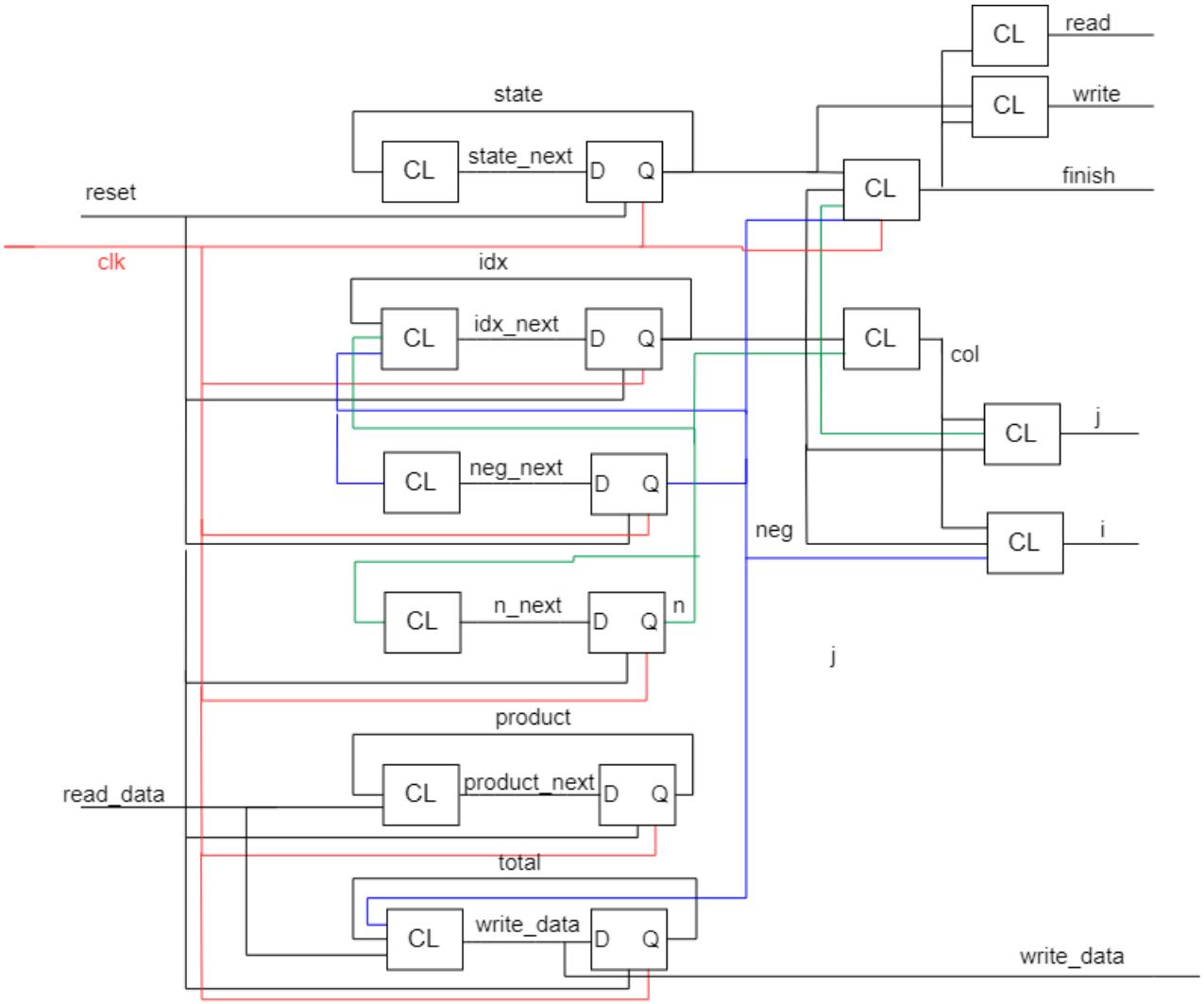
col	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
idx	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
i(neg==0)	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
i(neg==1)	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
j	0	1	2	3	1	2	3	0	2	3	0	1	3	0	1	2

推算得知：

```
    if(col<n-1) idx_next = idx + 1;
    else idx_next = (neg==1'b0)? idx-(n-1) : idx + 1; //如果剛才是做加法 idx 就回到該行的開始，做減法
    col = idx%n;
    i = (neg==1'b0)? col : n-1-col;
    j = ((idx-col)/n + col)%n;
```

*這樣 register 只要有 neg 和 idx 就可以了，其他都是 wire。

2) Block Diagram



3) ncverilog simulation (sim)

```
[dld0119@ic26 ~/lab4]$ make sim_bonus
ncverilog header.v Det.v Det_tb.v +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Det.v
        module worklib.Det:v
                errors: 0, warnings: 0
file: Det_tb.v
        module worklib.test:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.Det:v <0x20269703>
                        streams:  10, words:  6171
                worklib.test:v <0x07a7022b>
                        streams:   7, words:  7593
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                 Instances  Unique
                Modules:                 2       2
                Registers:              18      18
                Scalar wires:            5       -
                Vectored wires:          5       -
                Always blocks:           5       5
                Initial blocks:          3       3
                Cont. assignments:       5       6
                Pseudo assignments:      1       1
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v .................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
ay crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Det.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
###################
#Congratulation!!!#
###################
Simulation complete via $finish(1) at time 1025 NS + 0
./Det_tb.v:98           $finish;
ncsim> exit
```

4) ncverilog simulation (syn)

```
[dld0119@ic26 ~/lab4]$ make syn_bonus
ncverilog header.v Det_syn.v Det_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/t
smc13.v +define+SDF +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Loading snapshot worklib.test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file ma
y crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Det_syn.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
###################
#Congratulation!!!#
###################
Simulation complete via $finish(1) at time 1025333 PS + 0
./Det_tb.v:98           $finish;
ncsim> exit
```