RepCut: Superlinear Parallel RTL Simulation with Replication-Aided Partitioning

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About me

- Education
  - BS in School of Electronic and Information, South China University of Technology, China, 2020.
  - MS in Department of ECE, Rutgers University, 2021.
  - Second-year PhD student (supervisor: Prof. Tsung-Wei Huang).
- Current research
  - Incremental task graph partitioning.
  - A paper[1] of task graph partitioning was accepted to DAC'24.
  - I am submitting a paper to ICCAD'24.

[1] Boyang Zhang, Dian-Lun Lin, Che Chang, Cheng-Hsiang Chiu, Bojue Wang, Wan Luan Lee, Chih-Chun Chang, Donghao Fang, and Tsung-Wei Huang, "G-PASTA: GPU Accelerated Partitioning Algorithm for Static Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024

Outline

- Introduction to RTL simulation
  - What is RTL simulation?
  - Why partitioning?
  - Partitioning challenges?
- Introduction to RepCut
  - Partitioning algorithm walkthrough
  - Scheduling the partitions
  - Experimental results
- Current research
  - Limitations of RepCut partitioning
  - PASTA partitioning

Introduction to RTL simulation

What is RTL simulation?

- A process to simulate the behaviors of a Register Transfer Level(RTL) design to verify its functionality.
- **Event-driven**(more accurate) or **full-cycle**(less time-consuming).
- Full-cycle simulator: Verilator[2], **ESSENT**[3](unoptimized).

[2] https://github.com/verilator/verilator
[3] https://github.com/ucsc-vama/essent

Why partitioning?

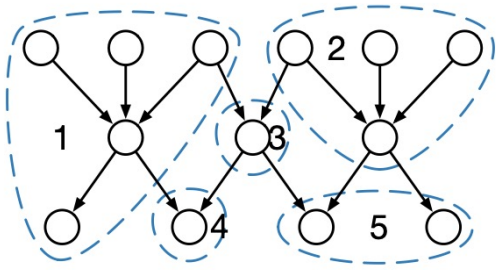
- RTL simulation is very **time-consuming** for large designs.

- RTL simulation in parallel?

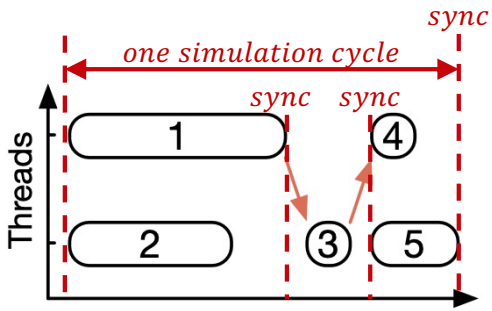
- Represent the design as a task dependency graph(**TDG)**.
  → Node: the simulation task of a logic gate/register.
  → Edge: the connection between logic gates/registers.
  → Too **fine-grained.**
  → Partition the TDG.

Partitioning challenges?

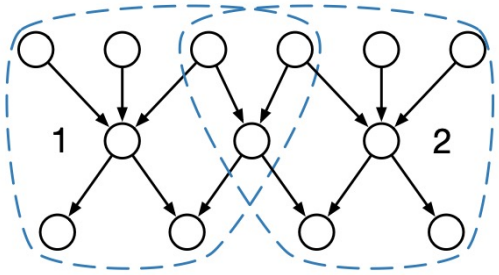
- Goal: **Balanced partitions** and **minimal synchronization effort**.



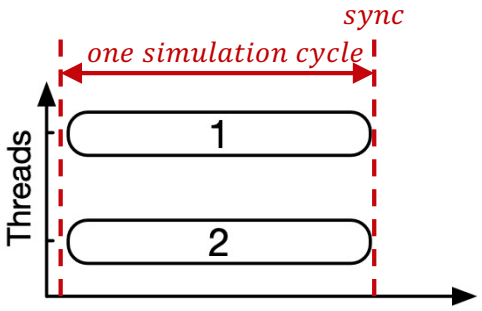
(a) Verilator Partitioning



(b) Verilator Schedule



(c) RepCut Partitioning



(d) RepCut Schedule

Introduction to RepCut

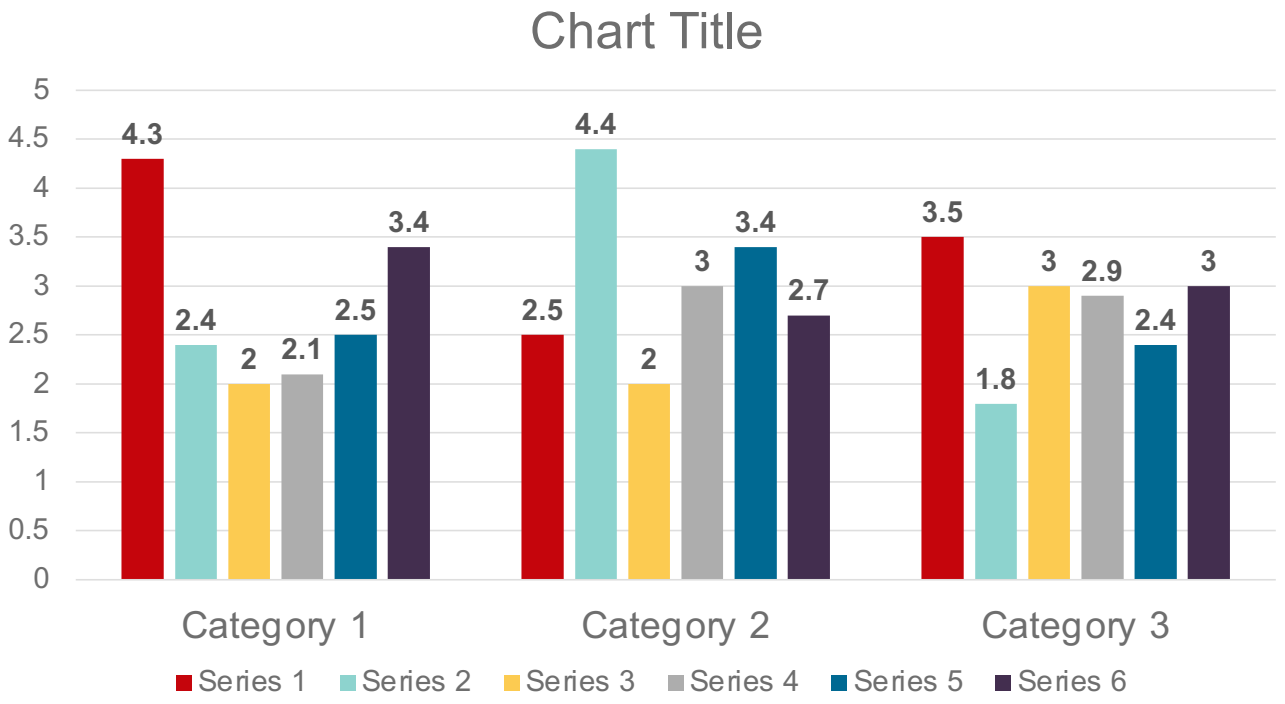


Chart Title
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
4.3
2.4
2
2.1
2.5
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3.5
1.8
3
2.9
2.4
3
Category 1
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Category 3
Series 1
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Series 3
Series 4
Series 5
Series 6

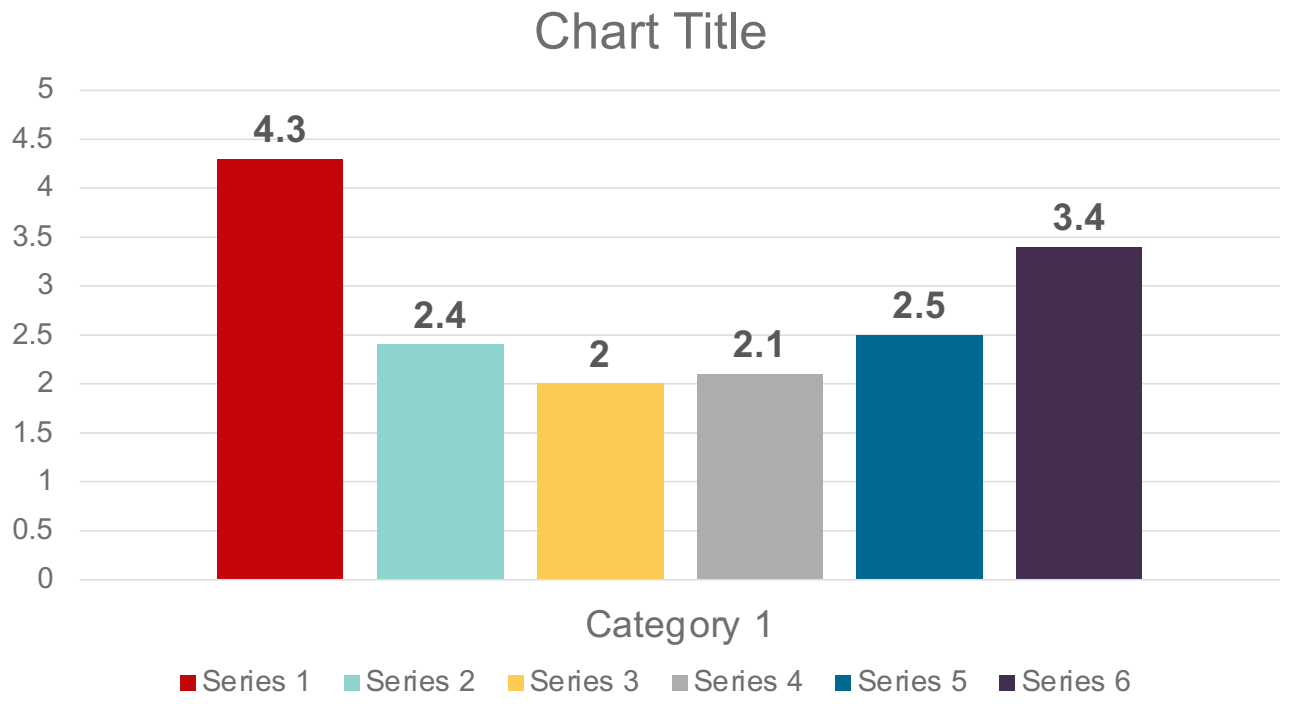
Chart Title
5
4.5
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3
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1.5
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0
4.3
2.4
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Category 1
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Series 2
Series 3
Series 4
Series 5
Series 6

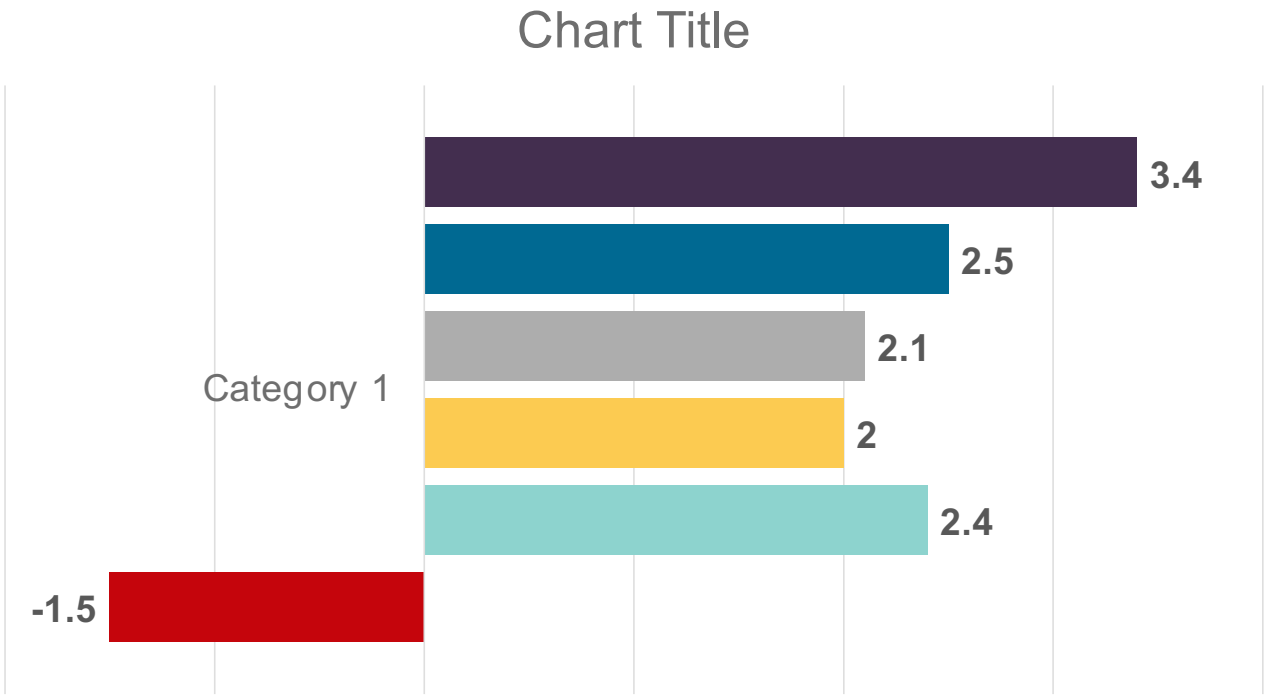


Chart Title
Category 1
3.4
2.5
2.1
2
2.4
-1.5

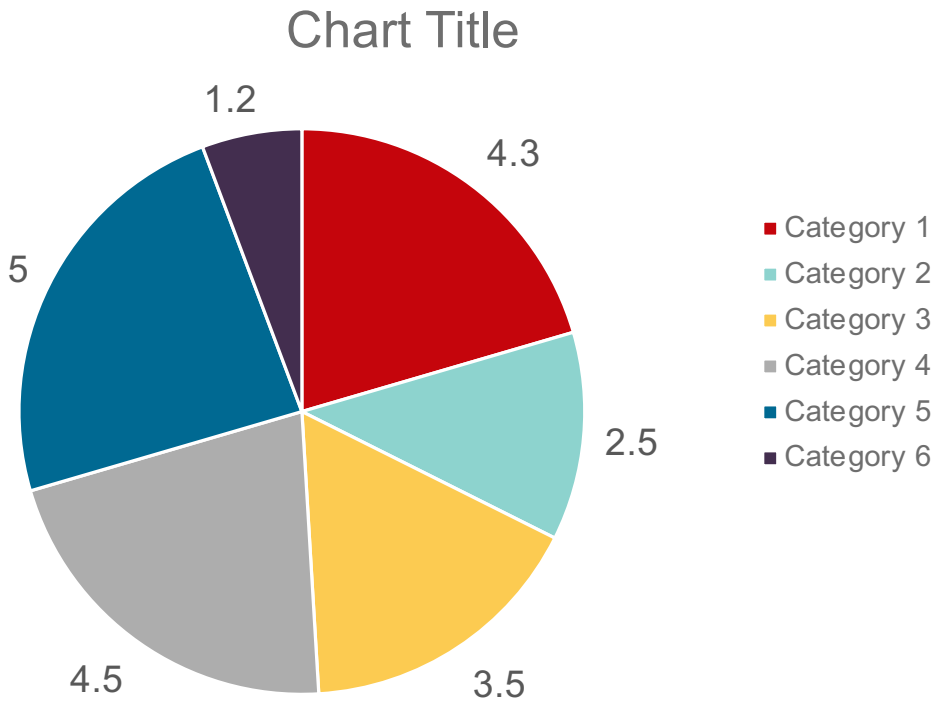
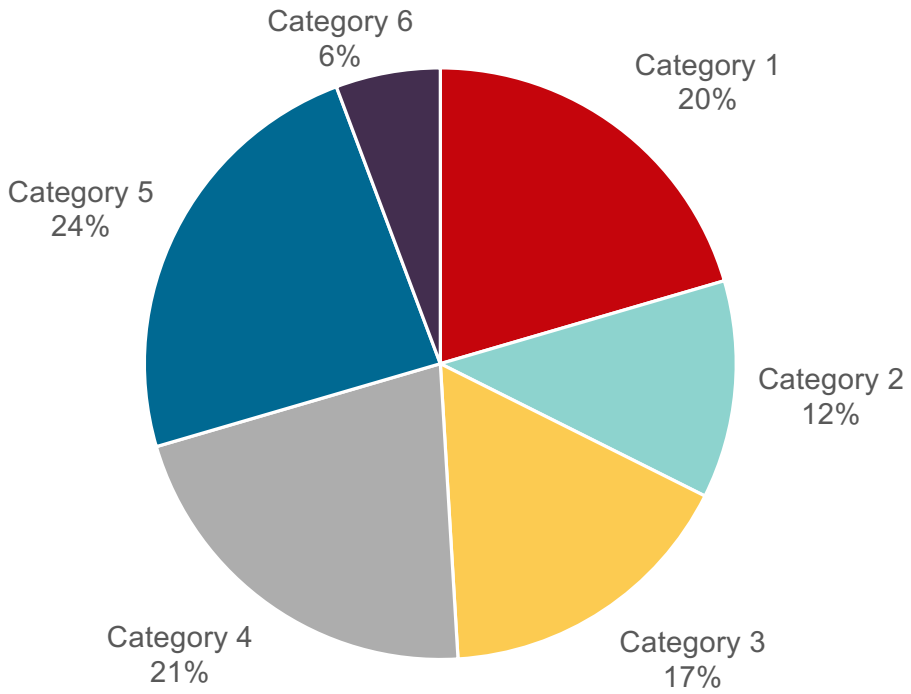


Chart Title
1.2
4.3
5
2.5
4.5
3.5
Category 1
Category 2
Category 3
Category 4
Category 5
Category 6

Chart Title


Category 6
6%
Category 1
20%
Category 5
24%
Category 2
12%
Category 4
21%
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