Advanced VLSI

Bitcoin

Stage 3 : Placement

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3.1 Warmup Questions

1. **[#P3.1_Q1] Why is the floorplan stage important in physical design?**

For a number of reasons, the floorplan stage of integrated circuit (IC) physical design is crucial.

1. **Layout Optimization:** The key functional blocks of the IC are initially positioned according to the floorplan. Because it dictates the overall layout, which impacts the chip's performance, power consumption, and area usage, its location is crucial. A well-designed floorplan can maximize accessible silicon area, minimize power usage, and minimize interconnect delays.

2. **Interconnect Planning:** The routing of the interconnects, or cables, that link various components is planned by designers during the floorplan stage. These interconnects' length and complexity can be reduced with careful planning, which lowers power consumption and signal latency—two critical factors in high-performance devices.

3. **Power Distribution:** The initial planning of the power distribution network takes place at the floorplan stage. This network makes sure that every component of the chip gets enough power without producing hot spots or large voltage drops. Reliability and performance of the chip depend on proper power distribution.

4. **Timing Closure:** To make sure that signals may travel between components within the necessary time restrictions, timing analysis is frequently carried out at the floorplan stage. Early detection and resolution of possible timing problems in the design phase helps prevent later, expensive redesigns.

5. **Area Estimation:** The IC's estimated area is provided by the layout. Given that larger chips are typically more expensive to make, this is crucial for figuring out the cost of production. Additionally, it aids in determining if the design will fit inside the desired silicon region.

6. **Design for Manufacturability (DFM):** Designers can take manufacturability concerns into account during the layout stage. Designers can lower the possibility of flaws and increase the production process's total yield by positioning components to minimize manufacturing problems.

2**.[#P3.1_Q2] What are some of the factors to consider when creating a floorplan?**

An integrated circuit's (IC) floorplan must take into account a number of important aspects to guarantee maximum performance, effectiveness, and manufacturability. In order to create a design that satisfies timing, power, thermal, and area restrictions, these elements are essential.

Hierarchy and Module Placement :

Design Hierarchy: In order to reduce power consumption and communication delays, the floorplan should adhere to the design's hierarchical structure by positioning

related modules next to one another. Signal integrity is preserved and routing is made easier by this close proximity.
Blocks that are essential to the IC's performance, like CPUs or memory, should be positioned in key areas that allow for fast communication; central placement is frequently necessary to reduce latency.

Ratio of Area to Aspect :

Silicon Utilization: To make sure the design fits within the silicon that is available while still providing space for buffers and interconnects, the floorplan's overall area must be optimized. Making effective use of space lowers expenses and avoids routing issues.
Aspect Ratio: Reducing wiring complexity and guaranteeing manufacturability require maintaining an acceptable aspect ratio, or the width to height ratio. A balanced aspect ratio contributes to improved yield and performance.

Length of Interconnect and Routing Congestion :

Reducing Interconnect Length: Shorter interconnects are better since they use less power and delay, especially for high-speed lines. The length of important interconnects should be kept to a minimum in the floorplan.
Preventing Routing Congestion: Too many interconnects converge in one place, which can cause timing problems and make routing more difficult. This should be avoided in the floorplan. Early in the design phase, these problems are frequently found and fixed using congestion analysis methods.

Planning for Power :

Power Distribution Network (PDN): A carefully thought-out PDN is necessary to provide consistent power to every component without

large drops in voltage or producing hot areas. Power grid and distribution network layouts must be included in the floorplan.
Decoupling Capacitors: These capacitors must be positioned correctly to remove noise from the power source and guarantee steady performance, particularly in close proximity to delicate analog and fast digital circuitry.

Distribution of Clocks :

Clock Tree Synthesis (CTS): Keeping timing integrity throughout the chip requires a balanced clock distribution network with minimal clock skews. Clock tree routing and clock buffer placement must be supported by the layout.
Clock Domain Isolation: Physically separating various clock domains aids in minimizing timing problems and interference. Timing integrity is preserved and clock routing is made easier by this isolation.

Timing Closure :

Critical Path Optimization: To reduce delay, the floorplan should make sure that parts on critical paths are positioned close to one another. To achieve time closure, components must be identified and their placement along these paths optimized.
Buffer Insertion: Especially on lengthy interconnects or pathways with possible timing problems, strategically placing buffers in the floorplan helps preserve signal integrity and satisfy time restrictions.

[#P3.1_Q3] Congestion:

What is congestion in a floorplan?

When a particular region of the chip layout has a high density of connections and routing channels, it is referred to as congestion in floorplan design. This happens when the region's capacity is exceeded by the demand for routing resources, like metal wires or vias. Areas with components like multiplexers or I/O interfaces that need extensive routing frequently experience congestion. It may be challenging to successfully link all the required signals in these crowded places due to the restricted routing space.

Why is congestion a concern in floor planning?

In floorplanning, congestion is a major worry since it can negatively affect the design's usefulness and manufacturing feasibility in a number of ways. Longer routing paths caused by high congestion lengthen signal propagation delays and may cause timing requirements like setup and hold periods to be broken. The chip's overall performance may suffer as a result. Signal integrity problems, such as capacitive coupling (crosstalk) between neighboring wires, are also more likely to occur in crowded places. This can disrupt signal transmission and result in functional faults. Furthermore, the efficiency and thermal management of the chip may be impacted by increased dynamic power consumption and localized overheating brought on by longer routing pathways' increased parasitic capacitance.

Furthermore, during the manufacturing process, congestion presents serious difficulties. It raises the possibility of breaking manufacturing rules, which could result in possible flaws in the physical design of the device. The economics of the design might be affected by crowded areas since they can make it more difficult to create masks and lithography, which lowers yield rates and raises the cost per functional chip. Effective congestion management is necessary to guarantee a chip architecture that is reliable, effective, and scalable.

[#P3.1_Q4] In what situations might a worker need to do manual work to assist an automatic program in floor planning?

In a number of scenarios when automated technologies are inadequate, manual intervention in floor planning is required. Important situations consist of:

1. Congestion Management: High congestion regions brought on by dense standard cell placement or improper macro positioning are sometimes difficult for automated

solutions to handle. In order to increase routing performance and decrease time violations, designers may need to manually reorder scan chains, apply blocks, or modify the location of cells and macros.

2. Power Distribution: To prevent IR drop and efficiently control power delivery, complex designs with several power domains need careful planning. Designers frequently physically reposition power rails, decoupling capacitors, and level shifters since automated tools might not properly optimize power grids.

3. Optimization Critical Timing Paths: Automated placement may not satisfy the exacting timing specifications when crucial timing paths require optimization. Flip-flops or other important logic components must frequently be manually positioned closer to I/O ports or other components in order to minimize delays on timing-critical pathways.

4. custom Macro Placement: In designs containing IP cores or bespoke analog blocks, manual intervention is required to satisfy particular layout or performance requirements that automated tools are unable to handle efficiently.
By ensuring that performance, power, and manufacturability objectives are fulfilled, these tasks aid in optimizing design quality.

Option 1: Automatic floorplan

2.1. **Explain how the parameters core_utilization and side_ratio in set_auto_floorplan_constraints procedure effect the automatic floorplan.**

The amount of a chip's available core area that is devoted to design elements like functional logic cells (standard cells) is known as core usage. Usually, a percentage is used to express it.

A denser arrangement of components within the chip due to high core utilization may result in a smaller overall chip size. Congestion, on the other hand, can make it more difficult to route connections between cells, which could affect performance and result in violations of design rules.

Reduced core utilization frees up more bandwidth for routing, which eases congestion and facilitates control over power distribution and signal integrity. But this also leads to a bigger chip, which can raise power consumption and manufacturing costs.

The general structure and shape of the floorplan are defined by the side ratio, which establishes the proportion between the width and height of the core area and might influence the effectiveness of routing and placement. Depending on certain design needs or limits, a rectangular core may be required, although it can present routing issues. A square core, on the other hand, typically facilitates balanced routing with shorter and more uniform connection paths.

What metals are we using for the power grid?

From the tcl script, the power grid is constructed using multiple metal layers:

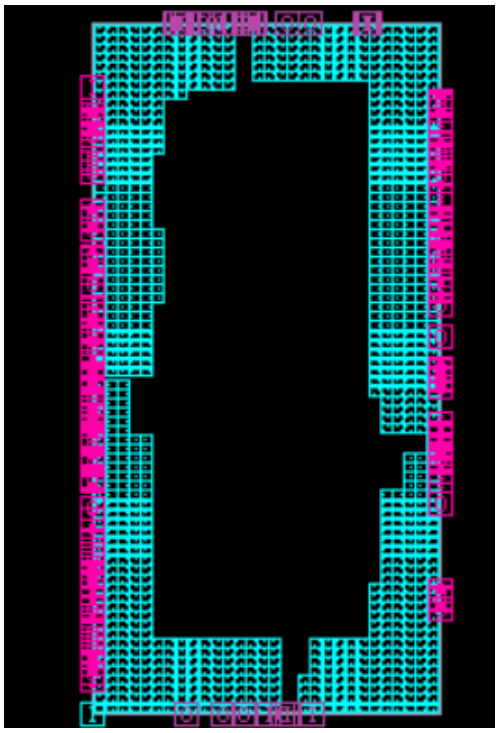
M1: Metal 1 is used for creating power rails for standard cells. These rails are typically the lowest metal layer and are critical for distributing power close to the logic cells.
M5 to M9: These metal layers are used for creating vertical and horizontal power straps. The straps are arranged in a mesh pattern, ensuring robust power distribution throughout the chip:
M5: Vertical power straps are created on Metal 5.
M6: Horizontal power straps are created on Metal 6.
M7: Additional vertical power straps on Metal 7.
M8: Horizontal power straps on Metal 8.
M9: Vertical power straps on Metal 9.

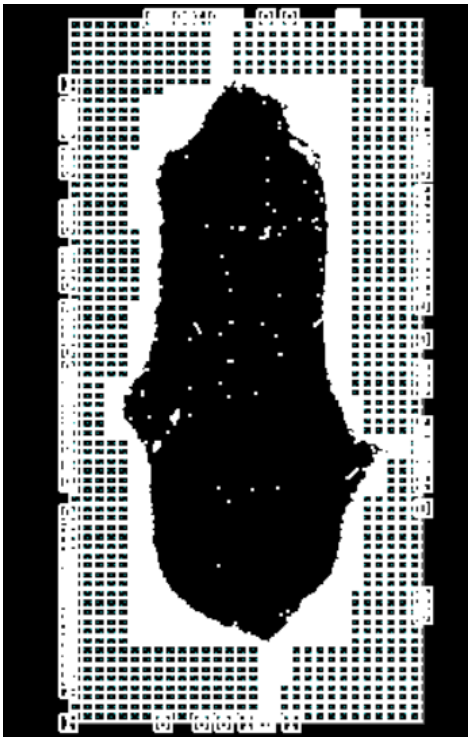
Task 1:

[#P3.2_Q1] For each of the three floorplan options submit:

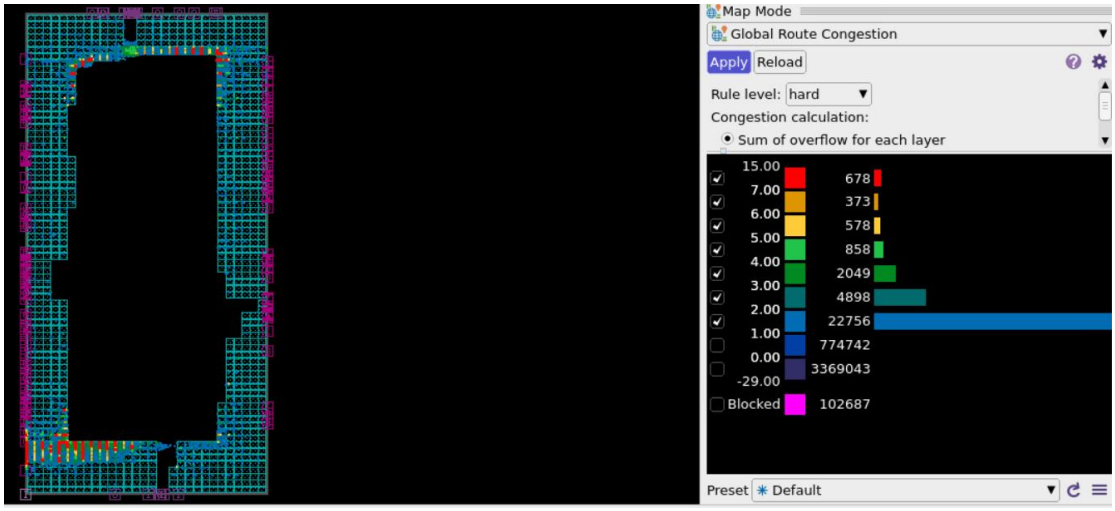
Print screen of the layout with and without the congestion map. If needed take more than one print screen with a different zoom (F in keyboard might help) and remove from the object's view the objects that aren't necessary for the floorplan

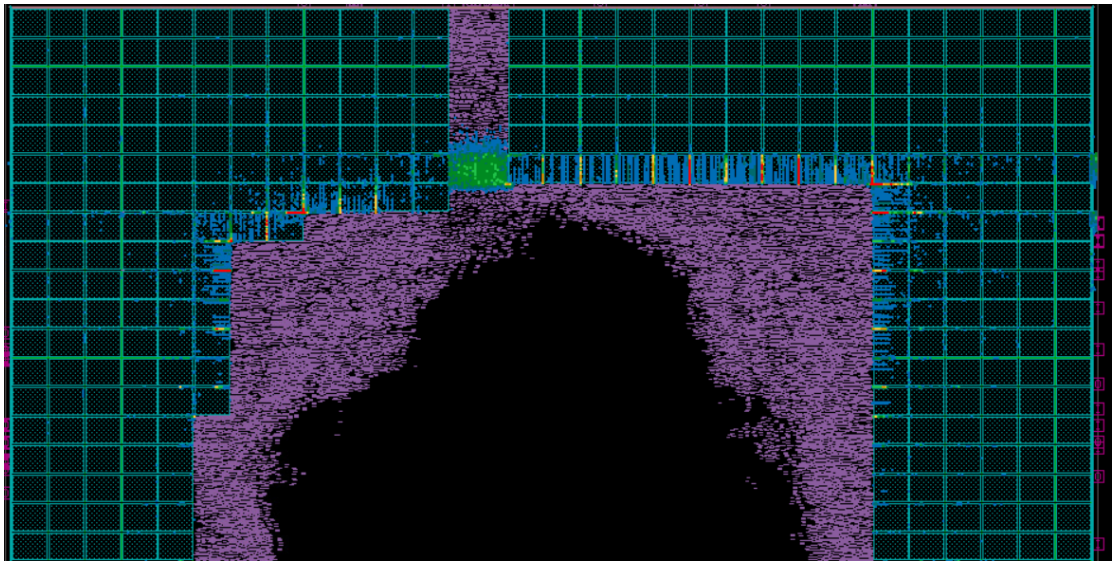
Layout:

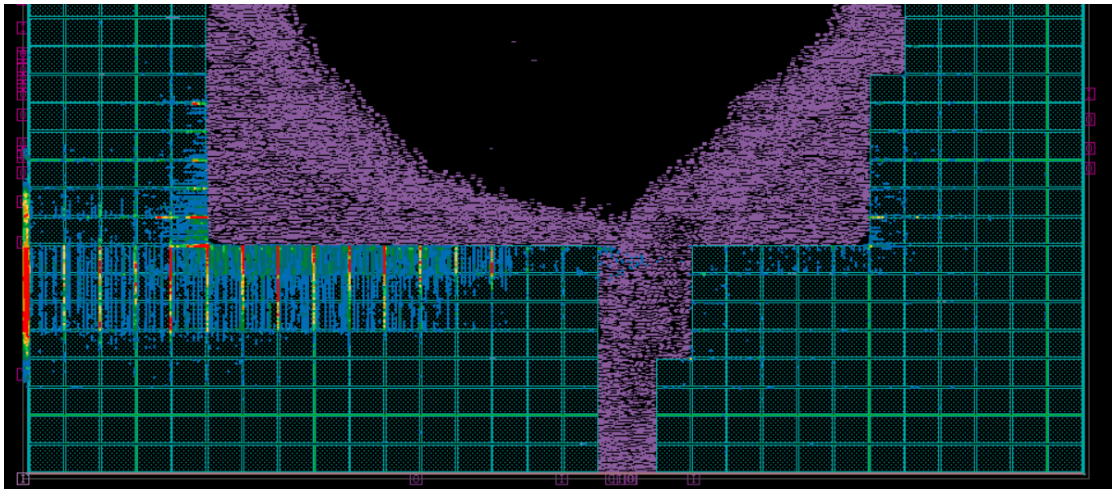




Layout print screen with the congestion map:







List the major pros and cons of the floorplan option:

Cons: This automated floorplan is an early design method and does not include improvements, optimizations, or problem-solving strategies. Fundamental and general examinations are typically completed quickly and easily by initial tests. These checks could involve making sure the workspace functions properly, making sure reports are produced appropriately, and making sure system files are arranged and stored in the right places. With its overview of how the layout might appear depending on the tool's algorithms, it offers a useful place to start, particularly for intricate ideas. Therefore, it is best to begin with this fundamental check before moving on to a more complex design.

Cons: Most activity is focused on the perimeter, where memory are positioned close to the ports at the chip's edges, leaving a sizable amount of the chip unused. The usual positioning issues with SRAMs are not addressed by this approach. Significant congestion is also seen around the periphery, especially when the SRAMs are closely spaced, according to the congestion map. This may result in serious routing problems, such as possible short circuits because of inadequate pin spacing, which may impair the chip's performance. Furthermore, as the congestion map illustrates, a high density of SRAMs along the boundaries combined with small gaps between macros causes a large number of overflows. Furthermore, pin congestion in small channels might result from the concentration of macros close to the corners, aggravating the overall .

Suggest how can the floorplan be improved (automatically or manually) and discuss the tradeoffs.

With the present core utilization at 50%, the center area has a sizable amount of unused capacity. This vacant space can be filled with standard cells by boosting core utilization, which will enable macros to be distributed more evenly throughout the layout. Congestion would be lessened by this change, especially in densely populated areas. Therefore, macros can be positioned more strategically, cutting wire lengths and increasing routing efficiency, since there is more space available as a result of higher core utilization. By manually adjusting the power grid and I/O pin location after increasing core utilization, we can guarantee appropriate signal routes and balanced power distribution, lowering latency and enhancing overall design integrity.

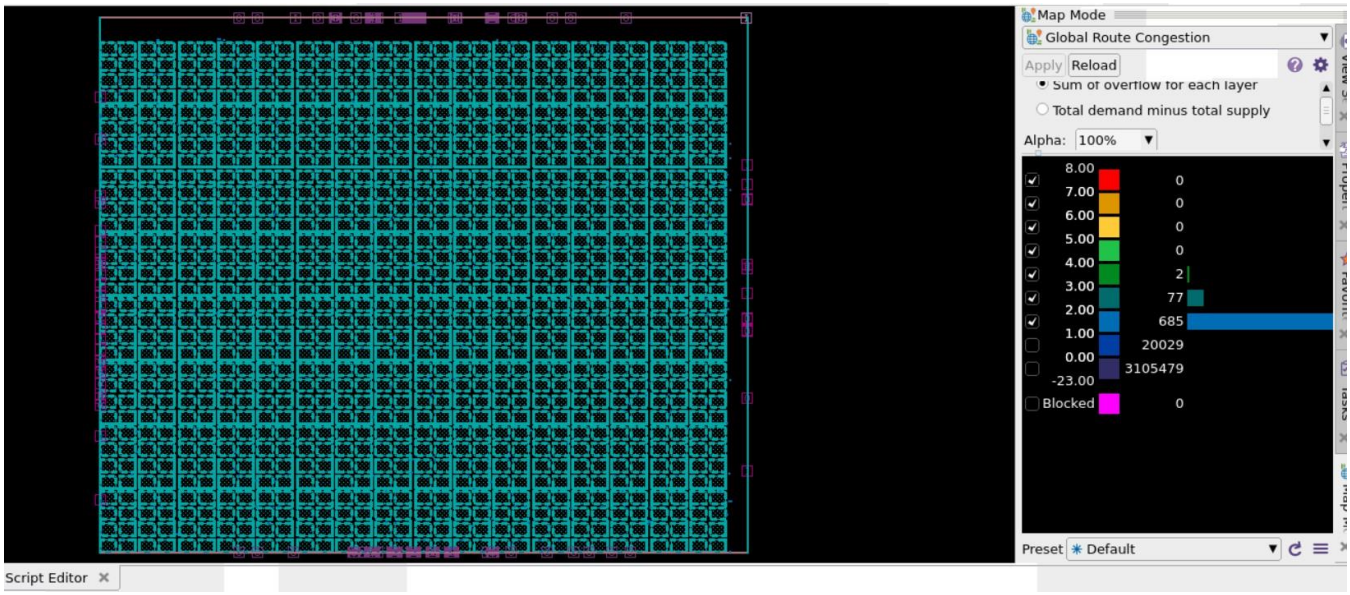
Option 2: Re-organized the location of the SRAMs into a matrix shape (fixed spaces)

Task 2

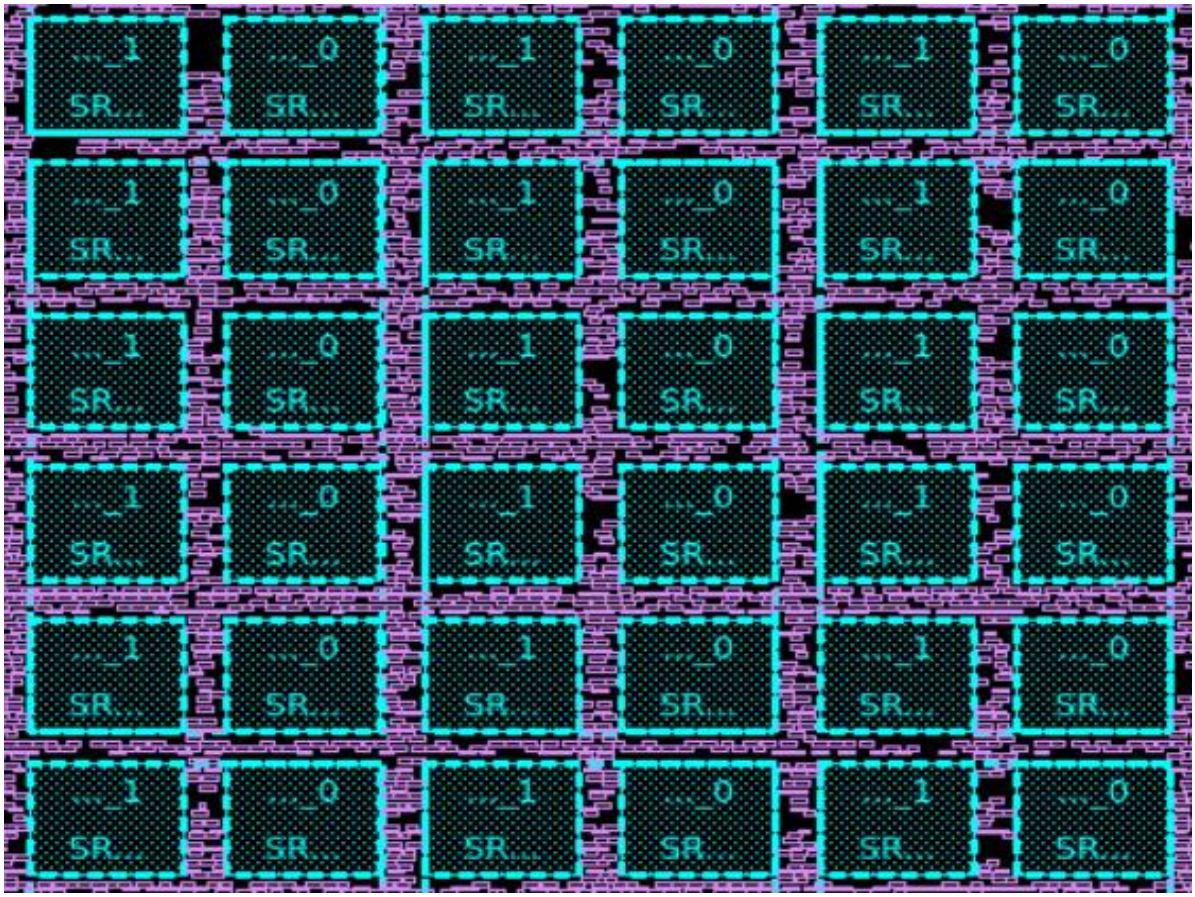
[#P3.2_Q1] For each of the three floorplan options submit:

2.1. Print screen of the layout with and without the congestion map. If needed take more than one print screen with a different zoom (F in keyboard might help) and remove from the object's view the objects that aren't necessary for the floorplan.

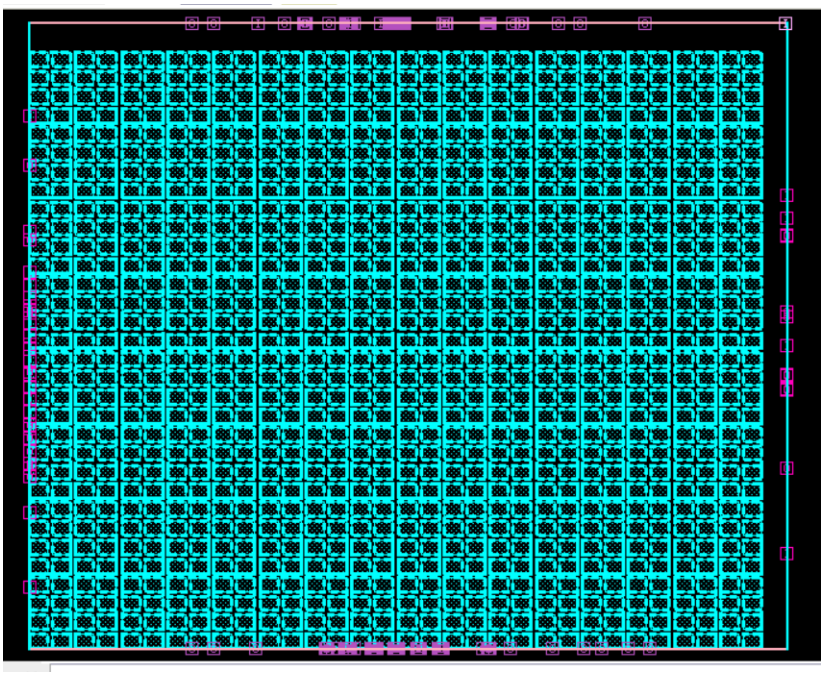
Layout with Congestion Map:



Layout zoom in to standard cells:



Layout without Congestion Map:



List the major pros and cons of the floorplan option.

Pros:

By effectively utilizing the chip's whole square area, the matrix arrangement prevents significant space waste and lowers production costs. As can be observed from the congestion map, which displays fewer high-density zones, this arrangement produces a more equal distribution of component density throughout the circuit, reducing the likelihood of routing congestion and possible failures. Furthermore, distributing macros evenly makes more routing channels available between them, which streamlines routing and may cut down on delays. All things considered, the orderly arrangement helps prevent significant overflows, resulting in a design with controllable routing paths.

Cons:

Although the structure is balanced, the absence of a clearly defined area for regular cells and macros can make routing more difficult because macros can block pathways and cause congestion in small routing channels. Furthermore, many of the memories are situated far from the borders of the chip due to their matrix placement, which raises the signal transmission delay between the memory and external ports and may affect hardware performance. Buffers might be needed to improve the signal in order to solve this, however doing so could result in a larger chip because of the extra parts.

Suggest how can the floorplan be improved (automatically or manually) and discuss the tradeoffs.

We might arrange the memories closer to the chip's edges to optimize the design. This would put them in closer proximity to the ports, improving timing and chip area efficiency. We can cut down on the time and resources required to fix problems later by taking care of this early in the design phase. However, as there may not be enough room for routing and port buffers due to the high component density, placing these cells close to the ports could result in severe congestion. To balance better timing against the possibility of congestion, this tradeoff needs to be carefully considered.

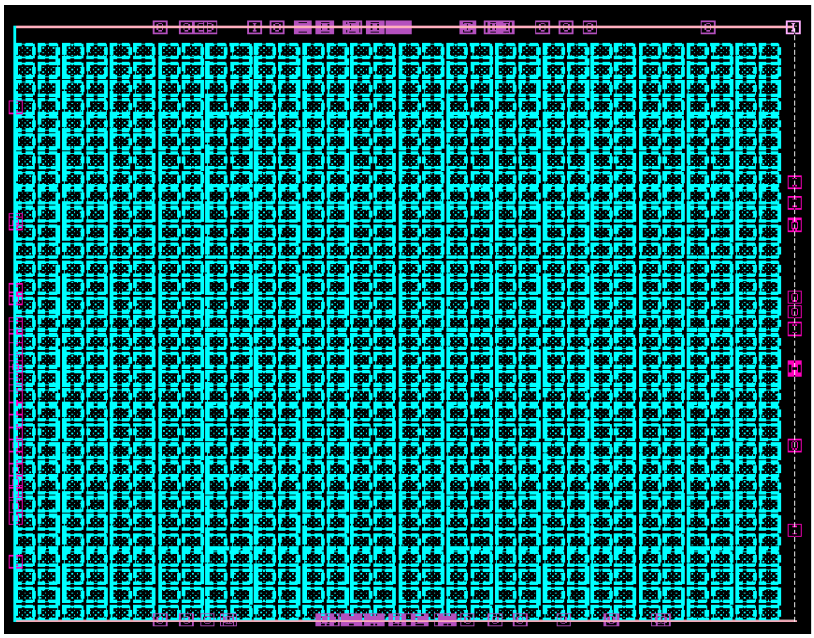
Furthermore, a clearly defined space for standard cells in the middle of the layout, surrounded by macros, may lessen congestion and bottlenecks. Pin accessibility would be enhanced by this arrangement, which would make greater use of blockages and allow for suitable spacing between macros. The difficulty, though, is in controlling a fixed-size region; shrinking the chip to satisfy design specifications may result in congestion problems, raise chip prices, and maybe affect profitability. Consequently, a hybrid strategy that balances manual and automated changes could maximize placement while taking these trade-offs into account.

Task 3

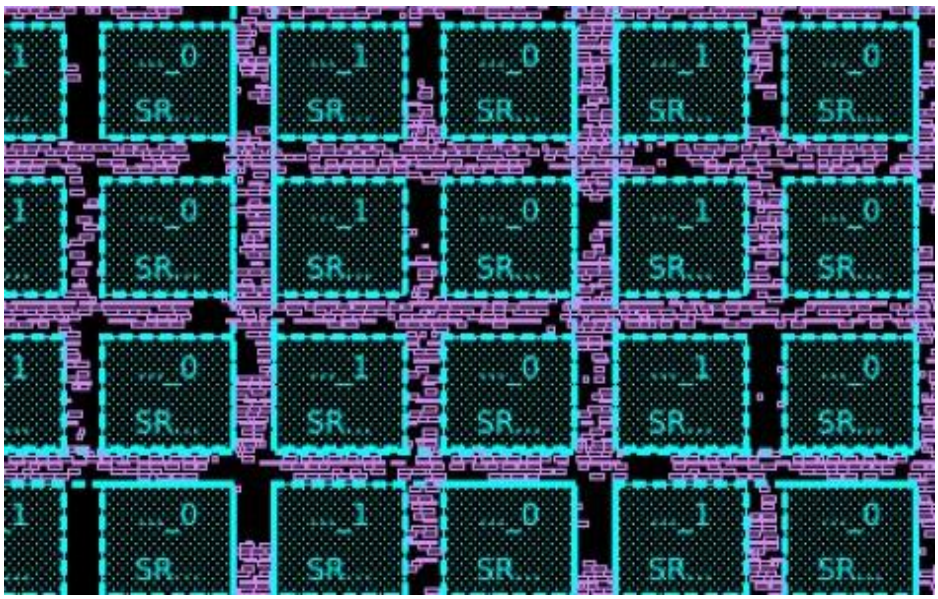
[#P3.2_Q1] For each of the three floorplan options submit:

Print screen of the layout with and without the congestion map. If needed take more than one print screen with a different zoom (F in keyboard might help) and remove from the object's view the objects that aren't necessary for the floorplan.

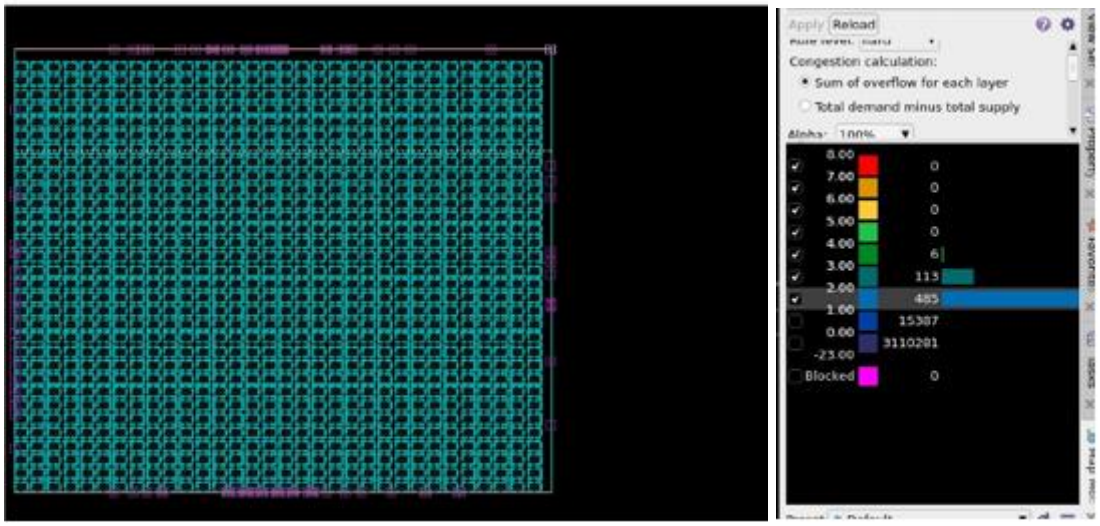
Layout without Congestion Map:



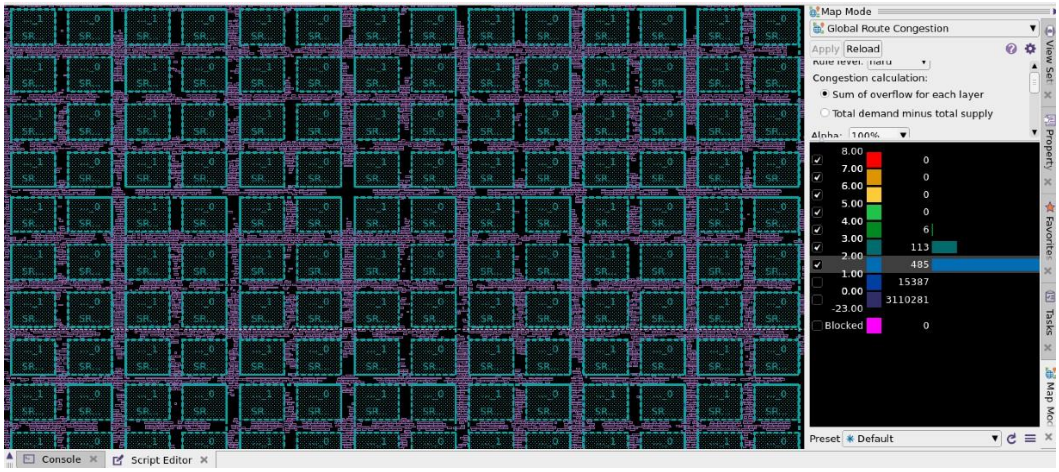
Layout zoom in to standard cells:



Layout with Congestion Map:



Layout zoom in to standard cells:



List the major pros and cons of the floorplan option.

Pros: Designers can regulate the size and density of macros by rearranging SRAMs into a matrix shape with unfixed spaces, which enables modifications dependent on silicon size limitations. This method allows for a structured and scalable layout, which is particularly useful when working with several identical sub-units, like arrays. Additionally, according to congestion maps, the design often exhibits low levels of congestion, with the exception of the areas close to the ports. Because rows and columns can easily added or removed to allow designers to change the design as needed, this structure also helps reduce wirelength, boosting power efficiency and scalability.

Cons: This approach does not, however, make use of complex algorithms that take into consideration variables like density, timing, and distances—all of which are critical for maximizing silicon area and circuit performance. Despite their flexibility, the unfixed spaces may result in high-density layouts that could jeopardize heat management and performance. Chip size is influenced by a variety of design limitations in real-world applications, and depending only on this method may make it challenging to satisfy timing and space requirements. Additionally, the matrix structure can create localized routing issues close to the ports, making it more difficult to efficiently balance area, speed, and performance.

Suggest how can the floorplan be improved (automatically or manually) and discuss the tradeoffs

This floorplan option can be improved by applying both manual adjustments and automated optimizations. Manually, we can focus on finding the optimal balance between size and the need for minimal delay while considering the density factor. Specifically, we can create a more elongated structure to avoid high density around critical areas such as ports, where congestion could negatively impact signal speed. Once the manual floorplan adjustments are

complete, automatic improvements can be introduced to further enhance performance. This could involve applying algorithms to improve signal transfer speed by, for example, strategically adding buffers. The process will involve several iterations, alternating between manual fine-tuning of the structure and automated optimizations to achieve the best balance of performance, area, and power efficiency. This approach allows for an iterative design process that progressively improves the floorplan based on real-time feedback, balancing density, timing, and congestion management.

Option 4: Divide and conquer

Pros: By splitting the design into 16 identical bit_top instances, this method makes use of secondary hierarchy, which facilitates and expedites the replication process. The bit_top level may be readily multiplied and abutted into rows after it is properly built, which minimizes design faults and increases accuracy while lowering manual labor. Additionally, engineers can save a lot of time and effort by concentrating on optimizing a single smaller block, freeing them up to invest in producing a higher-quality and more efficient design. In addition to providing better space utilization, the back-to-back row configuration permits the pooling of resources like Vdd and Vss lines, which helps to lessen congestion and any delays.

This approach's distinct hierarchical structure makes the design easier to handle by guaranteeing scalability and streamlining verification. Additionally, there is enough room for managing port connections and appropriate integration of different units in the space left between pairs of rows, such as between bit_top instances, which promotes seamless operation.

Cons:

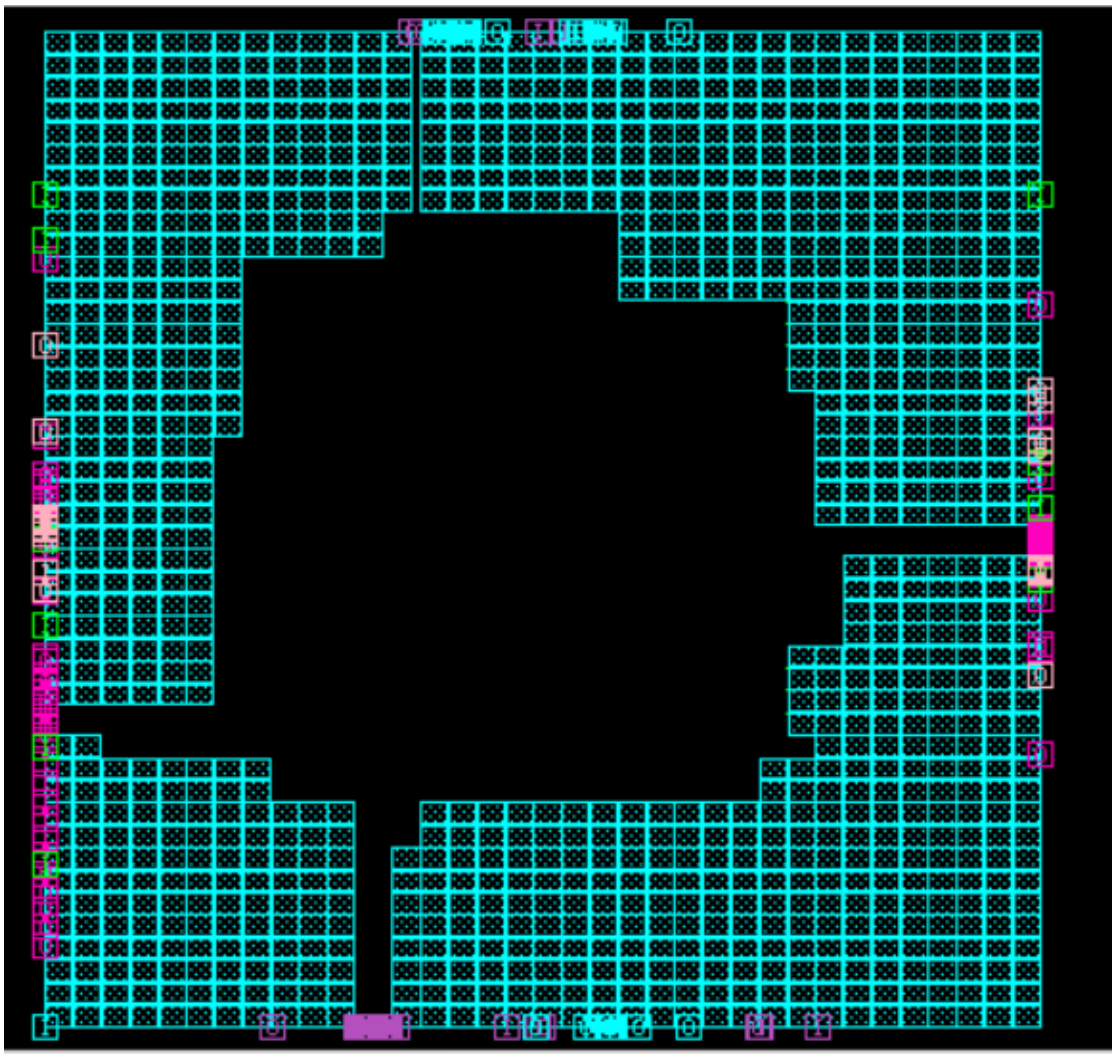
However, because it can only be used to designs with identical sub-units, this technique has limited utility. This approach loses its usefulness for increasingly complicated systems that need a variety of components. Furthermore, integrating replicated units might present other difficulties, such making sure that flipped or mirrored rows are connected correctly, which could cause timing and routing problems. Furthermore, manufacturers might restrict the arrangement of rows back-to-back in specific circumstances, which would make this arrangement unfeasible. Timing discrepancies could also arise from the mirrored design, especially in high-speed applications where even minor delays can have a big effect on performance. Therefore, even while this strategy has obvious advantages in terms of efficiency and space, it is not always practical and could add more complexity during the integration stage.

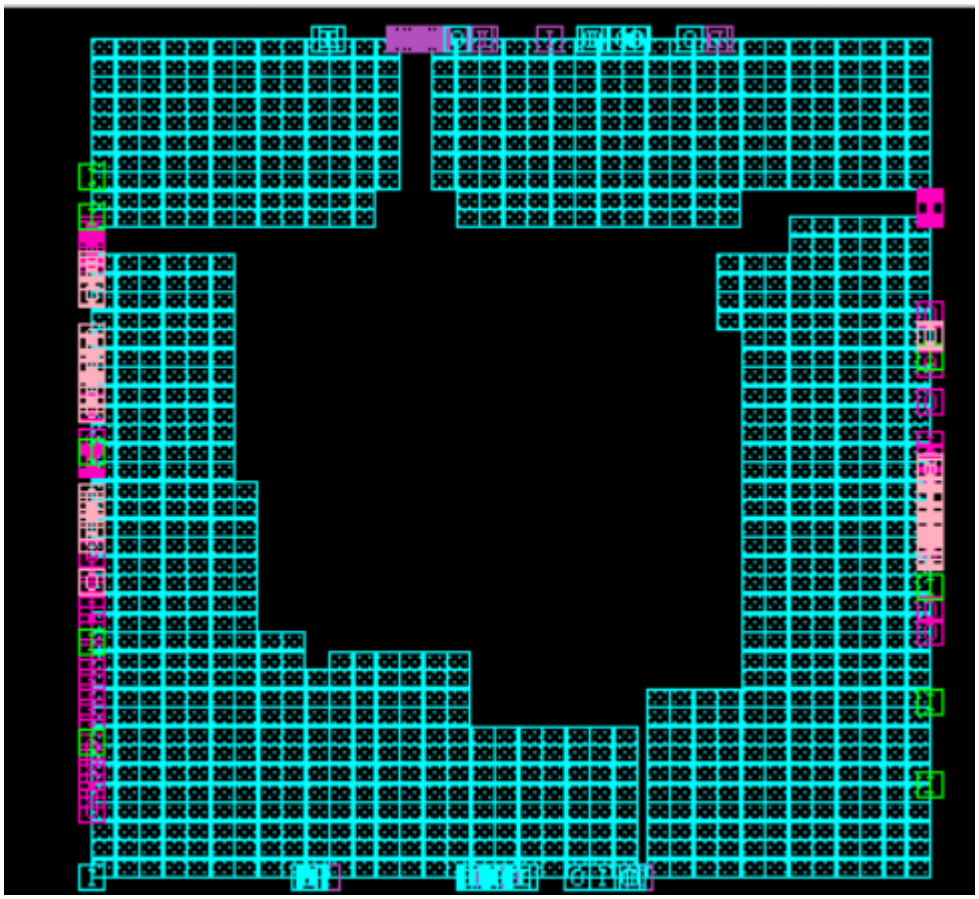
Choose the best floorplan option from those options and explain your decision.

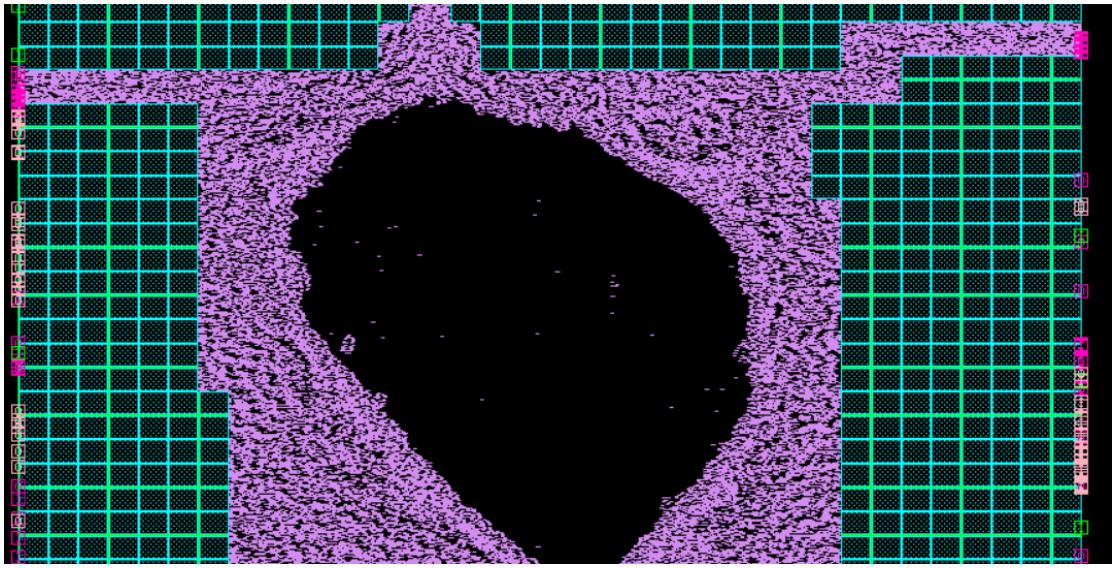
Option 4 is the best option for the floorplan. By breaking the design up into readily replicable smaller sub-units, Option 4 offers an organized, hierarchical approach that saves time and improves space efficiency by sharing resources

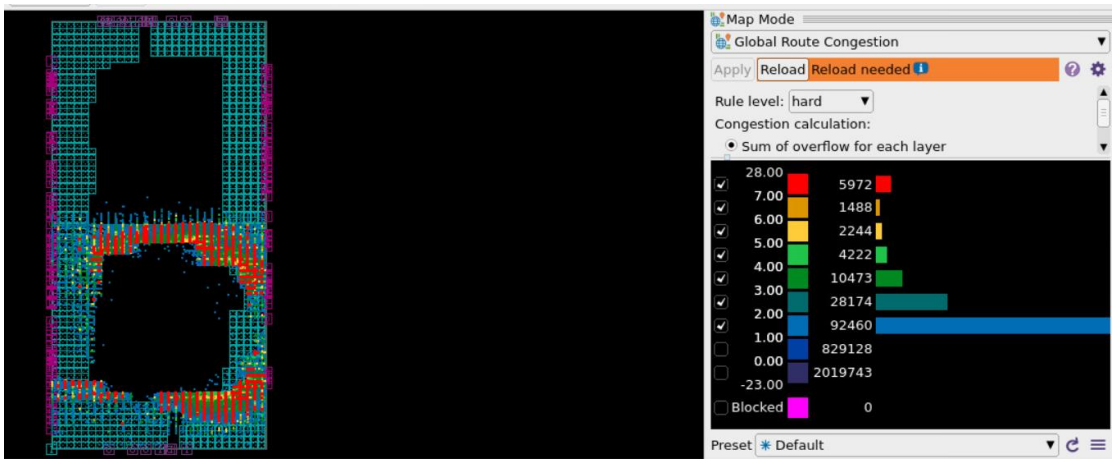
like Vdd and Vss lines efficiently. We can expedite the procedure and provide a more efficient and optimal floorplan that strikes a balance between structure, flexibility, and efficiency by utilizing Option 4's replication advantages.

appendix :





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Reload
Reload needed
Rule level:
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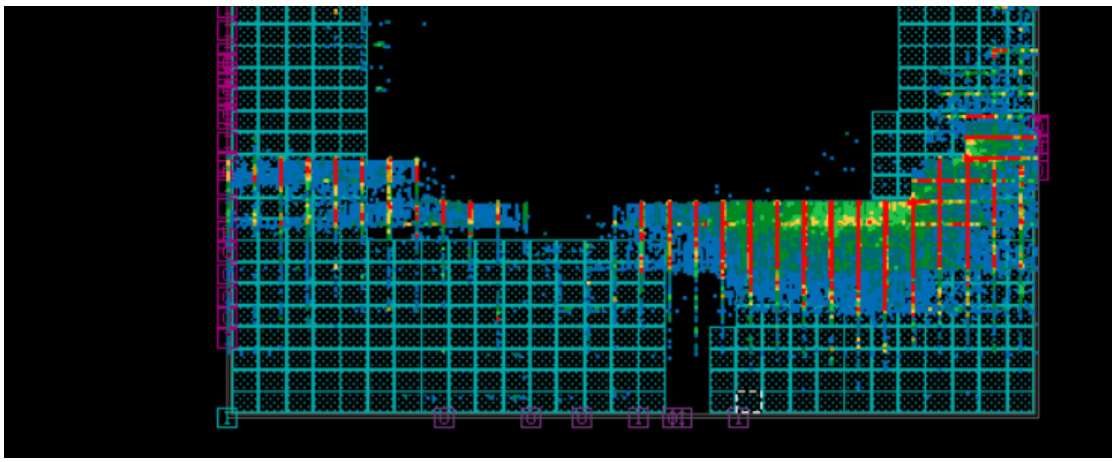

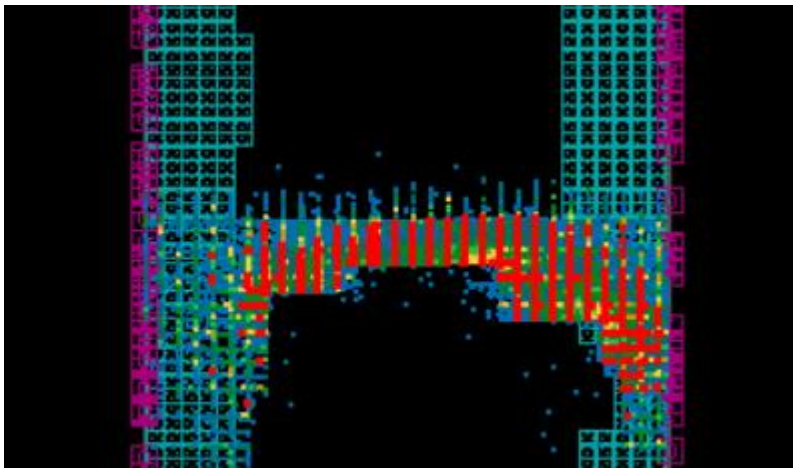

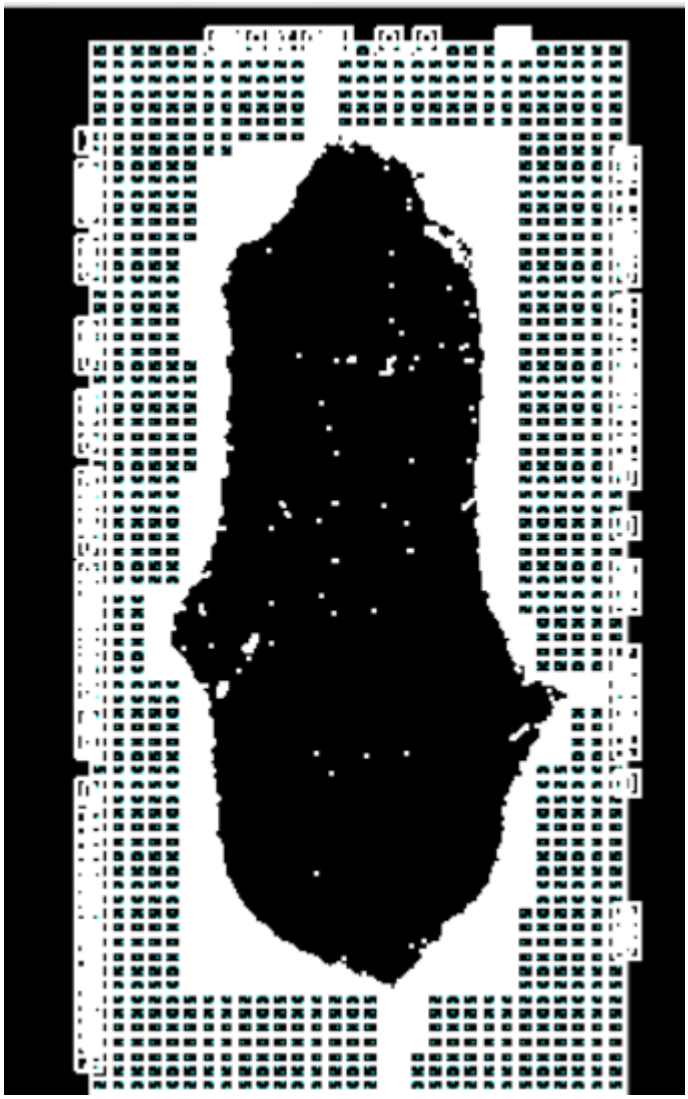

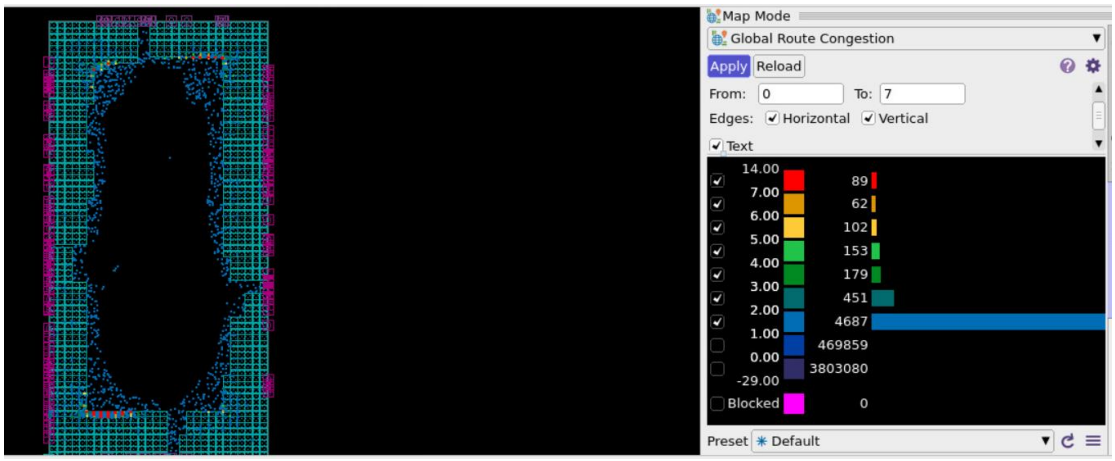
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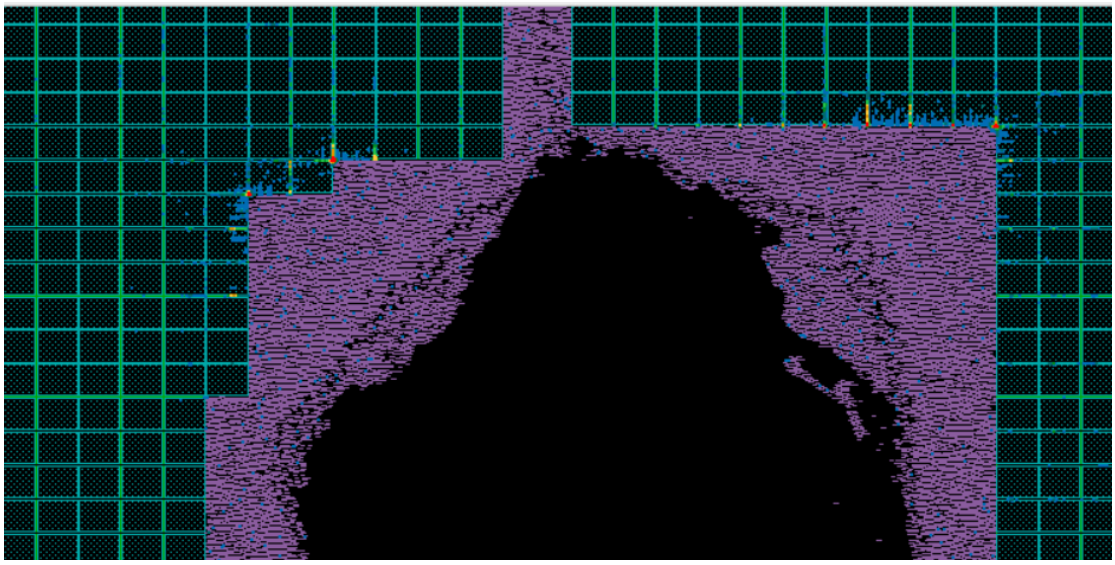

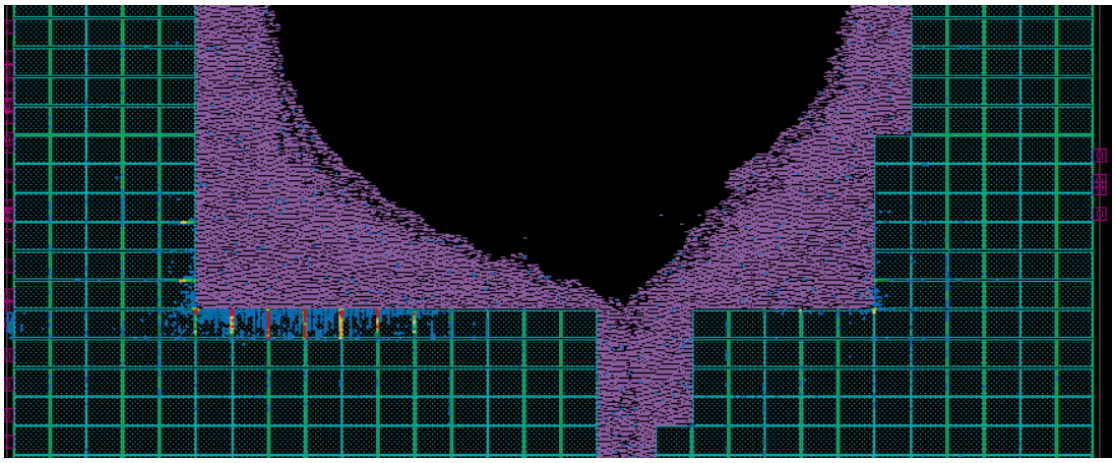

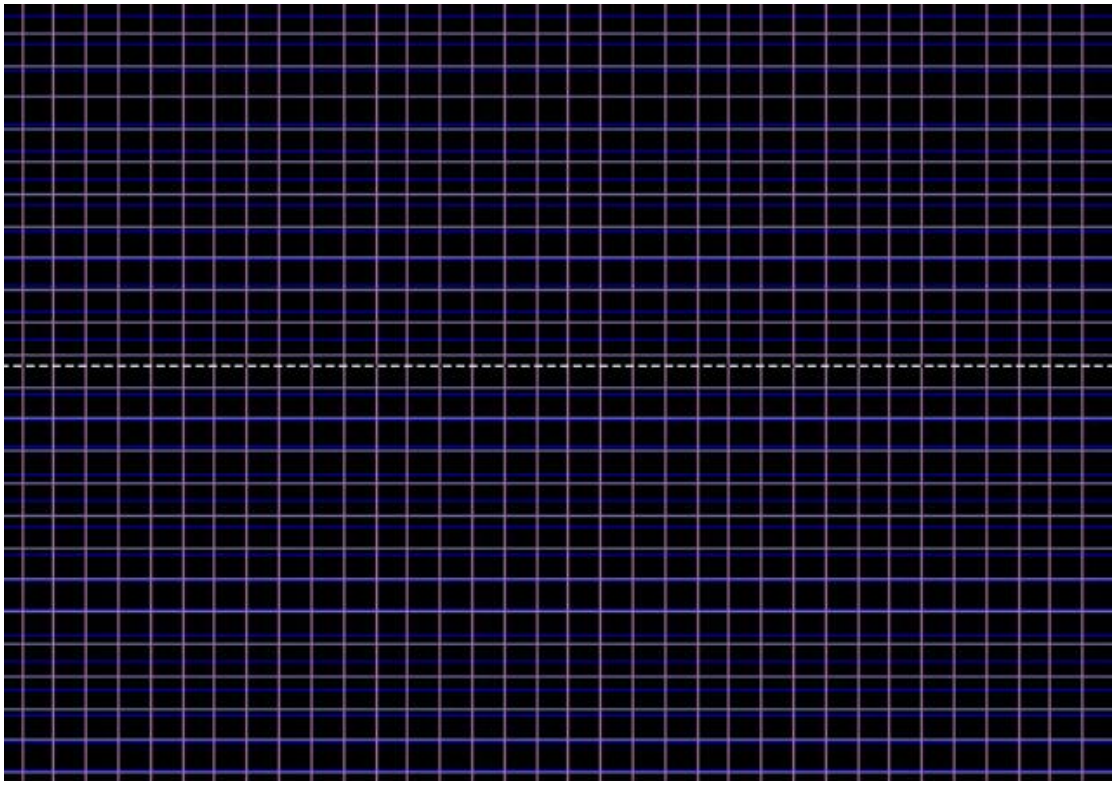

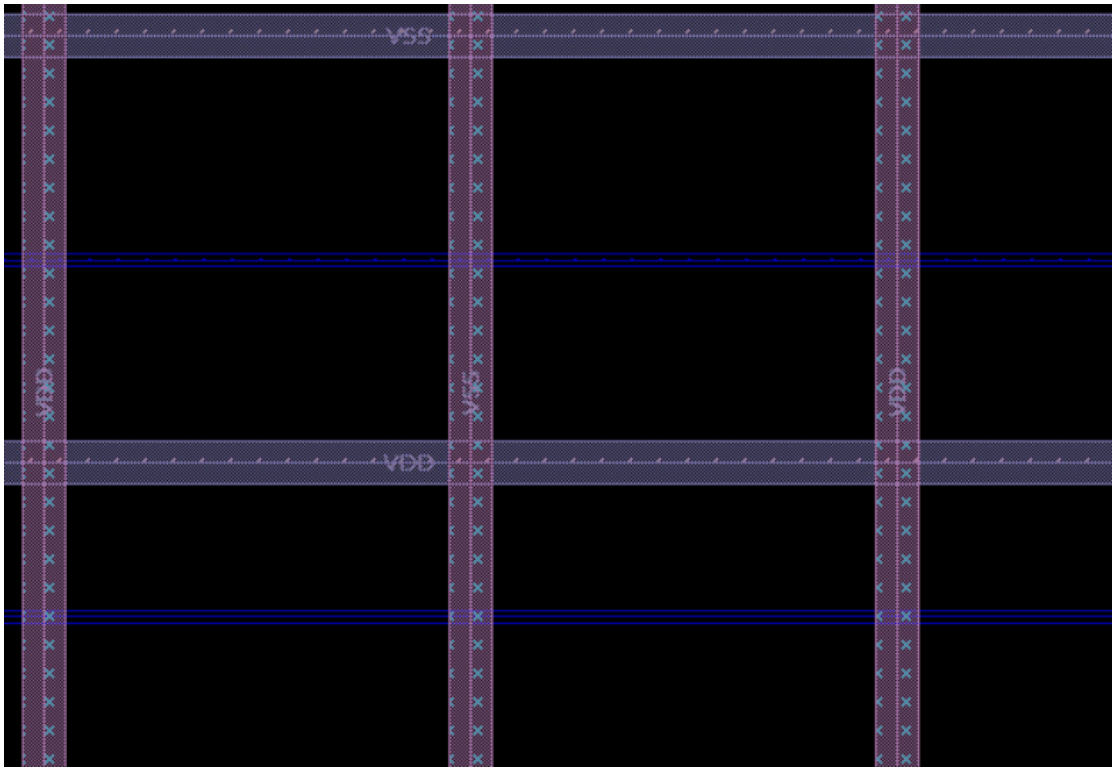
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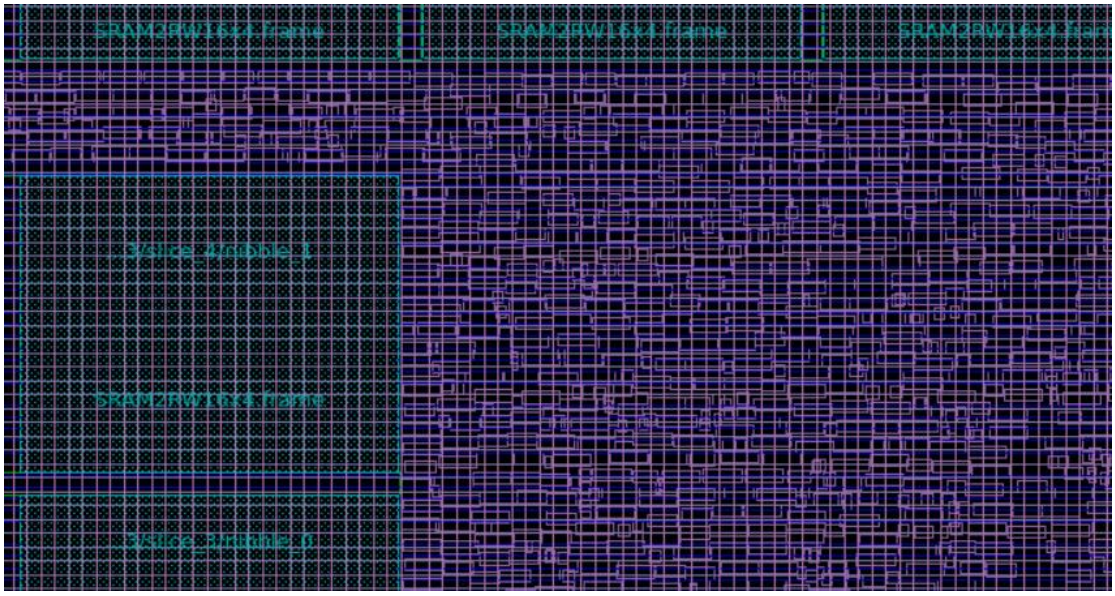
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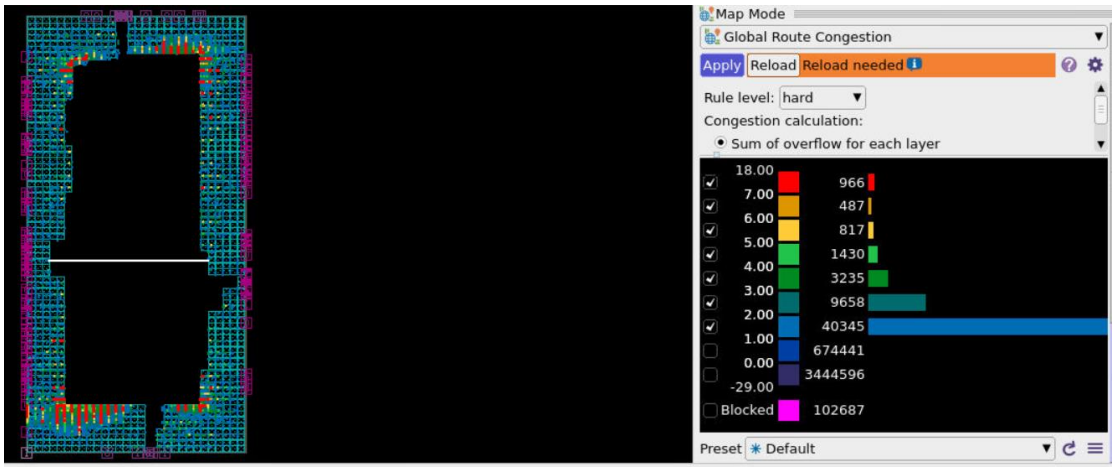
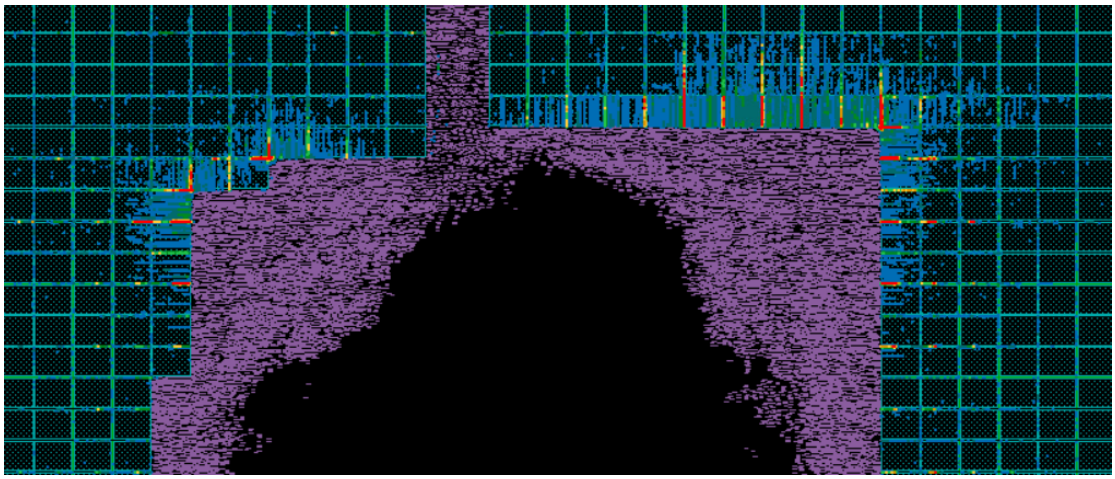
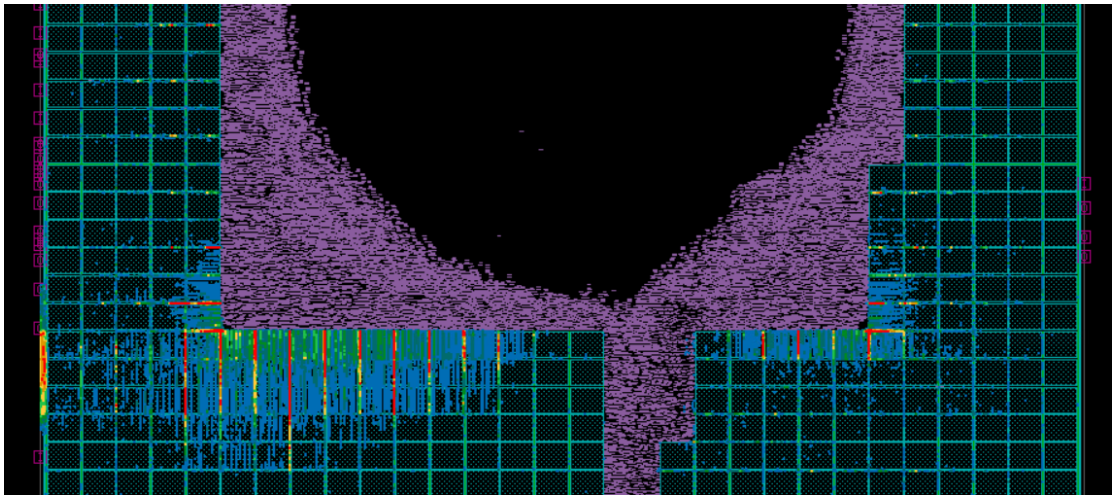
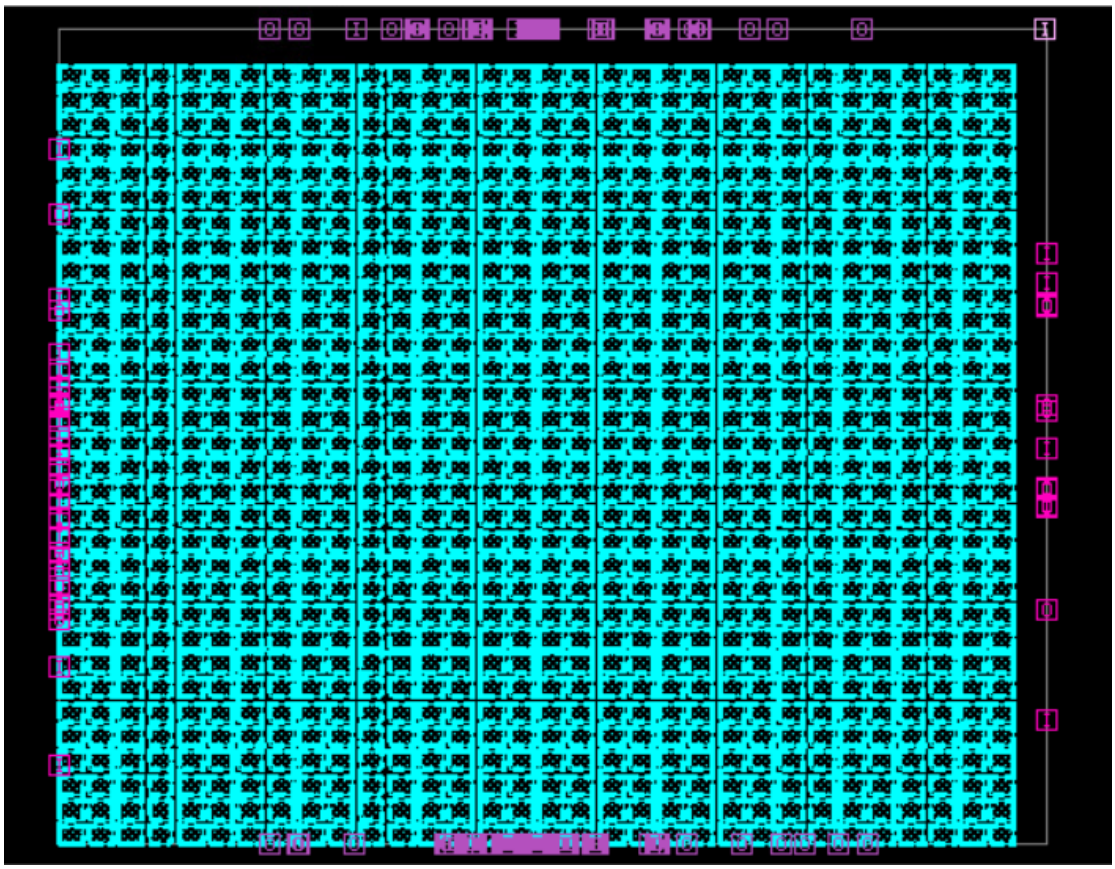
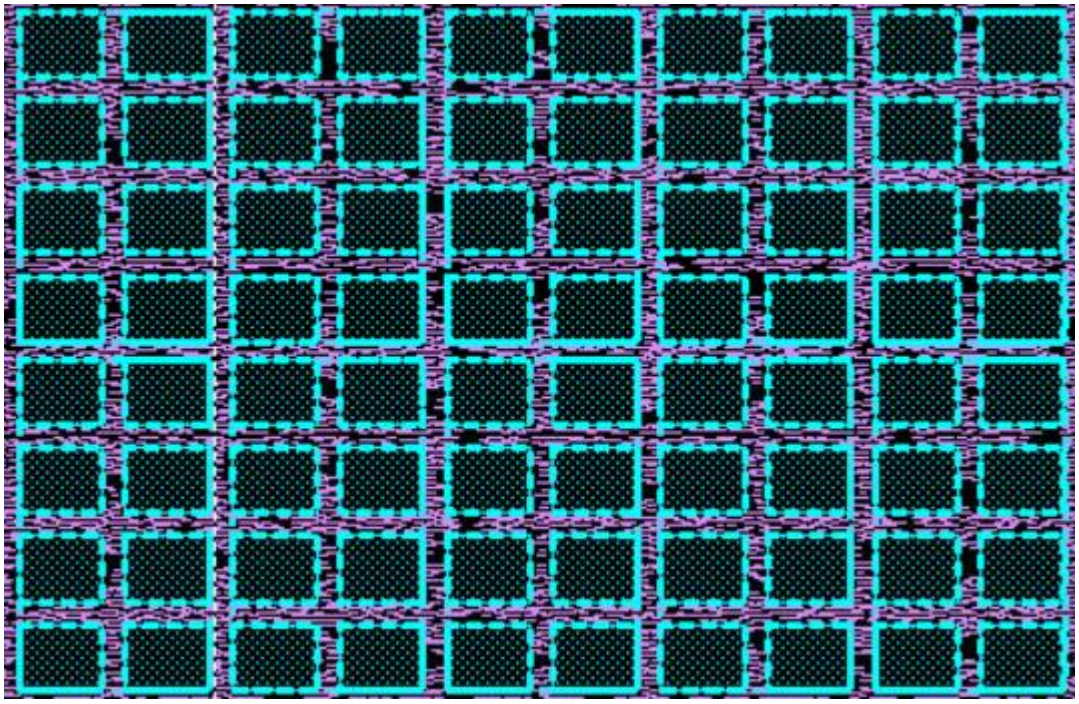
SRAM2RW16x4 frame
3slice_3nibble_0


Map Mode
Global Route Congestion
Apply
Reload
Reload needed
Rule level:
hard
Congestion calculation:
Sum of overflow for each layer
18.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
-29.00
Blocked
966
487
817
1430
3235
9658
40345
674441
3444596
102687
Preset
Default









Task 3 :