Advanced VLSI

Bitcoin

Stage 5 : CTS (Clock Tree Synthesis)

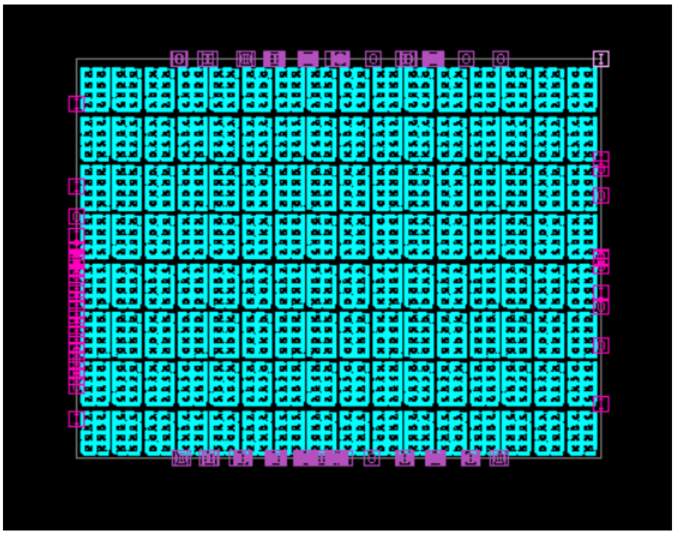
Ahmad foqara 322389982

Mohammad foqara 212193916

Neama hebi 212100705

Ward aboyonis 212021869

Work path: /project/advvlsi/users/ mohammadf1 /ws/bitcoin



[#P3.1_Q1] What is the main goal of CTS? in your answer also discuss classic CTS and CCD?

Clock Tree Synthesis (CTS) aims to minimize insertion latency and clock skew while effectively distributing the clock signal to all registers across a semiconductor. This prevents timing violations (setup or hold violations) and permits dependable and synchronized operation of the digital circuit by guaranteeing that the clock signal reaches all required components at almost the same time. Therefore, creating a balanced clock tree is the primary goal of conventional CTS. The clock signal is transported from the source to various flip-flops via the clock distribution network, which is organized like a tree.

A more recent and sophisticated approach known as CCD (Clock Concurrent Design) optimizes the clock tree while simultaneously incorporating other design components. CCD incorporates clock optimization with other design stages, including as placement and routing, rather than handling CTS as a stand-alone step. In order to improve the overall quality of the design, CCD aims to optimize power, timing, and area simultaneously with clock distribution.

To conclude:

	Classic CTS	CDD
Timing	Post-placement	alongside placement and routing
Focus	minimizing clock skew and insertion delay	Optimizes clock skew, insertion delay, power, area, and timing concurrently
Power and Area	Power and area optimizations are less effective	More power-efficient and area-optimized
Complexity	Simpler but potentially less optimal in terms of overall design	More complex, but with better overall design optimization

[#P3.1_Q2] What is the role of clock buffers in the CTS stage, and how are they optimized to meet design constraints?

Clock buffers are essential for guaranteeing that the clock signal is distributed correctly over the whole chip during the Clock Tree Synthesis (CTS) stage. Clock skew, clock delay, and signal integrity issues are addressed by carefully placing these buffers across the clock distribution network. To clarify, Clock Buffers play a number of roles in CTS, including: Amplification (improving the clock signal as it deteriorates with distance), Skew Reduction (ensuring that the clock arrives across the chip simultaneously to prevent synchronization problems), Latency Management (regulating the delay from the clock source to the clocked elements), Load Balancing (equalizing the load across the clock tree to preserve signal integrity), and Power Control (reducing the clock network's power consumption).

Timing, power, and space limits are all taken into consideration when optimizing clock buffers. These optimizations include: clock gating—integrating gating to reduce power by turning off unused clock signals; parasitic management—taking into account wire capacitance and resistance; delay balancing—aligning signal delays across various clock tree parts; buffer sizing—adjusting size based on load to balance power and performance; buffer insertion—placing buffers strategically to reduce skew and latency using algorithms; and Optimizing across several operating situations to guarantee that time is satisfied is known as multi-corner optimization.

[#P3.1_Q3] Explain the following concepts: Skew - global and local, Jitter, PLL.

Skew: The variation in the clock arrival time between two distinct registers. Global skew, which is the greatest skew between two distant registers on the chip, is more noticeable in large systems with lengthy interconnects and has a direct impact on the system's overall synchronization. The maximum skew between two close registers that communicate with one another (not between all the registers) is known as local skew. It is usually less than global skew, but improper management can still result in timing problems.

Jitter: The variation in clock time between cycles. Stated differently, it describes how the clock signal's timing deviates from its ideal periodicity. It is possible for the clock edges to move slightly over time rather than arriving at precisely predicted intervals.

PPL: A control system known as a Phase-Locked Loop (PLL) compares its output to a reference clock and makes adjustments to produce a clock signal with a particular frequency and phase. Even though they frequently have different frequencies, the PLL makes sure that the output clock and reference clock are in synchronization.

[#P3.1_Q4] We discussed during the lecture about several approaches for clock trees. Choose one, describe it and explain its pros and cons (like mesh …)

In CTS, an H-tree is a symmetric, hierarchical routing structure that disperses clock signals uniformly throughout a chip. The clock signal travels the same distances to each terminal thanks to the symmetric construction of the H-tree. The clock signal splits at the "H"'s center at each level and keeps moving outward in both directions. The building process is recursive. The clock signal splits into a "H" form at each intersection of the "H," then advances to the next level.

Advantages:

1**. Symmetry and Skew Reduction**: Because the clock pathways to the various chip components are of equal length, the symmetric and balanced design of the H-tree helps reduce clock skew. This guarantees that the clock signal reaches every endpoint at the same time.

2. **Predictability**: Better control over timing and skew is possible due to the regular and hierarchical structure, which makes it easier to forecast when the clock signal will occur.

3. **Scalability**: Because H-tree structures may be recursively split into multiple branches to accommodate more clock destinations, they are scalable and suitable for both small and big systems.

4. **Low Placement Complexity**: The clock network's design and placement are made simpler by its organized nature. Tools find it easier to balance and optimize the tree because of its regular structure.

disadvantages :

1**. Long Wire Lengths**: In big designs, an H-tree network may have long wire lengths. increased RC (resistance-capacitance) delays caused by these longer cables may result in increased clock latency and power usage.

2. **High Power Consumption**: In areas of the semiconductor where the clock signal may not always be required, the consistent clock signal distribution across the tree may result in needless power consumption. For designs that are power-sensitive, this is especially problematic.

3. **Limited Flexibility:** The H-tree's symmetrical and rigid construction limits its ability to handle irregular or non-uniform designs, where various chip components may

need different skew requirements or clock frequencies. In some situations, the standard structure might not always work well.

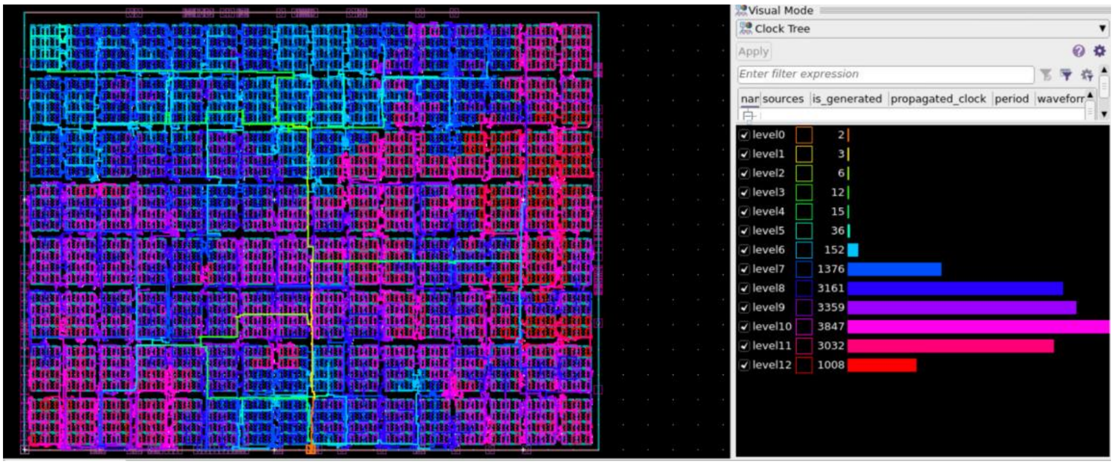
4. **Routing Congestion**: The H-tree structure's numerous wires can lead to routing congestion in intricate designs, particularly when the clock signal must pass through dense logical areas.

### [#P3.1_Q5] What are shielding and spacing techniques regarding the CTS stage?

Both strategies help to maintain the integrity of the clock signal and lessen crosstalk issues between signal lines, which can result in clock signal delays.
Clock nets are shielded against crosstalk, or noise produced by adjacent signal lines, by encircling them with grounded or power-connected metal wires. This reduces signal distortion by forming a barrier that either reflects or absorbs interference.
Conversely, spacing reduces the capacitive coupling and further reduces crosstalk by physically extending the distance between clock nets and neighboring signal lines. improving the integrity of the signal.

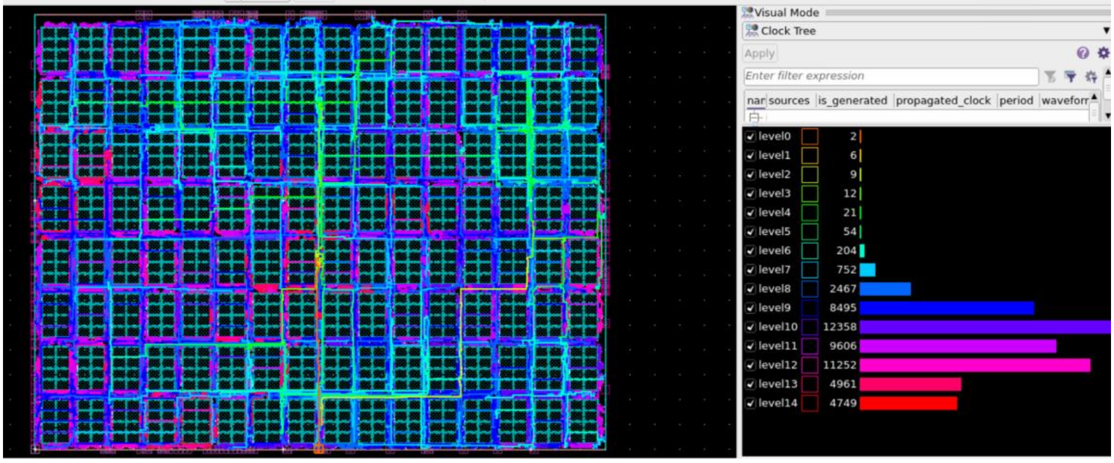
### [#P3.2_Q1] Attach a print screen of the clock tree distribution

HCLK:



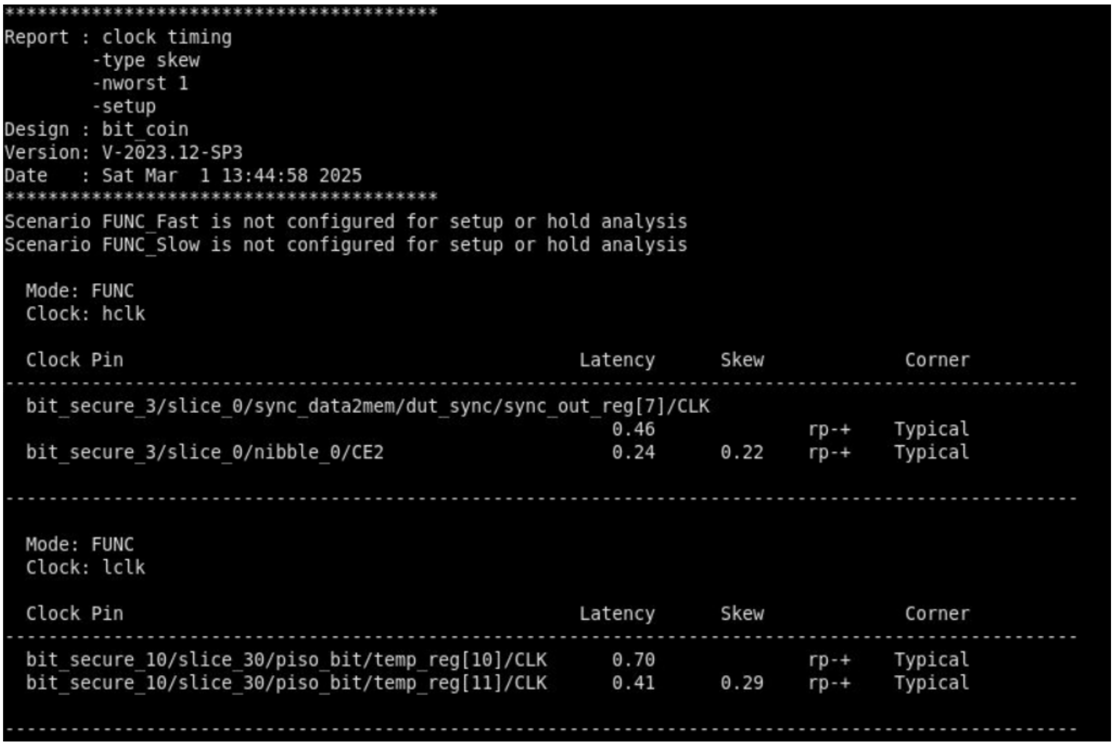
☑ level0	2
☑ level1	3
☑ level2	6
☑ level3	12
☑ level4	15
☑ level5	36
☑ level6	152
☑ level7	1376
☑ level8	3161
☑ level9	3359
☑ level10	3847
☑ level11	3032
☑ level12	1008

LCLK:



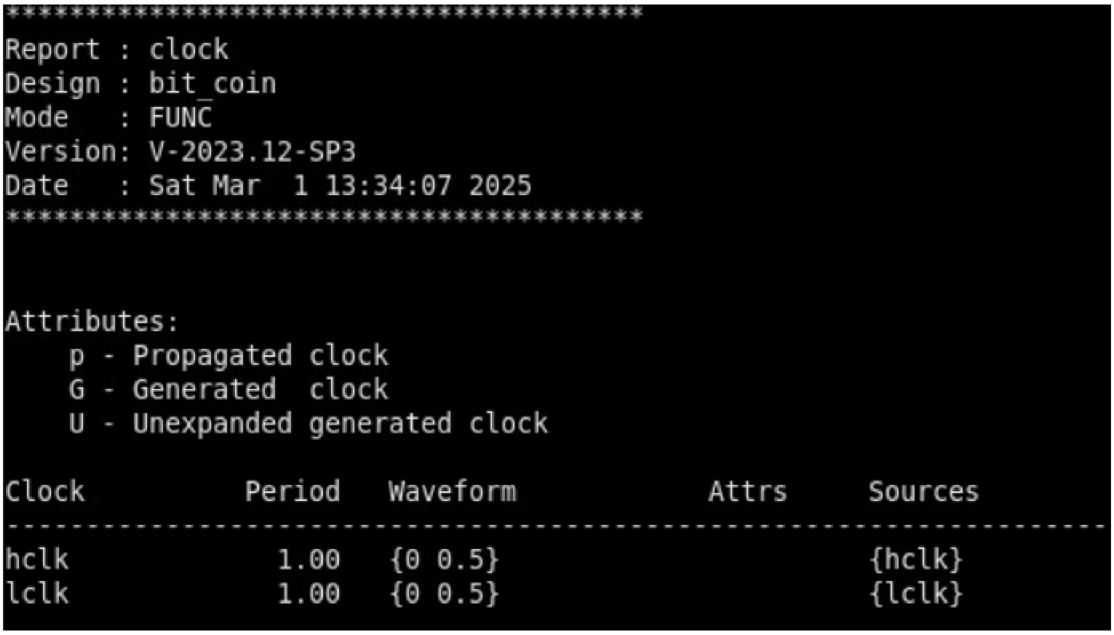
☑ level0	2
☑ level1	6
☑ level2	9
☑ level3	12
☑ level4	21
☑ level5	54
☑ level6	204
☑ level7	752
☑ level8	2467
☑ level9	8495
☑ level10	12358
☑ level11	9606
☑ level12	11252
☑ level13	4961
☑ level14	4749

[#P3.2_Q2] What is the skew of lclk and hclk? Is it high or low in your opinion?



```
****************************************
Report : clock timing
        -type skew
        -nworst 1
        -setup
Design : bit_coin
Version: V-2023.12-SP3
Date   : Sat Mar  1 13:44:58 2025
****************************************
Scenario FUNC_Fast is not configured for setup or hold analysis
Scenario FUNC_Slow is not configured for setup or hold analysis

  Mode: FUNC
  Clock: hclk

  Clock Pin                                   Latency      Skew           Corner
-------------------------------------------------------------------------------------
  bit_secure_3/slice_0/sync_data2mem/dut_sync/sync_out_reg[7]/CLK
                                                 0.46              rp-+    Typical
  bit_secure_3/slice_0/nibble_0/CE2               0.24      0.22    rp-+    Typical

-------------------------------------------------------------------------------------

  Mode: FUNC
  Clock: lclk

  Clock Pin                                   Latency      Skew           Corner
-------------------------------------------------------------------------------------
  bit_secure_10/slice_30/piso_bit/temp_reg[10]/CLK      0.70              rp-+    Typical
  bit_secure_10/slice_30/piso_bit/temp_reg[11]/CLK      0.41      0.29    rp-+    Typical

-------------------------------------------------------------------------------------
```

From the report we can see that the skew for HCLK is 0.22 and for LCLK is 0.29.

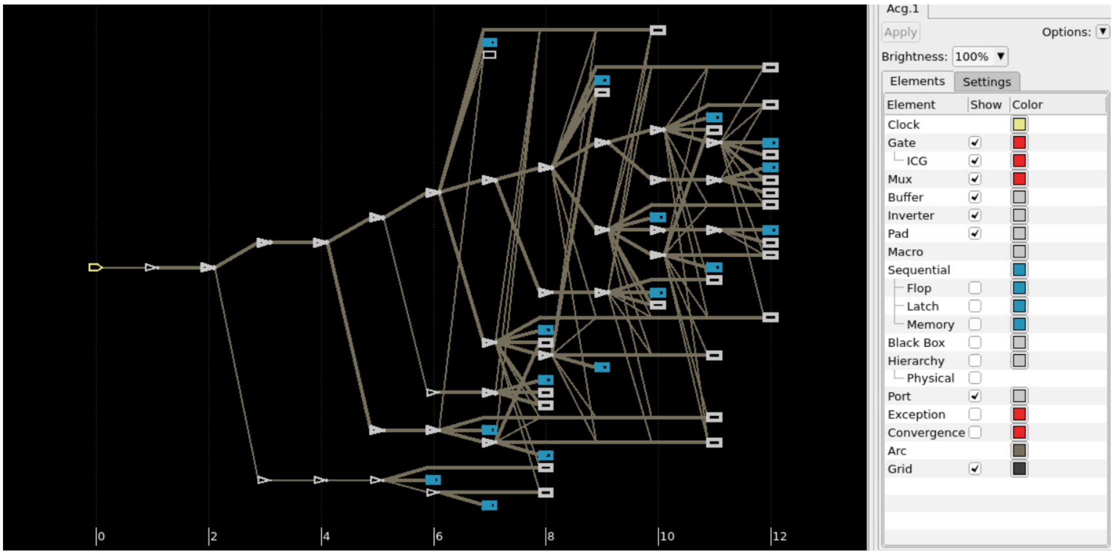


```
****************************************
Report : clock
Design : bit_coin
Mode   : FUNC
Version: V-2023.12-SP3
Date   : Sat Mar  1 13:34:07 2025
****************************************


Attributes:
    p - Propagated clock
    G - Generated  clock
    U - Unexpanded generated clock

Clock          Period   Waveform            Attrs     Sources
--------------------------------------------------------------------
hclk             1.00   {0 0.5}                       {hclk}
lclk             1.00   {0 0.5}                       {lclk}
```

The clock period for both clocks is 1.00, thus we can conclude that the skew for both clocks is high because they are both higher than 20% of the clock period. The skew for both clocks is 22% and 29% of the clock period, respectively. We want to reduce the skew as much as possible without violating setup or hold, however a skew of more than 20% is regarded as high.

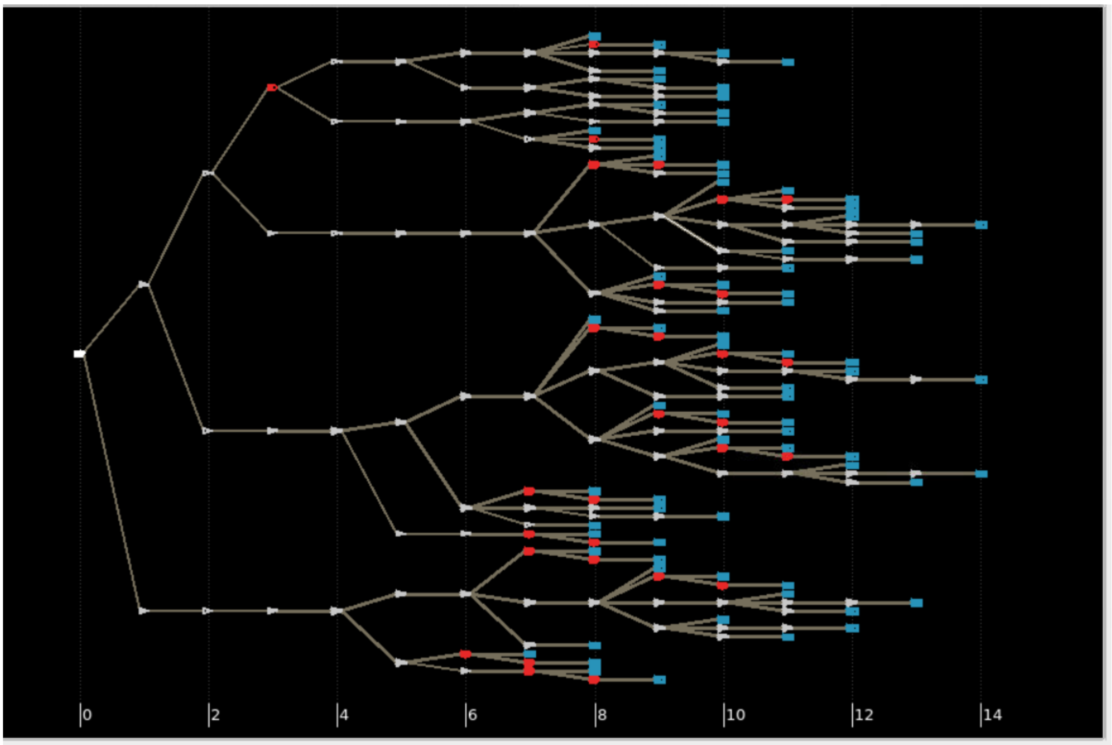
### [#P3.2_Q3] Attach a print screen of each clock (lclk and hclk).

HCLK:



Element	Show	Color
Clock		🟨
Gate	☑	🟥
└ICG	☑	🟥
Mux	☑	🟥
Buffer	☑	⬜
Inverter	☑	⬜
Pad	☑	⬜
Macro		⬜
Sequential		🟦
├Flop	□	🟦
├Latch	□	🟦
└Memory	□	🟦
Black Box	□	⬜
Hierarchy	□	⬜
└Physical	□	
Port	☑	⬜
Exception	□	🟥
Convergence	□	🟥
Arc		🟫
Grid	☑	⬛

LCLK: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