FA95/VA95
NAND Chip Supported
Application Note
V1.0

Support Chips:
W55FA95 Series

Support Platforms:
Non-OS

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1. General Description

FA95/VA95 provides all required elements to support NAND-type flash access. It includes Storage Interface Controller (SIC), Internal Boot ROM (IBR) driver for NAND flash, and SIC driver for NAND flash.

The **Storage Interface Controller (SIC)** is a subsystem within FA95/VA95 chip. It provides an interface for NAND flash access. This interface include all required signals for NAND flash chip such R/–B, –CS, CLE, ALE, –WE, –RE and 8 data pins.

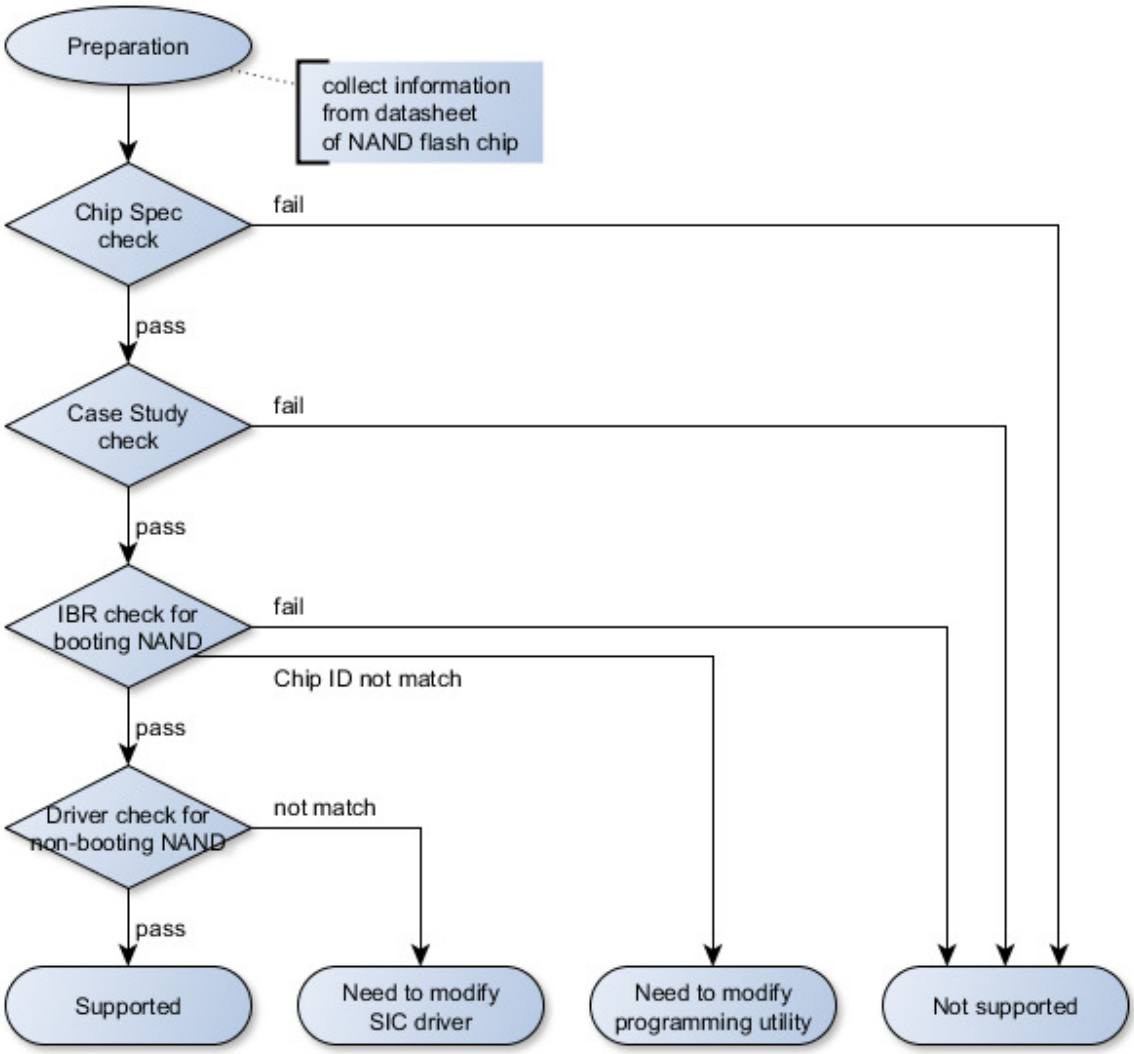
The **Internal Boot ROM (IBR)** that build-in FA95/VA95 chip includes the boot code to boot up system. It is the first executing code to initial FA95/VA95 chip when power on. After chip initiated, IBR will load the next stage booting code that located at NAND flash chip or other storage and then hand over the chip controlling right to them. If the next stage booting code locates at NAND flash chip, you MUST choose a NAND flash chip that IBR supported. Since the IBR is build-in FA95/VA95 chip, it is impossible to modify IBR. If IBR don't support a NAND flash chip, there are two ways to make it work with IBR. First, we can modify the NAND chip programming utility, such as TurboWriter or NANDWriter, to write booting code into NAND chip with special format that IBR can recognized. Second, we can use Power-On-Setting for NAND page size to force IBR to use correct read command to read data in NAND chip. Else, you have to choose another NAND chip that IBR supported.

We also provides SIC driver to support many types of NAND flash chip after system boot up. It is pure software and allowed to modify to support more types of NAND flash chip. If the NAND flash chip you prefer to use is not for booting, we can modify SIC driver to support it.

However, FA95/VA95 cannot support all types of NAND flash chips since not all of them support same standard. This document help you to judge whether the NAND flash chip you preferred supported by FA95/VA95 or not, and judge whether we need to modify software or utility to support it.

2. Step by Step Checking

Please follow the flowchart at below to judge whether a NAND flash chip supported by FA95/VA95 or not. The detail information about each step in flowchart will be described at following sections.



2.1. Preparation

The first step is to collect NAND flash chip information from its datasheet. The following information is necessary.

- The pin assignment for NAND flash chip
- The information about NAND flash capacity

Item	Description	Value for example
Chip ID	Each NAND flash chip contains a specific product identification to identify itself. It is 4 or 5 bytes length hexadecimal number.	0xAD 0xF1 0x00 0x1D
Bus width	The width of I/O interfaces for both data and address.	8-bit / 16-bit
Page size	The byte number for a page that don't include spare area.	512 / 2K / 4K / 8K
Spare area size	The byte number for the spare area in page.	16 / 64 / 128 / 256
Page number per block	The page number for a block.	32 / 64 / 128
Block number	The block number for whole NAND flash chip.	1024 / 2048 / 4096

NOTE: In this document, 1K = 1024, 2K = 2048, 4K = 4096, 8K = 8192, and 16K = 16384.

- The command set for some basic NAND access functions.

Basic Function	Description	Commands for example	
Read ID	To read Chip ID	0x90	--
Read Page	To read a page of data from NAND chip	0x00	0x30
Read Spare Area	To read spare area data from page in NAND chip (for page size 512 NAND chip only)	0x50	--
Write Page	To write a page of data to NAND chip	0x80	0x10
Erase Block	To erase a block	0x60	0xD0
Read Status	To read the status register from NAND chip to find out whether read, write or erase operation is completed, and whether the write or erase operation is completed successfully.	0x70	--
Reset	To abort the current command and reset chip to ready for next command.	0xFF	--

2.2. Chip Specification Checking

It focuses on hardware compatibility between FA95/VA95 and NAND flash chip for the chip specification checking. Following table is some critical items that FA95/VA95 supported. Please make sure they are matched with NAND flash chip.

Item	FA95/VA95 Supported
Page Size	512 / 2K / 4K / 8K bytes only
Bus Width	8 bits only
NAND Flash Type	Both SLC and MLC
ECC Algorithm	BCH 4 / 8 / 12 / 15 / 24 bits only

The pin assignment of FA95/VA95 is as below.

Name	Description	I/O Direction	Note
CS0	Chip Select 0 for first NAND chip	Output	Low activity
CS1	Chip Select 1 for second NAND chip	Output	Low activity
ALE	Address Latch Enable	Output	High activity
CLE	Command Latch Enable	Output	High activity
R/B0	Ready/Busy 0 for first NAND chip	Input	Low for Busy
R/B1	Ready/Busy 1 for second NAND chip	Input	Low for Busy
RE	Read Enable	Output	Low activity
WE	Write Enable	Output	Low activity
DATA0	Data Line 0 (bit 0)	Input / Output	Bus width is 8-bit
DATA1	Data Line 1 (bit 1)	Input / Output	
DATA2	Data Line 2 (bit 2)	Input / Output	
DATA3	Data Line 3 (bit 3)	Input / Output	
DATA4	Data Line 4 (bit 4)	Input / Output	
DATA5	Data Line 5 (bit 5)	Input / Output	
DATA6	Data Line 6 (bit 6)	Input / Output	
DATA7	Data Line 7 (bit 7)	Input / Output	

NOTE:

1. FA95/VA95 don't provide Write Protect (WP) pin. It is not necessary for basic NAND flash access function.
2. CS (Chip Select) pin sometimes called CE (Chip Enable).

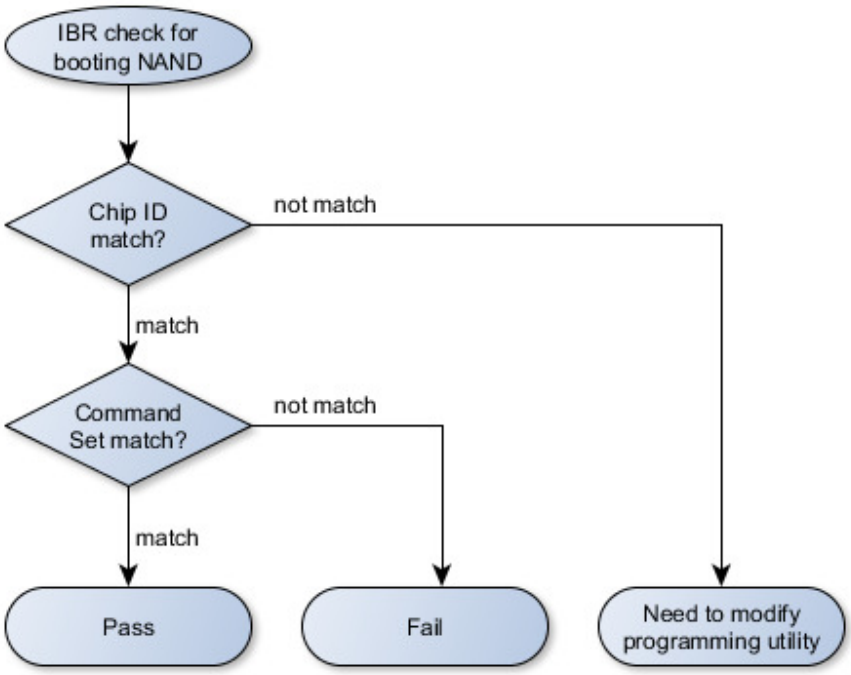
More detail hardware specification such as voltage and timing please refer to the datasheet of FA95/VA95.

2.3. Case Study Checking

Sometimes, the NAND flash chip cannot work fine with FA95/VA95 because of some special reasons. We had collected some case study in Chapter 4 for your reference. Please check whether you have similar requests or problems within these cases.

2.4. IBR Checking for Booting NAND Chip

The IBR is build-in FA95/VA95 chip and cannot be modified. If the NAND flash chip you prefer to use is for booting, you should choose a NAND flash chip that IBR supported. Please do following checking to judge whether IBR support your NAND flash chip or not.



2.4.1. Chip ID Checking

The IBR just support NAND flash chip with following Chip ID. Please search the following table to find out an entry that matches up your NAND flash chip. If you cannot found it, we need to modify the NAND chip programming utility, such as TurboWriter or NANDWriter, to write booting code into NAND chip with special format that IBR can recognized. Else, you have to choose another NAND chip that IBR supported.

Chip ID				Page size	Page number per block
ID [0]	ID [1]	ID [2]	ID [3]		
--	0x5A	--	--	512	32
--	0x6B	--	--	512	16
--	0x71	--	--	512	32
--	0x73	--	--	512	32
--	0x75	--	--	512	32
--	0x76	--	--	512	32
--	0x79	--	--	512	32
--	0xA1	--	--	2K	64
--	0xD1	--	--	2K	64
--	0xD3	--	ID[3]&0x33 == 0x11	2K	64
--		--	ID[3]&0x33 == 0x21	2K	128
--		--	ID[3]&0x33 == 0x32	4K	128
--		--	ID[3]&0x03 == 0x03	8K	128
--	0xD5	--	ID[3]&0x33 == 0x11	2K	64
--		--	ID[3]&0x33 == 0x21	2K	128
--		--	ID[3]&0x33 == 0x32	4K	128
--		--	ID[3]&0x03 == 0x03	8K	128
--	0xDA	--	ID[3]&0x33 == 0x11	2K	64
--		--	ID[3]&0x33 == 0x21	2K	128
--	0xDC	--	ID[3]&0x33 == 0x11	2K	64
--		--	ID[3]&0x33 == 0x21	2K	128
--	0xE3	--	--	512	16
--	0xE5	--	--	512	16
--	0xE6	--	--	512	16

Chip ID				Page size	Page number per block
ID [0]	ID [1]	ID [2]	ID [3]		
--	0xF1	--	--	2K	64
0xAD	--	0x94	0x25	4K	128
0xAD	--	0x94	0x9A	8K	256

NOTE:

1. The ID[0] is the byte read at first cycle and means Manufacture Code. The ID[1] is the byte read at second cycle and means Device Code.
2. ID[3] & 0x33 means do bit-wise AND operation for ID[3] and 0x33. For example, if ID[3] = 0x25, ID[3] & 0x33 = 0x25 & 0x33 = 0x021.
3. If NAND Chip ID is not in the table, IBR will regards it as 512 page NAND Chip.

2.4.2. Command Set Checking

The IBR just support NAND flash chip with following command set for each basic function. Please search the following table to find out an entry that matches up your NAND flash chip. If you cannot found it, the IBR don't support your NAND flash chip.

Since the IBR only read NAND flash content, so it does not check other commands such as write page or erase block.

Some commands differ between 512 bytes page and larger page NAND flash chip. Please search correct table according to the page size of your NAND flash chip.

For NAND flash chip that page size is **512 bytes**:

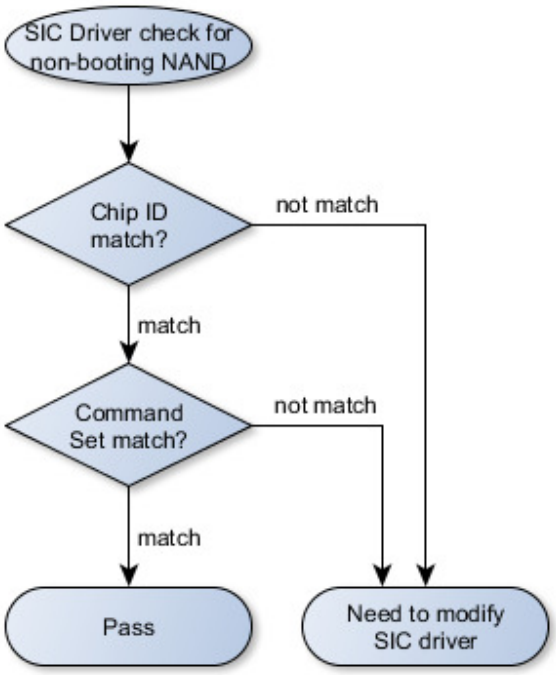
Basic Function	Description	Commands	
Read ID	To read Chip ID	0x90	--
Read Page	To read a page of data from NAND chip	0x00	--
Read Spare Area	To read spare area data from page in NAND chip	0x50	--
Reset	To abort the current command and reset chip to ready for next command.	0xFF	--

For NAND flash chip that page size **equal or larger than 2K bytes**:

Basic Function	Description	Commands	
Read ID	To read Chip ID	0x90	--
Read Page	To read a page of data from NAND chip	0x00	0x30
Reset	To abort the current command and reset chip to ready for next command.	0xFF	--

2.5. SIC Driver Checking for Non-Booting NAND Chip

The SIC driver is a pure software and allowed to modify to support more types of NAND flash chip. If the NAND flash chip you prefer to use is not for booting, we can modify SIC driver to support it. Please do following checking to judge whether current SIC driver support your NAND flash chip or not.



2.5.1. Chip ID Checking

The current SIC driver just support NAND flash chip with following Chip ID. Please search the following table to find out an entry that matches up your NAND flash chip. If you cannot found it, the current SIC driver could not yet support your NAND flash chip.

Chip ID				Page size	Page number per block	Block number
ID [0]	ID [1]	ID [2]	ID [3]			
--	0x5A	--	--	512	32	4K
--	0x73	--	--	512	32	1K
--	0x75	--	--	512	32	2K
--	0x76	--	--	512	32	4K

Chip ID				Page size	Page number per block	Block number
ID [0]	ID [1]	ID [2]	ID [3]			
--	0x79	--	--	512	32	8K
--	0xD1	--	--	2K	64	1K
--	0xD3	--	ID[3]&0x33 == 0x11	2K	64	8K
--		--	ID[3]&0x33 == 0x21	2K	128	4K
--		--	ID[3]&0x33 == 0x22	4K	64	4K
--		--	ID[3]&0x33 == 0x32	4K	128	2K
0x98	0xD5	0x94	0x32	8K	128	2K
0xAD	0xD5	0x94	0x25	4K	128	1K
0xAD	0xD5	0x94	0x9A	8K	256	1K
--	0xD5	--	ID[3]&0x33 == 0x11	2K	64	16K
--		--	ID[3]&0x33 == 0x21	2K	128	8K
--		--	ID[3]&0x33 == 0x32	4K	128	4K
--	0xDA	--	ID[3]&0x33 == 0x11	2K	64	2K
--		--	ID[3]&0x33 == 0x21	2K	128	1K
--	0xDC	--	ID[3]&0x33 == 0x11	2K	64	4K
--		--	ID[3]&0x33 == 0x21	2K	128	2K
--	0xF1	--	--	2K	64	1K

NOTE:

1. This table updated according to SIC driver released at **Jan 20, 2012**.
2. The ID[0] is the byte read at first cycle and means Manufacture Code. The ID[1] is the byte read at second cycle and means Device Code.
3. ID[3] & 0x33 means do bit-wise AND operation for ID[3] and 0x33. For example, if ID[3] = 0x25, ID[3] & 0x33 = 0x25 & 0x33 = 0x21.

2.5.2. Command Set Checking

The current SIC driver just support NAND flash chip with following command set for each basic function. Please search the following table to find out an entry that matches up your NAND flash chip. If you cannot found it, the current SIC driver could not yet support your NAND flash chip.

Some commands differ between 512 bytes page and larger page NAND flash chip. Please search correct table according to the page size of your NAND flash chip.

For NAND flash chip that page size is **512 bytes**:

Basic Function	Description	Commands	
Read ID	To read Chip ID	0x90	--
Read Page	To read a page of data from NAND chip	0x00	--
Read Spare Area	To read spare area data from page in NAND chip	0x50	--
Write Page	To write a page of data to NAND chip	0x80	0x10
Erase Block	To erase a block	0x60	0xD0
Read Status	To read the status register from NAND chip to find out whether read, write or erase operation is completed, and whether the write or erase operation is completed successfully.	0x70	--
Reset	To abort the current command and reset chip to ready for next command.	0xFF	--

NOTE:

1. This table updated according to SIC driver released at**Jan 20, 2012**.

For NAND flash chip that page size **equal or larger than 2K bytes**:

Basic Function	Description	Commands	
Read ID	To read Chip ID	0x90	--
Read Page	To read a page of data from NAND chip	0x00	0x30
Write Page	To write a page of data to NAND chip	0x80	0x10
Erase Block	To erase a block	0x60	0xD0
Read Status	To read the status register from NAND chip to find out whether read, write or erase operation is completed, and whether the write or erase operation is completed successfully.	0x70	--
Reset	To abort the current command and reset chip to ready for next command.	0xFF	--

NOTE:

1. This table updated according to SIC driver released at **Jan 20, 2012**.

3. Example

Now, we step by step to check a NAND flash chip to see whether FA95/VA95 support it or not.

3.1. Preparation

For Hynix HY27UF084G2B NAND flash chip, we collect the information from its datasheet as below.

Pin assignment about Hynix HY27UF084G2B.

IO15 - IO8	Data Input / Outputs (x16 only)
IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Information about NAND flash chip capacity.

Item	Description	Value
Chip ID	Each NAND flash chip contains a specific product identification to identify itself. It is 4 or 5 bytes length hexadecimal number.	**0xA0 0xDC 0x10 0x95 0x54**
Bus width	The width of I/O interfaces for both data and address.	**8-bit**
Page size	The byte number for a page that don't include spare area.	**2K**

Spare area size	The byte number for the spare area in page.	**64**
Page number per block	The page number for a block.	**64**
Block number	The block number for whole NAND flash chip.	**4096**

The command set for some basic NAND access functions:

Basic Function	**Description**	**Commands for example**	
Read ID	To read Chip ID	**0x90**	**--**
Read Page	To read a page of data from NAND chip	**0x00**	**0x30**
Write Page	To write a page of data to NAND chip	**0x80**	**0x10**
Erase Block	To erase a block	**0x60**	**0xD0**
Read Status	To read the status register from NAND chip to find out whether read, write or erase operation is completed, and whether the write or erase operation is completed successfully.	**0x70**	**--**
Reset	To abort the current command and reset chip to ready for next command.	**0xFF**	**--**

3.2. Chip Specification Checking

The chip specification and pin assignment are matched between FA95/VA95 and Hynix HY27UF084G2B NAND flash chip but Write Protect (WP) pin. This checking is passing since WP is not necessary for basic NAND flash access function.

3.3. Case Study Checking

This checking is passing since we have no similar requests or problems like the case study.

3.4. Chip ID Checking

For Hynix HY27UF084G2B NAND flash chip, we can found its Chip ID in the supported table in both section 2.4.1 and 2.5.1 that ID[1] is 0xDC and ID[3] & 0x33 = 0x95 & 0x33 = 0x11. All the information about page size, page number per block, and block number are also matched.

So, both IBR and SIC driver support this Chip ID.

3.5. Command Set Checking

For Hynix HY27UF084G2B NAND flash chip, we found that its command set is totally same to the command set in both section 2.4.2 and 2.5.2 that supported for larger page NAND flash chip.

So, both IBR and SIC driver support this command set.

3.6. Final Result

Since all steps are passing, the FA95/VA95 should support Hynix HY27UF084G2B NAND flash chip.

4. Case Study

Even if you pass all above checking for a NAND flash chip, we cannot guarantee there are no any problem for this NAND chip since there are so many types of NAND flash chip in the market. So, we collect many cases as far as possible here for case study. It is helpful if you have similar requests or problems like them.

4.1. Two CS/CE Pins for One NAND Flash Chip

Synopsis

NAND flash chip has two chip select (CS) or chip enable (CE) pins. For example, Hynix HY27UH08AG5B NAND flash chip has pin assignment as below.

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE1}$, $\overline{CE2}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B1}$, R/$\overline{B2}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Description

FA95/VA95 has two CS pins, CS0 and CS1, to support two separated NAND flash chips at the same time. One CS pin for one NAND chip. For a NAND flash chip with two CS pins, how to connect up the CS pins between FA95/VA95 chip and NAND flash chip correctly?

Solution

We should modify the circuit connection of CS pins between FA95/VA95 and NAND flash chip according to the request of NAND flash chip. For example, if NAND chip treats itself as two independent NAND modules inside one chip, we should connect up two pairs CS pins between FA95/VA95 and NAND chip. That is, FA95/VA95 also treats this NAND chip as two separated NAND flash chips.

It is possible to support this type of NAND flash chip if the pin connection or circuit design is correct.

4.2. Limitation about ECC Correctable Length

Synopsis

What is the maximum ECC correctable length that FA95/VA95 supported for a NAND flash chip?

Description

FA95/VA95 supports BCH algorithm for error detection and error correction. The BCH algorithm can correct up to 4 or 8 or 12 or 15 or 24 bits errors depend on how many BCH parity code stored at spare area of NAND flash chip. That is, the larger page size and longer ECC correctable length need larger spare area to store longer BCH parity code.

Solution

Please check following table to find out the request about BCH parity code length for different BCH algorithm and page size.

	Page Size 512	Page Size 2K	Page Size 4K	Page Size 8K
BCH_T4	8 bytes	32 bytes	64 bytes	128 bytes
BCH_T8	15 bytes	60 bytes	120 bytes	240 bytes
BCH_T12	23 bytes	92 bytes	184 bytes	368 bytes
BCH_T15	29 bytes	116 bytes	232 bytes	464 bytes
BCH_T24	Don't support	90 bytes	180 bytes	360 bytes

Since the spare area not only for ECC but also for other features such as bad block marking, the final request about spare area is larger than the BCH parity code length in above table. Please reserve at least 6 bytes for other features.

FA95/VA95 supports a NAND flash chip if its spare area is large enough to store both the BCH parity code and other 6 bytes information.

NOTE:

1. BCH algorithm used in first four blocks for booting

	BCH function
XtraROM	Disable BCH
512 Page Size	BCH T4
2048 Page Size	BCH T4
4096 Page Size	BCH T8
8192 Page Size	BCH T12

2. BCH algorithm used in other blocks in NAND driver

	BCH function
XtraROM	Disable BCH
512 Page Size	BCH T4
2048 Page Size	BCH T8
4096 Page Size	BCH T8
8192 Page Size	BCH T24

4.3. Page Size Larger Than 8K

Synopsis

The page size of NAND flash chip is larger than 8K bytes.

Description

FA95/VA95 just supports page size for 512, 2K, 4K and 8K bytes.

Solution

The NAND flash chip with page size larger than 8K bytes is not supported.

4.4. Bus Width is 16 Bits

Synopsis

The bus width of NAND flash chip is 16 bits or more .

Description

FA95/VA95 just supports 8 bits bus width.

Solution

The NAND flash chip with bus width 16 bits or more is not supported.

4.5. Support NAND ROM Chip ?

Synopsis

Does FA95/VA95 support NAND ROM chip?

Description

There is a new type NAND chip called **NAND ROM** or **OTP NAND** that supports One-Time-Program (OTP) technology. NAND ROM chip with NAND interface and supports all NAND operations and command set, however commands that are associated with erase operation are ignored and will return error status.

Solution

FA95/VA95 support NAND ROM chip if it passes all checking items.

For example, Infinite Memory IM90A001GT is a 128M bytes NAND ROM chip. It passes all checking items for FA95/VA95 but the command for reading spare area. IM90A001GT with 512 bytes page size but don't support command 0x50 (refer to section 2.5.2) to read spare area. According to the checking flowchart, FA95/VA95 supports it as booting NAND chip for NAND booting CS0 with NAND type Power-On-Setting or NAND booting CS1 without NAND type Power-On-Setting.

4.6. Support NAND Chip Not in IBR NAND ID Table?

Synopsis

When ID of the NAND chip you prefers to use is not in IBR NAND table,

Description

Does there is workaround method when NAND chip is not in FA95/VA95 NAND ID table?

Solution

FA95/VA95 IBR supports NAND Power-On-Setting for user to configure the NAND setting instead of IBR default setting. The information needs for NAND booting is as follows.

- NAND Type

CHIP_CFG[10]	NAND Type
0	EF (Error Free) NAND Flash Memory
1	Raw NAND Flash Memory

- Page size

CHIP_CFG[9:8]		Page size & NAND Power-On-Setting Control
0	0	NAND page size is 2KB
0	1	NAND page size is 4KB
1	0	NAND page size is 8KB
1	1	Ignore NAND Power-On-Setting

- Default Page per block in IBR

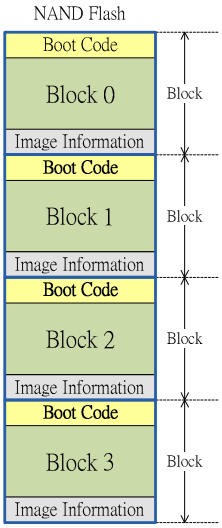
	Page per Block
512 Page Size	32
2048 Page Size	64
4096 Page Size	128
8192 Page Size	128

- NAND address cycle

CHIP_CFG[7]	Address Cycle
0	The NAND address cycle is 4.
1	The NAND address cycle is 5.

NOTE:

1. When IBR default page per block value is not correct, some Boot code backup will not work and SIC Driver and NandLoader need to modify to match the format in IBR.


NAND Flash
Boot Code
Block 0
Image Information
Boot Code
Block 1
Image Information
Boot Code
Block 2
Image Information
Boot Code
Block 3
Image Information
Block
Block
Block
Block

5. Revision History

Version	Date	Description
V1.0	Feb. 22, 2012	● Created

Important Notice

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