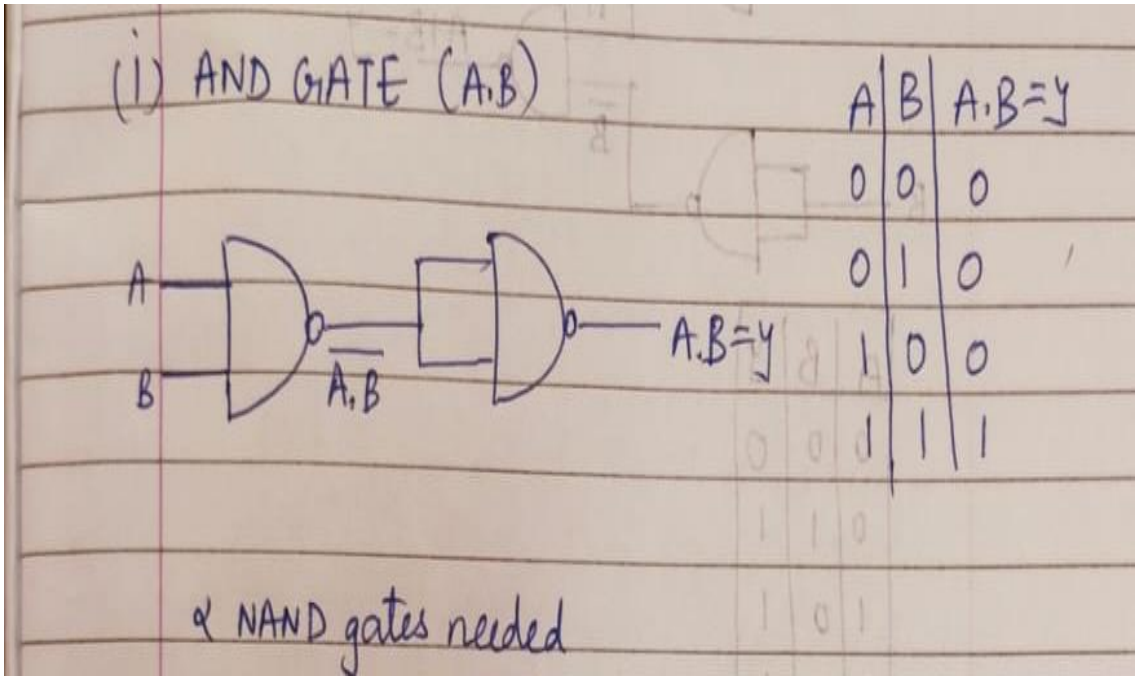
LAB REPORT

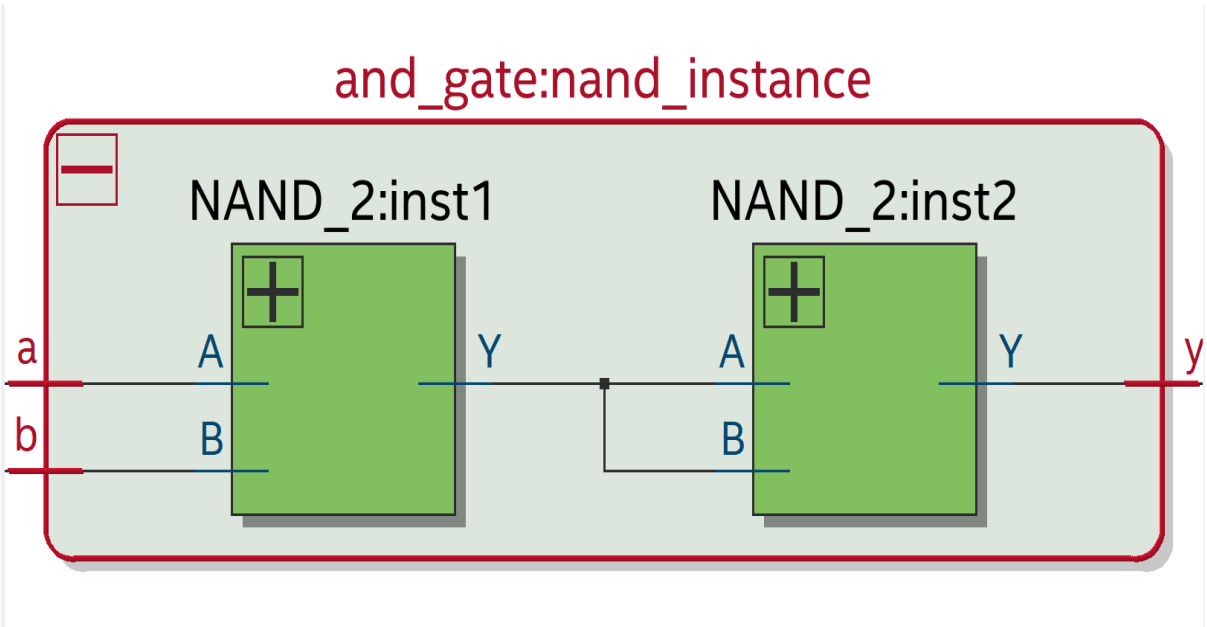
LAB -1

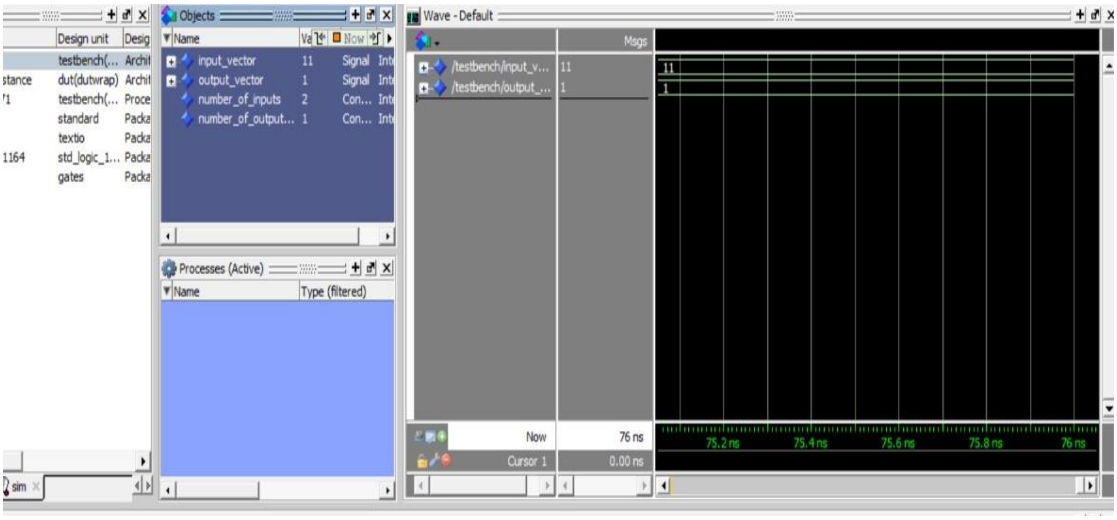
1. AND Gate

   Boolean expression – A.B

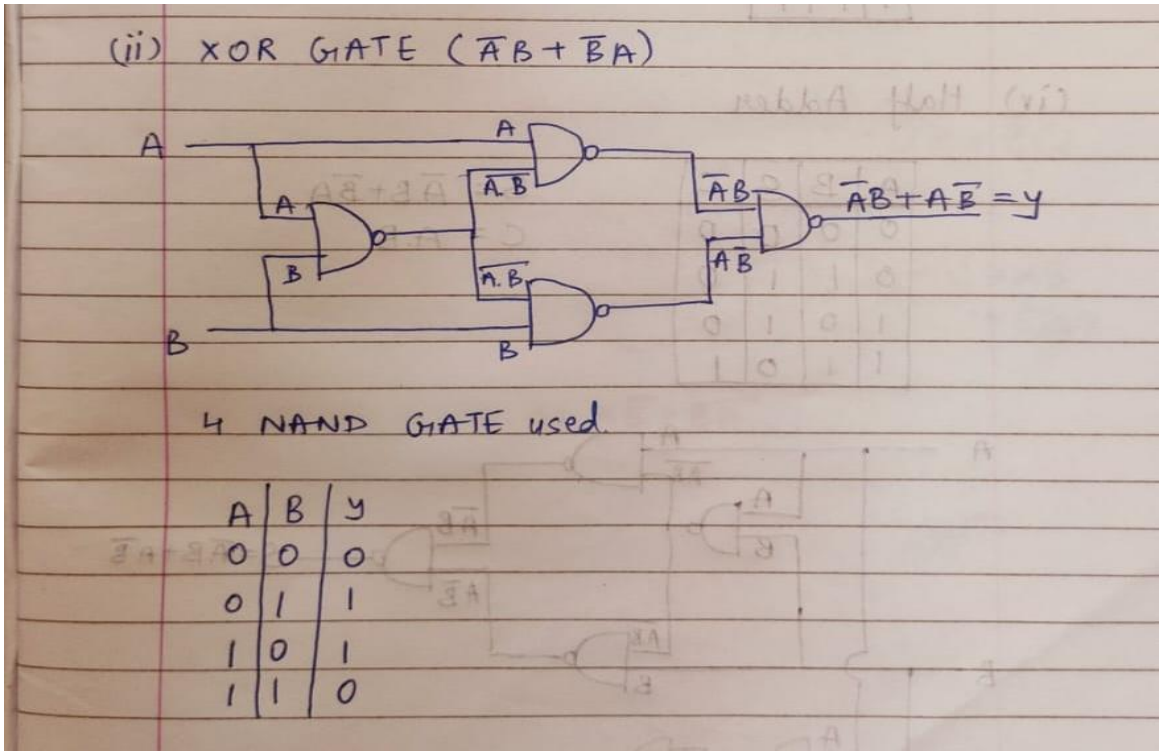


   Simulations

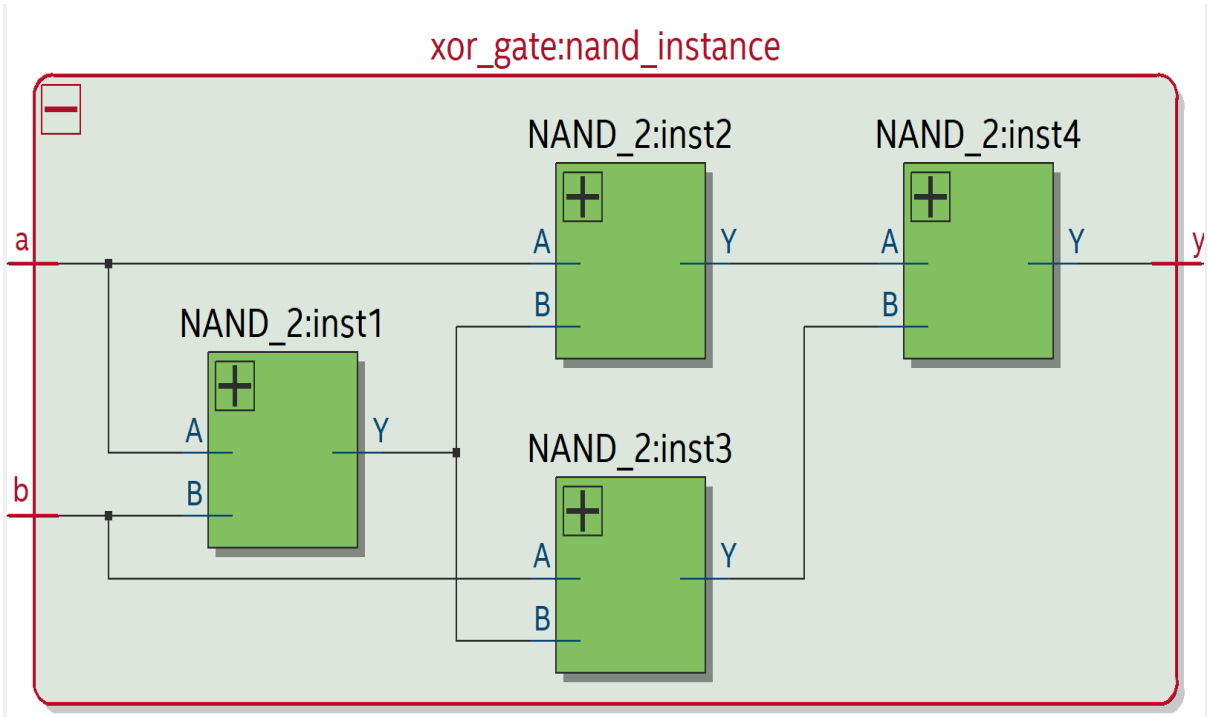


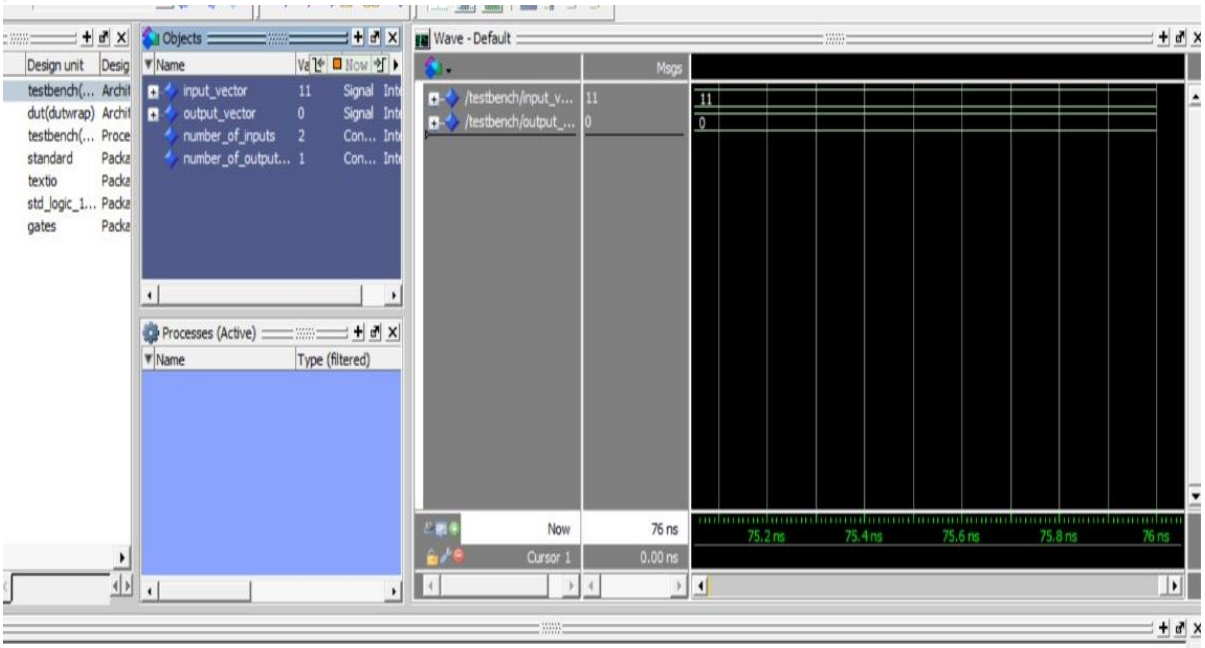

Objects
Name
input_vector
output_vector
number_of_inputs
number_of_output...
Processes (Active)
Name
Type (filtered)
Wave - Default
Msgs
/testbench/input_v...
/testbench/output_...
Now
Cursor 1
76 ns
0.00 ns
75.2 ns
75.4 ns
75.6 ns
75.8 ns
76 ns

2. XOR Gate


(ii) XOR GATE ($\bar{A}B + \bar{B}A$)
A
B
$\bar{A}B + A\bar{B} = y$
4 NAND GATE used.
A | B | y
0 | 0 | 0
0 | 1 | 1
1 | 0 | 1
1 | 1 | 0

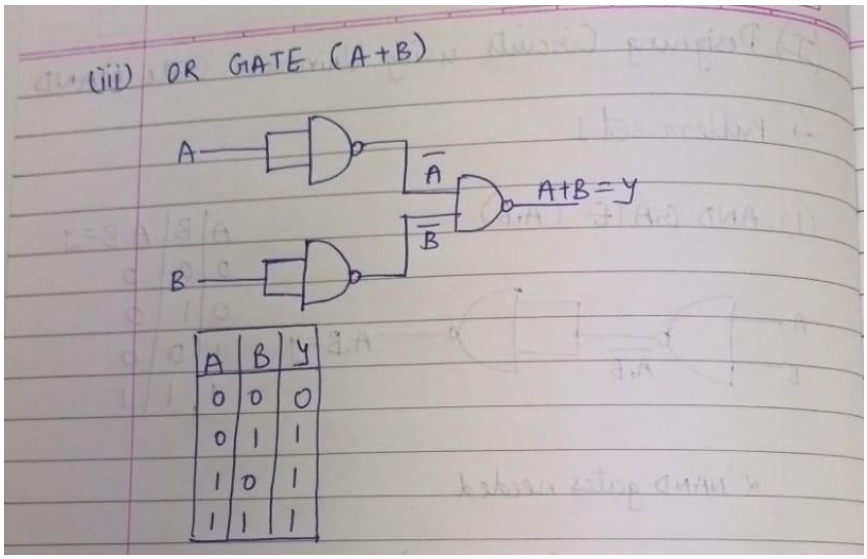
Simulations



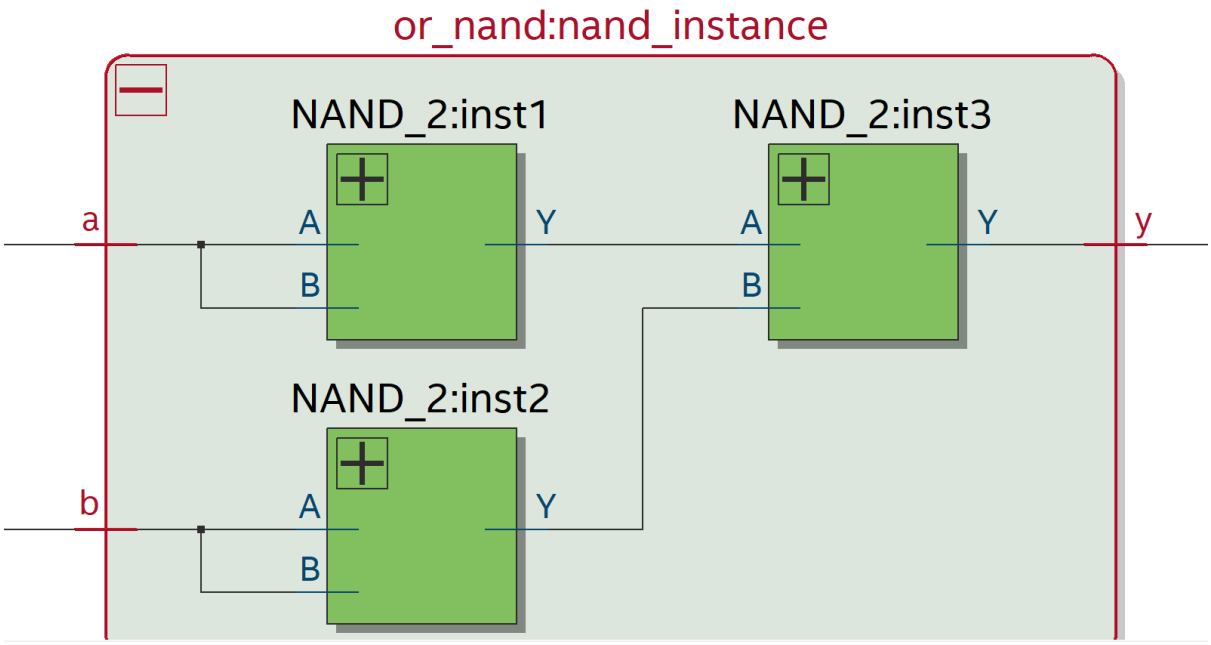


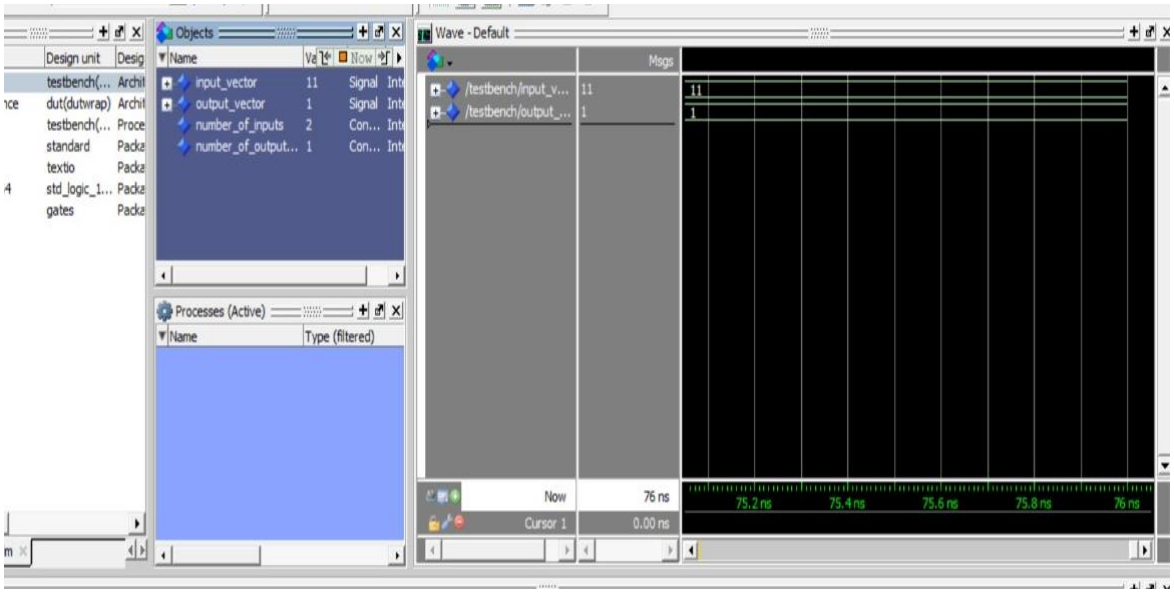
4. OR Gate

Boolean expression – A+B

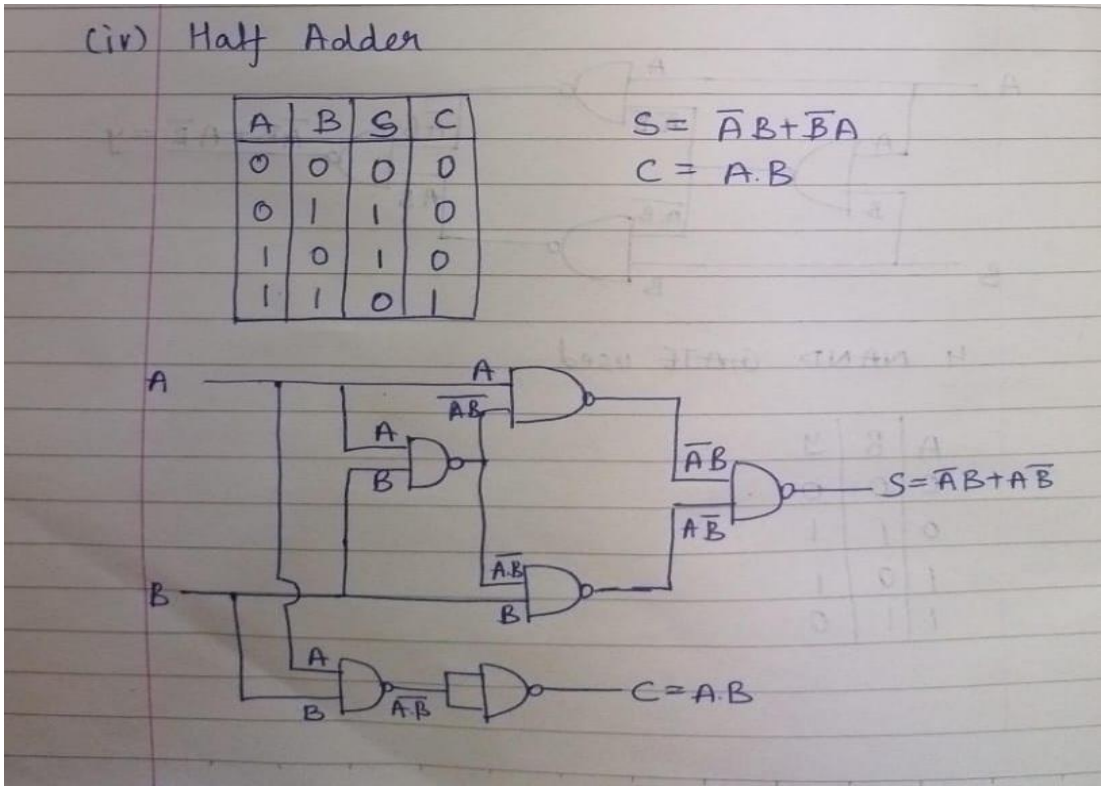


Simulations

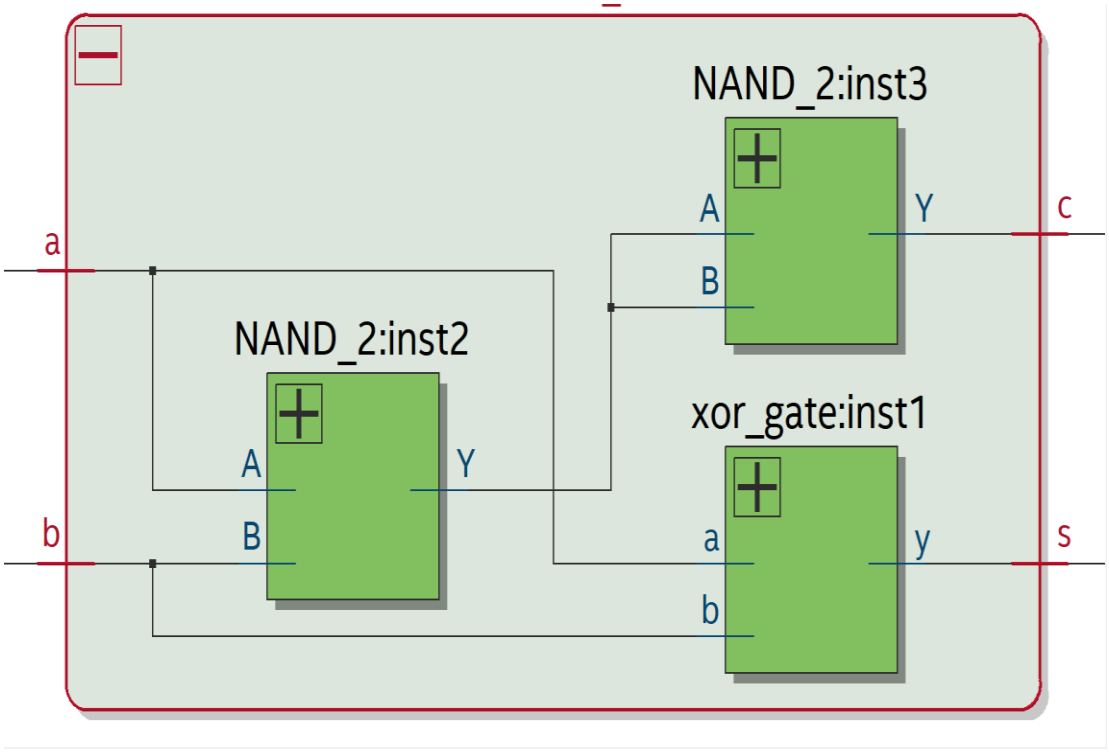


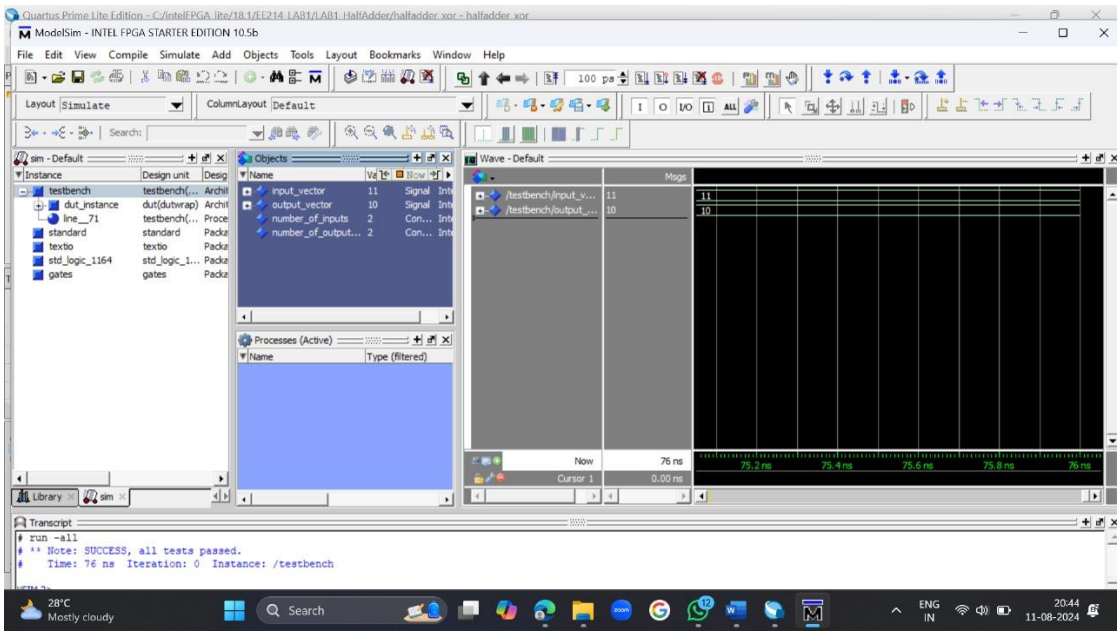

Objects
Name
input_vector
output_vector
number_of_inputs
number_of_output...
Processes (Active)
Name
Type (filtered)
Wave - Default
Msgs
/testbench/input_v...
/testbench/output_...
Now
76 ns
Cursor 1
0.00 ns
75.2 ns
75.4 ns
75.6 ns
75.8 ns
76 ns

5. HALF ADDER


(iv) Half Adder
A B S C
0 0 0 0
0 1 1 0
1 0 1 0
1 1 0 1
S = $\bar{A}B + \bar{B}A$
C = A.B
S = $A\bar{B} + \bar{A}B$
C = A.B

Simulations





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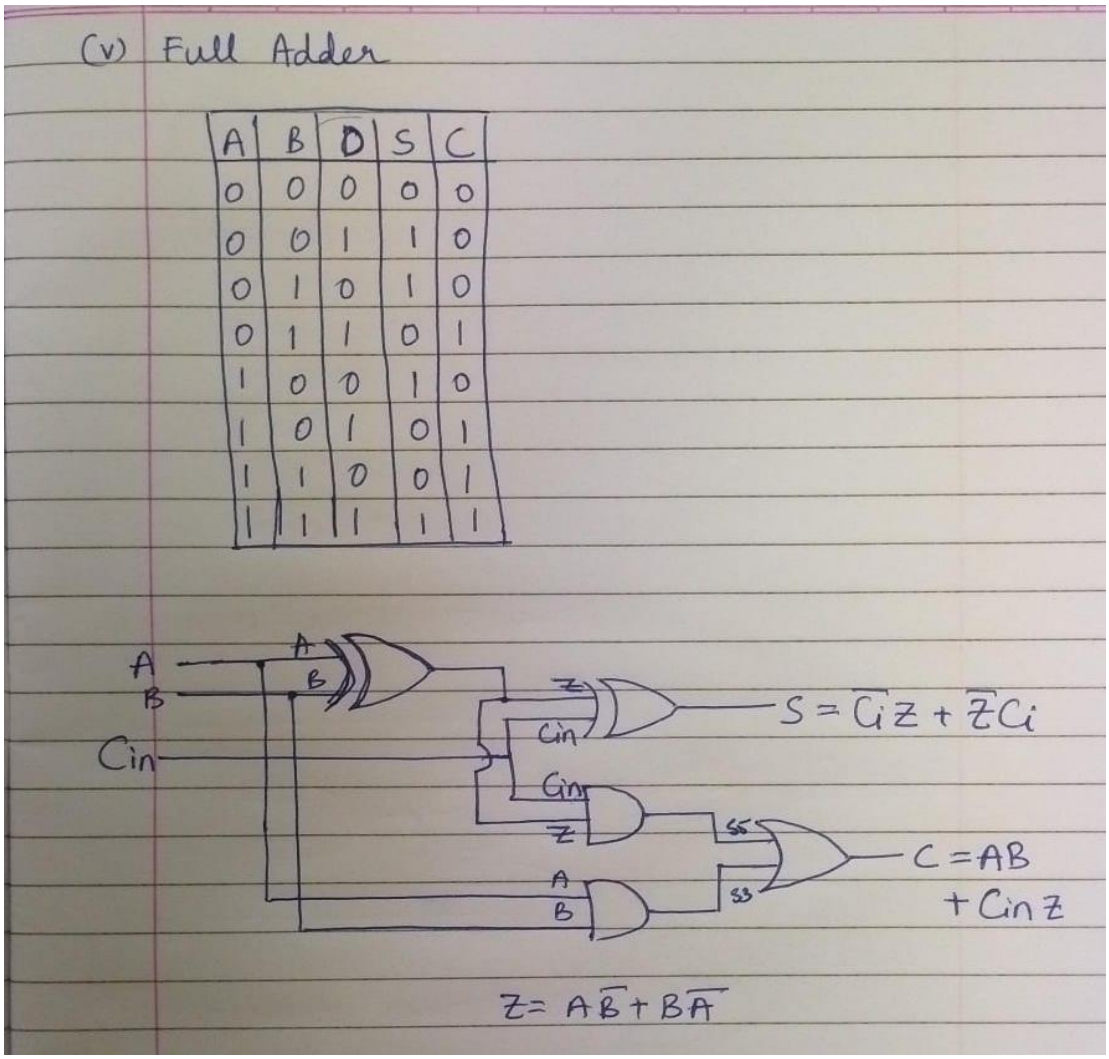
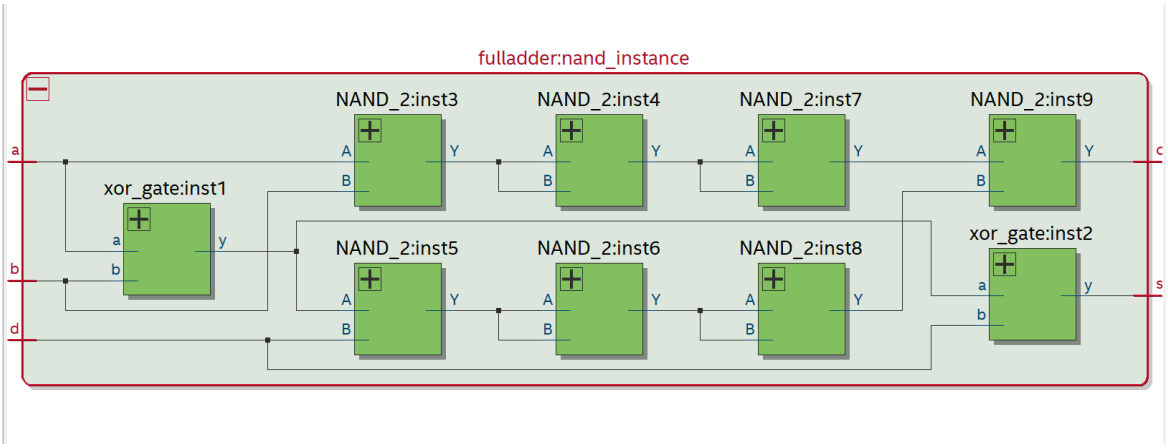
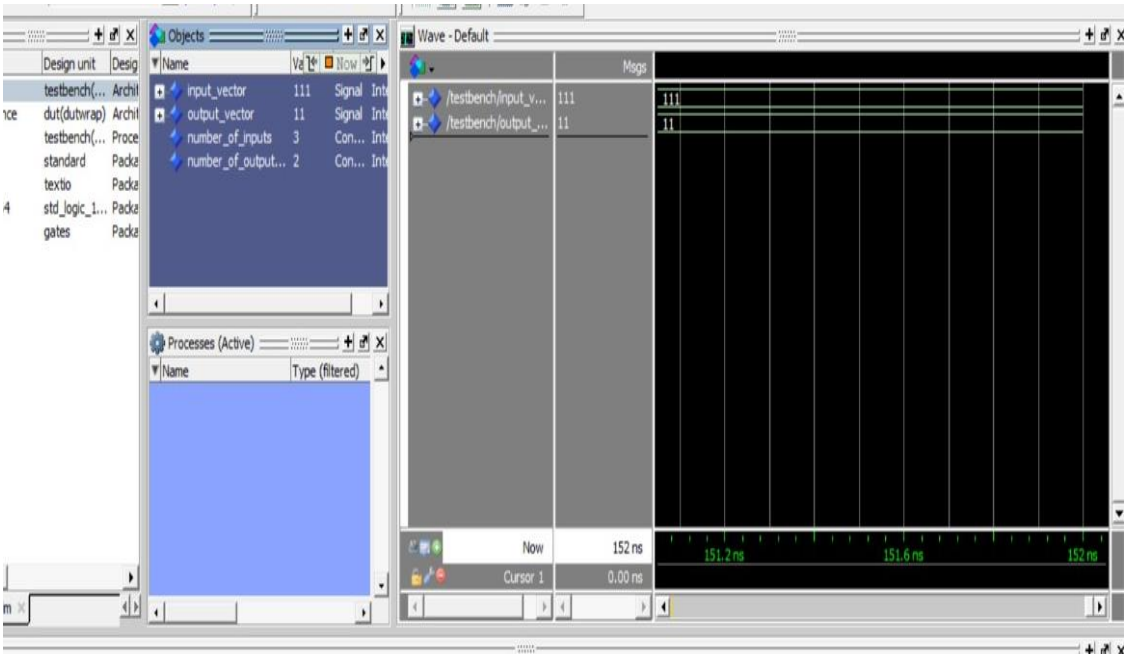
6. FULL ADDER



Simulations




Design unit
testbench(...
dut(dutwrap)
testbench(...
standard
textio
std_logic_1...
gates
Objects
Name
input_vector
output_vector
number_of_inputs
number_of_output...
Processes (Active)
Name
Type (filtered)
Wave - Default
Msgs
/testbench/input_v...
/testbench/output_...
111
11
Now
152 ns
Cursor 1
0.00 ns
151.2 ns
151.6 ns
152 ns