EE214 Digital Circuits Laboratory
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Problem set: 8 Date: October 10, 2024

Clock Divider

Instructions:

1. Use **Behavioral** modeling for writing VHDL description
2. Write the testbench to perform RTL simulation.
3. Demonstrate the simulations to your TA
4. Perform Pin-Planning, run on Xenon board and demonstrate to your TA.
5. Submit the entire project files in .zip format in moodle.

Clock Divider

Designing of the Clock Divider

In this experiment you will be doing clock divider. There is a 50 Mhz on board clock. You will divide it to generate 500 Hz clock and 1 Hz clock. Code for testbench will be provided. You can run the simulation to check the waveform. You can map it in the board also so that you can assign an LED and can check if the LED is blinking.

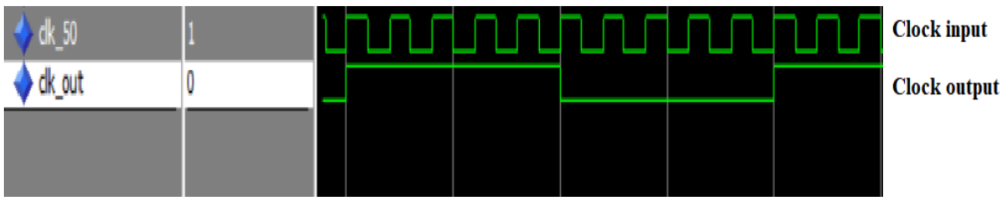

Figure 1: Waveform

NOTE: The above image(1) is for representative purpose only. May not have any similarity with the waveform that will be generated after simulation.

Method of this experiment

Suppose we need to generate f = 5 MHz from 50 MHz master clock. For this, we need a counter such that the clock out remains HIGH for 5 Input (master) Clock Cycles and LOW for next 5 Clock Cycles. In order to do this, we set-up a counter that starts from 1 and increments at every positive edge of the Input Clock (master) till the count reaches its maximum value which is 5 in this case.

$$count = 50MHz/(2 \star f) = 5$$

After the count reaches 5, count will be initialized back to 1. And clock output will go LOW till count reaches maximum again. **Note:** Here we are counting from 1 to maximum count. (Not from 0 to maximum count -1).

Method to generate any arbitrary frequency from 50 MHz clock

Suppose you want to generate the frequency of f = 10 Hz.

$$count = 50MHz/(2 \star f)$$

Count = 2.5 Million. So till the count reaches maximum the clock out will be 1. After the count reaches maximum count will be initialized to 1. And output clock will be off till count reaches maximum again.

VHDL Description and RTL Simulation

- Generate a 75 Hz square wave by creating your own testbench. Please verify the simulation using the Testbench. (Use a switch to give reset input)
- Design a system by with following characteristics:
  - System has a switch input
  - if switch is "0" then three LEDs will blink for 1 sec. (if LED1, LED2, LED3 is ON for 1 sec and rest are OFF then for next 1 sec LED2, LED3, LED4 will be ON and rest will be OFF. Similarly after reaching LED6, LED7, LED8 the next sequence should be LED5, LED6, LED7 which is the reverse.)
  - if switch is "1", then we will count from 0 to 100 in steps of 2 continuously and show it on corresponding LEDs with LED1 as LSB and LED8 as MSB with each count will change after 1 sec.
  - Modify the given testbench to incorporate the new testbench

On Xenon board

- For the generated system output show it on LED1-LED8 on Xenon board.
- Do Pin-mapping for the clock output to LEDs and 50 MHz input clock, reset to SW8 and input switch as SW1. Refer the Pin-mapping given below and do accordingly.
- Keep SW8 ON for some time then make it OFF.
- Get the LED output verified by your respective TA.

Clock Source Frequency	FPGA Pin no.
1 Hz CLK	55
50 MHz CLK	26
Ext CLK	27
10 MHz CLK	29

Figure 2: Pin-mapping for on-board Clock Sources

Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Figure 3: Pin-mapping for on-board Switches and LED's