



## 4-bit Adder-Subtractor

### Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA on the respective upcoming lab days.

### Problem Statement: 4-bit Adder-Subtractor

1. VHDL Description: Using the full adder and XOR gate as a component, describe a 4-bit ripple carry adder-subtractor in VHDL.

INFO: 4-bit ripple carry adder-subtractor has following parts

- (a) Two 4-bit inputs : A ( $A_3 A_2 A_1 A_0$ ) , B ( $B_3 B_2 B_1 B_0$ )
- (b) One 1-bit input: M
- (c) One 4-bit output : S ( $S_3 S_2 S_1 S_0$ )
- (d) One 1-bit output: Cout

NOTE: It is a simple binary adder-subtractor that can be implemented by cascading four full adders such that the carry generated by the addition of lower significant bits forms the incoming carry for addition of the next significant bits.

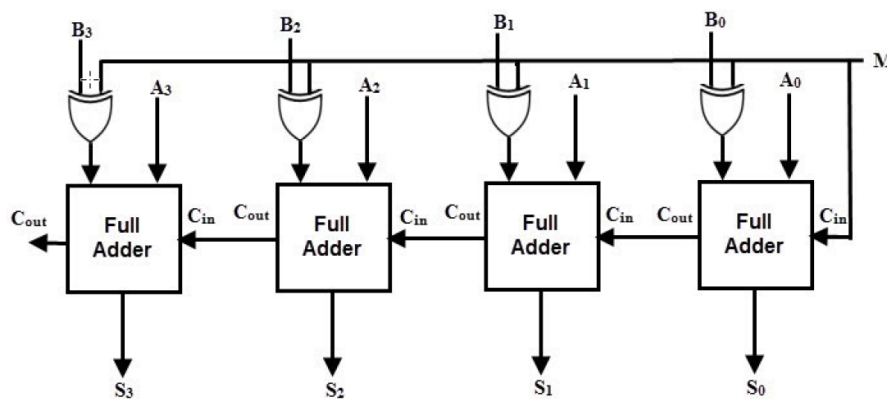


Figure 1: Design of 4 Bit Adder-Subtractor

2. Simulation: Simulate the design using the generic testbench to confirm the correctness of your description. NOTE: To do this, you need to use the given tracefile and modify the testbench given to you appropriately. Tracefile format: ( $a_3 a_2 a_1 a_0$ ) ( $b_3 b_2 b_1 b_0$ ) ( $M$ ) ( $Cout$ ) ( $S_3 S_2 S_1 S_0$ ) 11111) [Tracefile](#)

### 3. Expected Simulation Result of 4 Bit Adder-Subtractor:

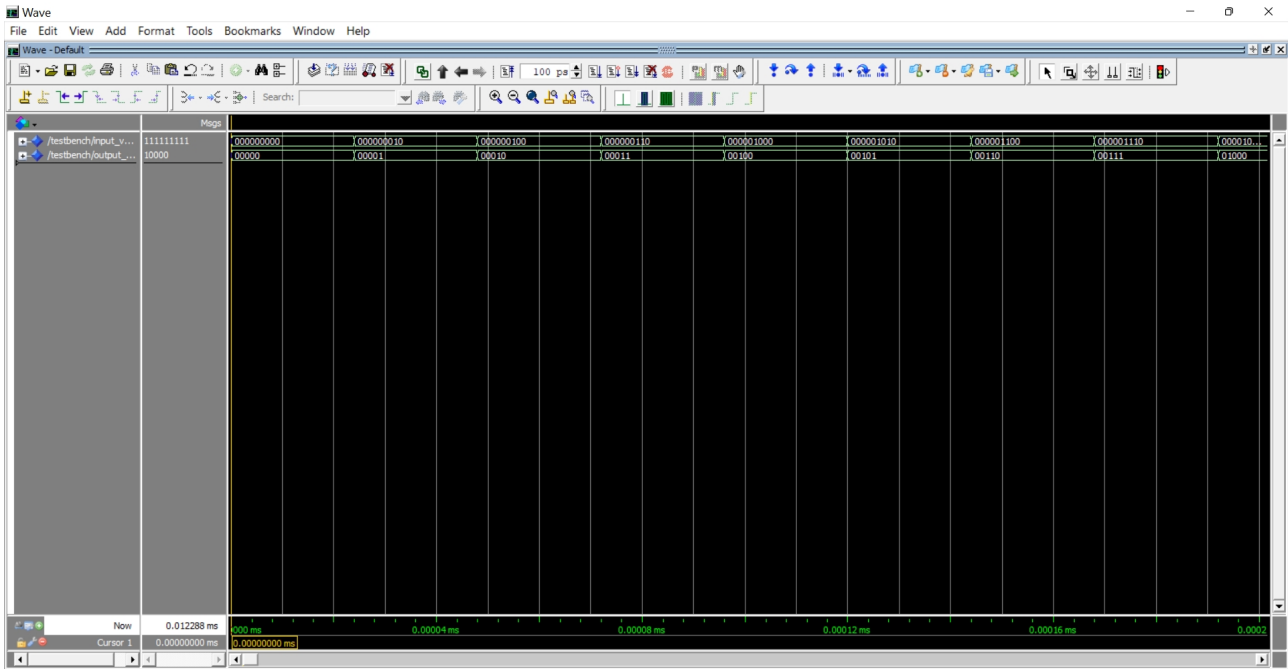


Figure 2: 4 Bit Adder-Subtractor Simulation Result