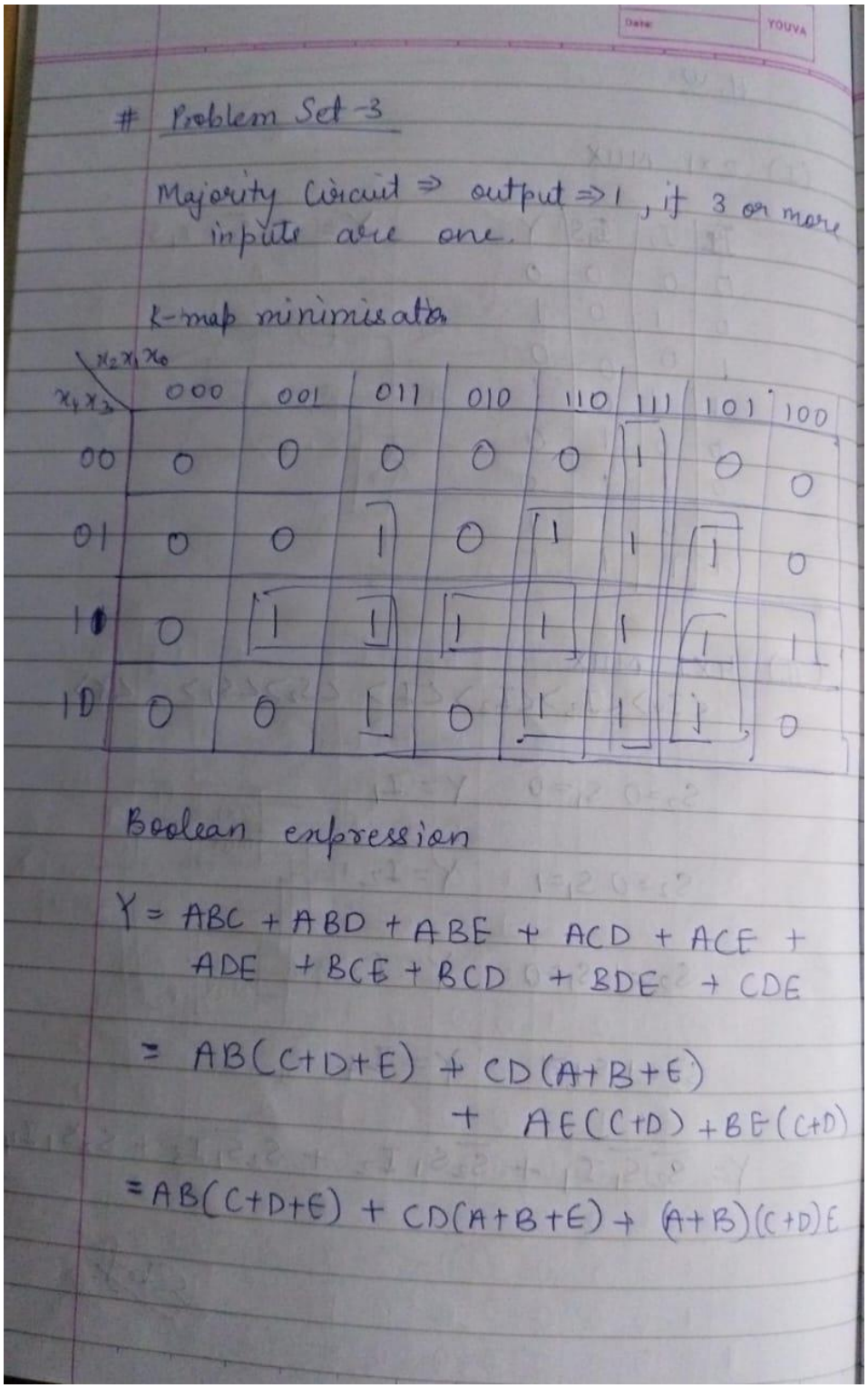
Majority circuit

Pen paper design



Problem Set-3

Majority Circuit ⇒ output ⇒ 1, if 3 or more inputs are one.

K-map minimisation

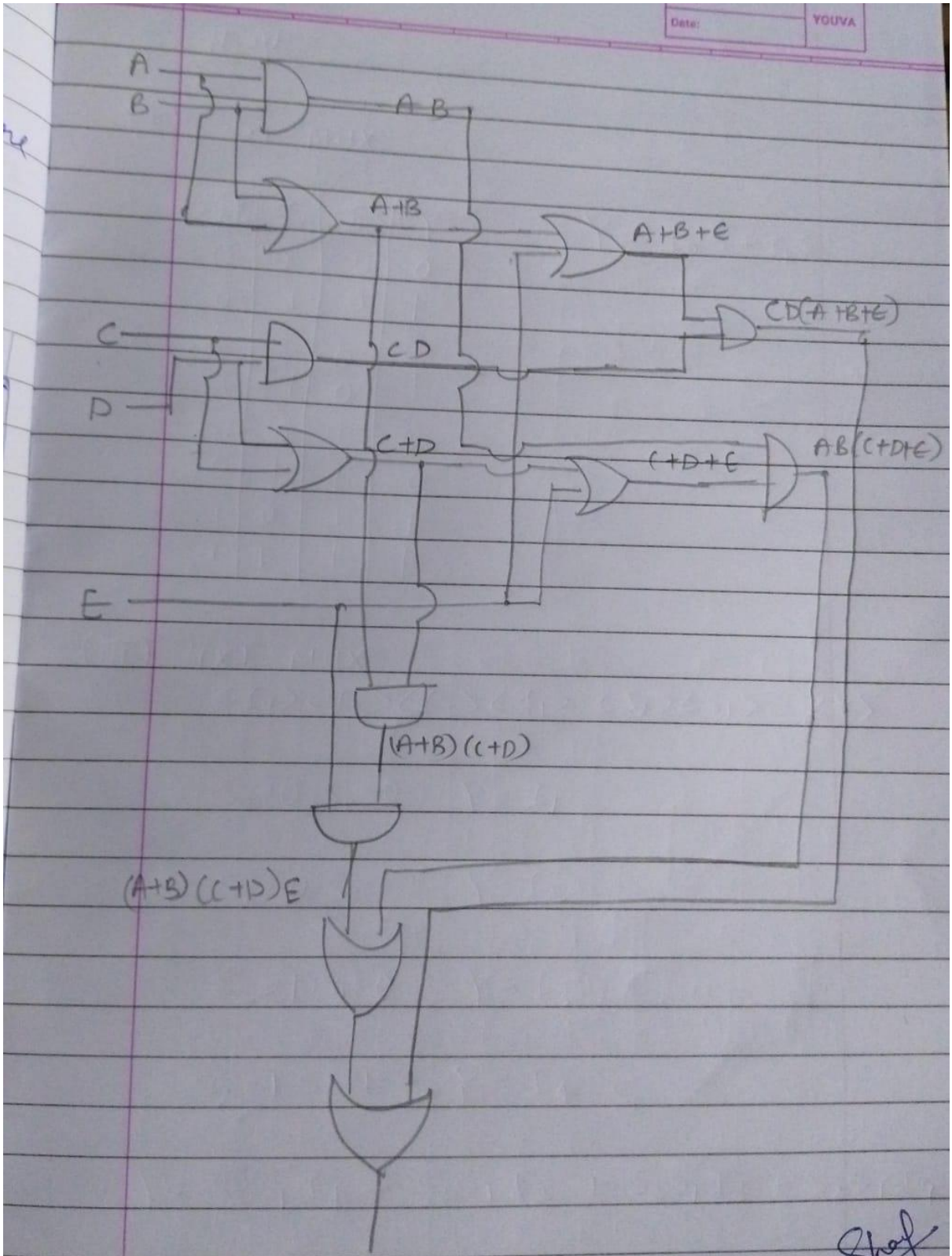
x_4x_3 \ $x_2x_1x_0$	000	001	011	010	110	111	101	100
00	0	0	0	0	0	1	0	0
01	0	0	1	0	1	1	1	0
11	0	1	1	1	1	1	1	1
10	0	0	1	0	1	1	1	0

Boolean expression

$$Y = ABC + ABD + ABE + ACD + ACE + ADE + BCE + BCD + BDE + CDE$$

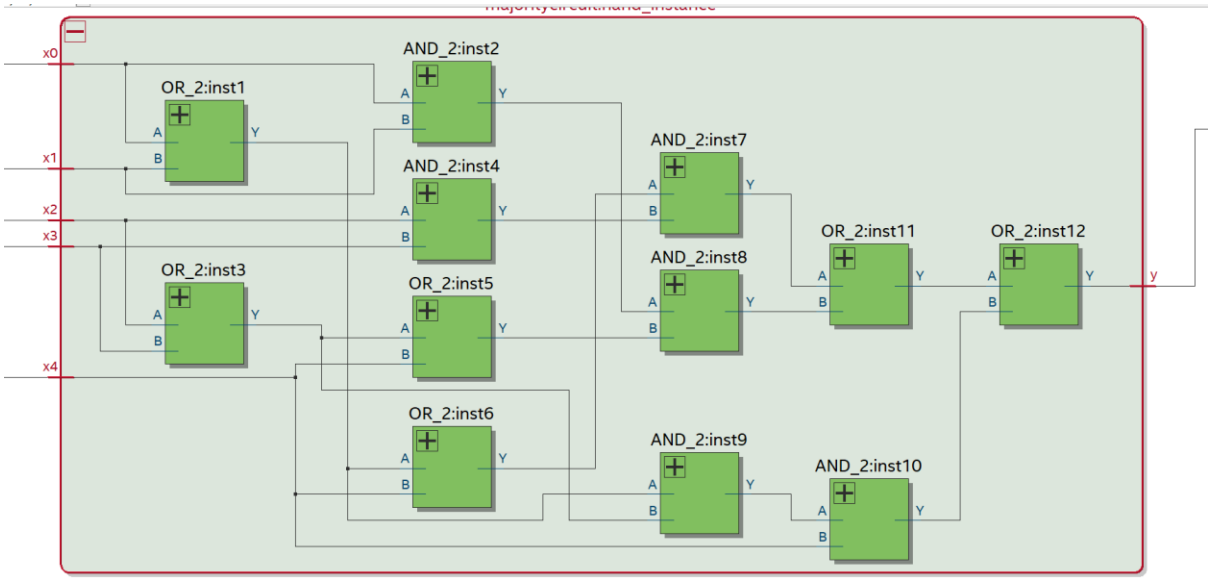
$$= AB(C+D+E) + CD(A+B+E) + AE(C+D) + BE(C+D)$$

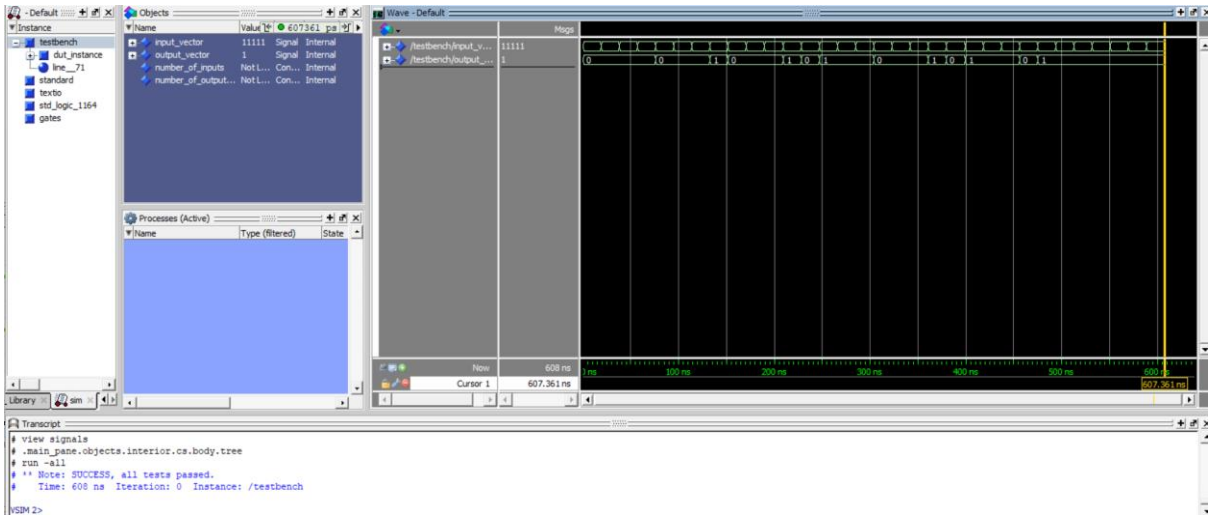
$$= AB(C+D+E) + CD(A+B+E) + (A+B)(C+D)E$$



$$(A+B)(C+D)E + AB(C+D+E) + CD(A+B+E)$$

Simulations





Xen 10 installation completion

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WARNING: UrJTAG may damage your hardware!
Type "quit" to exit, "help" for help.

jtag> cable ft2232
Connected to libftd2xx driver.
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x00000000031840DD)
  Manufacturer: Altera
  Part(0):         10M25SAE144
  Stepping:     1
  Filename:     c:\users\acer\desktop\sem3\ee214 lab\xen10_files\xen10_files\urjtag_max10\urjtag\data/altera/10m25sae144/10M25SAE144
jtag> D:\intelFPGA_lite\18.1\MAJORITYCIRCUIT.vhdl\majoritycircuit.svf
D:\intelFPGA_lite\18.1\MAJORITYCIRCUIT.vhdl\majoritycircuit.svf: unknown command
jtag> svf D:\intelFPGA_lite\18.1\MAJORITYCIRCUIT.vhdl\majoritycircuit.svf progress
svf: cannot open file 'D:\intelFPGA_lite\18.1\MAJORITYCIRCUIT.vhdl\majoritycircuit.svf/majoritycircuit.svf' for reading
svf: syntax error!
jtag> svf majoritycircuit.svf progress
Warning svf: unimplemented mode 'ABSENT' for TRST
Parsing   3740/3748 ( 99%)
Scanned device output matched expected TDO values.
jtag>
```

Hardware photos