EE214 Digital Circuits Laboratory
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Problem set: 3 Date: August 29, 2024

Majority Circuit

Instructions

1. Use structural modelling for this experiment i.e. instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA/RA.
3. In pen paper design use proper labeling for each wire. And use the same labels for the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.
5. Perform manual verification using xen-10 board.
6. Demonstrate the experiment to your TA/RA.
7. Submit the entire project files in .zip format in Moodle.

Design

Design and implement a majority circuit. A majority circuit outputs '1' when most of its inputs are '1' (The output is '1' when three or more inputs are '1'). Show the pen-paper design and minimized expression using K-Maps to the corresponding evaluating TAs.

VHDL Description

Write a VHDL description for the given problem statement.

Inputs(5-bit): $x_4x_3x_2x_1x_0$
Output(1-bit): y
Tracefile format: $< x_4x_3x_2x_1x_0 >$ $< y >$ 1

Design Verification

- Perform RTL Level Simulation of the Majority Circuit using the generic testbench to confirm the correctness of your description using the TRACEFILE
- Pin plan switches S5 to S1 as input and LED 8 as output and show the correctness of the design on board.

Testing on Board

- Test the correctness of your design on the Xen-10 board.
- Perform the pin mapping as follows:

$$\begin{aligned} \textit{x4-x0} &\implies \textit{SW5-SW1;} \\ y &\implies \textit{LED8} \end{aligned}$$