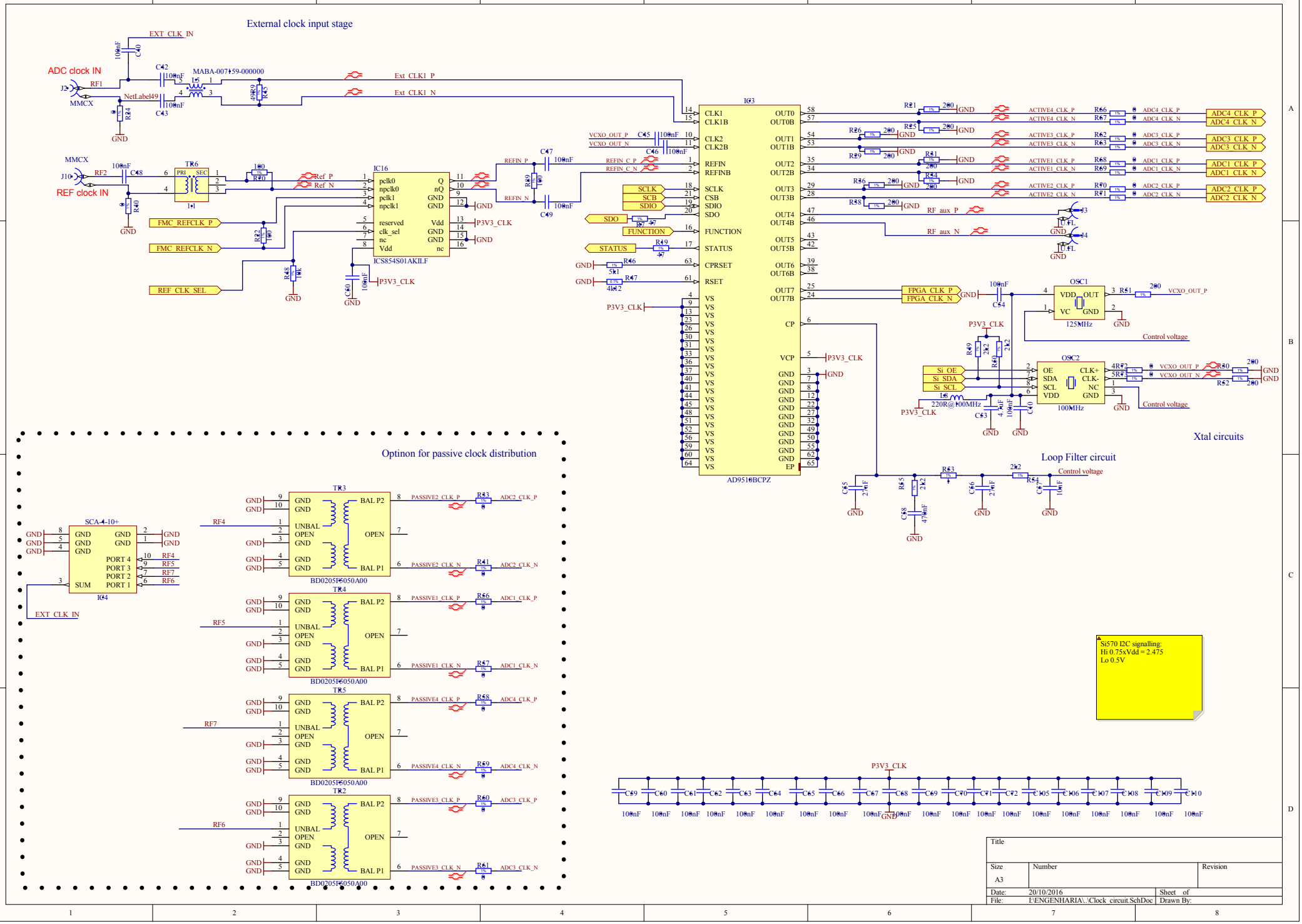
External clock input stage
ADC clock IN
REF clock IN
EXT_CLK_IN
MMCX
MABA-007159-000000
Ext_CLK1_P
Ext_CLK1_N
IC3
AD9510BCPZ
IC16
ICS854S01AKILF
TR6
1:1
FMC_REFCLK_P
FMC_REFCLK_N
REF_CLK_SEL
P3V3_CLK
SCLK
SCB
SDIO
SDO
FUNCTION
STATUS
RF_aux_P
RF_aux_N
FPGA_CLK_P
FPGA_CLK_N
OSC1
125MHz
OSC2
100MHz
Si_OE
Si_SDA
Si_SCL
Control voltage
Xtal circuits
Loop Filter circuit
Optinon for passive clock distribution
SCA-4-10+
IC4
TR3
TR4
TR5
TR2
BD0205F6050A00
Si570 I2C signalling:
Hi 0.75xVdd = 2.475
Lo 0.5V
Title
Size
A3
Number
Revision
Date: 20/10/2016
File: I:\ENGENHARIA\..\Clock_circuit.SchDoc
Sheet of
Drawn By: