Laboratório Nacional de Luz Síncrotron

ABTLuS CNPEM Centro Nacional de Pesquisa em Energia e Materiais

Specification of a 4-channel, high speed and high resolution ADC board fully compliant with the VITA 57.1-2010

(130 MSPS sampling rate)

Version 2.1

In this text we summarize the specification of the ADC (Analog to Digital Conversion) board which will be used in the SIRIUS EBPM (Electron Beam Position Monitor) design. The main purpose of this document is to provide companies with basic information to design and manufacture prototypes for the Brazilian Synchrotron Light Laboratory

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Diagnostics group

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Main description

In this text we summarize the specification of the ADC board which will be used in the SIRIUS EBPM (Electron Beam Position Monitor) design.

There are several commercial off-the-shelf digitizers covering a wide range of speed, bandwidth and resolution. The EBPM system necessities are not different from the usual high speed data acquisition systems, the main special requirements are related to the sampling clocks strategies. **A fine tuning sampling clock feature is required.** The most important desired features are listed below:

- VITA 57.1-2010 compliant
- Four Channel 16 bit 130 MSPS ADC. Required ADC: LTC2208IUP
- Internal ADC clock circuit: phase locked to the external reference clock input with fine frequency tuning capability. See specific section. Hold mode in case of loss of external reference is a desirable feature.
- Internal high frequency PLL oscillator output with amplitude control and locked to external reference.
- External ADC clock input (50 MHz up to 130 MHz, 0 dBm typ.)[1]
- External reference clock input: (0.5 MHz - 20 MHz digital signal, 0 dBm typ.)[2]
- External digital trigger input
- External digital trigger output

[1] *Consider an AC-coupled, 50 Ω, fast edges, 1 volt p-p square signal. Frequencies below 50 MHz will not be used.*

[2] *Consider an AC-coupled, 50 Ω, low jitter, fast edges, 1 volt p-p square signal. The reference signal frequency will be about 625 kHz or any integer multiple up to 32. Examples: 0.625 MHz, 1.25 MHz, 1.875 MHz … 20 MHz.*

Block diagram

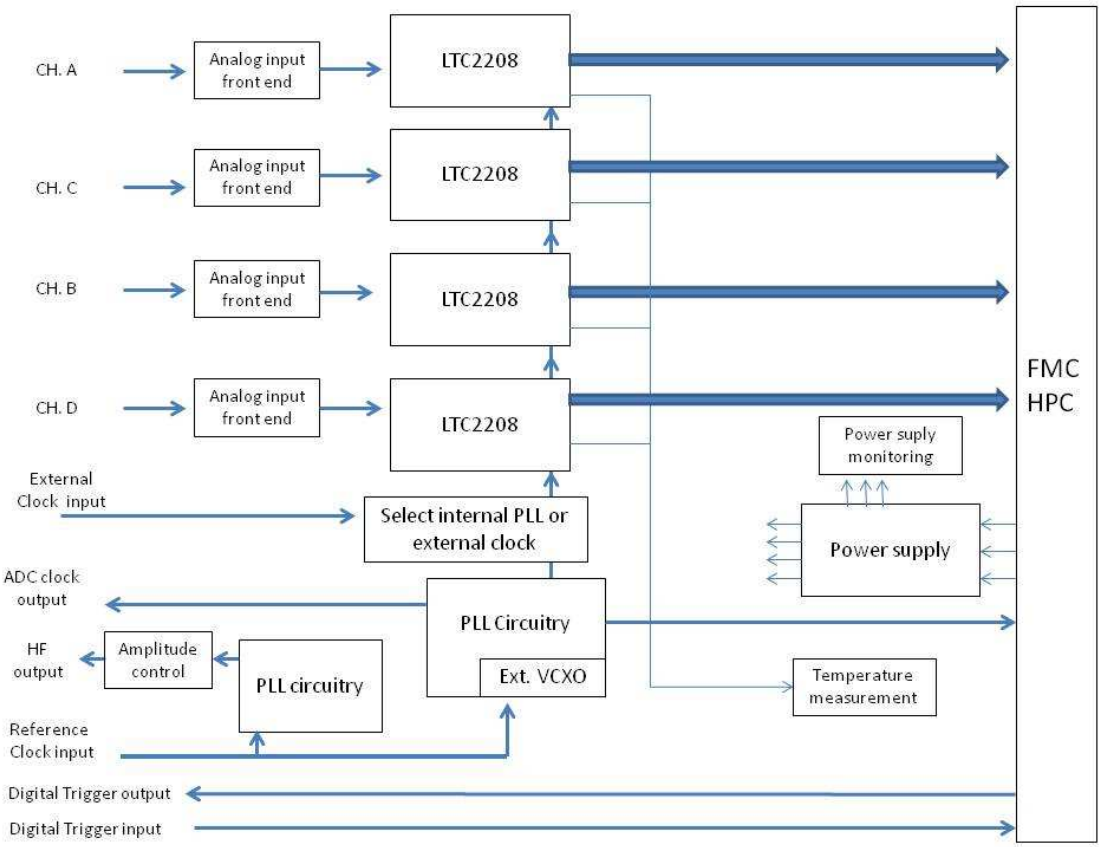

Figure 1: illustrative block diagram

Circuit details

Internal ADC clock circuit

The internal sampling clock circuit must provide signal with extremely lower jitter. The generated frequency represents the external ref. signal multiplied by 188 considering an external reference of 625 kHz. For different reference frequencies, the integer multiplier factor must be observed to generate 117.5 MHz.

The clock frequency tuning range must be about ± 10 kHz around the internal ADC clock frequency. The adjustment granularity should be 50 Hz, or less. Digital PLL components like AD9510 or a combination of the LMX2541 and a LMK04XXX family device together with a low phase noise VCXO crystal can implement the fine tuning feature (CVHD-950 from Crystek is suggested).

For Frequency flexibility, a programmable VCXO could be used. The Si570/Si571 from Silabs is also suggested.

In case of using external ADC clock, the internal PLL must be turned off.

Internal high frequency PLL oscillator

The circuit must provide a **sinusoidal** signal with frequency of [ref. freq.*N], where N is typically 800. Fine frequency tuning is also required: +/-10 MHz range with minimum step of few kHz. A low phase noise PLL must be used. Suggested PLL: LMX2541 accompanied of a digitally programmable attenuator for amplitude controlling.

Amplitude control must have a range of about 20 dB in steps of 0.25 dB with initial absolute amplitude of -10 dBm, in other words, control from -10 dBm to -30 dBm in steps of 0.25 dB. Another 20 dB range for the absolute amplitude of -50 dBm is required. It could be achieved using a fixed attenuator, RF switches and a digitally controlled attenuator. HMC792LP4E from Hittite and SKY12343-364LF from Skyworks are suggested.

Related to the spurious specification, the HF signal must have a spurious free bandwidth > 4 MHz around the main frequency. The SFDR for this signal must be > 60 dBFS for a BW of 40 MHz.

All controls must be available for the user. For example: turn on/off, frequency control, amplitude control, etc.

Specification tables

Parameter	***Description***	***Note***
Standard	*FMC double width (VITA 57.1-2010) with connector P2 not populated.*	*HPC (High-Pin Count) 400-Pin Connector. FMC single width can be used.*
Front panel connections	• *4 analog inputs* • *1 ext. ref. input* • *1 ext.ADC clock input* • *1 ADC clock output* • *1 HF output* • *1 digital trigger input* • *1 digital trigger output*	*All signals are 50 Ω - single-ended AC- coupled.*
Input connectors	*For analog input SMA is required. For other signals MMCX, SSMC, µ-connector model CMM 220 or other miniature RF coaxial can be used.*	*If extremely necessary, except by the four analog input connectors, all the other connectors can be installed inside the board using 180° connectors.*
Thermal dissipation	*conduction cooling.*	
Environment temperature range	*-40°C to +85°C*	*Industrial temperature range.*

Table 1: mechanical and electrical standard specification

Parameter	Description	Note
Number of Analog channels	4	See mechanical specification for connector type.
ADC resolution	16 bits	
Input analog BW	From 450 to 550 MHz	The interest signal will be near from 500 MHz.
Full scale range	2.25 or 1.5 volts p-p	Programmable in the case of the LTC2208IUP.
Full scale drift	< ±60 ppm / °C	The typical specification of the LT2208IUP with external reference is four times better than this spec.
Crosstalk between channels	> 100 dB @ 500 MHz	Evaluated after raw data post processing.
ENOB @ 500 MHz	≥ 10 bits	-1 dBFS input signal (internal PLL clock).
SFDR @ 500 MHz	≥ 60 dBFS	-1 dBFS input signal (internal PLL clock).
SNR@500 MHz	≥ 65 dB	-1 dBFS input signal (internal PLL clock).

Table 2: analog Input signals and dynamic performance specification

Parameter	Description	Note
Int. ADC clock freq. (from internal PLL)	117.5 MHz	See details in the specific section.
ADC clock fine tuning.	Step ≤50 Hz, range of ±10 kHz	See details in the specific section.
Ext.ref. clock freq. input	0. 5 MHz to 20 MHz digital signal – 0 dbm typical.	50 Ω - single-ended AC-coupled.
Ext.ADC clock input	50 MHz to 130 MHz	See details in the specific section.
HF output	Sinusoidal = Ref. freq.*800 With fine tuning capability, amplitude control	See details in the specific section.
Digital Trigger in	LVCMOS or LVTTL	Single ended - AC coupled.
Digital Trigger out	LVCMOS or LVTTL	Single ended - AC coupled.
PLL controls	All controls must be available for the user.	

Table 3: clocks and triggers in/out specification

Parameter	Description	Note
Outputs electrical standard	*LVDS or LVCMOS*	*Must be compatible with Xilinx evaluation board. Part number: EK-V6-ML605-G.*
Desired controls	• *Full scale range (PGA 0 or 1)* • *Dither on/off* • *Power shutdown* • *Output randomizer on/off* • *Digital output mode and clock duty cycle stabilizer*	*If it is not possible to implement some control, the default operation should be:* • *PGA = 0* • *Dither off* • *Output randomizer off* • *Output mode = 2's complement* • *Duty cycle stabilizer on*
Desired monitoring options	• *Over/Under flow digital output* • *Temperature of the heatsink** • *Power supply health*	**Ideally, the temperature of the 4 ADCs should be monitored.*

Table 4: digital signals and control requirements.

Revision history

05/23/2012 V2.0 to V2.1

- Cover – included: e-mail address;
- Internal ADC clock circuit:
  - ✓ *Corrected: description about clock signal;*
- Internal High frequency oscillator section
  - ✓ *Included: spurious specification;*
- Table 1:
  - ✓ *Changed: analog BW specification;*
  - ✓ *Changed: SFDR specification;*
  - ✓ *Included: SNR specification;*

05/20/2012 - V1.1 to V2.0

- Main specification
  - ✓ *Excluded specification: "Fully compatible with Xilinx Virtex 6 development kit. Model: ML605";*
  - ✓ *Included: High frequency PLL oscillator with amplitude control and external reference locked;*
  - ✓ *Included: External Trigger input;*
  - ✓ *Included: External Trigger output;*
- Included: basic block diagram
- Included sections:
  - ✓ *Internal ADC clock circuit;*
  - ✓ *Internal high frequency PLL oscillator;*
- Table 1:
  - ✓ *Included in the front panel connections: HF output and digital triggers;*
  - ✓ *Included the desired SMA connector for analog inputs;*
- Table 3:
  - ✓ *Included HF output;*
  - ✓ *Included digital input/output specification;*
  - ✓ *Included the PLL controls.*

03/01/2012 – V1.0 to V1.1

- Board specification section: "suggested ADC" changed for "Required ADC".

03/28/2012 – V1.0

- Initial version.