# Introduction

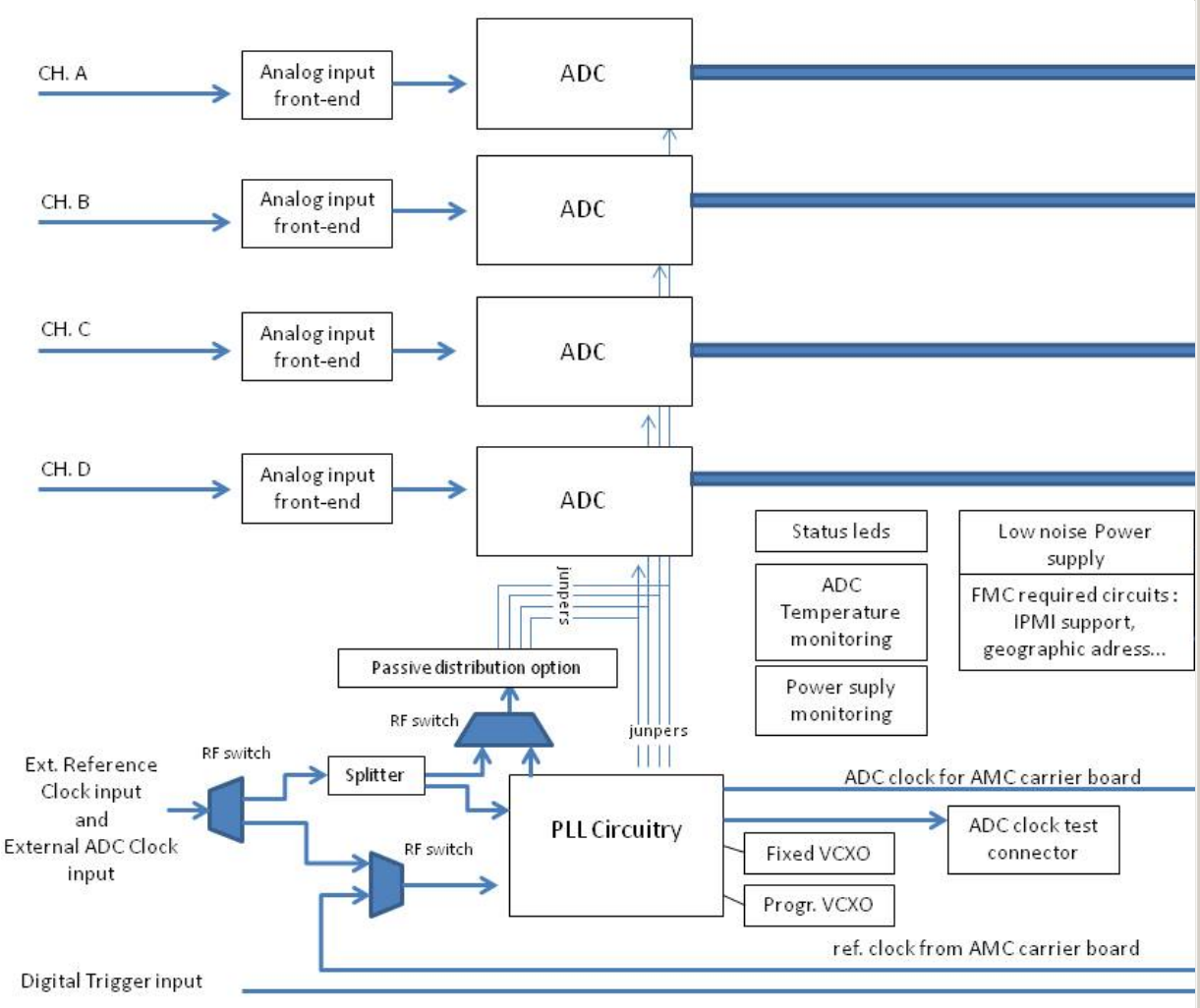
One of the most important goals in every light source is to achieve orbit stability for the electron beam within the required specifications for the stability of the photon beam in the experimental stations. Several technical challenges make the task of achieving sub-micrometer stability really demanding in terms of mechanical and electrical engineering. Fast feedback systems are employed to dump orbit distortions through accurate measurements of the beam positions, fast computation of the corrections and actuation back to the beam through fast power supplies and steering magnets. To realize this task in the *SIRIUS* **http://www.lnls.br**, the new brazilian synchrotron light source, a digital platform to measure the beam position is required. Inside this plattaform a key part is the analog to digital conversion. This text will describe the main specification for an FMC Analog-to-digital conversion board.

# Project description

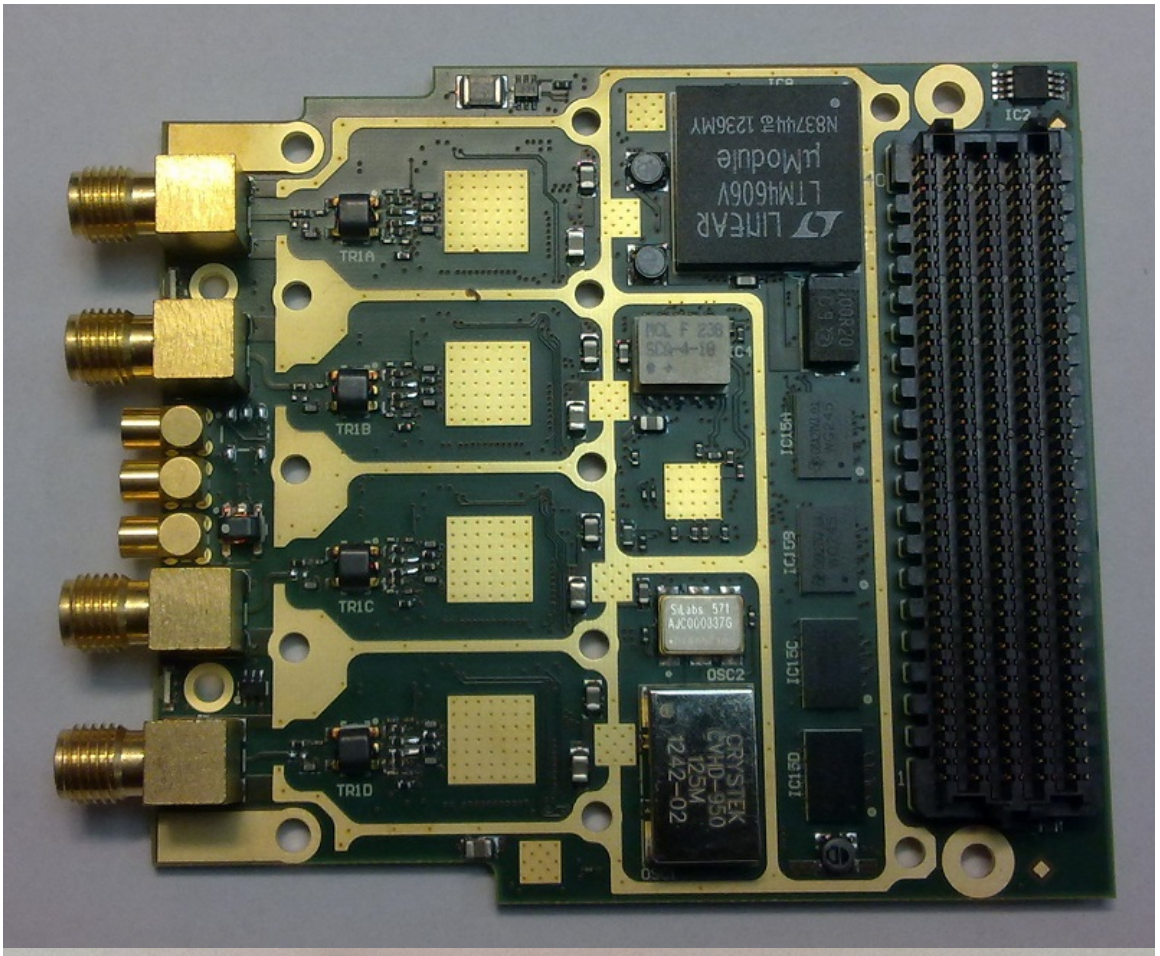
There are several commercial off-the-shelf digitizers covering a wide range of speed, bandwidth and resolution, but there is no board that cover all features required for the LNLS design.

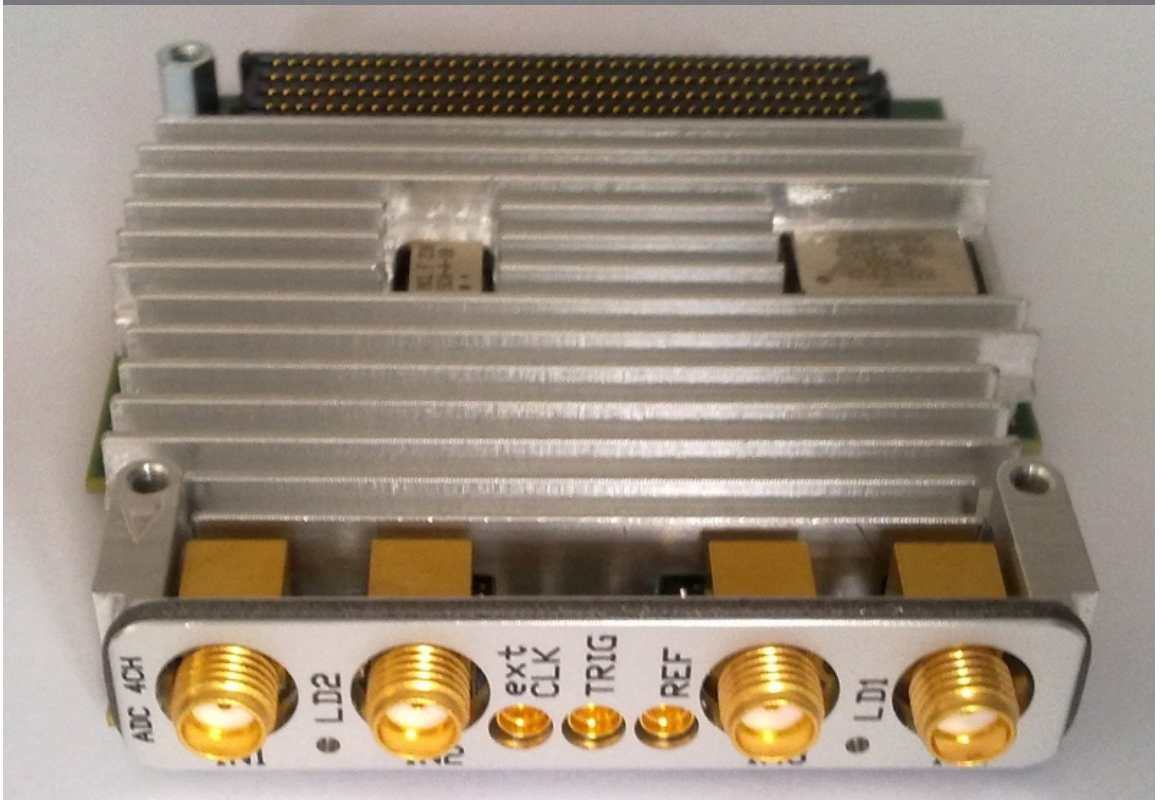
- VITA 57.1-2010 compliant
- Four Channel 16 bit 130 MSPS ADC. Required ADC: LTC2208IUP
- Internal ADC clock circuit: Phase locked to the external reference clock input with fine frequency tuning capability. See specific section. Hold mode in case of loss of external reference is a desirable feature.
- Internal high frequency PLL oscillator output with amplitude control and locked to external reference.
- External ADC clock input (50 MHz up to 130 MHz, 0 dBm typ.)
- External reference clock input: (0.5 MHz - 20 MHz digital signal, 0 dBm typ.)
- External digital Trigger input
- External digital Trigger output

# Block diagram




# Board drawing


LINEAR
LTM4606V
µModule
TR1A
TR1B
TR1C
TR1D
OSC2
CRYSTEK
CVHD-950
125M
1242-02


ADC 4CH
LD2
ext
CLK
TRIG
REF
LD1


# Status

| Date | Activity |
|---|---|
| 01/10/2011 | First sudies about necessities |
| 27/11/2011 | FMC standard choosed |
| 01/12/2011 | project stopped provisionally |
| 01/02/2012 | Discussion with FMC suppliers |
| 01/03/2012 | Commercial solution aborted=price vs desired features |
| 05/03/2012 | Project started at OHWR |
| 15/03/2012 | ADC choosed |
| 26/03/2012 | power dissipation solutions studied |
| 01/04/2012 | Clock frequency plan defined |
| 04/05/2012 | Specification document V1.0 done |
| 18/05/2012 | Discussions with OHWR companies about parallel development |
| 19/05/2012 | Discussions with Non OHWR companies about parallel development |
| 22/05/2012 | Start of block diagram design: clock schemes, PS, input stage,FMC interface,etc |
| 26/07/2012 | Many discussions with component manufacturers about details of implementation |
| 01/08/2012 | Start collaboration with WUT/Creotech for boards design (130 and 250 MSPS versions) |
| 22/10/2012 | Start schematics and discussions with WUT/Creotech |
| 22/11/2012 | Layout v1 70% done by LNLS - under revision and modification |
| 22/11/2012 | End of in-loco collaboration - layout sent to WUT/Creotech for refinements/layout optimization |
| ---------- | ---------- |
| 03/12/2012 | Decision of layout unification for reuse of heatsink in both boards |
| 06/12/2012 | Start of design modification, mechanical unification with FMC ADC 250M version |
| 19/12/2012 | Layout ready for review |
| 21/12/2012 | Fast review send from LNLS to WUT/Creotech |
| 01/01/2013 | Firmware verification and optimization to support the boards |
| 14/01/2013 | Bug found by OHWR user (7Solution) - power supply error in one IC |
| 30/01/2013 | Problems to find company to produce boards with some copper filled vias |

| | |
|---|---|
| 12/02/2013 | Pre-assembled boards received by WUT/Creotech |
| 14/02/2013 | Start basic tests |
| 26/02/2013 | Waiting for panels and heatsink - 2 weeks estimated |
| 20/03/2013 | Panels received |
| 30/03/2013 | Heatsinks received |
| 26/04/3013 | FMC ready, tested and assembled |

**diagramas_em_blocos_generico.jpg** (74,5 KB) Fernando Henrique Cardoso, 10/09/2012 19:30
**top.png** (320,9 KB) Grzegorz Kasprowicz, 19/12/2012 03:16
**bottom.png** (390,3 KB) Grzegorz Kasprowicz, 19/12/2012 03:17
**bot_r.jpg** (188,4 KB) Grzegorz Kasprowicz, 01/03/2013 20:28
**top_r.jpg** (478,4 KB) Grzegorz Kasprowicz, 01/03/2013 20:28
**top_r.jpg** (221,2 KB) Grzegorz Kasprowicz, 01/03/2013 20:28
**fmc_bot.jpg** (211,2 KB) Grzegorz Kasprowicz, 26/04/2013 17:19
**fmc_top.jpg** (146,2 KB) Grzegorz Kasprowicz, 26/04/2013 17:19