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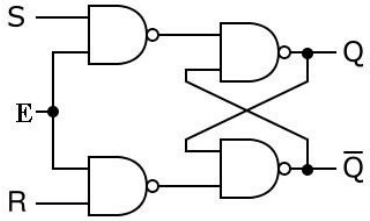
ICS 51 Homework 2
Due: Tuesday, March 11, 2014, at 11:55 pm

1. **[Sequential Elements]**

Given the following implementation of a gated(clocked) S-R latch,



fill in its truth table. [8 pts]

E	Q_t	S_t	R_t	Q_{t+1}
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	?

1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	?

*** use "?" for undefined state.**

**** Q_t, S_t, R_t are the values of Q, S and R at time t, while Q_{t+1} is the value of Q at time t+1.**

2. [Sequential Logic]

(a) Answer the following questions regarding SR and D latch. [6 pts]

i. Briefly enumerate the differences between an SR latch and a clocked D latch.

D Latches' only require one input when compared to SR latches.

ii. What problems of the SR latch does the clocked D latch solve?

It fixes the instability issue with SR latches, when both S and R are 1.

iii. What do "S" and "R" stand for? Explain what these two signals do in the context of an SR latch.

S stands for Set and R stands for Reset. S will set state to 1 and R will set the state to 0.

(b) Briefly discuss the differences between the way a clocked D latch works and the way an edge-triggered D flip-flop works. [3 pts]

Clocked D latches work when the clock is at a stable 1, but for edge-triggered D flip-flops, they take the clock input when the clock transitions from 0 to 1, which is easier and faster to read.

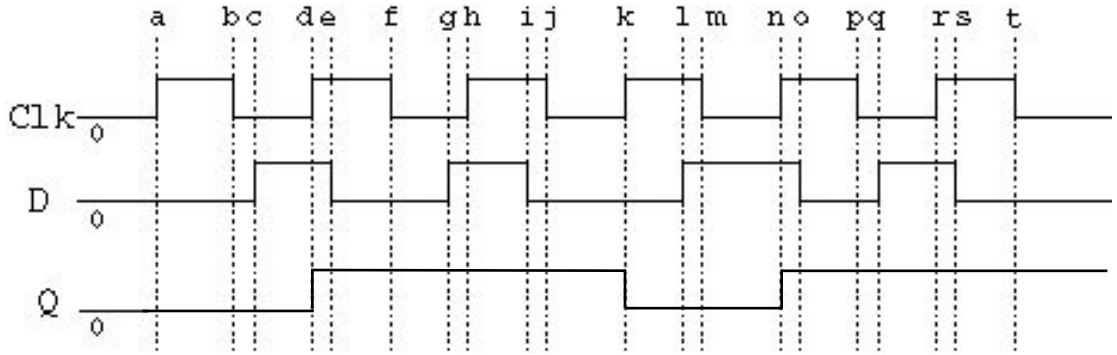
3. [Sequential Elements]

**** Assume NO time delay for transitions**

(a). D flip flop (positive edge triggered)

D	Q
0	0
1	1

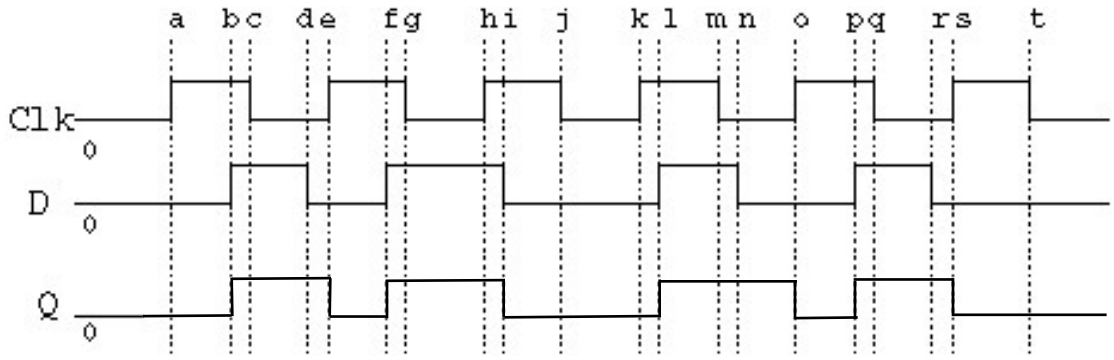
Draw the Q output in the timing diagram: [10 pts]



(b). Clocked D latch:

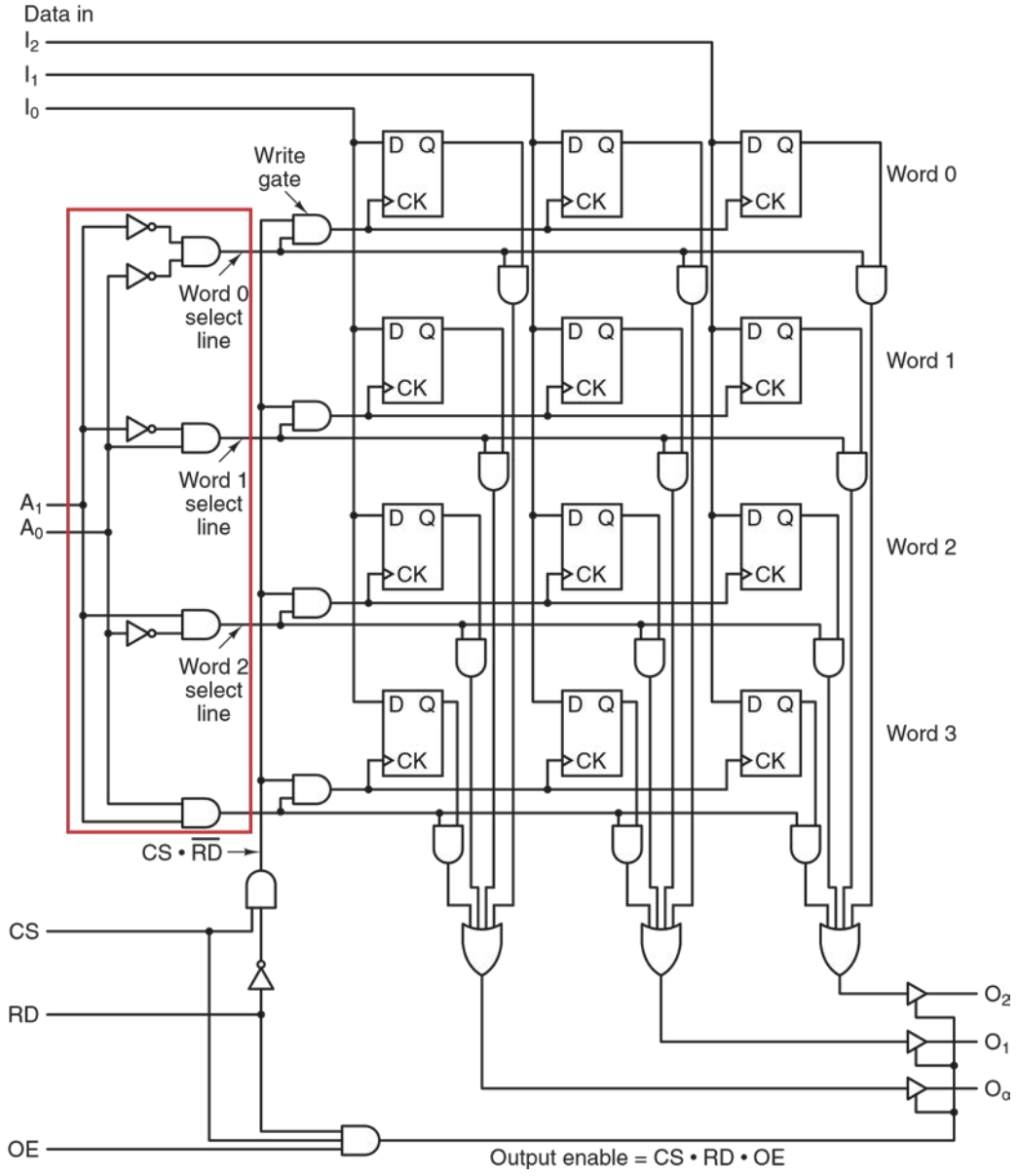
Clk	D	Q
1	0	0
1	1	1
0	x	last Q

Draw the Q output in the timing diagram: [10 pts]



4. [Memory Organization]

The following graph is the Figure 3-28 on page 176 of the textbook. (If you are using edition 5, it's Figure 3-29 on page 166.)



(a) What is the name of the circuit component bounded by the red box? [3 pts]

Two to Four Decoder

(b) In order to write the data on $\mathbf{I_0}$,$\mathbf{I_1}$,$\mathbf{I_2}$ to memory word 2, what should the signal be on $\mathbf{A_1}$,$\mathbf{A_0}$,**CS**,**RD** and **OE**? [5 pts]

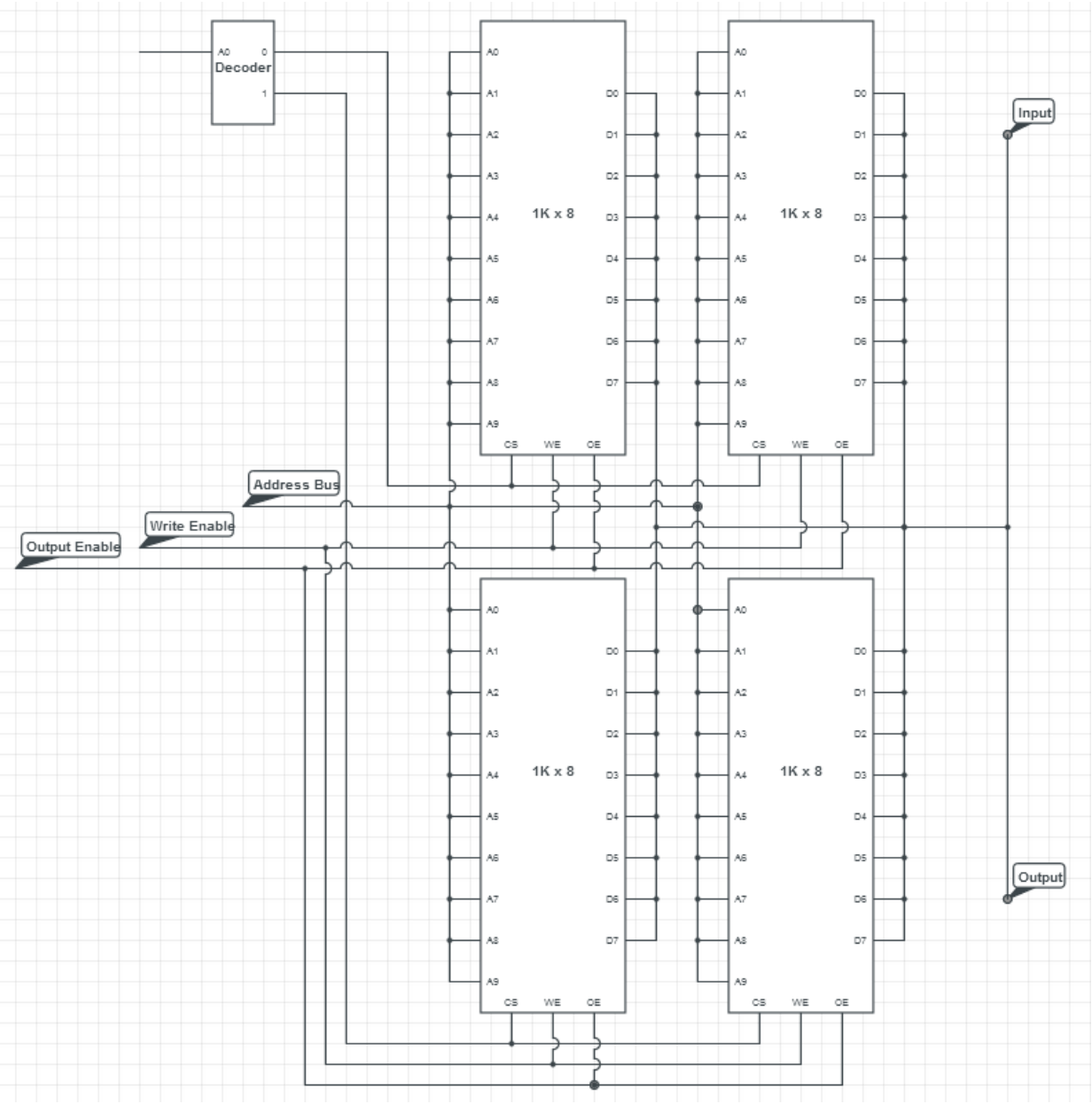
$A_1 = 1$, $A_0 = 0$, CS = 1, RD = 0, OE, = 1 or 0

5. [Memory Organization]

Build a 2K × 16 bit ROM using any number of 1K × 8 bit ROMs. Clearly show the control circuitry. [10 pts] Hint:

1 The block you use to represent 1K × 8 ROM should have and 10-bit wide address input, a chip-select (CS) input, and a 8-bit wide data output.

2 You may assume that there are tristate noninverting buffers controlled by the Chip Select signal that control the output of each 1K x 8 bit ROM.


A0
0
Decoder
1
1K x 8
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
D0
D1
D2
D3
D4
D5
D6
D7
CS
WE
OE
Input
Address Bus
Write Enable
Output Enable
Output

6. [Random Access Memory]

Briefly discuss the characteristics of static RAM vs. the characteristics of dynamic RAM in the following aspects: [8 pts]

(a) Basic storage element.

Static RAMs are made of D flip-flops while Dynamic RAMs are made of transistors and capacitors.

(b) Access speed / clock frequency.

Static RAMs are very fast, typical access time of about a nanosecond or less. Dynamic RAMs are slower with access in the tens of nanoseconds.

(c) Density / capacity.

Static RAMs are not as dense as they need six transistors per bit, while dynamic RAMs only need 1 transistor per bit. So dynamic RAMs are larger and used for main memory, while static RAMs are smaller and are used for cache memory.

(d) (d) Refresh.

Static RAMs keep their states as long as power is applied. For dynamic RAMs, they need to be refreshed every few milliseconds to prevent data from leaking away.

7. [Magnetic Disks]

(a) Define the following terms (one sentence each): [5 pts]

i. Track

Sequence of bits having same radius on disk.

ii. Cylinder

Set of tracks with same radius on many platters.

iii. Sector

Fixed length of segment within a track.

iv. Seek time

How much time it takes to position the head over a track.

v. Rotational latency

How much time it takes for a disk to rotate to desired sector.

(b) A certain hard disk has 320 platters, 10 tracks per platter, and 31 sectors of 1024 bytes each per track. It spins at 5400 revolutions per minute (RPMs), and has an average seek time of 35 msec, and a data transfer rate of 20 MB/second.

i. What is the total available storage capacity of the disk? [4 pts]

1024 x 31 x 10 x 320 = 101,580,800 bytes

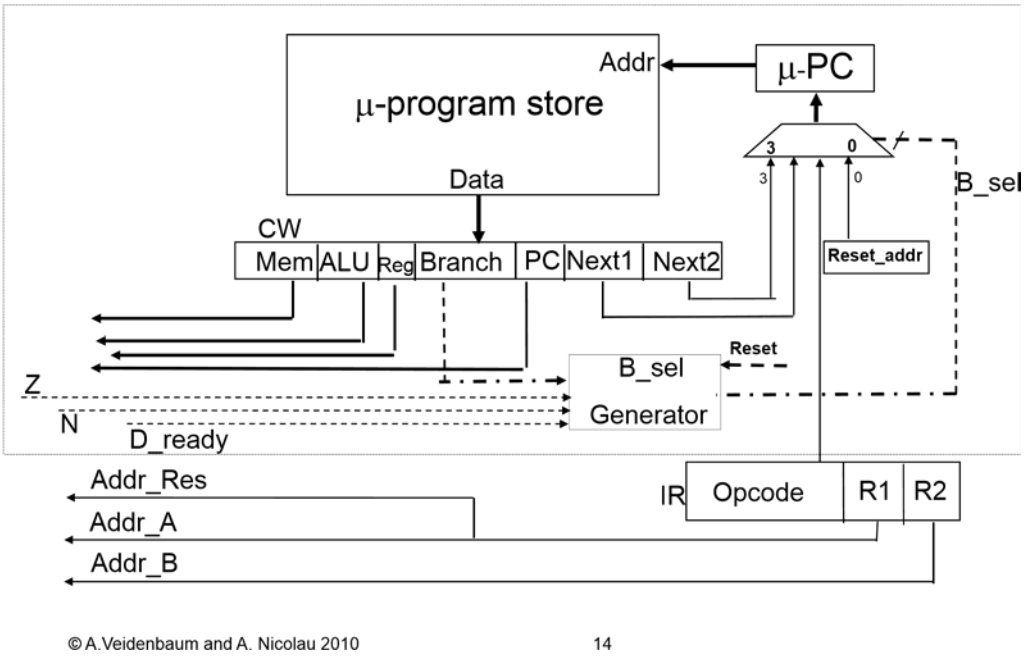
ii. What is the average time required to read 5 consecutive sectors from a random track? [4 pts]

Read speed is 20971520 bytes/second or about 20971 bytes/ms.
5400 RPM = 90 RPS = 1 revolution in 1/90 of a second. Half a revolution is the delay, which equals 5.5 ms
5 sectors equal 1024 x 5 = 5120 bytes.
Average seek time is 35 ms, plus 5.5 ms for rotational latency, plus 0.25 ms to read 5 sectors equals 40.75 ms.

8. [Microcode]

The following diagram is from the slide #14 of lecture #12. Please answer the questions based on this diagram. [12 pts]

Microcode Engine Organization



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(a) The branch field contains 4 bits: **N, Z, Opcode, D ready**. Explain the function of the **N** and **Z** bit in the branch fieldx.

N is the Negative flag, which results from a negative.
Z is the Zero flag, which results from a zero.

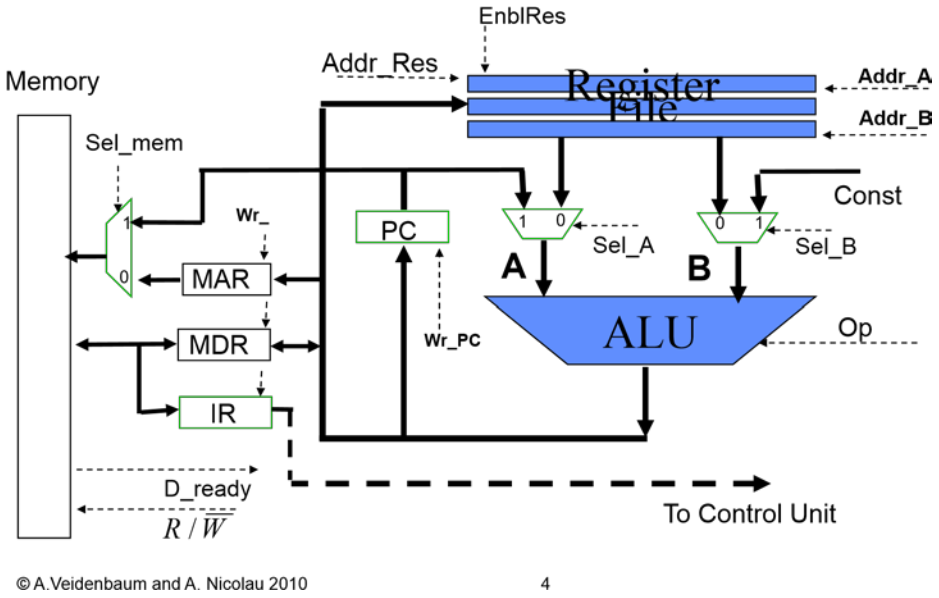
(b) Explain how the microcode branch engine is used by JZ instruction.

The JZ instruction takes two operands and subtracts them and sets the Z flag if the result is zero and jumps to the corresponding branch.

(c) Explain how the microcode branch engine is used by MUL instruction.

MUL uses OF and CF flags to determine when 2 registers has been filled.

The following diagram is from the slide #4 of lecture #12. Please answer the questions based on this diagram. [12 pts]



Based on the datapath shown above, fill in the proper control signals to achieve the operation in the left-most column. You can use "X" to represent "don't care" signals.

Operation	R/$\tilde{W}$	Sel-M	Wr-MAR	Wr-MDR	Wr-IR	EnblRes	Addr-A	Addr-B	Sel-A	Sel-B	Op	wr-PC
IR ← Mem [PC]	1	1	0	0	1	X	X	X	X	X	X	X
MDR ← Mem [MAR]	1	1	0	1	0	X	X	X	X	X	X	X
PC ← PC + Const	X	X	X	X	X	0	1	1	1	1	ADD	1