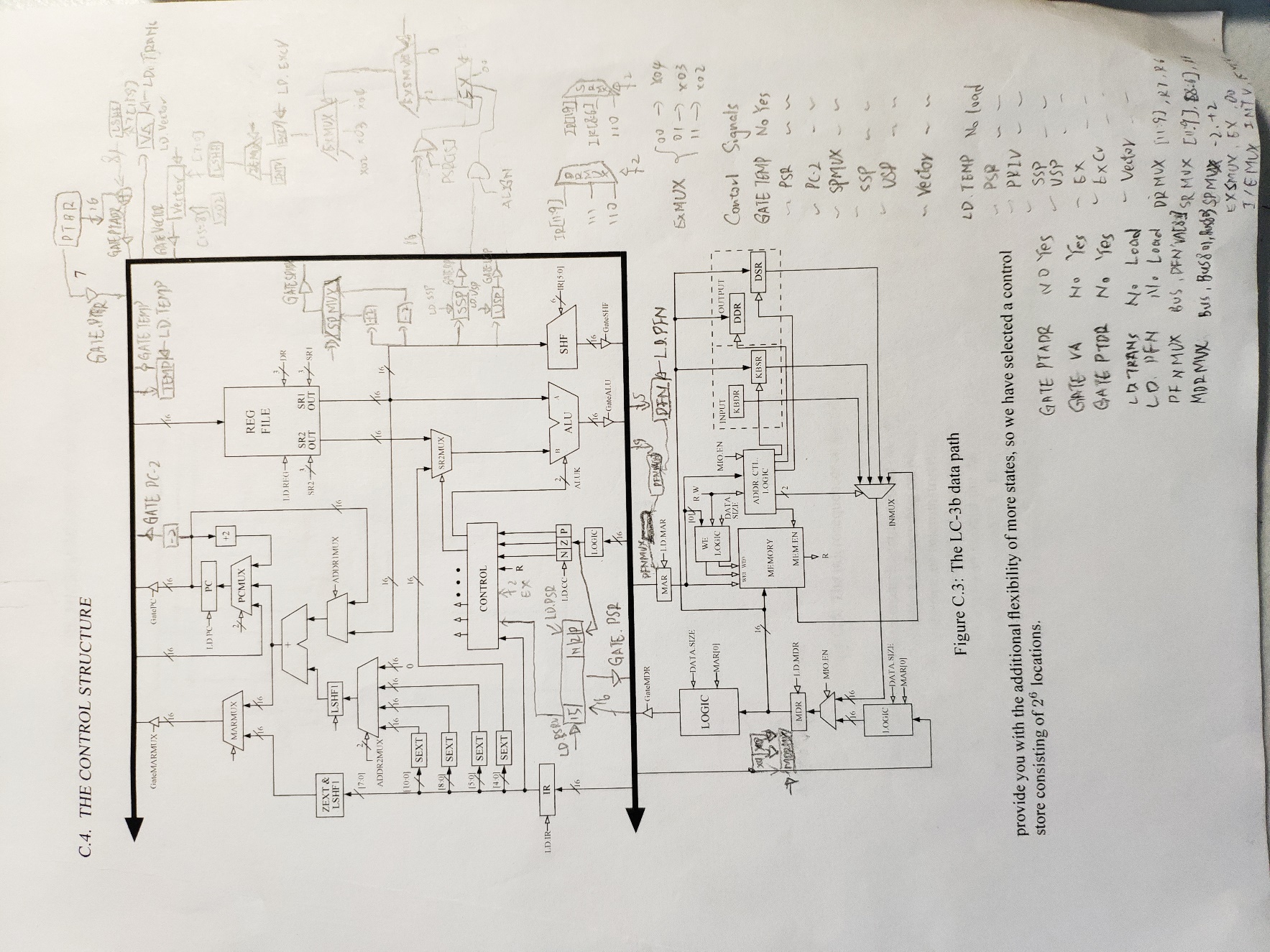
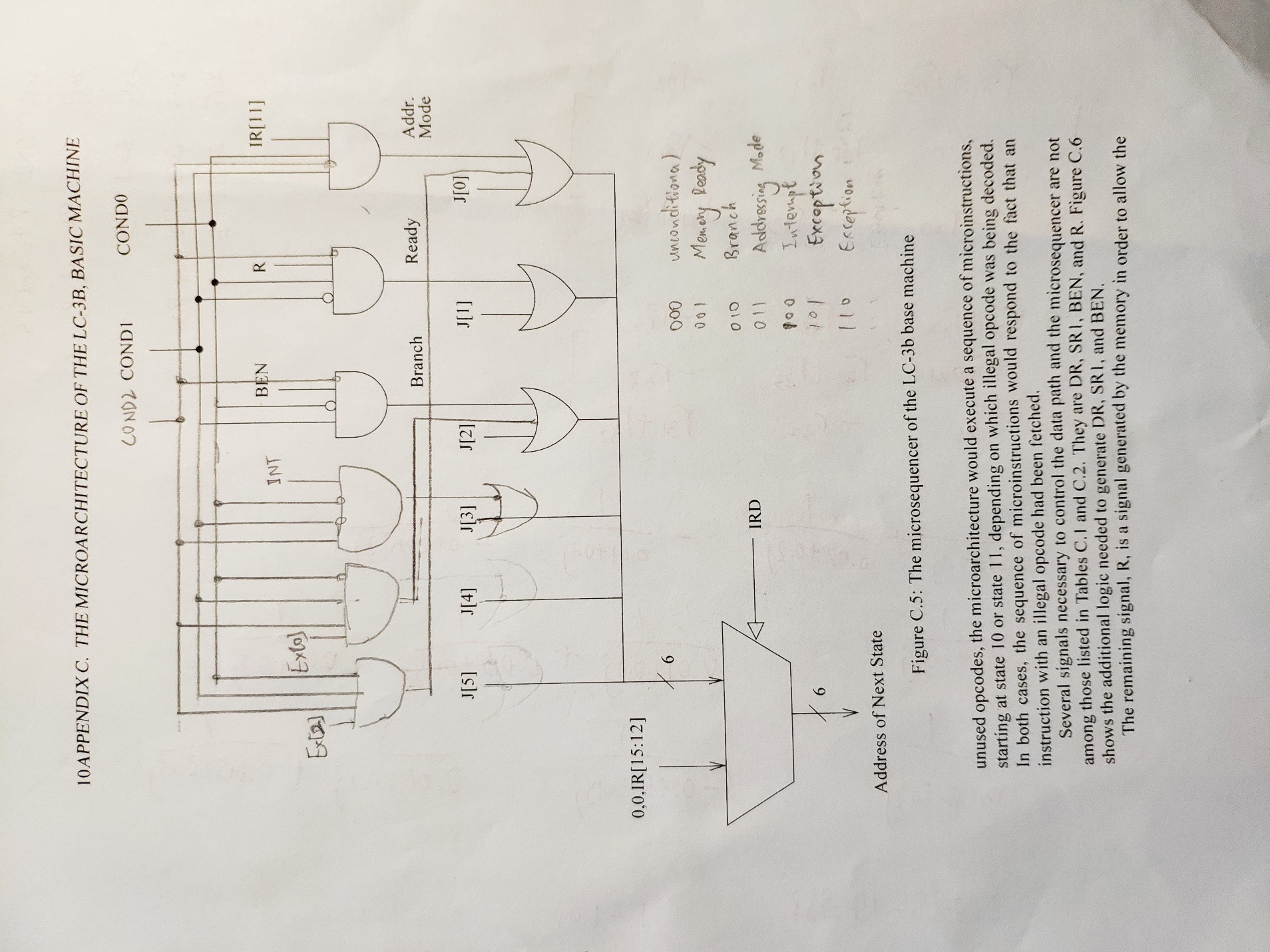


The memory translation is achieved by states starting from 26 and 34. Loads start at state 34 and store begin at state 26. They are separated because the modify bit is only set when there is a store. The unaligned access exception is checked along with the load of address of PTE. The page frame number is saved to obtain the physical address of data. Then it goes back to the normal states to complete the memory access with actual address.



Several new control signals and registers have been added to achieve address translation. PTBR is used as page table base register and it is controlled by GatePTBR. VA stores the virtual address and GATEVA drives the bus with the address stored in VA register. PFN is used to store the page frame number once it is gotten from memory and it is loaded with LD.PFN. When PFNMUX is set, MAR[8:0] is loaded from the bus with VA[8:0] and the higher bits MAR[13:9] is loaded with the PFN.



In this design, we have more conditions than before. Only 2 condition bits are not enough so we have to add one more condition bit. The six conditions are shown in the picture.