

高级练习2 基于 A7 的 DDR3 SDRAM IP 写实现

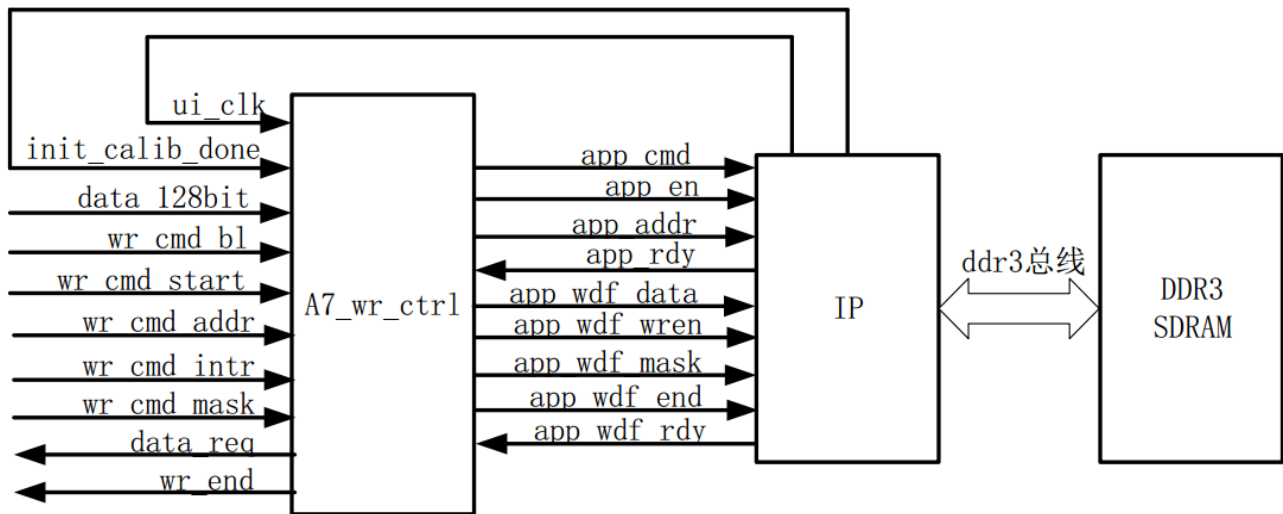
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高级练习2 基于 A7 的 DDR3 SDRAM IP 写实现

一、练习内容

DDR3 SDRAM IP写时序实现

二、系统框图



三、设计分析

1. 时序分析

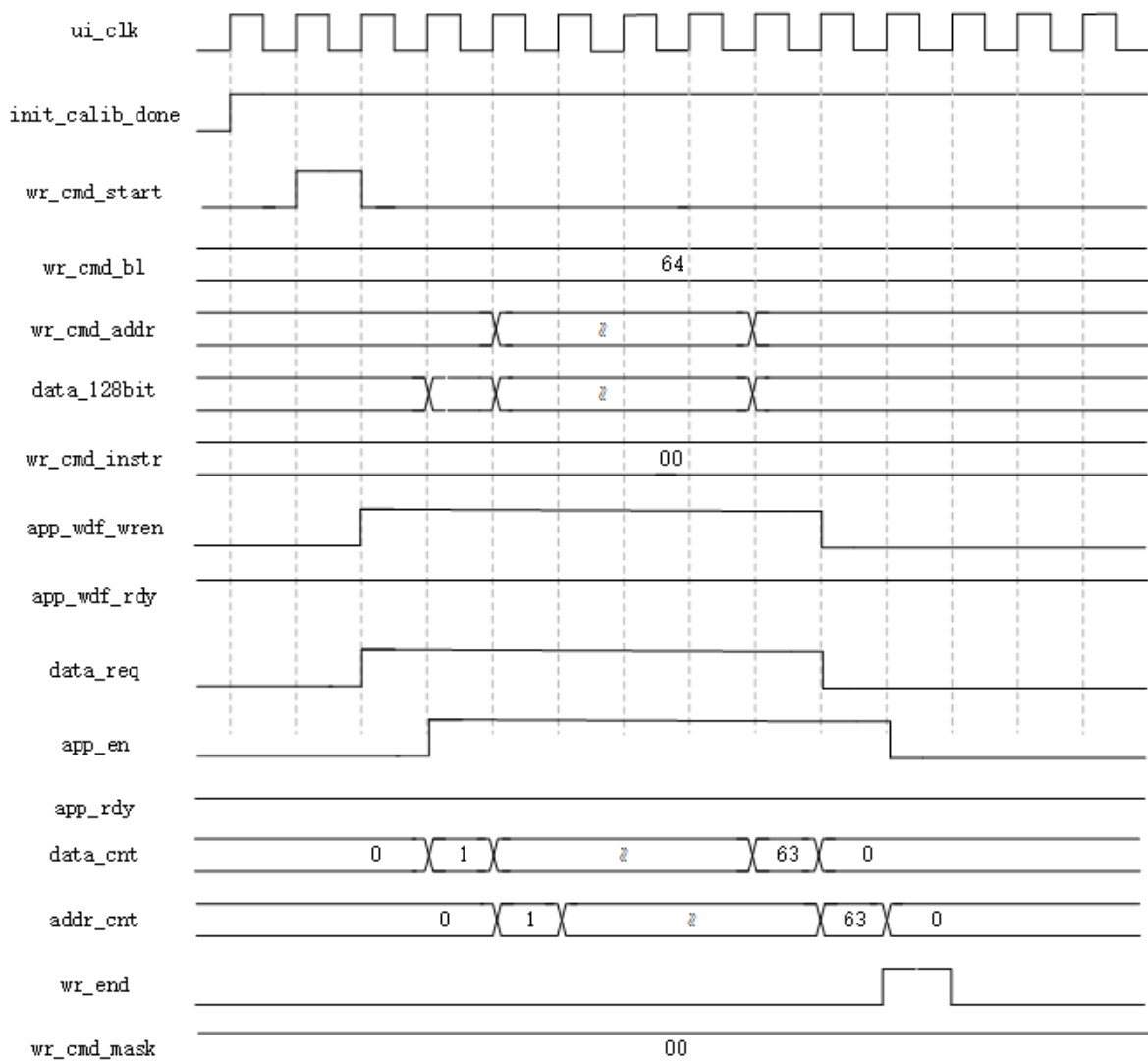
采用第2种实现方式，先写入数据，再写入地址，具体参考设计文档。

关键时序点需要把握。

(1) wr_cmd_start控制一次写突发的开始，相应的突发长度由wr_cmd_bl控制。

(2) 写入的数据由data_req发送请求，同时data_req由app_wdf_rdy和app_wdf_wren共同控制，两者都有效时发送请求，同时写入数据。

(3) wr_end是在写完最后一个数据后，拉高一个时钟周期后拉低，作为一次写入操作结束的标志。



根据关键点的时序，绘制成如上图所示的时序波形图。

四、练习步骤

1. A7_wr_ctrl模块程序编写

- (1) 把握输入输出信号
- (2) 把握关键时序点和关键信号

2. testbench文件测试

- (1) 实例化模块中信号的引入和输出

• 信号的引入

```
//output
force sclk = inst_ddr3_hdmi.inst_A7_wr_ctrl.clk;
force rst = inst_ddr3_hdmi.inst_A7_wr_ctrl.rst;
force data_req = inst_ddr3_hdmi.inst_A7_wr_ctrl.data_req;
```

• 信号的输出

```
//input
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_start = wr_cmd_start;
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_b1 = wr_cmd_b1;
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_addr = wr_cmd_addr;
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_instr = wr_cmd_instr;
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_mask = wr_cmd_mask;
```

```
force inst_ddr3_hdmi.inst_A7_wr_ctrl.data_128bit = data_128bit;
```

- 数据的控制

```
task gen_data;
    integer i;
    begin
        @ (posedge data_req);
        for (i = 0; i < 64; i = i + 1)
            begin
                if (data_req == 1'b0)
                    i = i - 1;
                data_128bit = i;
                @ (posedge sclk);
            end
        data_128bit = 0;
        @ (posedge sclk);
    end
endtask
```

五、实际波形仿真

1. 编译后，使用modelsim仿真。

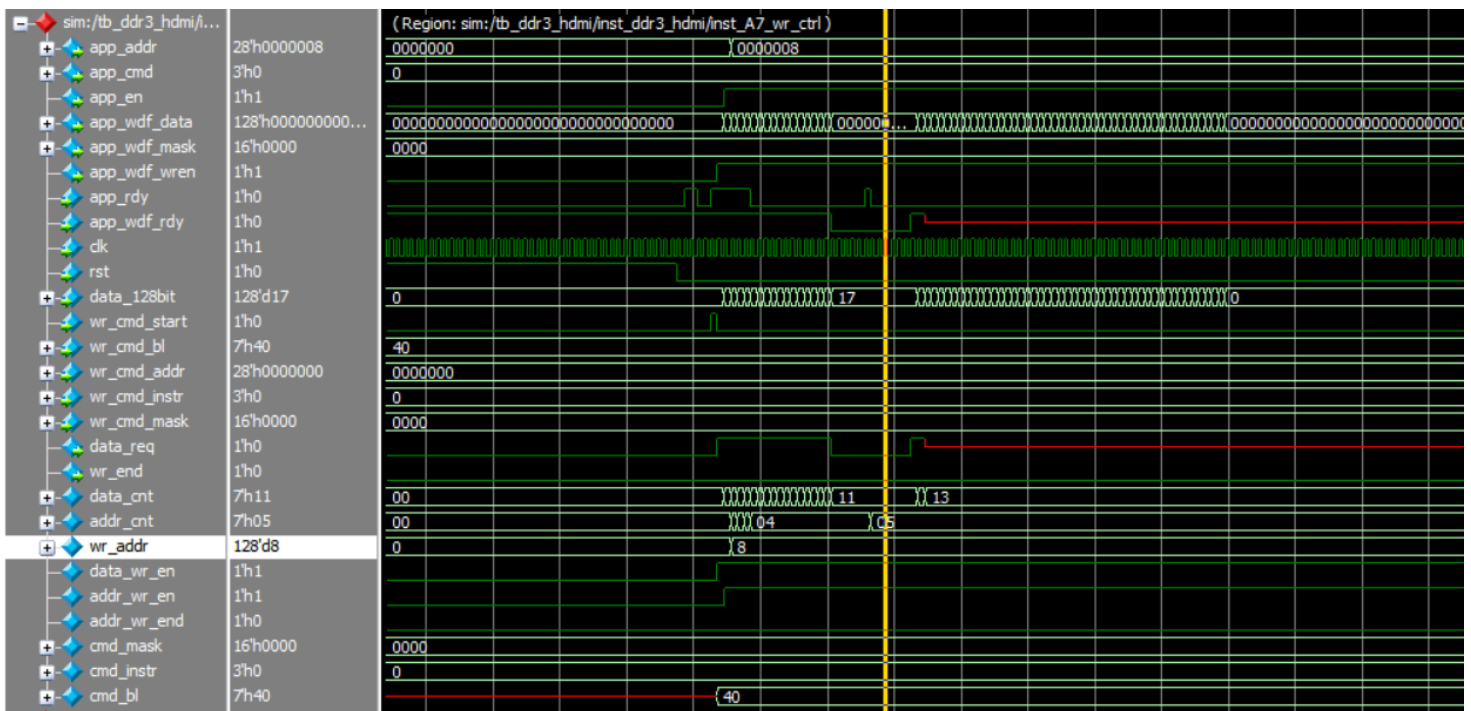
(1) 首先，查看是否能够产生数据。

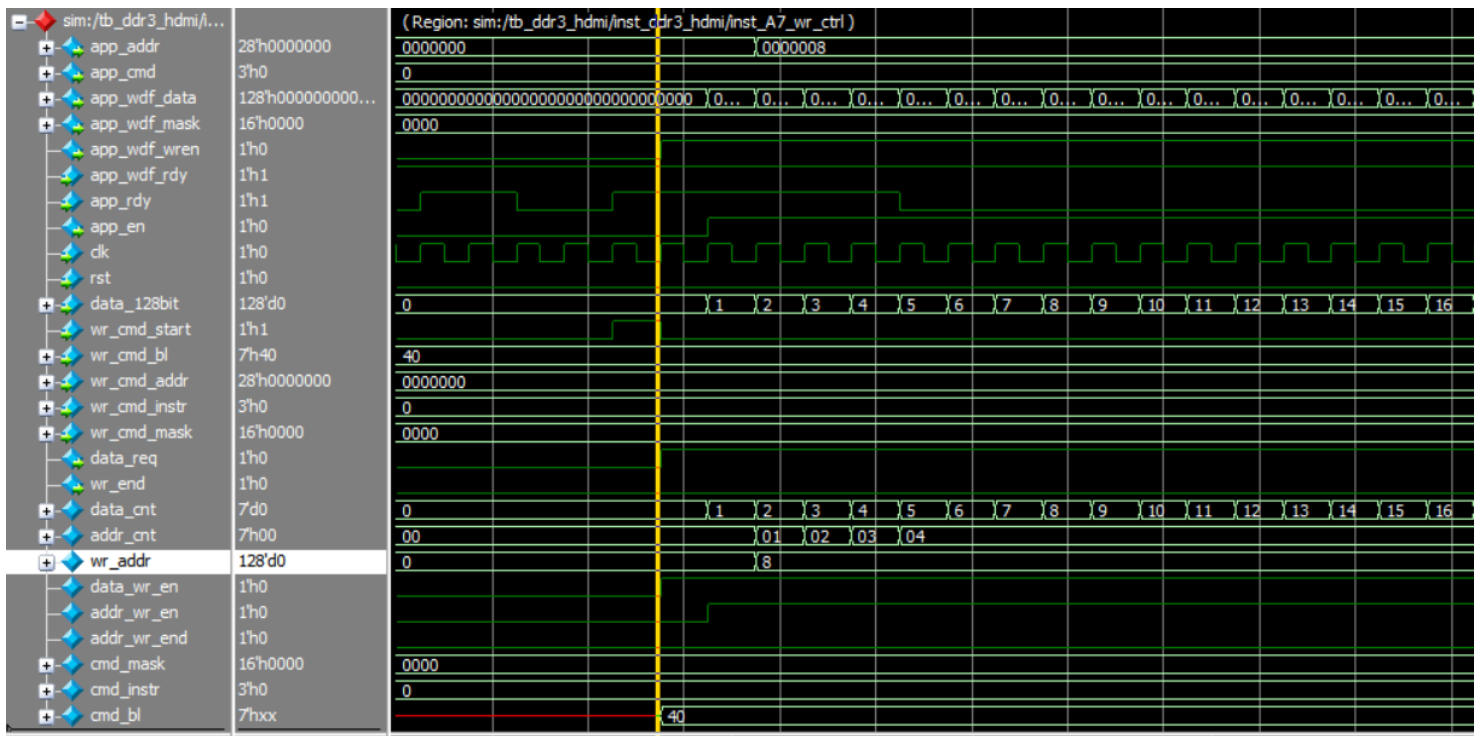
gen_data任务中的i变量如下变化，故能产生相应的值。



(2) 查看整个程序的执行是否有问题。

- 我们发现ddr3_wr_ctrl中的app_wdf_rdy信号出错，如下图所示。





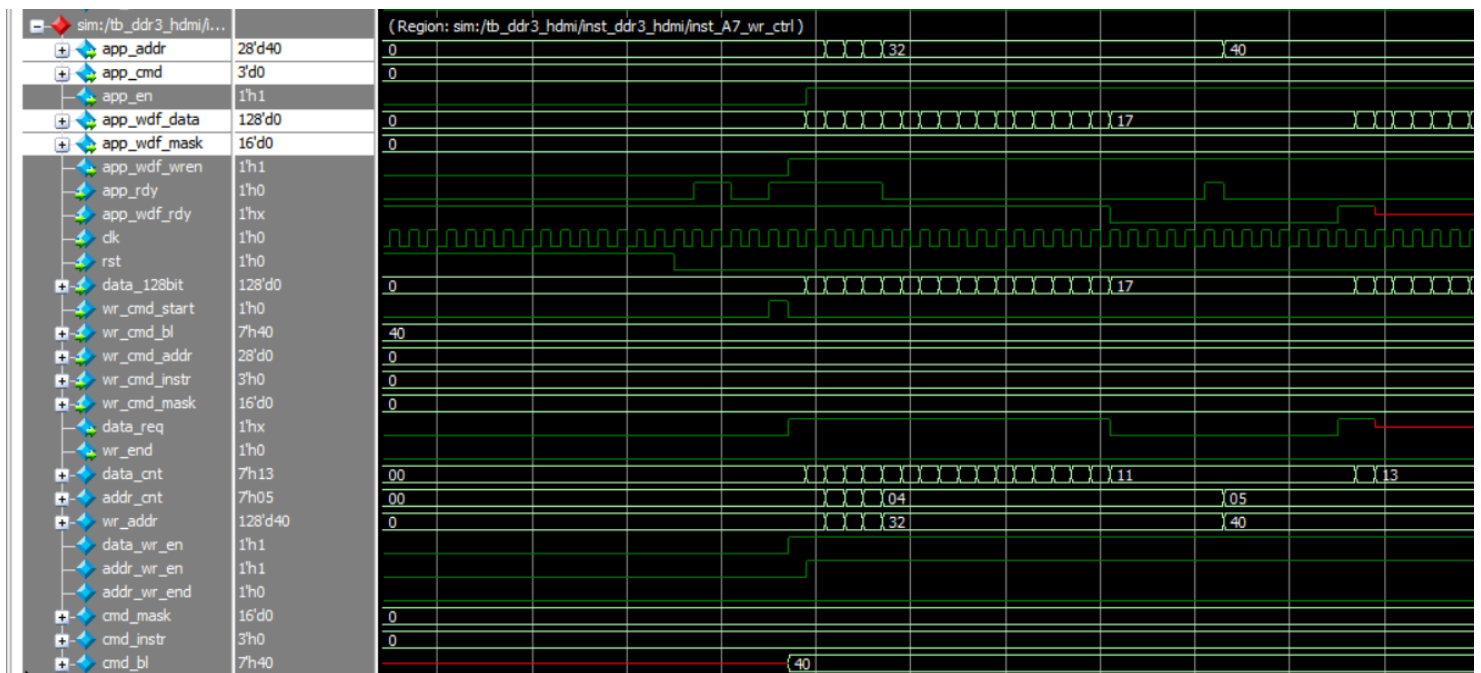
查看对应的代码，出现问题。

```

103 always @ (posedge clk)
104 begin
105     if (rst == 1'b1)
106         wr_addr <= 'd0;
107     else if (wr_cmd_start == 1'b1)
108         wr_addr <= wr_cmd_addr;
109     else if (app_rdy == 1'b1 && app_en == 1'b1)
110         wr_addr <= wr_cmd_addr + 'd8;
111 end

```

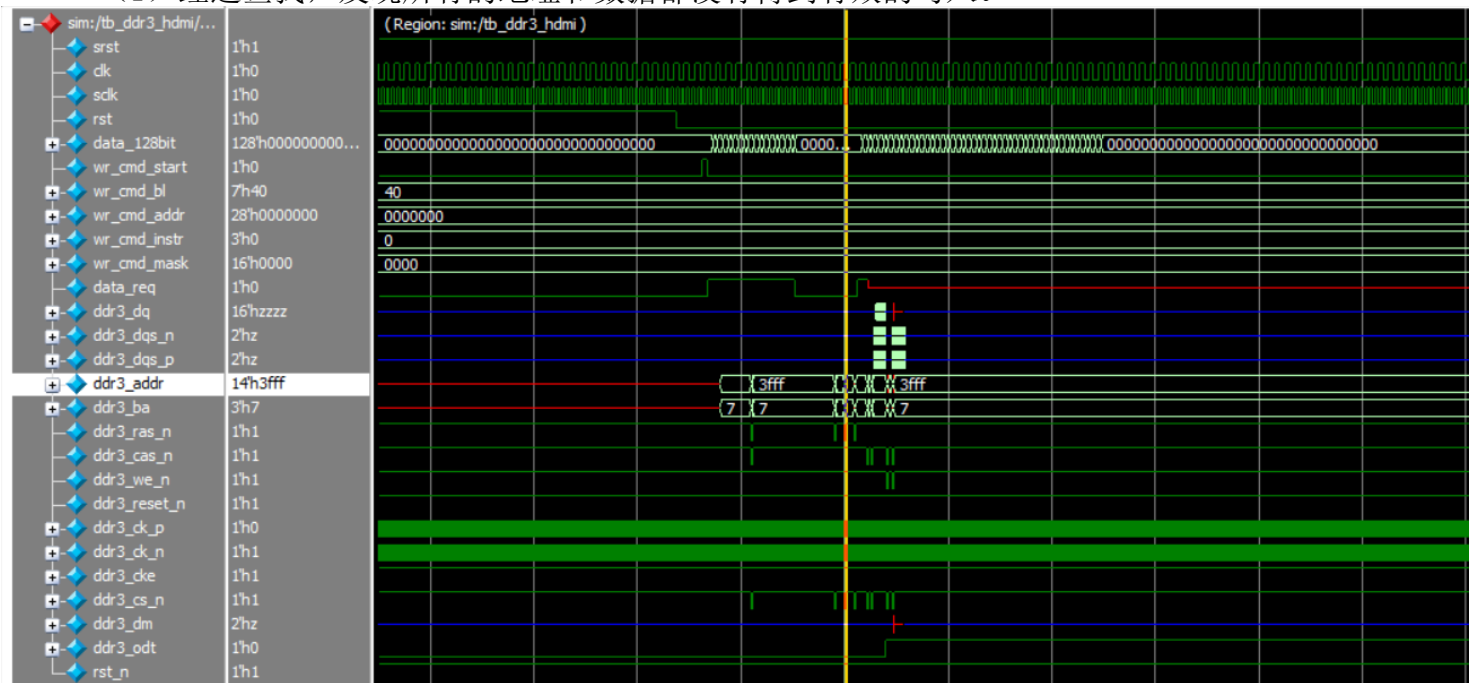
- 修改代码后，重新进行仿真，查看结果。



发现不是地址的问题，这问题依然存在。

2. 查找问题

(1) 经过查找，发现所有的地址和数据都没有得到有效的写入。



同时，modelsim中存在如下的报错，即端口数据位数不匹配的问题。

```
# Loading work.A7_wr_ctrl(fast)
# Loading work.glbl(fast)
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/new/ddr3_hdmi.v(56): [PCDPC] - Port size (28) does not match connection size (1) for port 'app_addr'. The port definition is at: ../../../../ddr3_hdmi.s
rcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v(92).
# Time: 0 fs Iteration: 0 Instance: /tb_ddr3_hdmi/inst_ddr3_hdmi/u_ddr3_ctrl File: ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/new/ddr3_hdmi.v(56): [PCDPC] - Port size (3) does not match connection size (1) for port 'app_cmd'. The port definition is at: ../../../../ddr3_hdmi.s
rcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v(93).
# Time: 0 fs Iteration: 0 Instance: /tb_ddr3_hdmi/inst_ddr3_hdmi/u_ddr3_ctrl File: ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/new/ddr3_hdmi.v(56): [PCDPC] - Port size (128) does not match connection size (1) for port 'app_wdf_data'. The port definition is at: ../../../../ddr3_h
dmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v(95).
# Time: 0 fs Iteration: 0 Instance: /tb_ddr3_hdmi/inst_ddr3_hdmi/u_ddr3_ctrl File: ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/new/ddr3_hdmi.v(56): [PCDPC] - Port size (16) does not match connection size (1) for port 'app_wdf_mask'. The port definition is at: ../../../../ddr3_h
dmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v(97).
# Time: 0 fs Iteration: 0 Instance: /tb_ddr3_hdmi/inst_ddr3_hdmi/u_ddr3_ctrl File: ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/new/ddr3_hdmi.v(56): [PCDPC] - Port size (128) does not match connection size (1) for port 'app_rd_data'. The port definition is at: ../../../../ddr3_h
dmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v(99).
# Time: 0 fs Iteration: 0 Instance: /tb_ddr3_hdmi/inst_ddr3_hdmi/u_ddr3_ctrl File: ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/ddr3_ctrl.v
# ** Warning: (vsim-3015) ../../../../ddr3_hdmi.srcs/sources_1/ip/ddr3_ctrl/ddr3_ctrl/user_design/rtl/phy/mig_7series_v4_1_ddr_mc_phy_wrapper.v(1579): [PCDPC] - Port size (1) does not match connection size (32) for
```

(2) 查看verilog中的代码，发现没有添加相应的信号接线，这样的话，默认就是移位数据位，这样是会出错的。

```
49 wire [27:0] app_addr;
50 wire [2:0] app_cmd;
51 wire app_en;
52 wire [127:0] app_wdf_data;
53 wire app_wdf_end;
54 wire [15:0] app_wdf_mask;
55 wire app_wdf_wren;
56 wire [127:0] app_rd_data;
57 wire app_rd_data_end;
58 wire app_rd_data_valid;
59 wire app_rdy;
60 wire app_wdf_rdy;
61 wire app_sr_active;
62 wire app_ref_ack;
63 wire app_zq_ack;
```

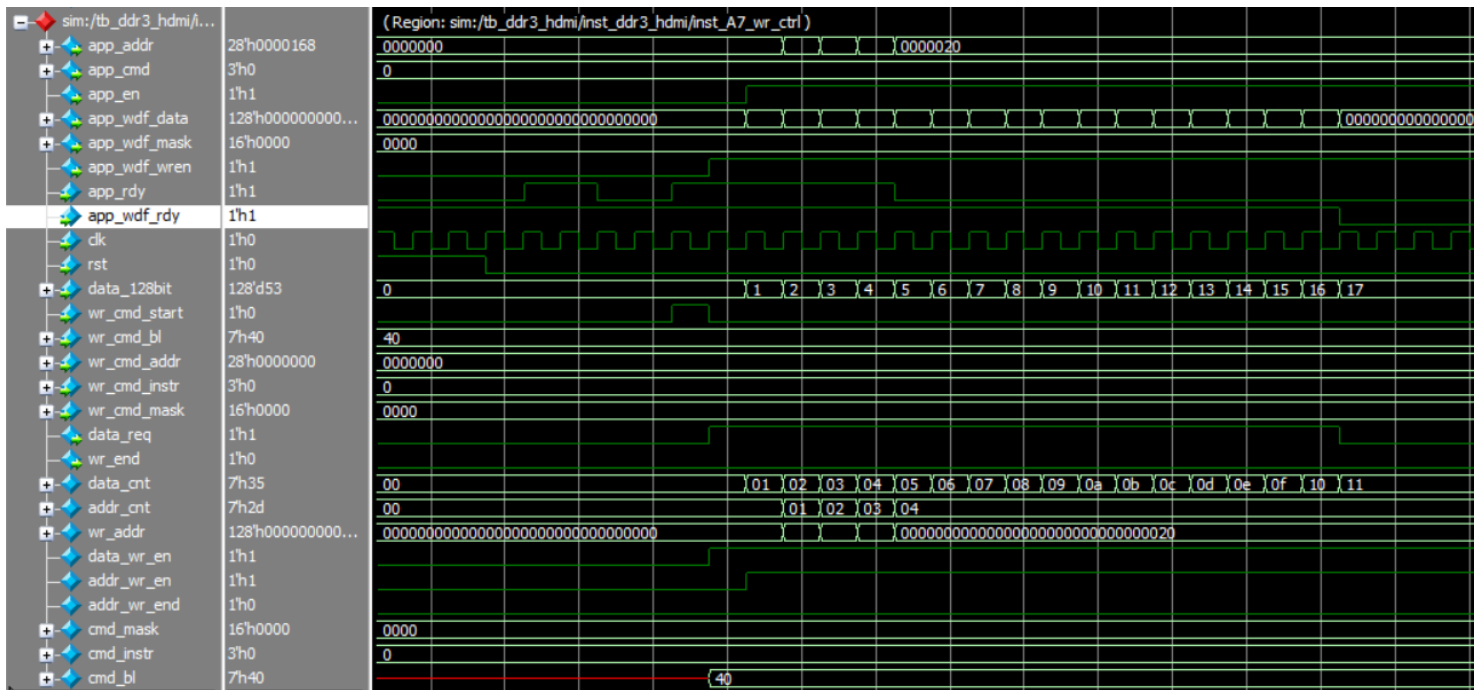
添加相关信号后，重新编译，查看仿真结果。

3. 查看结果

前面已经保证了整个程序的初始化过程，没有问题。

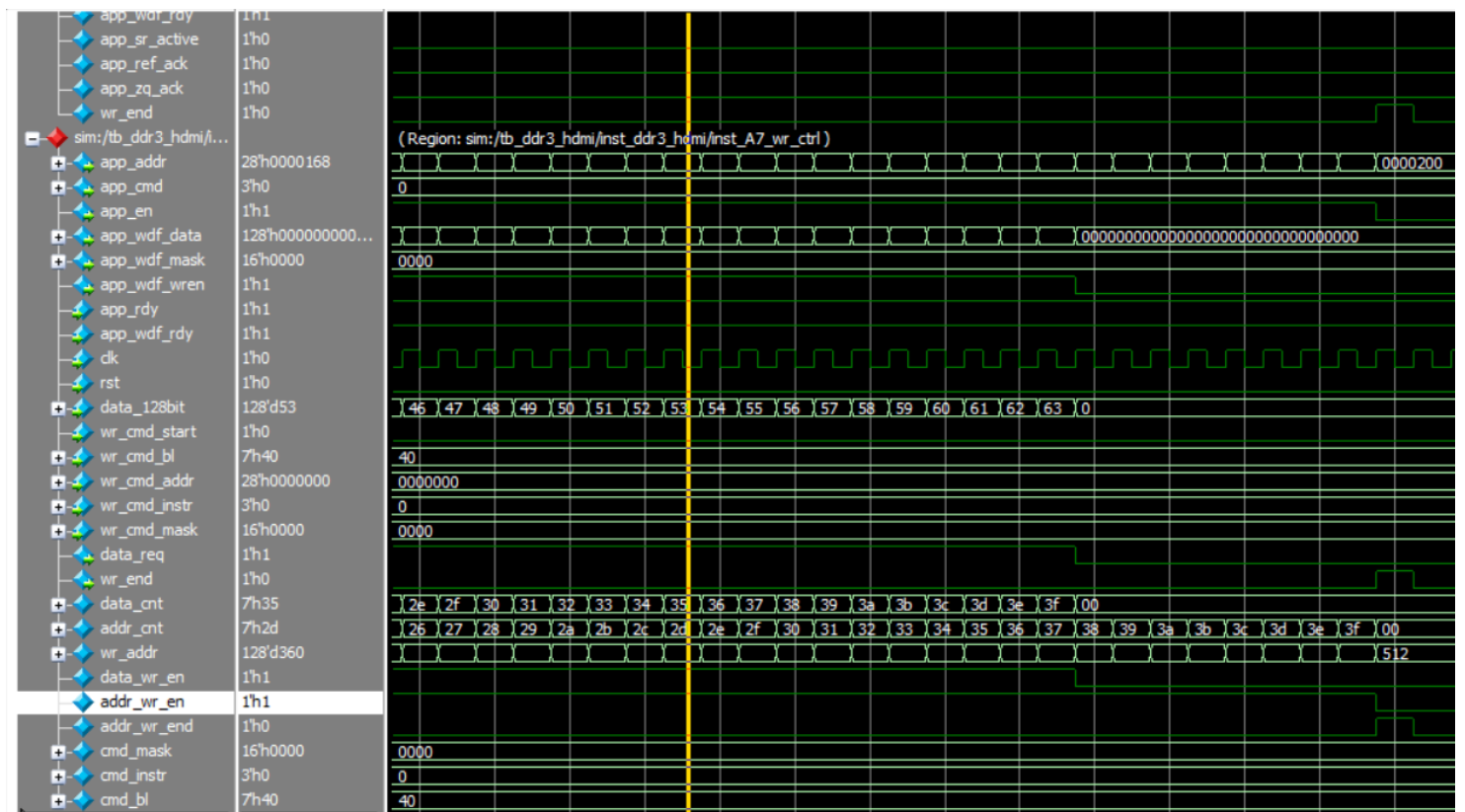
(1) 起始控制信号是否正确

- 起始控制信号wr_cmd_start拉高一个时钟周期后，相应的数据锁存，包括app_wdf_mask, app_cmd, cmd_bl等。
- 相应的addr_cnt和data_cnt在正确的控制条件下，开始进行计数，同时，相应的地址和数据即使写入到ddr中。



(2) 后期数据和地址写入是否正确

- data_cnt是否计数到63后清零，相应的data_wr_en和data_req是否也在这时刻清零。
- data_cnt是否计数到63后清零，相应的地址是否计数到 $8 \times 64 = 512$ 后保持不变。
- wr_end是否在地址计数到63后，拉高一个时钟周期后，清零。



上述的关键时序都一一验证，没有任何的问题。

(3) 写入的地址和对应的数据是否正确。

- 最开始16个地址写入的数据是0x00至0x01

```
# tb_ddr3_hdmi.inst_ddr3_model.cmd_task: at time 107083314.0 ps INFO: Write      bank 0 col 000, auto precharge 0
# tb_ddr3_hdmi.inst_ddr3_model.main: at time 107088314.0 ps INFO: Sync On Die Termination Rtt_NOM =      60 Ohm
# tb_ddr3_hdmi.inst_ddr3_model.cmd_task: at time 107093314.0 ps INFO: Write      bank 0 col 008, auto precharge 1
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107097064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000000 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107098314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000001 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107099564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000002 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107100814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000003 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107102064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000004 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107103314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000005 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107104564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000006 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107105814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000007 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107107064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000008 data = 0001
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107108314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 00000009 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107109564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000a data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107110814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000b data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107112064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000c data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107113314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000d data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107114564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000e data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107115814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 0000000f data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.main: at time 107118314.0 ps INFO: Sync On Die Termination Rtt_NOM =      0 Ohm
# tb_ddr3_hdmi.inst_ddr3_model.main: at time 107130814.0 ps INFO: Auto Precharge bank      0
```

- 最后16个地址写入的数据是0x3e至0x3f

```
# tb_ddr3_hdmi.inst_ddr3_model.cmd_task: at time 107953314.0 ps INFO: Write      bank 0 col 1f8, auto precharge 0
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107954564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001ee data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107955814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001ef data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107957064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f0 data = 003e
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107958314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f1 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107959564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f2 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107960814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f3 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107962064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f4 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107963314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f5 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107964564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f6 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107965814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f7 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107967064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f8 data = 003f
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107968314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001f9 data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107969564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001fa data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107970814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001fb data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107972064.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001fc data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107973314.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001fd data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107974564.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001fe data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.data_task: at time 107975814.0 ps INFO: WRITE @ DQS= bank = 0 row = 0000 col = 000001ff data = 0000
# tb_ddr3_hdmi.inst_ddr3_model.main: at time 107978314.0 ps INFO: Sync On Die Termination Rtt_NOM =      0 Ohm
```

这些都是正确的，没有问题哦。

六、总结与讨论

1, 关于testbench信号的引入和输出

(1) 引入

原信号是输出信号，这里引入输出端的信号作为其他信号的控制信号。

```
//output
force sclk = inst_ddr3_hdmi.inst_A7_wr_ctrl.clk;
```

(2) 输出

原信号是输入信号，这里直接控制相应的信号，输出相应的数据。

```
//input
force inst_ddr3_hdmi.inst_A7_wr_ctrl.wr_cmd_start = wr_cmd_start;
```

2. task任务的编写

(1) 不带参数

```
task gen_data;
integer i;
begin
    for (i = 0; i < 64; i = i + 1)
```

```
        begin
        end
    end
endtask
```

(2) 带参数

```
task readbit(input [7:0] data);
    integer i;
    begin
        for (i = 0; i < 10; i = i + 1)
            begin
                if (i == 0)
                    rx = 0;
                else if (i >= 1 && i <= 8)
                    rx = data[i - 1];
                else
                    rx = 1;
                #104160;
            end
        end
    end
endtask
```

3. 模块间信号的连接

- (1) 不添加wire变量，默认是1位数据位
- (2) 不是一位数据位的变量，必须添加wire信号作为连接信号。