Table 3. Functionalities depending on the mode

Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (up to 64 Kbytes)	O(1)	O(1)	O(1)	O(1)	-	-	-	-	-	-	-	-	-
SRAM1 (8 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	-	-	-	-	-
SRAM2 (4 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	O(3)	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x = 1, 2, 3)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High-speed Internal (HSI16)	O	O	O	O	(4)	-	(4)	-	-	-	-	-	-
High-speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low-speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto-wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	2	2	2	2	2	O	2	O	2	O	2	O	2
USARTx (x = 1, 2, 3, 4)	O	O	O	O	O(5)	O(5)	-	-	-	-	-	-	-
LPUARTx (x = 1 to x = 2)	O	O	O	O	O(5)	O(5)	O(5)	O(5)	-	-	-	-	-
I2Cx (x = 2)	O	O	O	O	O(6)	O(6)	-	-	-	-	-	-	-
I2Cx (x = 1, 3)	O	O	O	O	O(6)	O(6)	O(6)	O(6)	-	-	-	-	-
SPIx (x = 1 to 2)	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMP1	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x = 1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
LPTIMx (x = 1 to 2)	O	O	O	O	O	O	O	O	-	-	-	-	-

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (RNG)	O(7)	O(7)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(8)	5 pins(9)	(10)	5 pins(9)	-

1. *The flash memory can be configured in power-down mode. By default, it is not in power-down mode.*
2. *The SRAM clock can be gated on or off.*
3. *SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.*
4. *Some peripherals with wake-up from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.*
5. *UART and LPUART reception is functional in Stop mode, and generates a wake-up interrupt on Start, address match or received frame event.*
6. *I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.*
7. *Voltage scaling Range 1 only.*
8. *I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.*
9. *The I/Os with wake-up from Standby/Shutdown capability are PA0, PA1, PA2, PB15, PC5, and PC13.*
10. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*

3.8 Peripheral interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.