4.2 Pin description

Table 25. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_c	I/O with USB Type-C power delivery function
		_d	I/O with USB Type-C power delivery dead battery function
		_f	I/O, Fm+ capable
		_h	I/O with high-speed low-voltage mode
		_o	I/O with OSC32_IN/OSC32_OUT capability
		_s	I/O supplied only by V_{DDIO2}
		_t	I/O with a function supplied by V_{SW}
		_u	I/O, with USB function supplied by V_{DDUSB}
		_v	I/O very high-speed capable
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in the table below are a concatenation of various options. Examples: FT_hat, FT_fs, FT_u, TT_a.

Table 26. STM32U575xx pin definitions(1)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	1	B3	1	A1	-	-	1	B3	1	A1	PE2	I/O	FT_ha	-	TRACECLK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, LPGPIO1_P14, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	C15	2	A2	2	D3	-	-	2	A2	2	D3	PE3	I/O	FT_hat	-	TRACED0, TIM3_CH1, OCTOSPIM_P1_DQS, TSC_G7_IO2, LPGPIO1_P15, FMC_A19, SAI1_SD_B, EVENTOUT	TAMP_IN6/ TAMP_OUT3
-	-	D14	3	B2	3	C2	-	-	3	B2	3	C2	PE4	I/O	FT_hat	-	TRACED1, TIM3_CH2, SAI1_D2, MDF1_SDI3, TSC_G7_IO3, DCMI_D4/PSSI_D4, FMC_A20, SAI1_FS_A, EVENTOUT	WKUP1, TAMP_IN7/ TAMP_OUT8
-	-	E13	4	A1	4	D2	-	-	4	A1	4	D2	PE5	I/O	FT_hat	-	TRACED2, TIM3_CH3, SAI1_CK2, MDF1_CKI3, TSC_G7_IO4, DCMI_D6/PSSI_D6, FMC_A21, SAI1_SCK_A, EVENTOUT	WKUP2, TAMP_IN8/ TAMP_OUT7
-	-	D16	5	C2	5	E4	-	-	5	C2	5	E4	PE6	I/O	FT_ht	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7/PSSI_D7, FMC_A22, SAI1_SD_A, EVENTOUT	WKUP3, TAMP_IN3/ TAMP_OUT6
1	1	C17	6	B1	6	C1	1	1	6	B1	6	C1	VBAT	S	-	-	-	-
-	-	-	-	-	-	F2	-	-	-	-	-	F2	VSS	S	-	-	-	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
2	2	E15	7	C3	7	E3	2	2	7	C3	7	E3	PC13	I/O	FT	(2) (3)	EVENTOUT	WKUP2, RTC_TS/ RTC_OUT1, TAMP_IN1/ TAMP_ OUT2
3	3	D18	8	C1	8	D1	3	3	8	C1	8	D1	PC14-OSC32_IN (PC14)	I/O	FT_o	(2) (3)	EVENTOUT	OSC32_IN
4	4	E17	9	D1	9	E1	4	4	9	D1	9	E1	PC15-OSC32_OUT (PC15)	I/O	FT_o	(2) (3)	EVENTOUT	OSC32_ OUT
-	-	-	-	D2	10	E2	-	-	-	D2	10	E2	PF0	I/O	FT_fh	-	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	-	-	-	E2	11	F3	-	-	-	E2	11	F3	PF1	I/O	FT_fh	-	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	-	-	-	E1	12	F4	-	-	-	E1	12	F4	PF2	I/O	FT_h	-	LPTIM3_CH2, I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	WKUP8
-	-	-	-	D3	13	G5	-	-	-	D3	13	G5	PF3	I/O	FT_h	-	LPTIM3_IN1, OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-
-	-	-	-	E3	14	G6	-	-	-	E3	14	G6	PF4	I/O	FT_hv	-	LPTIM3_ETR, OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	F2	15	G4	-	-	-	F2	15	G4	PF5	I/O	FT_hv	-	LPTIM3_CH1, OCTOSPIM_P2_NCLK, FMC_A5, EVENTOUT	-
-	-	-	10	F6	16	H2	-	-	10	F6	16	H2	VSS	S	-	-	-	-
-	-	-	11	F7	17	G1	-	-	11	F7	17	G1	VDD	S	-	-	-	-
-	-	-	-	-	18	H6	-	-	-	-	18	H6	PF6	I/O	FT_h	-	TIM5_ETR, TIM5_CH1, DCMI_D12/PSSI_D12, OCTOSPIM_P2_NCS, OCTOSPIM_P1_IO3, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	19	G2	-	-	-	-	19	G2	PF7	I/O	FT_h	-	TIM5_CH2, FDCAN1_RX, OCTOSPIM_P1_IO2, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	20	F1	-	-	-	-	20	F1	PF8	I/O	FT_h	-	TIM5_CH3, PSSI_D14, FDCAN1_TX, OCTOSPIM_P1_IO0, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	21	G3	-	-	-	-	21	G3	PF9	I/O	FT_h	-	TIM5_CH4, PSSI_D15, OCTOSPIM_P1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	-
-	-	-	-	-	22	H4	-	-	-	-	22	H4	PF10	I/O	FT_hv	-	OCTOSPIM_P1_CLK, PSSI_D15, MDF1_CCK1, DCMI_D11/PSSI_D11, SAI1_D3, TIM15_CH2, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
5	5	F18	12	F1	23	H1	5	5	12	F1	23	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	F16	13	G1	24	J1	6	6	13	G1	24	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	7	G17	14	G2	25	H3	7	7	14	G2	25	H3	NRST	I/O	RST	-	-	-
-	8	F14	15	H2	26	J2	-	8	15	H2	26	J2	PC0	I/O	FT_fha	-	LPTIM1_IN1, OCTOSPIM_P1_IO7, I2C3_SCL(boot), SPI2_RDY, MDF1_SDI4, LPUART1_RX, SDMMC1_D5, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC1_IN1, ADC4_IN1
-	9	G15	16	G3	27	J3	-	9	16	G3	27	J3	PC1	I/O	FT_fhav	-	TRACED0, LPTIM1_CH1, SPI2_MOSI, I2C3_SDA(boot), MDF1_CKI4, LPUART1_TX, OCTOSPIM_P1_IO4, SDMMC2_CK, SAI1_SD_A, EVENTOUT	ADC1_IN2, ADC4_IN2
-	10	F12	17	F3	28	J4	-	10	17	F3	28	J4	PC2	I/O	FT_ha	-	LPTIM1_IN2, SPI2_MISO, MDF1_CCK1, OCTOSPIM_P1_IO5, LPGPIO1_P5, EVENTOUT	ADC1_IN3, ADC4_IN3
-	11	G13	18	F4	29	K1	-	11	18	F4	29	K1	PC3	I/O	FT_ha	-	LPTIM1_ETR, LPTIM3_CH1, SAI1_D1, SPI2_MOSI, OCTOSPIM_P1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4, ADC4_IN4
8	12	H18	19	H1	30	K2	8	12	19	H1	30	K2	VSSA	S	-	-	-	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	-	-	-	-	-	20	-	31	-	VREF-	S	-	-	-	-
-	-	H16	20	J1	31	L1	-	-	21	J1	32	L1	VREF+	S	-	-	-	VREFBUF_OUT
9	13	J17	21	K1	32	L2	9	13	22	K1	33	L2	VDDA	S	-	-	-	-
10	14	G11	22	J2	33	K3	10	14	23	J2	34	K3	PA0	I/O	FT_hat	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, SPI3_RDY, USART2_CTS, UART4_TX, OCTOSPIM_P2_NCS, SDMMC2_CMD, AUDIOCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC1_IN5, WKUP1, TAMP_IN2/TAMP_OUT1
-	-	-	-	H3	-	M1	-	-	-	H3	-	M1	OPAMP1_VINM	I	TT	-	-	-
11	15	J13	23	G4	34	L3	11	15	24	G4	35	L3	PA1	I/O	FT_hat	-	LPTIM1_CH2, TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS/USART2_DE, UART4_RX, OCTOSPIM_P1_DQS, LPGPIO1_P0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC1_IN6, WKUP3, TAMP_IN5/TAMP_OUT4
12	16	J15	24	K2	35	M2	12	16	25	K2	36	M2	PA2	I/O	FT_ha	-	TIM2_CH3, TIM5_CH3, SPI1_RDY, USART2_TX(boot), LPUART1_TX, OCTOSPIM_P1_NCS, UCPD1_FRSTX1, TIM15_CH1, EVENTOUT	COMP1_INP3, ADC1_IN7, WKUP4/LSCO

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
13	17	H10	25	L1	36	N2	13	17	26	L1	37	N2	PA3	I/O	TT_ hav	-	TIM2_CH4, TIM5_CH4, SAI1_CK1, USART2_RX(boot), LPUART1_RX, OCTOSPIM_P1_CLK, LPGPIO1_P1, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_ VOUT, ADC1_IN8, WKUP5
-	18	K18	26	G7	37	M3	-	18	27	G7	38	M3	VSS	S	-	-	-	-
-	19	K16	27	G6	38	N3	-	19	28	G6	39	N3	VDD	S	-	-	-	-
14	20	H14	28	L3	39	N1	14	20	29	L3	40	N1	PA4	I/O	TT_ha	-	OCTOSPIM_P1_NCS, SPI1_NSS(boot), SPI3_NSS, USART2_CK, DCMI_HSYNC/PSSI_DE, SAI1_FS_B, LPTIM2_CH1, EVENTOUT	ADC1_IN9, ADC4_IN9, DAC1_ OUT1, WKUP2
15	21	H12	29	M1	40	K4	15	21	30	M1	41	K4	PA5	I/O	TT_a	-	CSLEEP, TIM2_CH1, TIM2_ETR, TIM8_CH1N, PSSI_D14, SPI1_SCK(boot), USART3_RX, LPTIM2_ETR, EVENTOUT	ADC1_IN10, ADC4_IN10, DAC1_ OUT2, WKUP6
16	22	F10	30	L2	41	N4	16	22	31	L2	42	N4	PA6	I/O	FT_ha	-	CDSTOP, TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK/PSSI_PDCK, SPI1_MISO(boot), USART3_CTS, LPUART1_CTS, OCTOSPIM_P1_IO3, LPGPIO1_P2, TIM16_CH1, EVENTOUT	OPAMP2_ VINP, ADC1_IN11, ADC4_IN11, WKUP7

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	M2	-	H5	-	-	-	M2	-	H5	OPAMP2_VINM	I	TT	-	-	-
17	23	K14	31	K3	42	J5	17	23	32	K3	43	J5	PA7	I/O	FT_fha	-	SRDSTOP, TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI(boot), USART3_TX, OCTOSPIM_P1_IO2, LPTIM2_CH2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC1_IN12, ADC4_IN20, WKUP8
-	-	-	-	M3	-	L4	-	24	33	M3	44	L4	PC4	I/O	FT_ha	-	USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM2, ADC1_IN13, ADC4_IN22
-	-	G9	-	J3	-	M4	-	25	34	J3	45	M4	PC5	I/O	FT_at	-	TIM1_CH4N, SAI1_D3, PSSI_D15, USART3_RX, EVENTOUT	COMP1_INP1, ADC1_IN14, ADC4_IN23, WKUP5, TAMP_IN4/TAMP_OUT5
18	24	K12	32	M4	43	K5	18	26	35	M4	46	K5	PB0	I/O	TT_ha	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LPTIM3_CH1, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, LPGPIO1_P9, COMP1_OUT, AUDIOCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN15, ADC4_IN18

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
19	25	J11	33	L4	44	N5	19	27	36	L4	47	N5	PB1	I/O	FT_ha	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LPTIM3_CH2, MDF1_SDI0, USART3_RTS/USART3_DE, LPUART1_RTS/LPUART1_DE, OCTOSPIM_P1_IO0, LPGPIO1_P3, LPTIM2_IN1, EVENTOUT	COMP1_INM1, ADC1_IN16, ADC4_IN19, WKUP4
-	26	K10	34	K4	45	L5	20	28	37	K4	48	L5	PB2	I/O	FT_hat	-	LPTIM1_CH1, TIM8_CH4N, I2C3_SMBA, SPI1_RDY, MDF1_CKI0, OCTOSPIM_P1_DQS, UCPD1_FRSTX1, EVENTOUT	COMP1_INP2, ADC1_IN17, WKUP1, RTC_OUT2
-	-	-	-	K5	46	M5	-	-	-	K5	49	M5	PF11	I/O	FT_hv	-	OCTOSPIM_P1_NCLK, DCMI_D12/PSSI_D12, LPTIM4_IN1, EVENTOUT	-
-	-	-	-	L5	47	K6	-	-	-	L5	50	K6	PF12	I/O	FT_h	-	OCTOSPIM_P2_DQS, FMC_A6, LPTIM4_ETR, EVENTOUT	-
-	-	-	-	-	48	M7	-	-	-	-	51	M7	VSS	S	-	-	-	-
-	-	-	-	-	49	N7	-	-	-	-	52	N7	VDD	S	-	-	-	-
-	-	-	-	M5	50	M6	-	-	-	M5	53	M6	PF13	I/O	FT_h	-	I2C4_SMBA, UCPD1_FRSTX2, FMC_A7, LPTIM4_OUT, EVENTOUT	-
-	-	-	-	J5	51	L6	-	-	-	J5	54	L6	PF14	I/O	FT_fha	-	I2C4_SCL, TSC_G8_IO1, FMC_A8, EVENTOUT	ADC4_IN5

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	L6	52	N6	-	-	-	L6	55	N6	PF15	I/O	FT_fha	-	I2C4_SDA, TSC_G8_IO2, FMC_A9, EVENTOUT	ADC4_IN6
-	-	-	-	M6	53	J6	-	-	-	M6	56	J6	PG0	I/O	FT_ha	-	OCTOSPIM_P2_IO4, TSC_G8_IO3, FMC_A10, EVENTOUT	ADC4_IN7
-	-	-	-	K6	54	H7	-	-	-	K6	57	H7	PG1	I/O	FT_ha	-	OCTOSPIM_P2_IO5, TSC_G8_IO4, FMC_A11, EVENTOUT	ADC4_IN8
-	-	H8	35	K7	55	L7	-	-	38	K7	58	L7	PE7	I/O	FT_h	-	TIM1_ETR, MDF1_SDI2, FMC_D4/FMC_AD4, SAI1_SD_B, EVENTOUT	WKUP6
-	-	J9	36	J6	56	K7	-	-	39	J6	59	K7	PE8	I/O	FT_h	-	TIM1_CH1N, MDF1_CKI2, FMC_D5/FMC_AD5, SAI1_SCK_B, EVENTOUT	WKUP7
-	-	K8	37	M7	57	J7	-	-	40	M7	60	J7	PE9	I/O	FT_hv	-	TIM1_CH1, ADF1_CCK0, MDF1_CCK0, OCTOSPIM_P1_NCLK, FMC_D6/FMC_AD6, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	58	-	-	-	-	-	61	-	VSS	S	-	-	-	-
-	-	-	-	J4	59	-	-	-	-	J4	62	-	VDD	S	-	-	-	-
-	-	J7	38	J7	60	H8	-	-	41	J7	63	H8	PE10	I/O	FT_hav	-	TIM1_CH2N, ADF1_SDI0, MDF1_SDI4, TSC_G5_IO1, OCTOSPIM_P1_CLK, FMC_D7/FMC_AD7, SAI1_MCLK_B, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	39	L7	61	M8	-	-	42	L7	64	M8	PE11	I/O	FT_ha	-	TIM1_CH2, SPI1_RDY, MDF1_CKI4, TSC_G5_IO2, OCTOSPIM_P1_NCS, FMC_D8/FMC_AD8, EVENTOUT	-
-	-	-	40	J8	62	N8	-	-	43	J8	65	N8	PE12	I/O	FT_ha	-	TIM1_CH3N, SPI1_NSS, MDF1_SDI5, TSC_G5_IO3, OCTOSPIM_P1_IO0, FMC_D9/FMC_AD9, EVENTOUT	-
-	-	-	41	M8	63	L8	-	-	44	M8	66	L8	PE13	I/O	FT_ha	-	TIM1_CH3, SPI1_SCK, MDF1_CKI5, TSC_G5_IO4, OCTOSPIM_P1_IO1, FMC_D10/FMC_AD10, EVENTOUT	-
-	-	-	42	K8	64	K8	-	-	45	K8	67	K8	PE14	I/O	FT_h	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPIM_P1_IO2, FMC_D11/FMC_AD11, EVENTOUT	-
-	-	-	43	L8	65	M9	-	-	46	L8	68	M9	PE15	I/O	FT_h	-	TIM1_BKIN, TIM1_CH4N, SPI1_MOSI, OCTOSPIM_P1_IO3, FMC_D12/FMC_AD12, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	27	H6	44	K9	66	K9	21	29	47	K9	69	K9	PB10	I/O	FT_fhv	-	TIM2_CH3, LPTIM3_CH1, I2C4_SCL, I2C2_SCL(boot), SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPIM_P1_CLK, LPGPIO1_P4, COMP1_OUT, SAI1_SCK_A, EVENTOUT	WKUP8
-	-	-	45	L9	67	L9	-	-	-	L9	-	L9	PB11	I/O	FT_fh	-	TIM2_CH4, I2C4_SDA, I2C2_SDA(boot), SPI2_RDY, USART3_RX, LPUART1_TX, OCTOSPIM_P1_NCS, COMP2_OUT, EVENTOUT	-
20	28	K6	46	M10	68	N9	-	-	-	-	-	-	VLXSMPS	S	-	-	-	-
21	29	K4	47	M9	69	N10	-	-	-	-	-	-	VDDSMPS	S	-	-	-	-
22	30	J5	48	L10	70	M10	-	-	-	-	-	-	VSSSMPS	S	-	-	-	-
-	-	-	-	-	-	-	22	30	48	L10	70	N11	VCAP	S	-	-	-	-
23	31	K2	49	M11	71	N11	-	-	-	-	-	-	VDD11	S	-	-	-	-
24	32	J3	50	E9	72	M11	23	31	49	E9	71	M11	VSS	S	-	-	-	-
25	33	J1	51	D4	73	N12	24	32	50	D4	72	N12	VDD	S	-	-	-	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	L11	-	L10	25	33	51	L11	73	L10	PB12	I/O	FT_hav	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS(boot), MDF1_SDI1, USART3_CK, LPUART1_RTS/LPUART1_DE, TSC_G1_IO1, OCTOSPIM_P1_NCLK, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-
26	34	H2	52	K10	74	N13	26	34	52	K10	74	N13	PB13	I/O	FT_fa	-	TIM1_CH1N, LPTIM3_IN1, I2C2_SCL, SPI2_SCK(boot), MDF1_CKI1, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
27	35	H4	53	K11	75	M12	27	35	53	K11	75	M12	PB14	I/O	FT_fda	-	TIM1_CH2N, LPTIM3_ETR, TIM8_CH2N, I2C2_SDA, SPI2_MISO(boot), MDF1_SDI2, USART3_RTS/USART3_DE, TSC_G1_IO3, SDMMC2_D0, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	UCPD1_DBCC2
28	36	G5	54	K12	76	L11	28	36	54	K12	76	L11	PB15	I/O	FT_c	(4)	RTC_REFIN, TIM1_CH3N, LPTIM2_IN2, TIM8_CH3N, SPI2_MOSI(boot), MDF1_CKI2, FMC_NBL1, SDMMC2_D1, SAI2_SD_A, TIM15_CH2, EVENTOUT	UCPD1_CC2, WKUP7

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	55	L12	77	L12	-	-	55	L12	77	L12	PD8	I/O	FT_h	-	USART3_TX, DCMI_HSYNC/PSSI_DE, FMC_D13/FMC_AD13, EVENTOUT	-
-	-	-	56	J10	78	L13	-	-	56	J10	78	L13	PD9	I/O	FT_h	-	LPTIM2_IN2, USART3_RX, DCMI_PIXCLK/PSSI_PDCK, FMC_D14/FMC_AD14, SAI2_MCLK_A, LPTIM3_IN1, EVENTOUT	-
-	-	-	57	M12	79	K11	-	-	57	M12	79	K11	PD10	I/O	FT_ha	-	LPTIM2_CH2, USART3_CK, TSC_G6_IO1, FMC_D15/FMC_AD15, SAI2_SCK_A, LPTIM3_ETR, EVENTOUT	-
-	-	-	58	J11	80	M13	-	-	58	J11	80	M13	PD11	I/O	FT_ha	-	I2C4_SMBA, USART3_CTS, TSC_G6_IO2, FMC_CLE/FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	ADC4_IN15
-	-	-	59	J12	81	K10	-	-	59	J12	81	K10	PD12	I/O	FT_fha	-	TIM4_CH1, I2C4_SCL, USART3_RTS/USART3_DE, TSC_G6_IO3, FMC_ALE/FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC4_IN16

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	60	H11	82	K12	-	-	60	H11	82	K12	PD13	I/O	FT_fha	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, LPGPIO1_P6, FMC_A18, LPTIM4_IN1, LPTIM2_CH1, EVENTOUT	ADC4_IN17
-	-	-	-	-	83	J12	-	-	-	-	83	J12	VSS	S	-	-	-	-
-	-	-	-	-	84	J13	-	-	-	-	84	J13	VDD	S	-	-	-	-
-	-	G1	61	H10	85	J10	-	-	61	H10	85	J10	PD14	I/O	FT_h	-	TIM4_CH3, FMC_D0/FMC_AD0, LPTIM3_CH1, EVENTOUT	-
-	-	G3	62	H12	86	J11	-	-	62	H12	86	J11	PD15	I/O	FT_h	-	TIM4_CH4, FMC_D1/FMC_AD1, LPTIM3_CH2, EVENTOUT	-
-	-	-	-	G10	87	K13	-	-	-	G10	87	K13	PG2	I/O	FT_hs	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	G11	88	J8	-	-	-	G11	88	J8	PG3	I/O	FT_hs	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	G9	89	H11	-	-	-	G9	89	H11	PG4	I/O	FT_hs	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	G12	90	J9	-	-	-	G12	90	J9	PG5	I/O	FT_hs	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	-	-	F9	91	H10	-	-	-	F9	91	H10	PG6	I/O	FT_hs	-	OCTOSPIM_P1_DQS, I2C3_SMBA, SPI1_RDY, LPUART1_RTS/LPUART1_DE, UCPD1_FRSTX1, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	F10	92	G8	-	-	-	F10	92	G8	PG7	I/O	FT_fhs	-	SAI1_CK1, I2C3_SCL, OCTOSPIM_P2_DQS, MDF1_CCK0, LPUART1_TX, UCPD1_FRSTX2, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	F12	93	H9	-	-	-	F12	93	H9	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	94	-	-	-	-	-	94	-	VSS	S	-	-	-	-
-	-	-	-	-	95	H12	-	-	-	-	95	H12	VDDIO2	S	-	-	-	-
-	37	G7	63	F11	96	H13	-	37	63	F11	96	H13	PC6	I/O	FT_a	-	CSLEEP, TIM3_CH1, TIM8_CH1, MDF1_CKI3, SDMMC1_D0DIR, TSC_G4_IO1, DCMI_D0/PSSI_D0, SDMMC2_D6, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
-	38	F4	64	E10	97	G12	-	38	64	E10	97	G12	PC7	I/O	FT_a	-	CDSTOP, TIM3_CH2, TIM8_CH2, MDF1_SDI3, SDMMC1_D123DIR, TSC_G4_IO2, DCMI_D1/PSSI_D1, SDMMC2_D7, SDMMC1_D7, SAI2_MCLK_B, LPTIM2_CH2, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	39	F2	65	E12	98	G10	-	39	65	E12	98	G10	PC8	I/O	FT_a	-	SRDSTOP, TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2/PSSI_D2, SDMMC1_D0, LPTIM3_CH1, EVENTOUT	-
-	40	F6	66	E11	99	G9	-	40	66	E11	99	G9	PC9	I/O	FT_a	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3/PSSI_D3, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, LPTIM3_CH2, EVENTOUT	-
29	41	F8	67	D12	100	G7	29	41	67	D12	100	G7	PA8	I/O	FT_hv	-	MCO, TIM1_CH1, SAI1_CK2, SPI1_RDY, USART1_CK, OTG_FS_SOF, TRACECLK, SAI1_SCK_A, LPTIM2_CH1, EVENTOUT	-
30	42	E11	68	D10	101	G11	30	42	68	D10	101	G11	PA9	I/O	FT_u	-	TIM1_CH2, SPI2_SCK, DCMI_D0/PSSI_D0, USART1_TX(boot), SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_ VBUS
31	43	E1	69	D11	102	F11	31	43	69	D11	102	F11	PA10	I/O	FT_u	-	CRS_SYNC, TIM1_CH3, LPTIM2_IN2, SAI1_D1, DCMI_D1/PSSI_D1, USART1_RX(boot), OTG_FS_ID, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
32	44	E3	70	C12	103	G13	32	44	70	C12	103	G13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, FDCAN1_RX, EVENTOUT	OTG_FS_ DM(boot)
33	45	D2	71	B12	104	F13	33	45	71	B12	104	F13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, OCTOSPIM_P2_NCS, USART1_RTS/USART1_DE, FDCAN1_TX, EVENTOUT	OTG_FS_ DP(boot)
34	46	D4	72	C10	105	F12	34	46	72	C10	105	F12	PA13 (JTMS/ SWDIO)	I/O	FT	(5)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT	-
-	47	-	-	-	-	-	-	47	-	-	-	-	VSS	S	-	-	-	-
-	48	C1	73	A12	106	E13	-	48	73	A12	106	E13	VDDUSB	S	-	-	-	-
35	-	B2	74	H4	107	E12	35	-	74	H4	107	E12	VSS	S	-	-	-	-
36	-	A1	75	D9	108	D13	36	-	75	D9	108	D13	VDD	S	-	-	-	-
37	49	C3	76	C11	109	C10	37	49	76	C11	109	C10	PA14 (JTCK/ SWCLK)	I/O	FT	(5)	JTCK/SWCLK, LPTIM1_CH1, I2C1_SMBA, I2C4_SMBA, OTG_FS_SOF, SAI1_FS_B, EVENTOUT	-
38	50	E5	77	A11	110	A10	38	50	77	A11	110	A10	PA15 (JTDI)	I/O	FT_c	(4) (5)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS/USART3_DE, UART4_RTS/UART4_DE, SAI2_FS_B, EVENTOUT	UCPD1_ CC1

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	51	E7	78	B11	111	C9	-	51	78	B11	111	C9	PC10	I/O	FT_a	-	TRACED1, LPTIM3_ETR, ADF1_CCK1, SPI3_SCK, USART3_TX(boot), UART4_TX, TSC_G3_IO2, DCMI_D8/PSSI_D8, LPGPIO1_P8, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
-	52	A3	79	A10	112	A9	-	52	79	A10	112	A9	PC11	I/O	FT_ha	-	LPTIM3_IN1, ADF1_SDI0, DCMI_D2/PSSI_D2, OCTOSPIM_P1_NCS, SPI3_MISO, USART3_RX(boot), UART4_RX, TSC_G3_IO3, DCMI_D4/PSSI_D4, UCPD1_FRSTX2, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
-	53	B4	80	B10	113	E8	-	53	80	B10	113	E8	PC12	I/O	FT_hav	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9/PSSI_D9, LPGPIO1_P10, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	-	C5	81	C9	114	B9	-	-	81	C9	114	B9	PD0	I/O	FT_h	-	TIM8_CH4N, SPI2_NSS, FDCAN1_RX, FMC_D2/FMC_AD2, EVENTOUT	-
-	-	D6	82	B9	115	F6	-	-	82	B9	115	F6	PD1	I/O	FT_h	-	SPI2_SCK, FDCAN1_TX, FMC_D3/FMC_AD3, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	54	A5	83	A9	116	F7	-	54	83	A9	116	F7	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS/USART3_DE, UART5_RX, TSC_SYNC, DCMI_D11/PSSI_D11, LPGPIO1_P7, SDMMC1_CMD, LPTIM4_ETR, EVENTOUT	-
-	-	-	84	C8	117	D8	-	-	84	C8	117	D8	PD3	I/O	FT_hv	-	SPI2_SCK, DCMI_D5/PSSI_D5, SPI2_MISO, MDF1_SDI0, USART2_CTS, OCTOSPIM_P2_NCS, FMC_CLK, EVENTOUT	-
-	-	D8	85	B8	118	C8	-	-	85	B8	118	C8	PD4	I/O	FT_h	-	SPI2_MOSI, MDF1_CKI0, USART2_RTS/USART2_DE, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-
-	-	B6	86	A8	119	E7	-	-	86	A8	119	E7	PD5	I/O	FT_h	-	SPI2_RDY, USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	-	-	120	B8	-	-	-	-	120	B8	VSS	S	-	-	-	-
-	-	-	-	-	121	A8	-	-	-	-	121	A8	VDD	S	-	-	-	-
-	-	-	87	A7	122	B7	-	-	87	A7	122	B7	PD6	I/O	FT_hv	-	SAI1_D1, DCMI_D10/PSSI_D10, SPI3_MOSI, MDF1_SDI1, USART2_RX, OCTOSPIM_P1_IO6, SDMMC2_CK, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	88	D7	123	D7	-	-	88	D7	123	D7	PD7	I/O	FT_h	-	MDF1_CKI1, USART2_CK, OCTOSPIM_P1_IO7, SDMMC2_CMD, FMC_NCE/FMC_NE1, LPTIM4_OUT, EVENTOUT	-
-	-	C7	-	B7	124	A7	-	-	-	B7	124	A7	PG9	I/O	FT_hs	-	OCTOSPIM_P2_IO6, SPI3_SCK(boot), USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	-	A7	-	C7	125	C7	-	-	-	C7	125	C7	PG10	I/O	FT_hs	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO(boot), USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	-	E9	-	-	-	-	-	-	-	M11	126	M10	PG11	I/O	FT_hs	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	-	B8	-	A6	126	E6	-	-	-	A6	127	E6	PG12	I/O	FT_hs	-	LPTIM1_ETR, OCTOSPIM_P2_NCS, SPI3_NSS(boot), USART1_RTS/USART1_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	C9	-	-	127	-	-	-	-	M10	128	N10	PG13	I/O	FT_fhs	-	I2C1_SDA, SPI3_RDY, USART1_CK, FMC_A24, EVENTOUT	-
-	-	A9	-	-	128	-	-	-	-	M9	129	N9	PG14	I/O	FT_fhs	-	LPTIM1_CH2, I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	B10	-	H9	129	-	-	-	-	H9	130	-	VSS	S	-	-	-	-
-	-	A11	-	D8	130	A6	-	-	-	D8	131	A6	VDDIO2	S	-	-	-	-
-	-	-	-	-	131	A5	-	-	-	B4	132	A5	PG15	I/O	FT_hs	-	LPTIM1_CH1, I2C1_SMBA, OCTOSPIM_P2_DQS, DCMI_D13/PSSI_D13, EVENTOUT	-
39	55	D10	89	C6	132	D6	39	55	89	C6	133	D6	PB3 (JTDO/TRACESWO)	I/O	FT_fa	-	JTDO/TRACESWO, TIM2_CH2, LPTIM1_CH1, ADF1_CCK0, I2C1_SDA, SPI1_SCK, SPI3_SCK, USART1_RTS/USART1_DE, CRS_SYNC, LPGPIO1_P11, SDMMC2_D2, SAI1_SCK_B, EVENTOUT	COMP2_INM2

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
40	56	C11	90	B6	133	B6	40	56	90	B6	134	B6	PB4 (NJTRST)	I/O	FT_fa	(5)	NJTRST, LPTIM1_CH2, TIM3_CH1, ADF1_SDI0, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS/UART5_DE, TSC_G2_IO1, DCMI_D12/PSSI_D12, LPGPIO1_P12, SDMMC2_D3, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP1
41	57	D12	91	D6	134	C6	41	57	91	D6	135	C6	PB5	I/O	FT_havd	-	LPTIM1_IN1, TIM3_CH2, OCTOSPIM_P1_NCLK, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI(boot), USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10/PSSI_D10, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	UCPD1_DBCC1, WKUP6
42	58	A13	92	A5	135	B5	42	58	92	A5	136	B5	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL(boot), I2C4_SCL, MDF1_SDI5, USART1_TX, TSC_G2_IO3, DCMI_D5/PSSI_D5, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP2, WKUP3

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
43	59	B12	93	D5	136	F5	43	59	93	D5	137	F5	PB7	I/O	FT_fhav	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA(boot), I2C4_SDA, MDF1_CKI5, USART1_RX, UART4_CTS, TSC_G2_IO4, DCMI_VSYNC/PSSI_RDY, FMC_NL, TIM17_CH1N, EVENTOUT	COMP2_INM1, PVD_IN, WKUP4
44	60	C13	94	B5	137	C5	44	60	94	B5	138	C5	PH3-BOOT0	I/O	FT	-	EVENTOUT	-
45	61	B14	95	C5	138	E5	45	61	95	C5	139	E5	PB8	I/O	FT_f	-	TIM4_CH3, SAI1_CK1, I2C1_SCL, MDF1_CCK0, SPI3_RDY, SDMMC1_CKIN, FDCAN1_RX(boot), DCMI_D6/PSSI_D6, SDMMC2_D4, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	WKUP5
-	-	A15	96	A4	139	D5	46	62	96	A4	140	D5	PB9	I/O	FT_f	-	IR_OUT, TIM4_CH4, SAI1_D2, I2C1_SDA, SPI2_NSS, SDMMC1_CDIR, FDCAN1_TX(boot), DCMI_D7/PSSI_D7, SDMMC2_D5, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	-	97	C4	140	D4	-	-	97	C4	141	D4	PE0	I/O	FT_h	-	TIM4_ETR, DCMI_D2/PSSI_D2, LPGPIO1_P13, FMC_NBL0, TIM16_CH1, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	A3	141	C4	-	-	98	A3	142	C4	PE1	I/O	FT_h	-	DCMI_D3/PSSI_D3, FMC_NBL1, TIM17_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	A4	VCAP	S	-	-	-	-
46	62	A17	98	B4	142	A4	-	-	-	-	-	-	VDD11	S	-	-	-	-
47	63	B16	99	E4	143	B4	47	63	99	E4	143	B4	VSS	S	-	-	-	-
48	64	B18	100	J9	144	A3	48	64	100	J9	144	A3	VDD	S	-	-	-	-
-	-	-	-	-	-	B11	-	-	-	-	-	B11	VSS	S	-	-	-	-
-	-	-	-	-	-	F10	-	-	-	-	-	F10	PH2	I/O	FT_h	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	-	-	E10	-	-	-	-	-	E10	PH4	I/O	FT_fh	-	I2C2_SCL, OCTOSPIM_P2_DQS, PSSI_D14, EVENTOUT	-
-	-	-	-	-	-	F9	-	-	-	-	-	F9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK/PSSI_PDCK, EVENTOUT	-
-	-	-	-	-	-	E11	-	-	-	-	-	E11	PH6	I/O	FT_hv	-	I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8/PSSI_D8, EVENTOUT	-
-	-	-	-	-	-	F8	-	-	-	-	-	F8	PH7	I/O	FT_fhv	-	I2C3_SCL, OCTOSPIM_P2_NCLK, DCMI_D9/PSSI_D9, EVENTOUT	-
-	-	-	-	-	-	D12	-	-	-	-	-	D12	PH8	I/O	FT_fh	-	I2C3_SDA, OCTOSPIM_P2_IO3, DCMI_HSYNC/PSSI_DE, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	-	-	E9	-	-	-	-	-	E9	PH9	I/O	FT_h	-	I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0/PSSI_D0, EVENTOUT	-
-	-	-	-	-	-	C13	-	-	-	-	-	C13	PH10	I/O	FT_h	-	TIM5_CH1, OCTOSPIM_P2_IO5, DCMI_D1/PSSI_D1, EVENTOUT	-
-	-	-	-	-	-	D9	-	-	-	-	-	D9	PH11	I/O	FT_h	-	TIM5_CH2, OCTOSPIM_P2_IO6, DCMI_D2/PSSI_D2, EVENTOUT	-
-	-	-	-	-	-	B13	-	-	-	-	-	B13	PH12	I/O	FT_h	-	TIM5_CH3, TIM8_CH4N, OCTOSPIM_P2_IO7, DCMI_D3/PSSI_D3, EVENTOUT	-
-	-	-	-	-	-	C12	-	-	-	-	-	C12	PH13	I/O	FT	-	TIM8_CH1N, FDCAN1_TX, EVENTOUT	-
-	-	-	-	-	-	C11	-	-	-	-	-	C11	PH14	I/O	FT	-	TIM8_CH2N, FDCAN1_RX, DCMI_D4/PSSI_D4, EVENTOUT	-
-	-	-	-	-	-	A13	-	-	-	-	-	A13	PH15	I/O	FT_h	-	TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11/PSSI_D11, EVENTOUT	-
-	-	-	-	-	-	A11	-	-	-	-	-	A11	VDD	S	-	-	-	-
-	-	-	-	-	-	B12	-	-	-	-	-	B12	PI0	I/O	FT_h	-	TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13/PSSI_D13, EVENTOUT	-
-	-	-	-	-	-	A12	-	-	-	-	-	A12	PI1	I/O	FT_h	-	SPI2_SCK, OCTOSPIM_P2_IO2, DCMI_D8/PSSI_D8, EVENTOUT	-

Table 26. STM32U575xx pin definitions[1] (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS UFQFPN48 SMPS	LQFP64 SMPS	WLCSP90 SMPS	LQFP100 SMPS	UFBGA132 SMPS	LQFP144 SMPS	UFBGA169 SMPS	LQFP48 UFQFPN48	LQFP64	LQFP100	UFBGA132	LQFP144	UFBGA169						
-	-	-	-	-	-	D11	-	-	-	-	-	D11	PI2	I/O	FT_hv	-	TIM8_CH4, SPI2_MISO, OCTOSPIM_P2_IO1, DCMI_D9/PSSI_D9, EVENTOUT	-
-	-	-	-	-	-	D10	-	-	-	-	-	D10	PI3	I/O	FT_h	-	TIM8_ETR, SPI2_MOSI, OCTOSPIM_P2_IO0, DCMI_D10/PSSI_D10, EVENTOUT	-
-	-	-	-	-	-	B2	-	-	-	-	-	B2	VSS	S	-	-	-	-
-	-	-	-	-	-	B1	-	-	-	-	-	B1	VDD	S	-	-	-	-
-	-	-	-	-	-	B10	-	-	-	-	-	B10	PI4	I/O	FT	-	TIM8_BKIN, SPI2_RDY, DCMI_D5/PSSI_D5, EVENTOUT	-
-	-	-	-	-	-	B3	-	-	-	-	-	B3	PI5	I/O	FT_h	-	TIM8_CH1, OCTOSPIM_P2_NCS, DCMI_VSYNC/PSSI_RDY, EVENTOUT	-
-	-	-	-	-	-	A2	-	-	-	-	-	A2	PI6	I/O	FT_hv	-	TIM8_CH2, OCTOSPIM_P2_CLK, DCMI_D6/PSSI_D6, EVENTOUT	-
-	-	-	-	-	-	C3	-	-	-	-	-	C3	PI7	I/O	FT_hv	-	TIM8_CH3, OCTOSPIM_P2_NCLK, DCMI_D7/PSSI_D7, EVENTOUT	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch (by V_{SW}). Since the switch only sinks a limited amount of current (3 mA), the use of PC13 to PC15 GPIOs in output mode is limited:
   - PC13 speed must not exceed 2 MHz with a maximum load of 30 pF. Refer to FT_o electrical characteristics for PC14, PC15.
   - These GPIOs must not be used as current sources (for example to drive a LED).

3. After a backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function depends then on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the backup domain and RTC register descriptions in the product reference manual.
4. After reset, a pull-down resistor (Rd = 5.1 kΩ from UCPD peripheral) can be activated on PA15 and PB15 (UCPD1_CC1, UCPD1_CC2). The pull-down on PA15 (UCPD1_CC1) is activated by high level on PB5 (UCPD1_DBCC1). The pull-down on PB15 (UCPD1_CC2) is activated by high level on PB14 (UCPD1_DBCC2). This pull-down control (dead battery support on UCPD) can be disabled by setting UCPD_DBDIS = 1 in the PWR_UCPDR register.
5. After reset, this pin is configured as JTAG/SWD alternate functions. The internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

4.3 Alternate functions

Table 27. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	SPI3_RDY	USART2_CTS
	PA1	LPTIM1_CH2	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_ RTS/USART2_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	SPI1_RDY	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_RX
	PA4	-	-	-	OCTOSPIM_P1 _NCS	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	CSLEEP	TIM2_CH1	TIM2_ETR	TIM8_CH1N	PSSI_D14	SPI1_SCK	-	USART3_RX
	PA6	CDSTOP	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCL K/PSSI_ PDCK	SPI1_MISO	-	USART3_CTS
	PA7	SRDSTOP	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	USART3_TX
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	SPI1_RDY	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	DCMI_D0/PSSI_D0	-	USART1_TX
	PA10	CRS_SYNC	TIM1_CH3	LPTIM2_IN2	SAI1_D1	-	DCMI_D1/PSSI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	OCTOSPIM_ P2_NCS	USART1_ RTS/USART1_ DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_CH1	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_ RTS/USART3_ DE

Table 27. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	LPTIM3_CH1	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	LPTIM3_CH2	-	MDF1_SDI0	USART3_ RTS/USART3_ DE
	PB2	-	LPTIM1_CH1	-	TIM8_CH4N	I2C3_SMBA	SPI1_RDY	MDF1_CKI0	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	LPTIM1_CH1	ADF1_CCK0	I2C1_SDA	SPI1_SCK	SPI3_SCK	USART1_ RTS/USART1_ DE
	PB4	NJTRST	LPTIM1_CH2	TIM3_CH1	ADF1_SDI0	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	OCTOSPIM_ P1_NCLK	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	MDF1_SDI5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	MDF1_CKI5	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	MDF1_CCK0	SPI3_RDY	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	-	-
	PB10	-	TIM2_CH3	LPTIM3_CH1	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	SPI2_RDY	-	USART3_RX
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS	MDF1_SDI1	USART3_CK
	PB13	-	TIM1_CH1N	LPTIM3_IN1	-	I2C2_SCL	SPI2_SCK	MDF1_CKI1	USART3_CTS
	PB14	-	TIM1_CH2N	LPTIM3_ETR	TIM8_CH2N	I2C2_SDA	SPI2_MISO	MDF1_SDI2	USART3_ RTS/USART3_ DE
	PB15	RTC_REFIN	TIM1_CH3N	LPTIM2_IN2	TIM8_CH3N	-	SPI2_MOSI	MDF1_CKI2	-

Table 27. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	-	OCTOSPIM_ P1_IO7	I2C3_SCL	SPI2_RDY	MDF1_SDI4	-
	PC1	TRACED0	LPTIM1_CH1	-	SPI2_MOSI	I2C3_SDA	-	MDF1_CKI4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	MDF1_CCK1	-
	PC3	-	LPTIM1_ETR	LPTIM3_CH1	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	TIM1_CH4N	-	SAI1_D3	PSSI_D15	-	-	USART3_RX
	PC6	CSLEEP	-	TIM3_CH1	TIM8_CH1	-	-	MDF1_CKI3	-
	PC7	CDSTOP	-	TIM3_CH2	TIM8_CH2	-	-	MDF1_SDI3	-
	PC8	SRDSTOP	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3/ PSSI_D3	-	-	-
	PC10	TRACED1	-	LPTIM3_ETR	ADF1_CCK1	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	LPTIM3_IN1	ADF1_SDI0	DCMI_D2/ PSSI_D2	OCTOSPIM_ P1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 27. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port D	PD0	-	-	-	TIM8_CH4N	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_ RTS/USART3_ DE
	PD3	-	-	-	SPI2_SCK	DCMI_D5/ PSSI_D5	SPI2_MISO	MDF1_SDI0	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	MDF1_CKI0	USART2_ RTS/USART2_ DE
	PD5	-	-	-	-	-	SPI2_RDY	-	USART2_TX
	PD6	-	-	-	SAI1_D1	DCMI_D10/ PSSI_D10	SPI3_MOSI	MDF1_SDI1	USART2_RX
	PD7	-	-	-	-	-	-	MDF1_CKI1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	LPTIM2_IN2	-	-	-	-	USART3_RX
	PD10	-	-	LPTIM2_CH2	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_ RTS/USART3_ DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 27. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECLK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPIM_ P1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	MDF1_SDI3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	MDF1_CKI3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	MDF1_SDI2	-
	PE8	-	TIM1_CH1N	-	-	-	-	MDF1_CKI2	-
	PE9	-	TIM1_CH1	-	ADF1_CCK0	-	-	MDF1_CCK0	-
	PE10	-	TIM1_CH2N	-	ADF1_SDI0	-	-	MDF1_SDI4	-
	PE11	-	TIM1_CH2	-	-	-	SPI1_RDY	MDF1_CKI4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	MDF1_SDI5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	MDF1_CKI5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_CH4N	-	SPI1_MOSI	-	-

Table 27. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	LPTIM3_CH2	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	LPTIM3_IN1	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	LPTIM3_ETR	-	-	OCTOSPIM_ P2_CLK	-	-
	PF5	-	-	LPTIM3_CH1	-	-	OCTOSPIM_ P2_NCLK	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	DCMI_D12/P SSI_D12	OCTOSPIM_ P2_NCS	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	PSSI_D14	-	-	-
	PF9	-	-	TIM5_CH4	-	PSSI_D15	-	-	-
	PF10	-	-	-	OCTOSPIM_ P1_CLK	PSSI_D15	-	MDF1_CCK1	-
	PF11	-	-	-	OCTOSPIM_ P1_NCLK	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_ P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	-	-
	PF14	-	-	-	-	I2C4_SCL	-	-	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 27. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_ P1_DQS	I2C3_SMBA	SPI1_RDY	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_ P2_DQS	MDF1_CCK0	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_ P1_IO5	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_ P2_NCS	SPI3_NSS	USART1_ RTS/USART1_ DE
	PG13	-	-	-	-	I2C1_SDA	-	SPI3_RDY	USART1_CK
	PG14	-	LPTIM1_CH2	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_CH1	-	-	I2C1_SMBA	OCTOSPIM_ P2_DQS	-	-

Table 27. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	-	-	OCTOSPIM_ P1_IO4	-	-	-	-
	PH3	-	-	-	-	-	-	-	-
	PH4	-	-	-	-	I2C2_SCL	OCTOSPIM_ P2_DQS	-	-
	PH5	-	-	-	-	I2C2_SDA	-	-	-
	PH6	-	-	-	-	I2C2_SMBA	OCTOSPIM_ P2_CLK	-	-
	PH7	-	-	-	-	I2C3_SCL	OCTOSPIM_ P2_NCLK	-	-
	PH8	-	-	-	-	I2C3_SDA	OCTOSPIM_P2_IO3	-	-
	PH9	-	-	-	-	I2C3_SMBA	OCTOSPIM_P2_IO4	-	-
	PH10	-	-	TIM5_CH1	-	-	OCTOSPIM_P2_IO5	-	-
	PH11	-	-	TIM5_CH2	-	-	OCTOSPIM_P2_IO6	-	-
	PH12	-	-	TIM5_CH3	TIM8_CH4N	-	OCTOSPIM_P2_IO7	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-
	PH15	-	-	-	TIM8_CH3N	-	OCTOSPIM_P2_IO6	-	-

Table 27. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2/5/8	LPTIM1/2/3/ TIM1/2/3/4/5	ADF1/I2C4/ OCTOSPIM_P1/ OTG_FS/SAI1/ SPI2/TIM1/8/ USART2	DCMI/ I2C1/2/3/4/ LPTIM3	DCMI/I2C4/MDF1/ OCTOSPIM_P1/2/ SPI1/2/3	I2C3/MDF1/ OCTOSPIM_P2/ SPI3	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_ P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	OCTOSPIM_ P2_IO2	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	OCTOSPIM_ P2_IO1	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	OCTOSPIM_ P2_IO0	-
	PI4	-	-	-	TIM8_BKIN	-	SPI2_RDY	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_ P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_ P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	OCTOSPIM_ P2_NCLK	-	-

1. Refer to the next table for AF8 to AF15.

Table 28. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port A	PA0	UART4_TX	-	OCTOSPIM_ P2_NCS	-	SDMMC2_CMD	AUDIOCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	OCTOSPIM_ P1_DQS	LPGPIO1_P0	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	OCTOSPIM_ P1_NCS	UCPD1_ FRSTX1	-	-	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	OCTOSPIM_P1_CLK	LPGPIO1_P1	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC/ PSSI_DE	-	-	SAI1_FS_B	LPTIM2_CH1	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	OCTOSPIM_P1_IO3	LPGPIO1_P2	-	-	TIM16_CH1	EVENTOUT
	PA7	-	-	OCTOSPIM_P1_IO2	-	-	LPTIM2_CH2	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	-	TRACECLK	SAI1_SCK_A	LPTIM2_CH1	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	-	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PA12	-	FDCAN1_TX	-	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS/ UART4_DE	-	-	-	-	SAI2_FS_B	-	EVENTOUT

Table 28. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port B	PB0	-	-	OCTOSPIM_P1_IO1	LPGPIO1_P9	COMP1_OUT	AUDIOCLK	-	EVENTOUT
	PB1	LPUART1_ RTS/LPUART1_ DE	-	OCTOSPIM_P1_IO0	LPGPIO1_P3	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPIM_ P1_DQS	UCPD1_ FRSTX1	-	-	-	EVENTOUT
	PB3	-	-	CRS_SYNC	LPGPIO1_P11	SDMMC2_D2	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS/ UART5_DE	TSC_G2_IO1	DCMI_D12/ PSSI_D12	LPGPIO1_P12	SDMMC2_D3	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10/ PSSI_D10	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	DCMI_D5/PSSI_D5	-	-	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC/ PSSI_RDY	-	FMC_NL	-	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_CKIN	FDCAN1_RX	DCMI_D6/PSSI_D6	SDMMC2_D4	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_CDIR	FDCAN1_TX	DCMI_D7/PSSI_D7	SDMMC2_D5	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPIM_P1_CLK	LPGPIO1_P4	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPIM_ P1_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS/ LPUART1_DE	TSC_G1_IO1	OCTOSPIM_ P1_NCLK	-	-	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	-	-	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	SDMMC2_D0	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	-	-	FMC_NBL1	SDMMC2_D1	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port C	PC0	LPUART1_RX	-	-	-	SDMMC1_D5	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	SDMMC2_CK	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	LPGPIO1_P5	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0/PSSI_D0	SDMMC2_D6	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1/PSSI_D1	SDMMC2_D7	SDMMC1_D7	SAI2_MCLK_B	LPTIM2_CH2	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2/PSSI_D2	-	SDMMC1_D0	-	LPTIM3_CH1	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	-	LPTIM3_CH2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8/PSSI_D8	LPGPIO1_P8	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4/PSSI_D4	UCPD1_ FRSTX2	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9/PSSI_D9	LPGPIO1_P10	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port D	PD0	-	FDCAN1_RX	-	-	FMC_D2/FMC_AD2	-	-	EVENTOUT
	PD1	-	FDCAN1_TX	-	-	FMC_D3/FMC_AD3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	DCMI_D11/ PSSI_D11	LPGPIO1_P7	SDMMC1_CMD	LPTIM4_ETR	-	EVENTOUT
	PD3	-	-	OCTOSPIM_P2_NCS	-	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	OCTOSPIM_P1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	OCTOSPIM_P1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	OCTOSPIM_P1_IO6	SDMMC2_CK	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	OCTOSPIM_P1_IO7	SDMMC2_CMD	FMC_NCE/ FMC_NE1	LPTIM4_OUT	-	EVENTOUT
	PD8	-	-	DCMI_HSYNC/ PSSI_DE	-	FMC_D13/FMC_AD13	-	-	EVENTOUT
	PD9	-	-	DCMI_PIXCLK/ PSSI_PDCK	-	FMC_D14/FMC_AD14	SAI2_MCLK_A	LPTIM3_IN1	EVENTOUT
	PD10	-	TSC_G6_IO1	-	-	FMC_D15/FMC_AD15	SAI2_SCK_A	LPTIM3_ETR	EVENTOUT
	PD11	-	TSC_G6_IO2	-	-	FMC_CLE/ FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	-	FMC_ALE/ FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	LPGPIO1_P6	FMC_A18	LPTIM4_IN1	LPTIM2_CH1	EVENTOUT
	PD14	-	-	-	-	FMC_D0/FMC_AD0	-	LPTIM3_CH1	EVENTOUT
	PD15	-	-	-	-	FMC_D1/FMC_AD1	-	LPTIM3_CH2	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port E	PE0	-	-	DCMI_D2/PSSI_D2	LPGPIO1_P13	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	DCMI_D3/PSSI_D3	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	LPGPIO1_P14	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	LPGPIO1_P15	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	DCMI_D4/PSSI_D4	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	DCMI_D6/PSSI_D6	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	DCMI_D7/PSSI_D7	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4/FMC_ AD4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5/FMC_ AD5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	OCTOSPIM_P1_NC LK	-	FMC_D6/FMC_ AD6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	OCTOSPIM_P1_CLK	-	FMC_D7/FMC_ AD7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	OCTOSPIM_ P1_NCS	-	FMC_D8/FMC_ AD8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	OCTOSPIM_P1_IO0	-	FMC_D9/FMC_ AD9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	OCTOSPIM_P1_IO1	-	FMC_D10/FMC _AD10	-	-	EVENTOUT
	PE14	-	-	OCTOSPIM_P1_IO2	-	FMC_D11/FMC _AD11	-	-	EVENTOUT
	PE15	-	-	OCTOSPIM_P1_IO3	-	FMC_D12/FMC _AD12	-	-	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPIM_P1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	FDCAN1_RX	OCTOSPIM_P1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	FDCAN1_TX	OCTOSPIM_P1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	OCTOSPIM_P1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11/ PSSI_D11	-	-	SAI1_D3	TIM15_CH2	EVENTOUT
	PF11	-	-	DCMI_D12/ PSSI_D12	-	-	LPTIM4_IN1	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	LPTIM4_ETR	-	EVENTOUT
	PF13	-	-	-	UCPD1_ FRSTX2	FMC_A7	LPTIM4_OUT	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS/ LPUART1_DE	-	-	UCPD1_ FRSTX1	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	UCPD1_ FRSTX2	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE/ FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	DCMI_D13/ PSSI_D13	-	-	-	-	EVENTOUT

Table 28. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	PSSI_D14	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK/ PSSI_PDCK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8/PSSI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9/PSSI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC/ PSSI_DE	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0/PSSI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1/PSSI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2/PSSI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3/PSSI_D3	-	-	-	-	EVENTOUT
	PH13	-	FDCAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	FDCAN1_RX	DCMI_D4/PSSI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11/ PSSI_D11	-	-	-	-	EVENTOUT

Table 28. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	CAN1/TSC	CRS/DCMI/ OCTOSPIM_P1/2/ OTG_FS	LPGPIO1/ SDMMC2/ UCPD1/FMC	COMP1/2/FMC/ SDMMC1/2	LPTIM2/4/ SAI1/2	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port I	PI0	-	-	DCMI_D13/ PSSI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8/PSSI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9/PSSI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10/ PSSI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5/PSSI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC/ PSSI_RDY	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6/PSSI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7/PSSI_D7	-	-	-	-	EVENTOUT

1. For AF0 to AF7 refer to the previous table.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range and supply voltage range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 22*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 23*.

Figure 22. Pin loading conditions

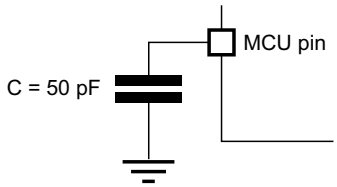
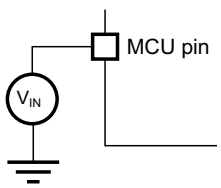


Figure 23. Pin input voltage



5.1.6 Power supply scheme

Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown in *Figure 24* and *Figure 25*. These capacitors must be placed