ABBREVIATIONS

CENTRAL PROCESSOR AND MEMORY

NOVA 1210/1220

ABC0 thru ACB15	Accumulator Buffer Register Outputs 0 thru 15
ACD	Destination Accumulator
ACD OUT	Destination Accumulator Out
ACDP	Accumulator Deposit
ACD 3 SEL	Destination Accumulator Select enable line
ACD 4 SEL	Destination Accumulator Select enable line
AC EX	Accumulator Examine
ACS	Source Accumulator
ACS 1 SEL	Source Accumulator Select enable line
ACS 2 SEL	Source Accumulator Select enable line
ACTG0, ACTG1	Accumulator Timing Generator outputs 0 & 1
ALC	Arithmetic Logic Class (instruction)
AND ENAB	AND (instruction) Enable
CLK	Clock
CLR	Clear
CLR ION	Clear Interrupt On
CON DATA	Console Data
CON INST	Console Instruction
CON RQ	Console Request
CONT	Continue switch at Console
CPU	Central Processor Unit
CPU CLK	Central Processor Unit Clock
CPU INST	Central Processor Unit Instruction
CRY ENAB	Carry Enable
CRY OUT	Carry Out
CRY SET	Carry Set
DATIA	Data In A (I/O instruction)
DATIB	Data In B (I/O instruction)
DATIC	Data In C (I/O instruction)
DATOA	Data Out A (I/O instruction)
DATOB	Data Out B (I/O instruction)
DATOC	Data Out C (I/O instruction)
DATA0 thru DATA15	I/O Data bus signals, 16 bits wide
D BUFFER	Destination (Accumulator) Buffer
INTA	Interrupt Acknowledge
INTP IN	Interrupt Priority In (to Device)
INTP OUT	Interrupt Priority Out (from Device)
INTR	Interrupt (Bus Signal from Device)
IO (F+D)	IO (instruction) (Fetch or Defer state)
IO or I/O	Input/Output
ION	Interrupt On
IO PLS	Input/Output Pulse
IORST	Input/Output Reset
IO SKIP	Input/Output Skip (instruction)
IR0 thru IR7	Instruction Register outputs 0 thru 7
ISTP	Instruction Step (Console switch)
ISZ	Increment and Skip if Zero(instruction)
JMP	Jump (instruction)
JSR	Jump to Subroutine (instruction)

KEYM	Key Memory (access cycle)
LOAD AC	Load Accumulator
LOAD ACB	Load Accumulator Buffer (Shifter)
LOAD IR	Load Instruction Register
LOAD MBO	Load Memory Bus Outputs (CPU Interface Register)
LOAD PC	Load Program Counter
MA1 thru MA15	Memory Address Register outputs 1 thru 15
MA LOAD	Load Memory Address Register
MB CLEAR	Memory Buffer Clear
MBC8 thru MBC15	Memory Buffer Computer outputs 8 thru 15
MB LOAD	Load Memory Buffer Register
MBO0 thru MBO15	Memory Bus Outputs (CPU Interface Register) 0 thru 15
MD SEL1	Multiply Divide Select 1
MD1-MD15	Memory Data 1 thru 15
SET ION	Set Interrupt On
SHIFT ACB	Shift Accumulator Buffer
SHL	Shift Left
SHR	Shift Right
SKIP INC	Skip Increment
SL0 thru SL15	Sense Lines (Memory Stack) 0 thru 15
S MULT	Source Multiplexer
SNS0 thru SNS15	Sense Amplifier Outputs 0 thru 15
S0 thru S2	(Adder function) Select Control Bits 0 thru 2
STOP INH	(Processor) STOP INHIBIT
STRB A	Strobe A (Memory Stack)
STRB B	Strobe B (Memory Stack)
STRB C	Strobe C (Memory Stack)
STRB D	Strobe D (Memory Stack)
STRT	Start (Console switch)
SWP	Swap (bytes)
TS0 thru TS3	Time State 0 thru 3
TT	Teletype
TTI	Teletype In (Teletype Keyboard/Reader Buffer)
TTO	Teletype Out (Teletype Teleprinter/Punch (Buffer)
XRS	X (plane) Read Source (Memory Stack)
XWS	X (plane) Write Source (Memory Stack)
YRS	Y (plane) Read Source (Memory Stack)
YWS	Y (plane) Write Source (Memory Stack)
32 VNR	+ 32 Volts, Not Regulated
+ VINH	+ (Memory) Inhibit Voltage
$+V_{Lamp}$	+ Lamp Voltage (Console indicators)
+ VMEM	+ Voltage Memory
+ 5 OK	+ 5 Volt (power) operating properly

ABBREVIATIONS (Continued)

AC-L-WRITE	Accumulator-Low Order (address bit)-Write
ACSX	Source Accumulators
AC WRITE	Write Accumulator
AC0	Accumulator 0
AC1	Accumulator 1
AC2	Accumulator 2
AC3	Accumulator 3
ADDER TO MEM	(Transfer) Adder (outputs) To Memory
ADDER = 0	Adder (outputs) equal zero
ALC	Arithmetic Logic Class (instruction)
ALC + IO SET	ALC or IO (instruction) SET (into the IR)
ALU	Arithmetic Logic Unit
AND	AND (logic instruction)
AND ENABLE	AND (instruction) Enable
AR	Arithmetic Register
AUT DEC	Autodecrement
AUT INC + DEC	Autoincrement or Autodecrement
CARRY	Carry (arithmetic function)
CG	Carry Generate (ALU carry function)
CLK-A	Clock A
CLK-B	Clock B
CLR	Clear
CON DATA	Console Data
CON INST	Console Instruction
CON RQ	Console Request
CONT	Continue switch at Console
CONT + ISTP + MSTP	Continue or Instruction Step or Memory Step Console switches

ABBREVIATIONS (Continued)

CPU	Central Processor Unit
CPU CLK	Central Processor Unit Clock
CPU INST	Central Processor Unit Instruction
CR	Carry Ripple (ALU carry function)
CRY	Carry
CRY SET	Carry Set
CRY TEST	Carry Test
CRY TO AR	Carry to Arithmetic Register
D	Defer
DATIA	Data In A (I/O instruction)
DATIB	Data In B (I/O instruction)
DATIC	Data In C (I/O instruction)
DATOA	Data Out A (I/O instruction)
DATOB	Data Out B (I/O instruction)
DATOC	Data Out C (I/O instruction)
DATA0 thru DATA15	I/O Data bus signals, 16 bits wide
DCH	Data Channels
DCHA	Data Channel Acknowledge
DCHA STUTTER	Extends DCHA during certain High Speed Channel operations
DCHI	Data Channel In
DCH INC EN	Data Channels Increment Enable
DCHM(0 or 1)	Data Channel Mode (0 or 1) Code type of Data Channel Cycle requested by Device
DCHO	Data Channel Out
DCHP IN	Data Channel Priority In
DCHP OUT	Data Channel Priority Out

ABBREVIATIONS (Continued)

DCHR	Data Channel Request
DCH SYNC	Data Channels Synchronization
DEFER	Defer (instruction execution state)
DIV ADD	Division Addition
DIV FIRST	First Division (cycle)
DIV LOAD CRY	Load Division Carry
D-L-H-SEL	Destination Multiplexer-Least Significant Byte-High Order (address) Selector Control line
D-L-READ	Destination Accumulator-Low Order (address bit)-Read
D-H-READ	Destination Accumulator-High Order (address bit)-Read
D-L-SEL	Destination Multiplexer-Low Order (address)-Selector Control line
D-M-H-SEL	Destination Multiplexer-Most Significant Byte-High Order (address)-Selector Control line
D-M-COM	Complement Destination Multiplexer outputs
D-MULT	Destination Multiplexer
DP	Deposit (Console function)
DP + DPN	Deposit or Deposit Next
DPN	Deposit Next (Console function)
DRIVE IO	Drive IO (Data bus)
DSZ	Decrement and Skip if Zero (instruction)
DS0-DS5	Device Select lines 0 thru 5
E	Execute
EFA	Effective Address

ABBREVIATIONS (Continued)

EFA•JSR	Effective Address and JSR (instruction)
EXEC	Execute
E•IO	Execute (State) and Input/Output (instruction)
EX	Examine (Console function)
EXN	Examine Next
EXN + DPN	Examine Next or Deposit Next
EX + EXN + DP + DPN + PL	Examine or Examine Next or Deposit or Deposit Next or Program Load (Console Key)
EX + STRT + ACDP	Examine or Start or Accumulator Deposit (Console Key)
EXT ION EN	External "Interrupt On" Enable
F	Fetch
FAST DCH	Fast (High Speed) Data Channels
FETCH	Fetch (State Accessing next instruction from Memory)
FETCH SKIP	Skip the next instruction
F + PI	Fetch or Program Interrupt (Cycle)
F SET	Fetch (State) Set
FORCE AR SHIFT	Force Arithmetic Register (to) Shift
FORCE D-L-SEL	Force Destination Accumulator-Low Order (address bit) to Selectors
FORCE MEM CY	Force Memory Cycle
FORCE MQ OUT & AC-L-WRITE	Multiply/Divide function

ABBREVIATIONS (Continued)

FORCE PLUS ONE	Adds one to Adder
FORCE SEL X	Control line which manipulates Adder output data via the SEL-N, SEL-L, SEL-R & SEL-S lines.
FORCE SEL Y	Control line which manipulates Adder output data via the SEL-N, SEL-L, SEL-R & SEL-S lines.
FORCE-SX-COM	Force Complement Source Multiplexer outputs
FORCE-SX-H-READ	Force Source (Accumulators) High Order (address bit) Read
FORCE SX-L-READ	Force Source (Accumulators) Low Order (address bit) Read
FORCE-SX-H-SEL	Force Source (Multiplexer) High Order (address bit) Selector line
FORCE-SX-L-SEL	Force Source (Multiplexer) Low Order (address bit) Selector line
GND LAMP	Special Ground for Console Display Lamps
HALT	Halt (Machine State)
HAS E CYCLE	Indicates instruction has execute Cycle
INC PC	Increment Program Counter
INH DCH	Inhibit Data Channels
INH GATE A	Inhibit Gate (signal) A (Memory)
INH GATE B	Inhibit Gate (signal) B (Memory)
INH0 thru INH15	Inhibit (Memory Buffer) Register outputs 0 thru 15
INHIBIT	Inhibit (Memory Writing function)
INHIBIT SELECT	Prevents Memory from being Selected
INH TRANS	Inhibit Transmission
INTP IN	Interrupt Priority In (to Device)
INTP OUT	Interrupt Priority Out (from Device)

ABBREVIATIONS (Continued)

INTR	Interrupt (Bus Signal from Device)
INT RQ	Interrupt Request
IO or I/O	Input/Output
ION	Interrupt On
ION SYNC	Interrupt On Synchronization
IO OUT EN	Input/Output-Output Enable
IO PLS	Input/Output Pulse
IORST	Input/Output Reset
IO SKIP	Input/Output Skip (instruction)
IO SKP PEND	Input/Output Skip Pending
IO SKP SYNC	Input/Output Skip Synchronization
IO STUTTER	Cycle extend for IO operation
IO UNPROTECTED	Indicates IR contains IO instruction
IR0 thru IR15	Instruction Register outputs 0 thru 15
ISTP	Instruction Step (Console switch)
ISZ	Increment and Skip if Zero (instruction)
JMP	Jump (instruction)
JSR	Jump to Subroutine (instruction)
JMP + JSR	Jump or Jump to Subroutine (instruction)
KEY	Operational Cycle manually implemented at the Console
KEY M	Key cycle with Memory (access Cycle).
KEY M • PL	Key Memory and Program Load
KEY • PRESET	Key (cycle) and Preset
KEY SEEN + RESTART	Key Seen or Restart (from Power Monitor Option)
LDA	Load Accumulator (instruction)
LOAD AR	Load Arithmetic Register
LOAD CRY	Load Carry
LOAD PC	Load Program Counter

ABBREVIATIONS (Continued)

MA LOAD	Memory Address Load
MA1 thru MA15	Memory Address Register Outputs 1 thru 15
MB	Memory Buffer
MB CLEAR	Memory Buffer Clear
MB LD EN	Memory Buffer Load Enable
MB LOAD	Memory Buffer Load
MBO INH	Memory Buffer Output (bus) Inhibit
MBO0 thru MBO15	Memory Buffer (bus) Outputs 0 thru 15
MD1 thru MD15	Memory (address) Data (input lines) 1 thru 15
MEM CLK	Memory Clock
MEM CY SET	Memory Cycle Set
MEM LATCH	Memory (Register, CPU-2) Latch
MEM OK	Memory OK (Power Supply Monitor signal)
MEM OUT	Memory (bus) Out
MEM 0 thru MEM15	Memory Bus lines 0 thru 15
MID	Midpoint (of 800ns extended DCH or IO cycle)
MQ0 thru MQ15	Multiplier Quotient Register Outputs 0 thru 15
MSKO	Mask Out (instruction)
MSTP	Memory Step (Console switch)
MUL + DIV	Multiply or Divide (instruction)
MUL + DIV DECODE	Multiply or Divide Decode
MUL + DIV TC	Multiply or Divide Terminal Count
NEW CRY	New Carry
NON ACD INST	Non Destination Accumulator Instruction
OMIT STROBE	Omit (Memory) Strobe
OVFLO	Signal to Device that memory location being incremented Via Data Channels has Overflowed

ABBREVIATIONS (Continued)

OVFLO TO DIV	Overflow (signal) to Divide Control
PC	Program Counter
PC CLK	Program Counter Clock
PC TO MEM	Program Counter to Memory
PI	Program Interrupt
PI SET	Program Interrupt Set
PL	Program Load
PL LAST	Program Load Last
PL• LAST WORD	Program Load Last Word
PLUS ONE	Plus One (to the Adder)
PRESET	Preset (Computer initializing signal)
PTG0 thru PTG3	Processor Timing (pulses) 0 thru 3
PWR LOW	Power Low (Power Monitor output signal)
READ CY	(Memory) Read Cycle
READ IO	Read IO (Data bus)
READ 1	Read 1 (Memory Timing signal, CPU-1)
READ 2	Read 2 (Memory Timing signal, CPU-1)
READ 1B	Read 1B (Memory Timing signal, Memory)
READ 2B	Read 2B (Memory Timing signal, Memory)
REAL IO INST	Indicates instruction is not Multiply/ Divide
RELOAD DISABLE	Disable Load inputs of (Memory) MB Register
RESTART	RESTART (power Monitor output signal)
RESTART ENABLE	Signal that permits RST and STOP Console Key functions
RINH0 thru RINH15	(Collector) Resistor, Inhibit Driver
ROM ENABLE	PL Read Only Memory Enable

ABBREVIATIONS (Continued)

RQENB	Request Enable
RST	Restart (Console switch)
RUN	Primary operational requirement for program execution
RUN SET	Input signal for Run Flip-flop
SARD	Select Address
SELB	Selected Busy (Bus signal)
SELD	Selected Done (Bus signal)
SELECT	Decoded (Memory) Select signal
SEL-L	Select Left Shift (Adder output data)
SEL-N	Select No Shift (Adder output data)
SEL-R	Select Right Shift (Adder output data)
SEL-S	Select Swap (Adder output data bytes)
SHIFT AR LEFT	Shift Arithmetic Register Left
SNS0 thru SNS15	Sense Amplifier Outputs 0 thru 15
STA	Store Accumulator (instruction)
STATE SUPPRESS	Supersedes Major States for DCH & certain Key cycle operations
STOP	(Processor) Stop
STROBE	Strobe (signal, CPU-1)
STOP RQ	(Processor) Stop Request
STRB A	Strobe A (Memory Stack)
STRB B	Strobe B (Memory Stack)
STRB C	Strobe C (Memory Stack)
STRB D	Strobe D (Memory Stack)
STRT	Start (Console switch)
SUM CRY	Sum Carry
SUPPRESS	Suppress signal implemented by Multiply/Divide

ABBREVIATIONS (Continued)

SX-COM	Complement Source Multiplexer outputs
SX-H-READ	Source Accumulator-High Order (address bit)-Read
SX-H-SEL	Source Multiplexer-High Order (address bit)-Selector Control line
SX-L-READ	Source Accumulator-Low Order (address bit)-Read
SX-L-SEL	Source Multiplexer-Low Order (address bit)-Selector Control line
SX-MULT	Source Multiplexer
TSM	PTG States 1 or 2, equivalent to 2nd half of TS0 & first half of TS3
TS0	Time State 0
TS3	Time State 3
TT	Teletype
TTI	Teletype In (Teletype Keyboard/ Reader Buffer)
TTO	Teletype Out (Teletype Teleprinter/ Punch (Buffer)
WAIT	Implements Processor pause during High Speed DCH operation
WRITE	Control function, Memory Cycle Timing, CPU-1
WRITE AC	Write Accumulator (logically associated with AC Write signal)
WRITE MEM	Write Memory (enables X and Y Memory drivers)

ABBREVIATIONS (Continued)

WRITE SYNC	Control function, Memory Cycle Timing, CPU-1
XRS	X (plane) Read Source (Memory Stack)
XWS	X (plane) Write Source (Memory Stack)
YRS	Y (plane) Read Source (Memory Stack)
YWS	Y (plane) Write Source (Memory Stack)
32 VNR	+ 32 Volts, Not Regulated
±SL0 thru ± SL15	Memory Stack Bipolar sense inputs to Sense Amplifiers
+ VINH	+ (Memory) Inhibit Voltage
+ V_{Lamp}	+ Lamp Voltage (Console indicators)
+ VMEM	+ Voltage Memory
+ 5 OK	+ 5 Volt (power) Operating properly
=0 ENABLE	Enables "Adder =0", gates for AC =0 and for auto indexing addressing