#### DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.

The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

#### **PIN CONFIGURATIONS**

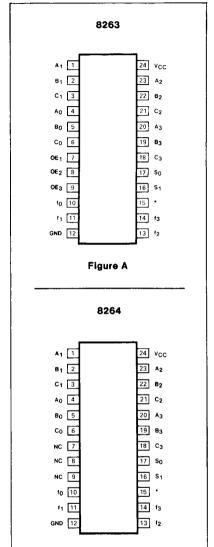


Figure B

\*Data complement

# ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN COMMERCIAL RANGES CONF. V <sub>CC</sub> =5V±5%; T <sub>A</sub> =0°C to +75°C		MILITARY RANGES  V <sub>CC</sub> =5V±5%; T <sub>A</sub> =-55°C to +125°C			
Plastic DIP	Fig.A Fig.B	N8263N N8264N				
Ceramic DIP	Fig.A Fig.B	N8263F N8264F	S8263F S8264F			
Flatpak	Fig.A Fig.B		\$8263Q \$8264Q			

### **TRUTH TABLE**

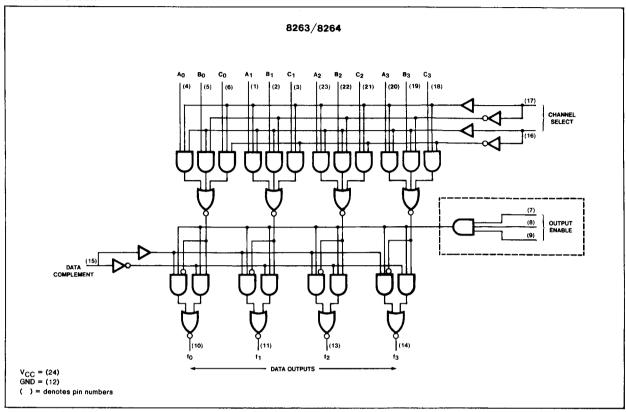
DATA INPUT		CHANNEL SELECT		DATA	OUTPUT ENABLE	DATA	
An	Bn	Cn	s <sub>0</sub>	S <sub>1</sub>	COMPLEMENT	(8264)	OUTPUTS
An	Х	Х	н	н	L	н	An
X	Bn	Х	L	Н	L	Н	Bn
Х	X	Cn	н	L	L	н	Cn
Χ	X	X.	L	L	L	н	0
An	Х	Х	Н	Н	н	н	$\overline{A}_n$
X.	$B_n$	Х	L	Н	н	н	Ā <sub>n</sub> <mark>B̄<sub>n</sub> C̄<sub>n</sub></mark>
Х	x	Cn	Н	L	Н	Н	$\overline{C}_n$
Х	X	x.	L	L	н	Н	нÏ
Х	Х	Х	Х	Х	x	L	н

H = HIGH

L = LOW

X = Don't care

## LOGIC DIAGRAM



## DC ELECTRICAL CHARACTERISTICS

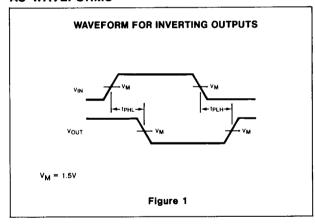
PARAMETER		TEST CONDITIONS	8263		8264		UNIT
		7201 GONDINIONS	Min	Max	Min	Max	UNIT
Voн	Output HIGH voltage	V <sub>CC</sub> = 4.75V, I <sub>OH</sub> = -800μA	2.6				V
ЮН	Output HIGH current	V <sub>CC</sub> = 4.75V, V <sub>OUT</sub> = 2.0V				200	μΑ
VOL	Output LOW voltage 8263 8264	V <sub>CC</sub> = 4.75V, I <sub>OL</sub> = 9.6mA I <sub>OL</sub> = 16.mA		0.4		0.4	٧
ΊL	Input LOW current A <sub>n</sub> ,B <sub>n</sub> ,C <sub>n</sub> ,OE,DC S <sub>0</sub> ,S <sub>1</sub>	V <sub>CC</sub> = 5.25V, V <sub>IN</sub> = 4.5V		-1.6 -3.2		-1.6 -3.2	mA mA
lHI.	Input HIGH current A <sub>n</sub> ,B <sub>n</sub> ,C <sub>n</sub> ,OE,DC S <sub>0</sub> ,S <sub>1</sub>	V <sub>CC</sub> = 5.25V, V <sub>IN</sub> = 4.5V		40 80		40 80	μ <b>Α</b> μ <b>Α</b>
los	Output short circuit current	V <sub>CC</sub> = 5V, V <sub>OUT</sub> = OV	-20	-70			mA
lcc	Supply current	V <sub>CC</sub> = 5.25V		80		90.4	mA

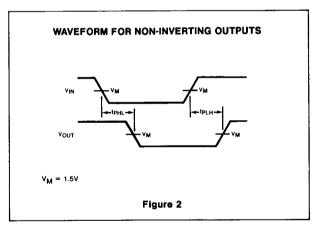
# AC CHARACTERISTICS: $T_A = 25^{\circ}C$ (See Section 4 for Waveforms and Conditions)

PARAMETER			$8263$ $C_{L} = 18pF$ $R_{1} = \infty \Omega$ $R_{2} = 150\Omega$		8264 C <sub>L</sub> = 30pF R <sub>1</sub> = 360Ω R <sub>2</sub> = 440Ω		UNIT
		TEST CONDITIONS					
			Min	Max	Min	Max	
tPLH tPHL	Propagation delay A <sub>n</sub> to f <sub>n</sub>	Figures 1 & 2		26 26		36 36	ns ns
tPLH tPHL	Propagation delay S <sub>0</sub> , S <sub>1</sub> to f <sub>n</sub>	Figures 1 & 2		36 36		36 36	ns ns
tPLH tPHL	Propagation delay DC to f <sub>n</sub>	Figures 1 & 2		26 26		30 30	ns ns
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation delay OE to f <sub>n</sub>	Figure 1				30 30	ns ns

#### NOTE

### **AC WAVEFORMS**





b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.