

8 | 7 | 6 | . | 5 | **4** | 3 | 2 | 1

REVISIONS				
BYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		CHG. PN. PN 002954 WAS 002754. AW REV B ECN 2490	11/17/75	JKR
B		ADDED R50 THRU R53 ECN 2732 AW REV A	5/21/76	JKR RLF
C		R12 WAS 5.6K 1/4W P/N 002780 PER ECN 3371 5/12/76 BR	5/12/ 76	JKR

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PARTS LIST

### SPARE GATES (OUTPUTS LISTED ONLY)

TYPE - 74

IC 8-8

TYPE - 07

IC9-8

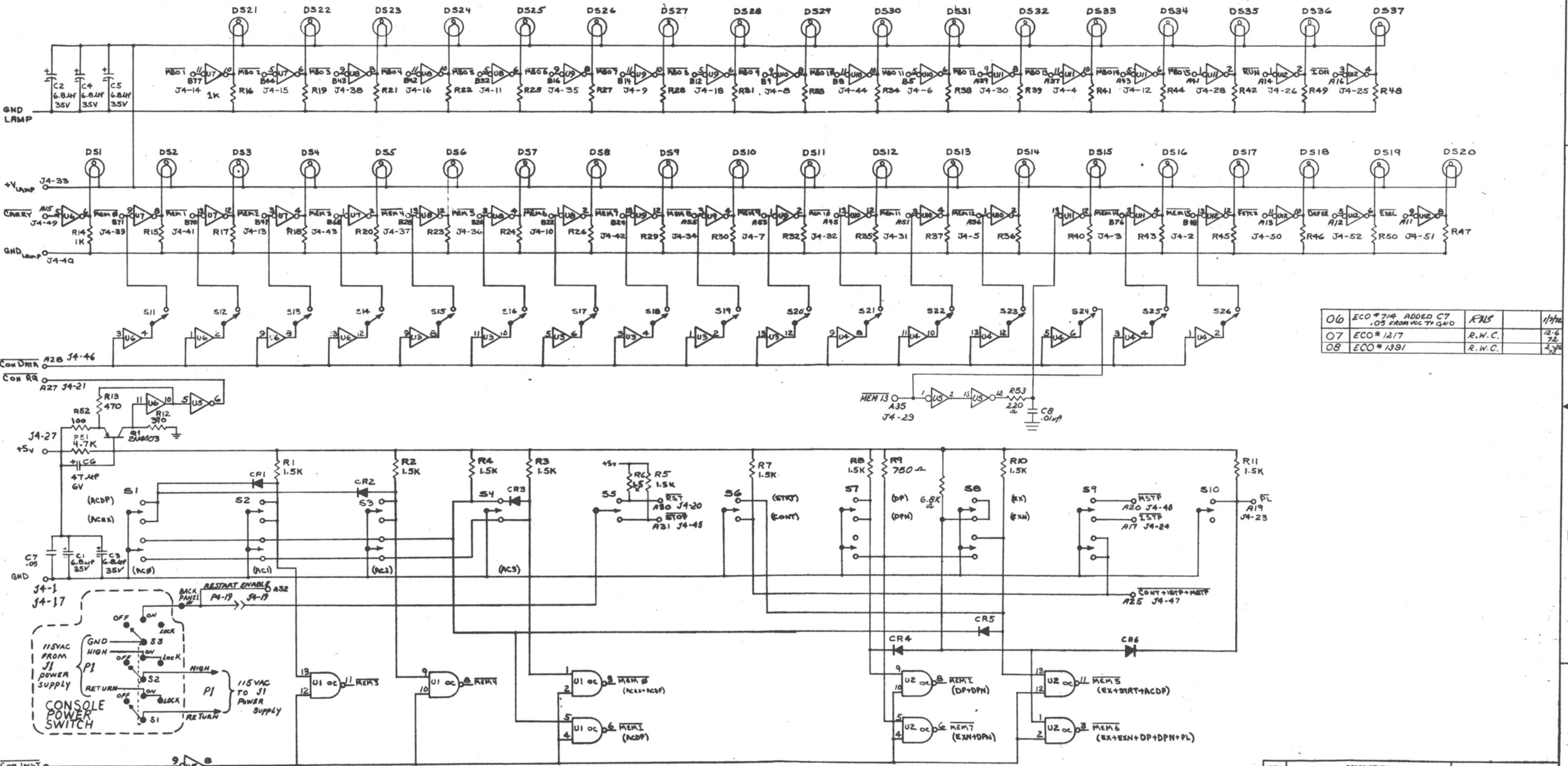
A C1,C2,C3,C5,C6,C8,C9,C10  
C12,C14,C15,C16,C18,C20,C22

G6	G5	G4	G3	G2	G1	ITEM NO.	SIZE	PART NO.	DESCRIPTION	M / P	U OF M															
QUANTITY PER GROUP						DRAWING NO.		LIST OF MATERIAL																		
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<p><b>DIGITAL COMPUTER CONTROLS, INC.</b> FAIRFIELD, NEW JERSEY 07006</p> <p>APPROVAL DATE</p> <table border="1"> <tr> <td>DR. FRANK LEPORE</td><td>10/25/74</td></tr> <tr> <td>CHK. <i>Alvin</i></td><td>11/16/74</td></tr> <tr> <td>ENG. <i>G. R. L.</i></td><td>11/20/74</td></tr> <tr> <td>APPD. <i>4-13</i></td><td>11/20/74</td></tr> </table> <p>MAT'L</p> <p>FINISH</p> <p>SIZE D</p> <p>SCALE</p> <p>SHEET 3 OF 3</p> <p>D-116 LED FRONT PANEL LOGIC</p> <p>REV C</p>												DR. FRANK LEPORE	10/25/74	CHK. <i>Alvin</i>	11/16/74	ENG. <i>G. R. L.</i>	11/20/74	APPD. <i>4-13</i>	11/20/74							
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REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
02	ECO #110	W.J.G.	W.J.G.	12-16-70
03	ECO #261	R45		5-10-71
04	G110 2A4403 / ECO #250	R45		5-20-71
05	ECO #407	W.J.G.		8/5/71

SEE BELOW

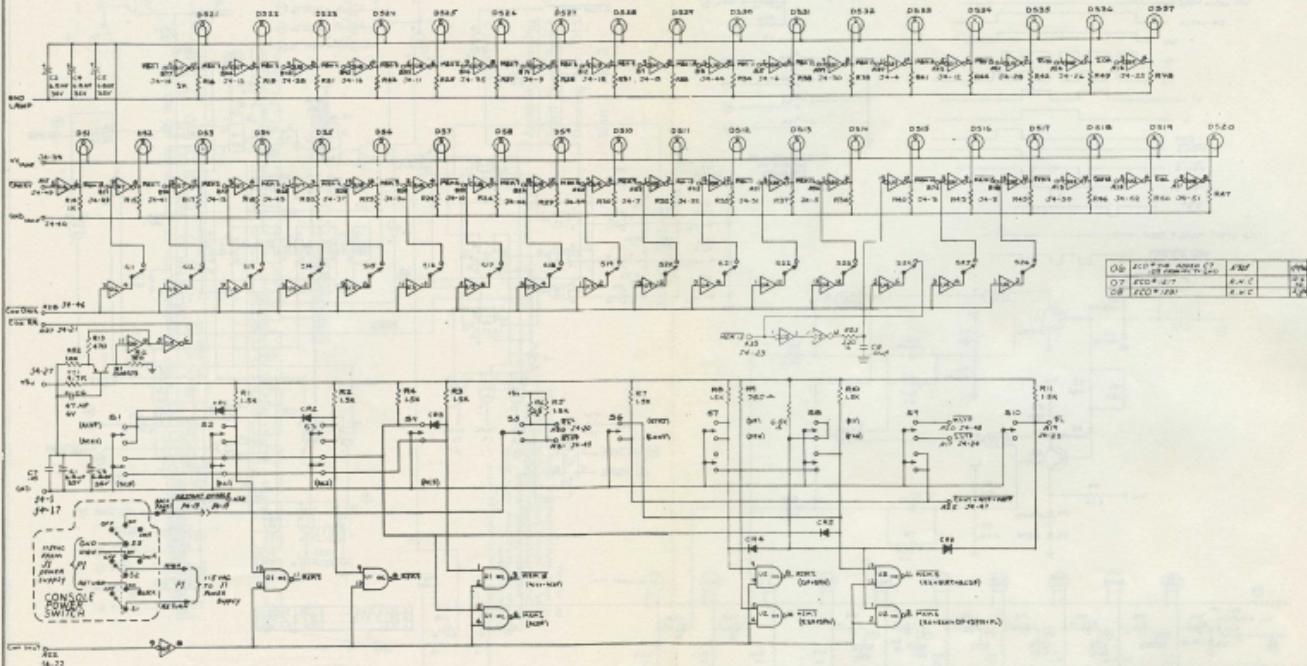


QTY.	DESCRIPTION	PART NO.
DRAWN G. G.	10-8-70	DATA GENERAL CORPORATION
CHECKED K. French	12/8/70	SOUTHBORO, MASSACHUSETTS 01772
ENGINEER G. G.	12/8/70	TITLE
APPROVED		NOVA 800/1200
MATERIAL		CONSOLE
FINISH		
SCALE		
SIZE D 001	CODE 000089	DRAWING NUMBER REV 08

SHEET 1 OF 1

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REVISED			
REV	DESCRIPTION	DATE	VER BY
DSS	ECCO 620	8/27/80	J.D.M.
DSS	ECCO 620	9/1/80	J.D.M.
DSS	QV70 Update Rev D	10/1/80	J.D.M.
DSS	ECCO 620	10/1/80	J.D.M.

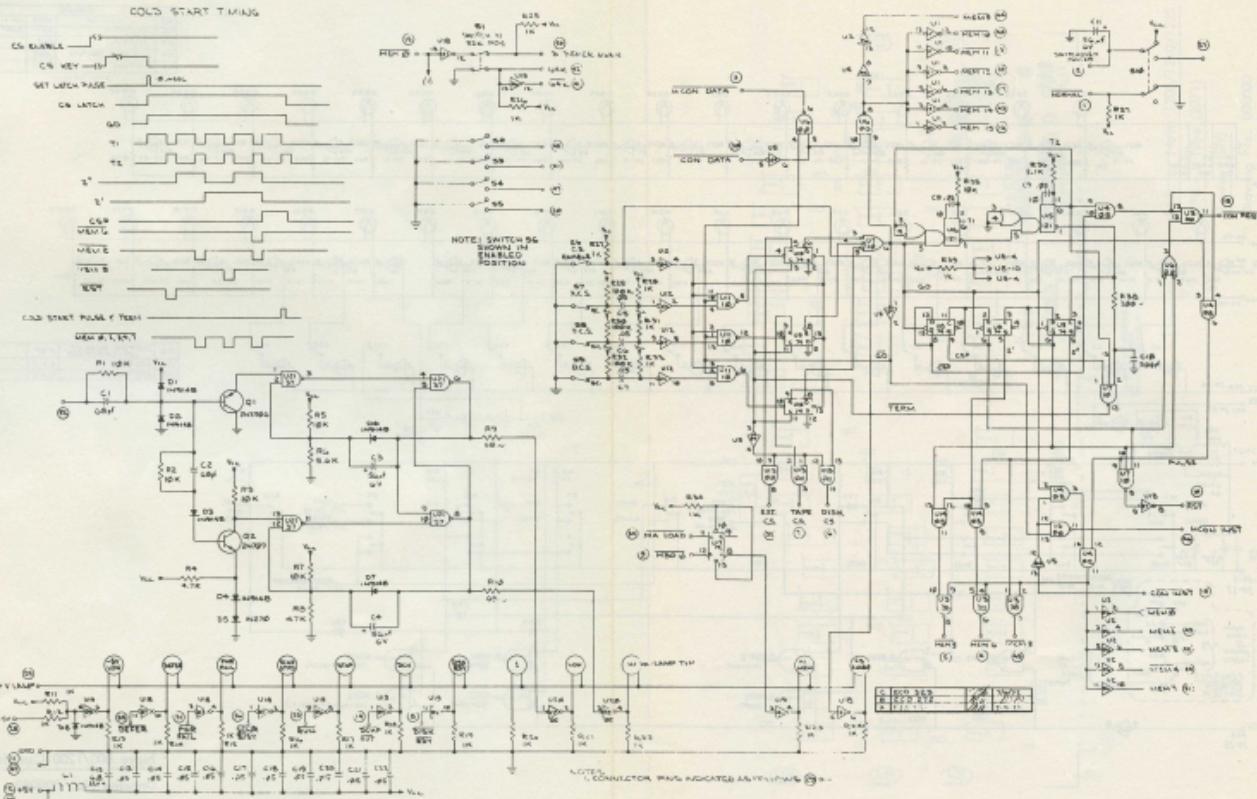


Nova 800/1200 Console

Drawing No. 000089

Blatt 1 von 1

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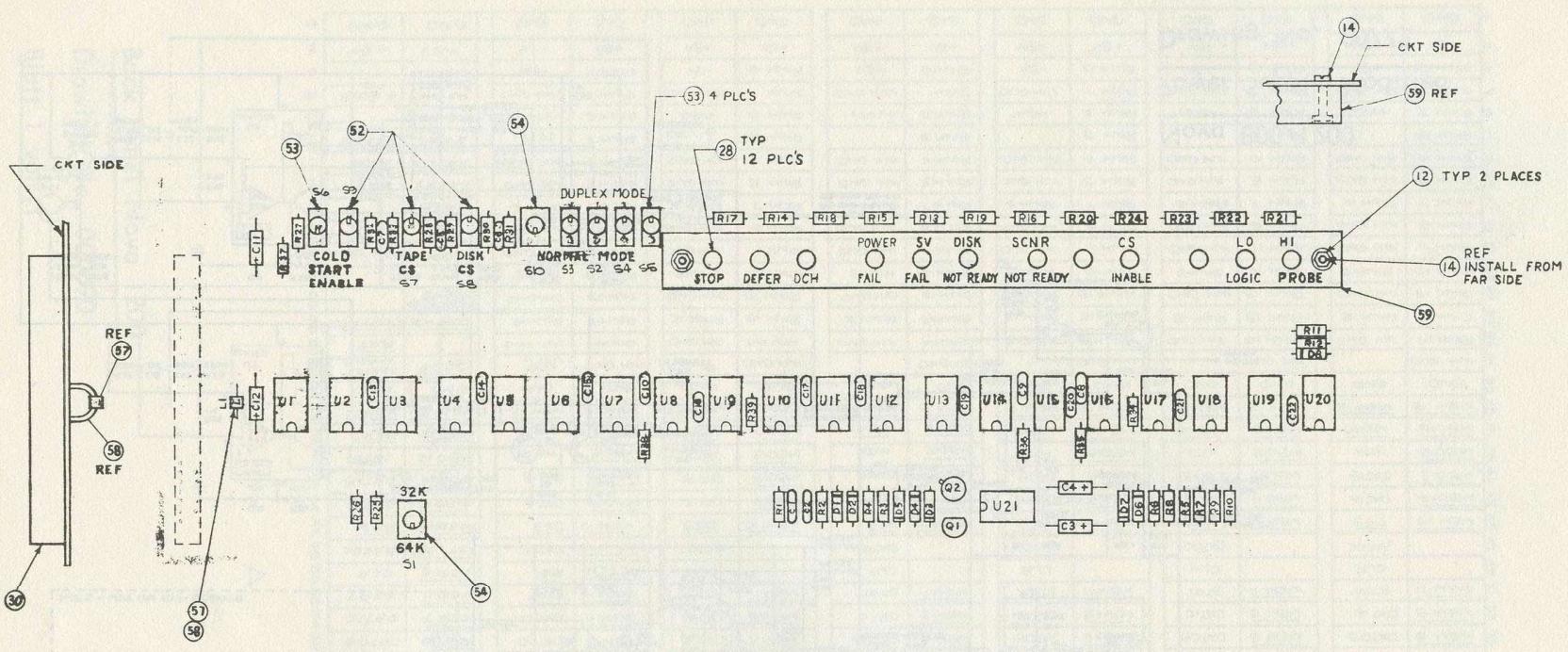
DSS 620

Assembly Drawing

Front Panel Board

Drawing No. 01571

Blatt 3 von 3



NOTES:

1. INSTALL ITEMS 12, 14, 30, & 59 AFTER WAVE SOLDERING.
2. MASK ITEM 30 MOUNTING HOLES ON THE CKT SIDE PRIOR TO WAVE SOLDER
3. LEAD PROTRUSION FROM CKT SIDE OF BOARD TO BE .062 IN. MAX EXCEPT SWITCHES S1 THRU S10 TO HAVE MAX ALLOWABLE LEAD PROTRUSION OF .156 IN.

## SECTION K

### THE OPERATOR'S CONSOLE

#### INTRODUCTION

The console illustrated in Figure K-1, has a set of ADDRESS lights which display the contents of the MBO bus; a set of DATA lights which display the contents of the MEM bus; a register of toggle switches which will output to the MEM bus; a row of control switches at the bottom of the panel which instruct the computer on what to display in the lights, what to do with the information in the toggle switches, where to start or stop and how. The console also has a three position keyed rotary switch which turns power on and off and locks some of the operating switches.

#### CONSOLE LIGHTS AND SWITCHES

All the lights in the console are continually drawing about 10ma each through series resistors, so their filaments are always hot (but not glowing) and large surge currents are avoided when the filaments are driven on.

#### The Console ADDRESS Lights

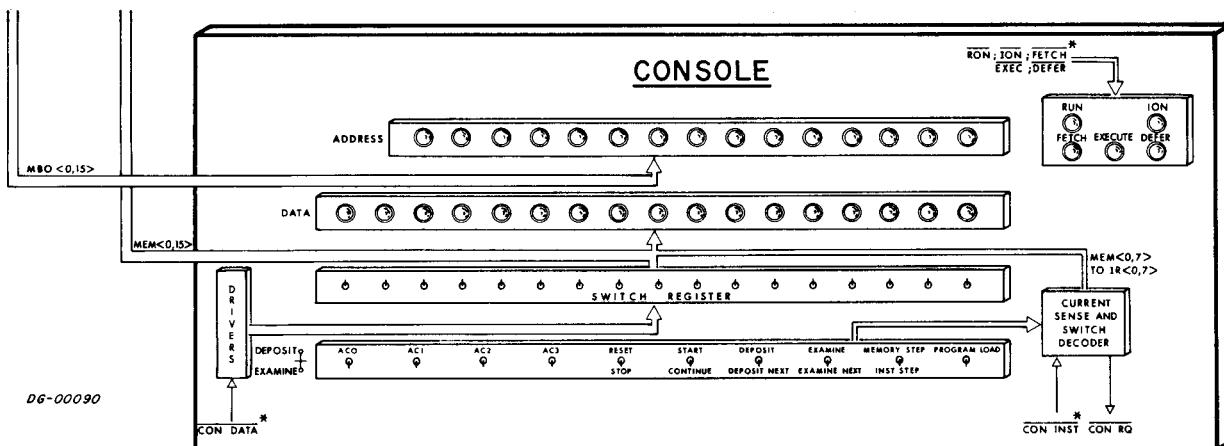
These lights are always showing the state of the MBO bus which is driven directly from the MBO register. When the machine is running, the MBO register is continually shifting, so the display is meaningless; when the machine is stopped, the MBO register shows the contents of the PC, i.e., the next address.

#### The Console DATA Lights

These lights are always showing the state of the MEM bus. When the machine is running this bus carries data from memory to the instruction and MBO registers; when the machine is stopped this bus contains the contents of the memory buffer of the last memory selected.

#### The Console Operational Indicators

These lights are driven directly from their corresponding flip-flops in the central processor.



\* Issued by CPU

Figure K-1 The Console

## The Console Switch Register

These switches connect non-inverting open collector buffers directly to the MEM bus. All Drivers go low when the CON DATA level goes low; CON DATA is issued by the CPU during the READS instruction or during a console operation that requires input from these switches, such as EXAMINE.

## The Console Control Switches

All the control switches except STOP and RESET are wired through pull-up resistors to a common circuit which detects when current is flowing through a switch, initiates a delay to suppress contact bounce and then issues the signal CON REQ to the CPU. This signal forces the CPU into the key sequence shown in Figure K-2 which returns the signal CON INST to the console. CON INST connects switches AC0, AC1, AC2, AC3, DEPOSIT, DEPOSIT NEXT, EXAMINE and EXAMINE NEXT through a decoder to the MEM <0, 7> lines, which are input to the Instruction Register and interpreted as shown in Table K-1. The computer then goes into either the KEY or KEYM major state and follows the flows of Figure K-3.

The switches RESET, STOP, MEMORY STEP, INSTRUCTION STEP and PROGRAM LOAD are wired separately to the CPU. RESET stops the computer at the end of the current cycle, issues the IORST pulse to all I/O devices, clears ION and sets the real time clock to the line frequency. STOP simply stops the computer at the end of the current instruction.

MEMORY STEP takes the processor through the current state and then stops. INST STEP takes the processor through the current state and on to the end of the current instruction. Both signals force a CON RQ to the CPU and output MSTP and ISTP respectively. PROGRAM LOAD deposits the contents of the bootstrap ROM into locations 0-37 and the machine at location 0. It outputs the signal PL to the CPU.

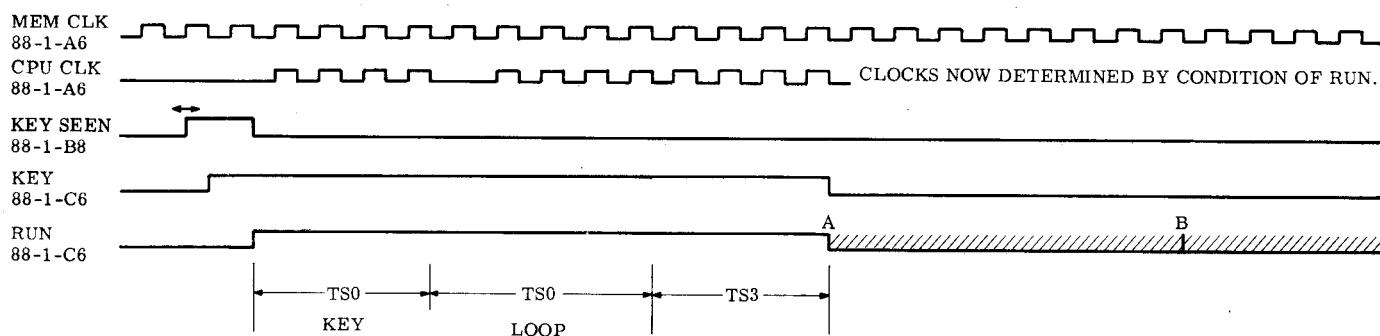
## The Console Rotary Switch

This switch controls the primary power to the power supply. It has three positions:

- |      |  |
|------|--|
| OFF  | - the primary power is removed from the power supply                                     |
| ON   | - the primary power is applied to the power supply                                       |
| LOCK | - the primary power is applied to the power supply but the STOP RESET switch is disabled |

## REFERENCES

1. "How To Use The Nova Computers" 015-000009-00.
2. Nova 800/1200 Console Print D-001-000089-05.



- A. RUN RESETS IF KEY WAS AC EXAMINE OR AC DEPOSIT;  
NEXT STATE IF RUN DOES NOT RESET;  
KEYM-IF KEY WAS DEPOSIT, DEPOSIT NEXT, EXAMINE, EXAMINE NEXT OR PROGRAM LOAD.  
FETCH-IF KEY WAS START
- B. RUN RESETS IF KEY WAS DEPOSIT, DEPOSIT NEXT, EXAMINE OR EXAMINE NEXT.

NOTE: IF KEY WAS CONTINUE, INSTRUCTION STOP OR MEMORY STOP

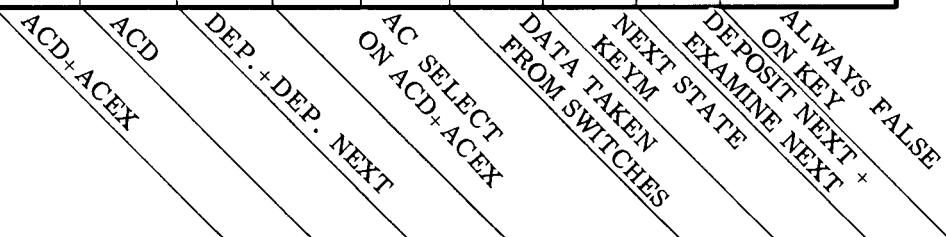


Figure K-2 The CPU Key Sequence Timing Diagram

Table K-1  
Control Switch Decoding To The Instruction Register

CONSOLE INSTRUCTION		IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7	IR8 TO 15
AC DEP.	AC0	0	0	1	0	0	0	1	1	0
	AC1	0	0	1	0	1	0	1	1	0
	AC2	0	0	1	1	0	0	1	1	0
	AC3	0	0	1	1	1	0	1	1	0
AC EXAM.	AC0	0	1	1	0	0	1	1	1	0
	AC1	0	1	1	0	1	1	1	1	0
	AC2	0	1	1	1	0	1	1	1	0
	AC3	0	1	1	1	1	1	1	1	0
DEPOSIT		1	1	0	1	1	1	0	1	0
DEPOSIT NEXT		1	1	0	1	1	1	0	0	0
EXAMINE		1	1	1	1	1	0	0	1	0
EXAMINE NEXT		1	1	1	1	1	1	0	0	0
MEMORY STEP		1	1	1	1	1	1	1	1	0
INSTRUCTION STEP		1	1	1	1	1	1	1	1	0
PROGRAM LOAD		1	1	1	1	1	1	0	1	0
START		1	1	1	1	1	0	1	1	0

WHEN BIT  
GOES FALSE



DG-00036

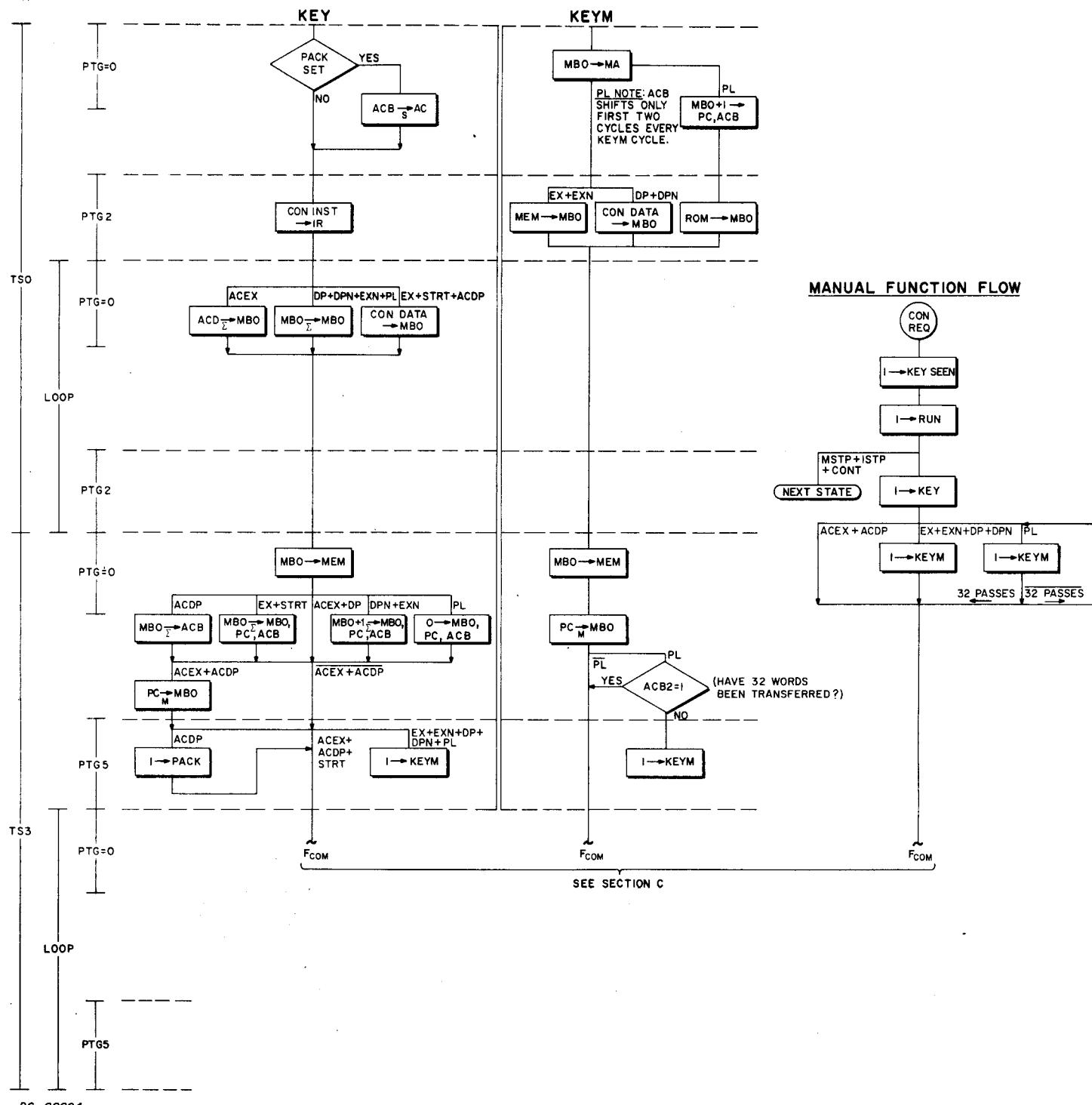


Figure K-3 Key, KEYM and Manual Flow Diagrams