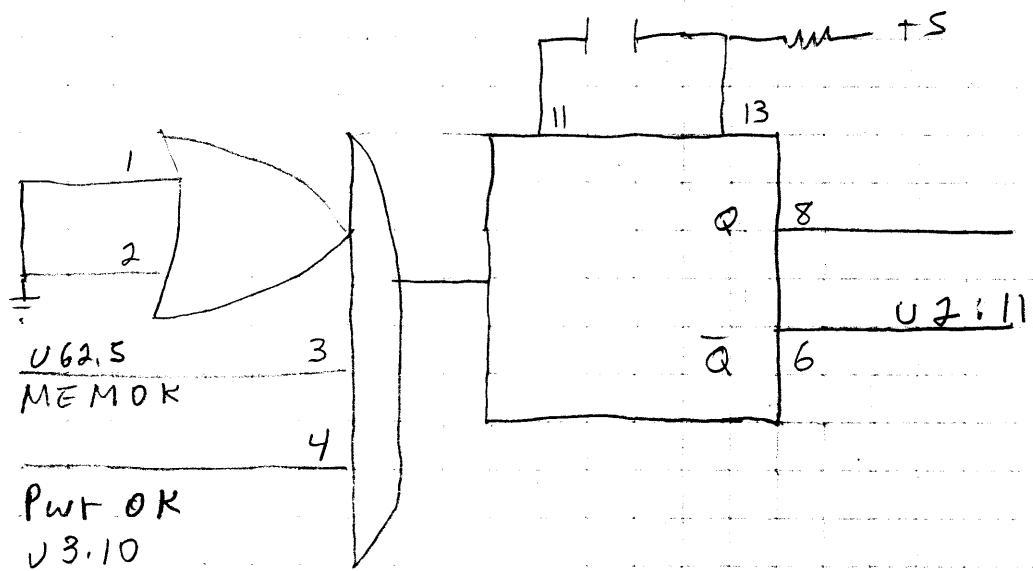


DG 1200 CPU

DG 1200 U1 9601



A9 Memor 5 top counting fingers

not actual pos

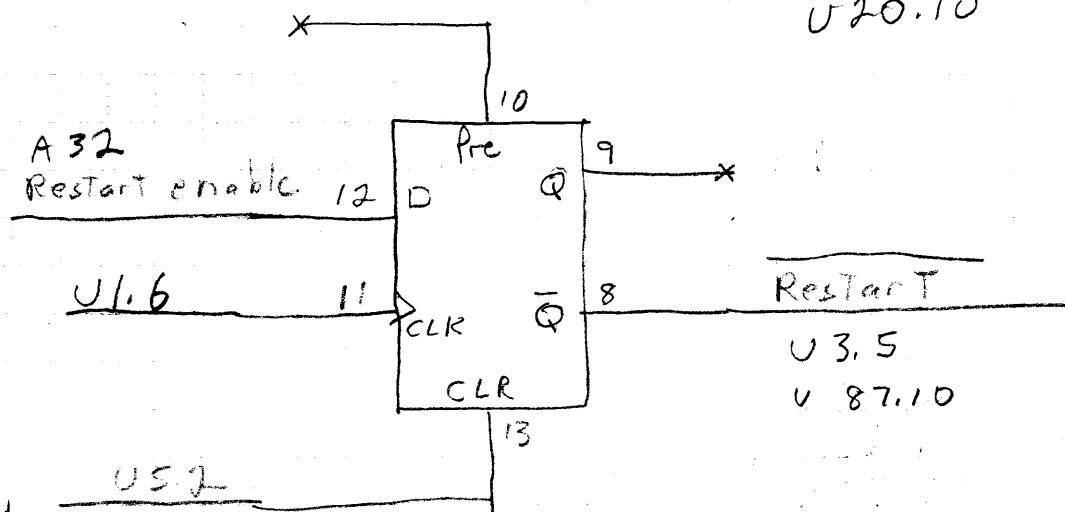
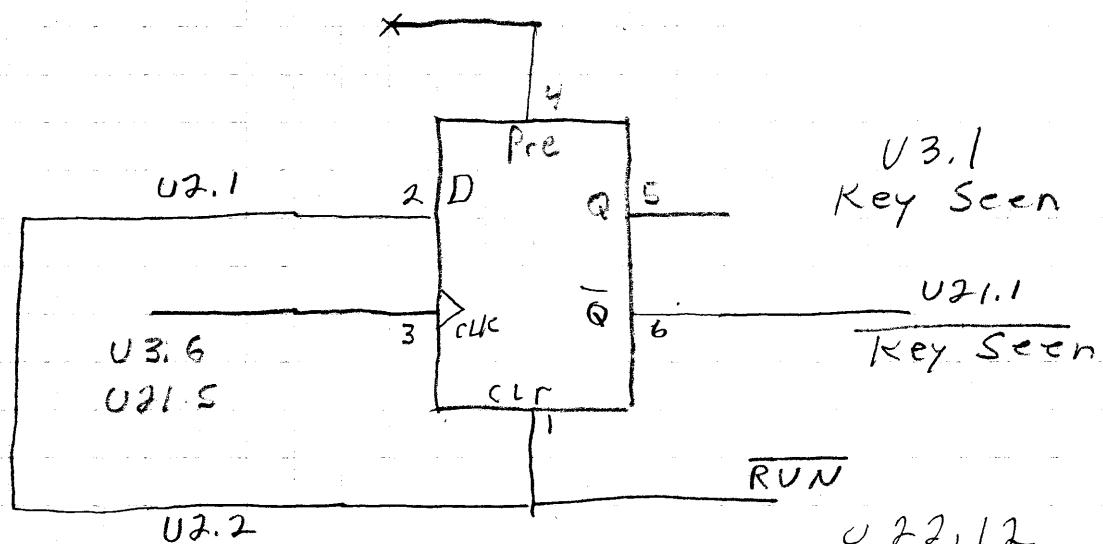
A8 Pwt ok 4 Bottom Counting fingers top or bottom

AS Pwfail 3 top U86.12

A32
Resta

U1

DG 1200 U2 7474
8828 OK



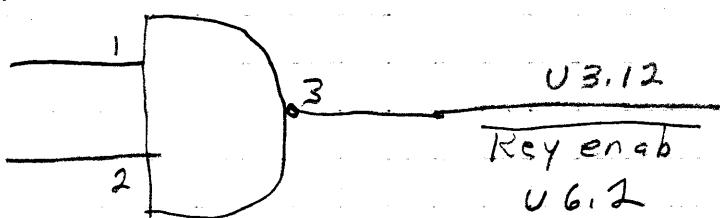
DG 1200 U3 9002
7400

OK

U2.5 U23.13

Key Seen

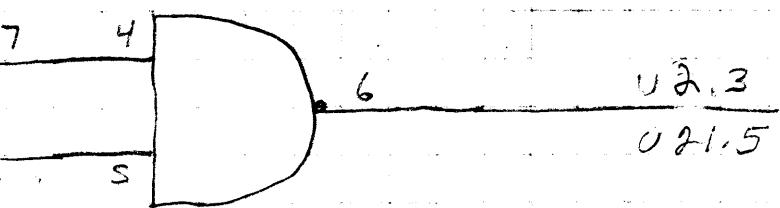
A2S
CONT+STP+ISTP



CON RQ A27 4

Restart

U87.10 U2.8



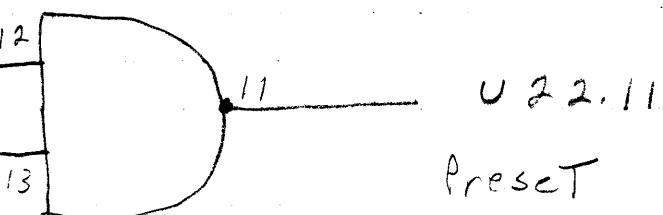
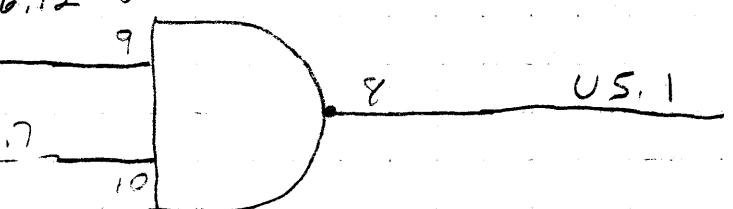
MTGO U16.12 U36.4

U1.4 U125.7

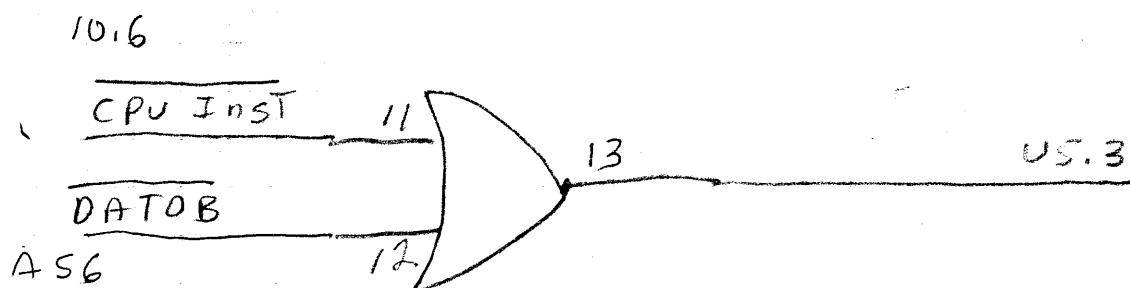
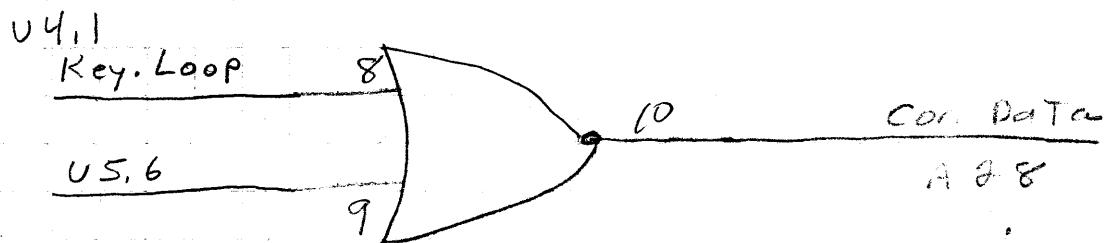
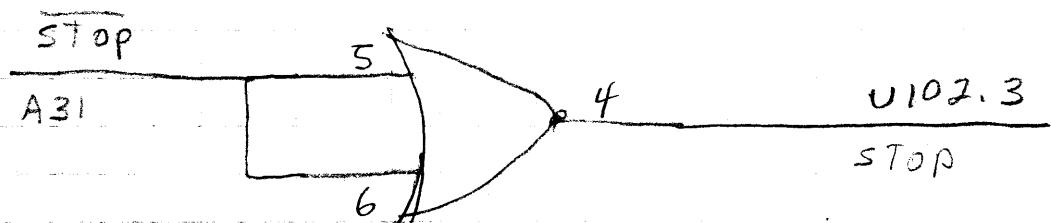
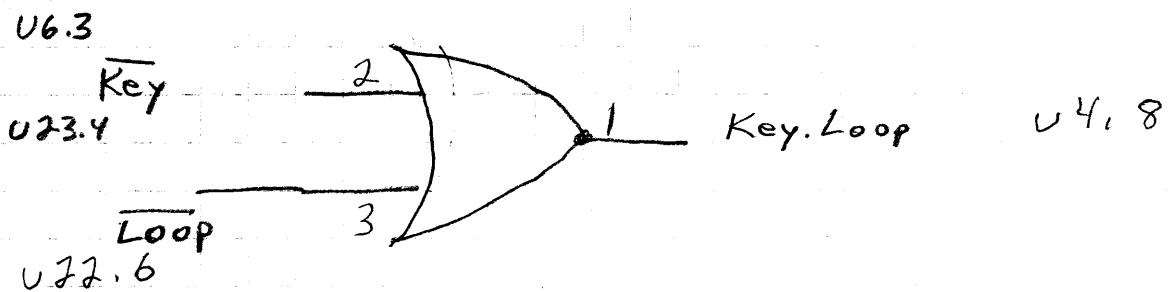
Pwr OK

Key enab U6.2
U3.3

U22.4
U21.9 Reset
U113.1 U10.13
U62.8



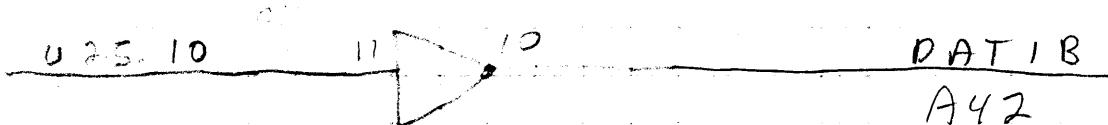
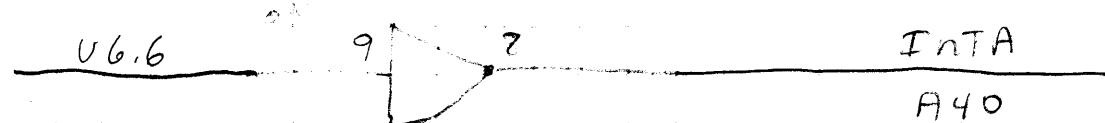
PG 1200 U4 8885
7402 OK



DG 1200.05

8H90

OK



OK

DG 1200 U6

OK

U 34.8 U 36.9
Key U 55.5
U 23.5 U 46.1 1
U 61.5 U 43.9 2
Key enab
U 3.3 U 3.12

9002
7400

OK

U 4.2 U 44.5
U 23.4 U 56.4, 9
Key U 70.11
U 84.10
U 99.10

DATIB A42 4
CPU INST
U 6.10 5
U 6.11

U 5.9

A54
DATIC 9
CPU INST
6.11 6.5 10

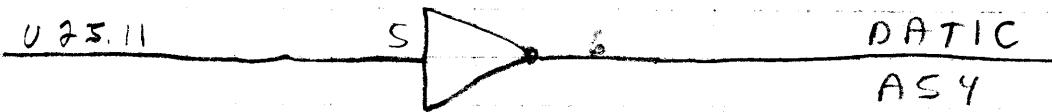
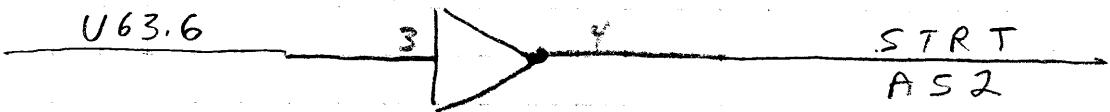
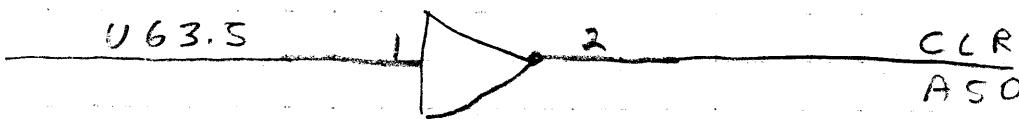
U 10.12
U 10.10
U 10.9

CPU Inst 12
U 10.6 13

11

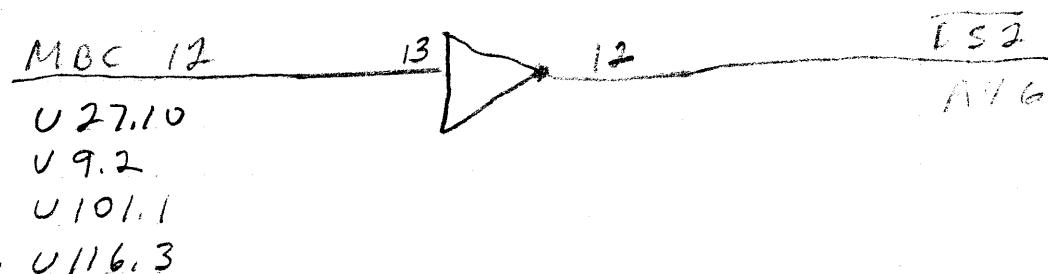
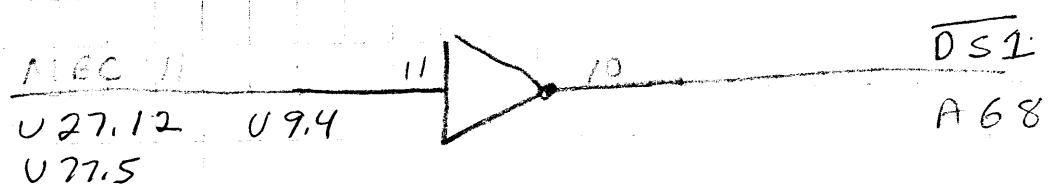
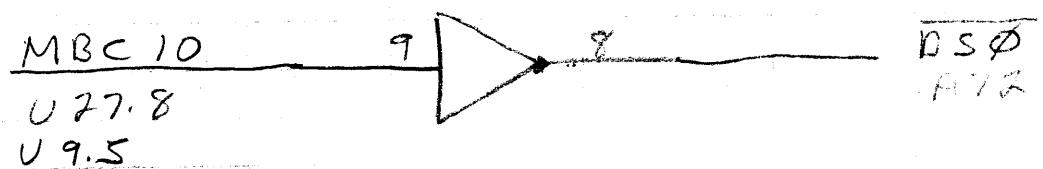
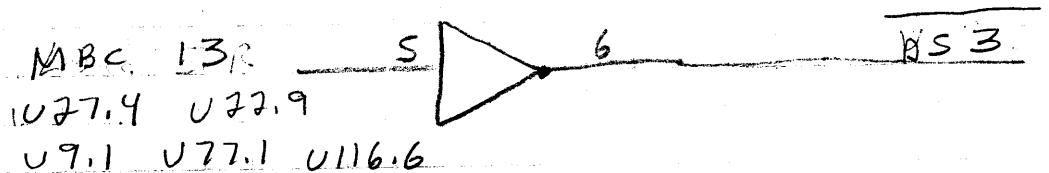
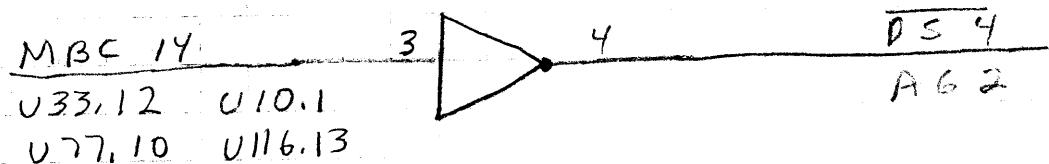
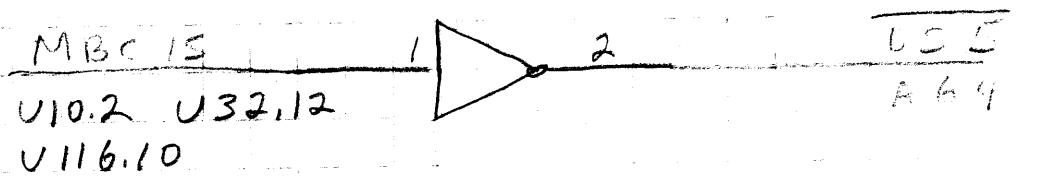
CPU INST
U 6.5 U 11.2
U 6.10 U 11.12
U 24.4 U 64.2
U 71.2 U 87.4

DC 1200 U7 8H90 -OK



PG 1200 U8 8H90

OK



DG 1200 U9

MC 3026

7.4.121

U27.4 U22.9

MBC 13

MBC 12 U27.10

MBC 11 U27.12

MBC 10

U27.8

U8.9

OK

OK

6

U70.5

U67.12 U1710 U88.1 U88.2

PTG = \emptyset , TS3

U27.6 U42.3

IOP+D

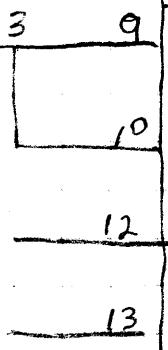
IP7

U44.3

U28.12

U64.13

U87.1



OK

U66.11

CPU CLK

DG 1200 U10

9009

7420 7440

OK

U33.12

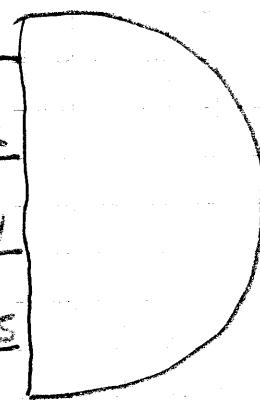
IC6017

U8.3 1

IC6015 U8.1 2

IC62 U13.9 4

U9.6 5



OK

CPU TEST

11

U4.611

U6.12,13

U6.8 9

10

12

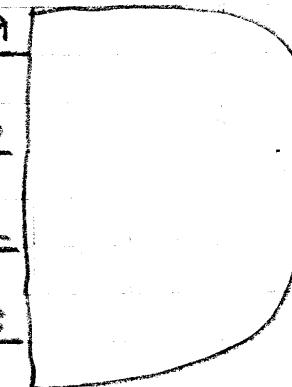
13

Reset

U113.1

U21.9

U62.8

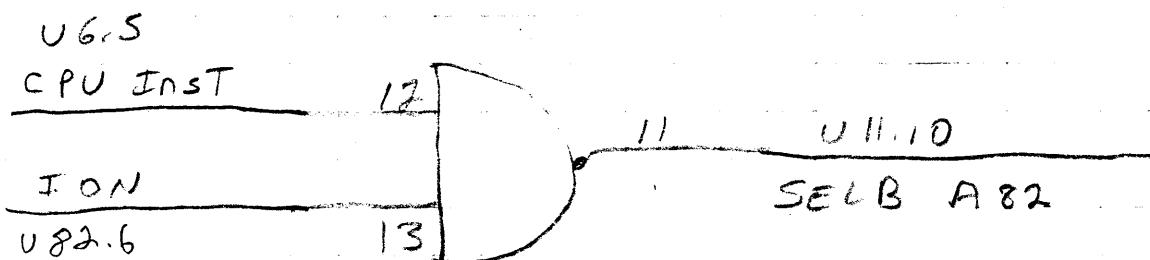
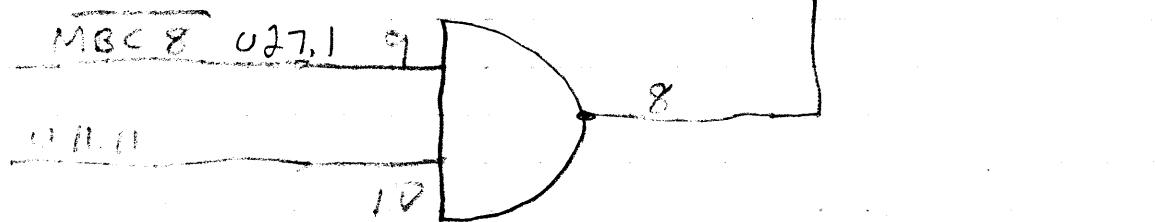
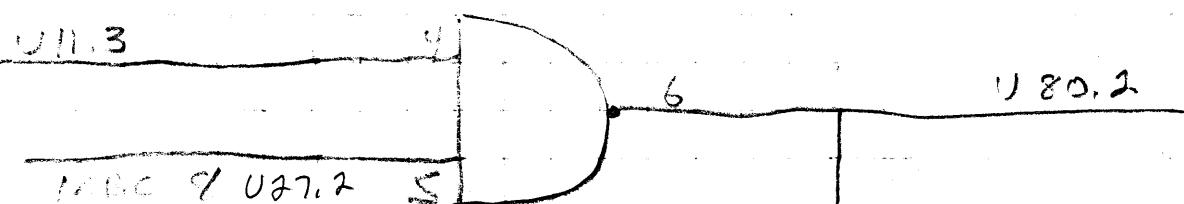
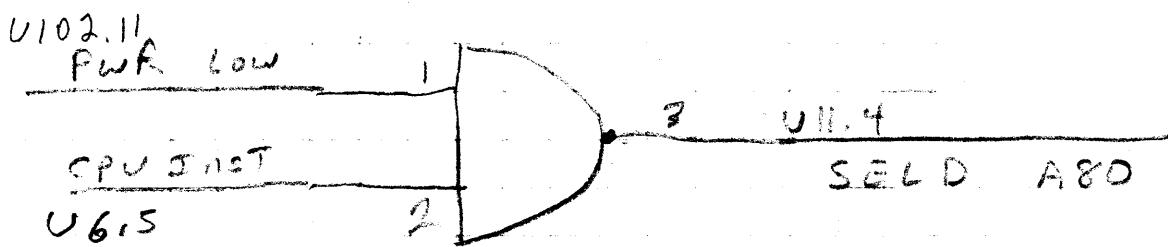


OK

I/O RST
A70

DG 1200 U 11 7438

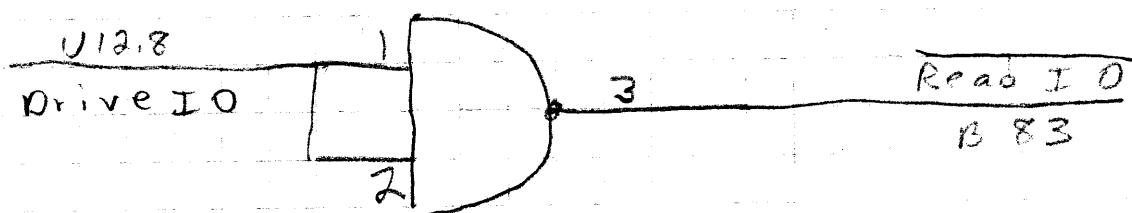
OK



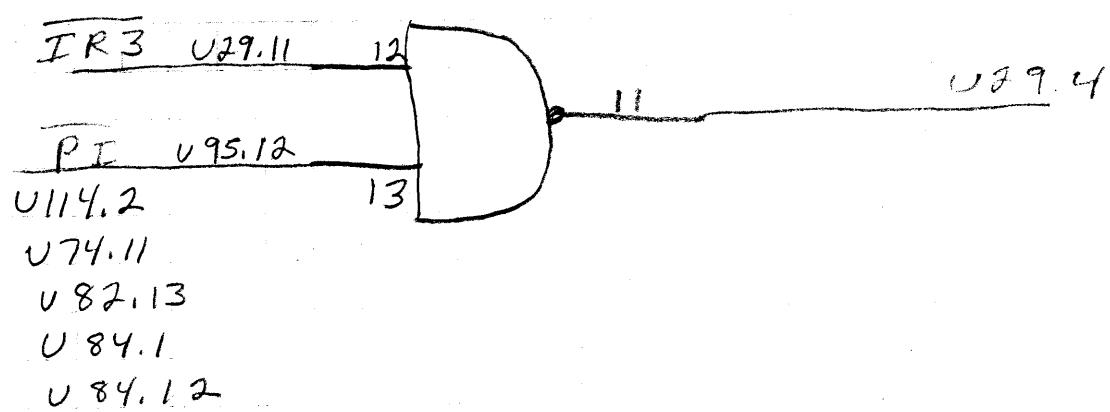
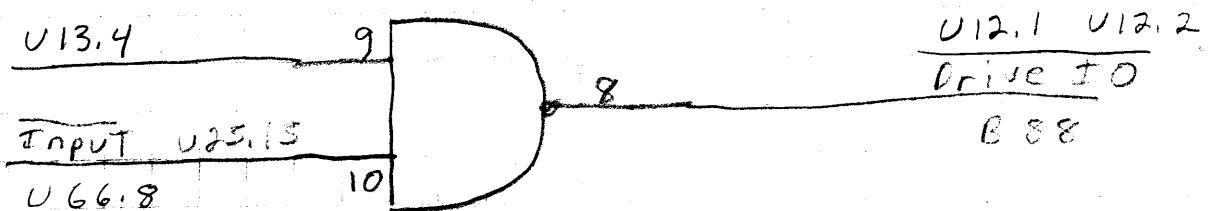
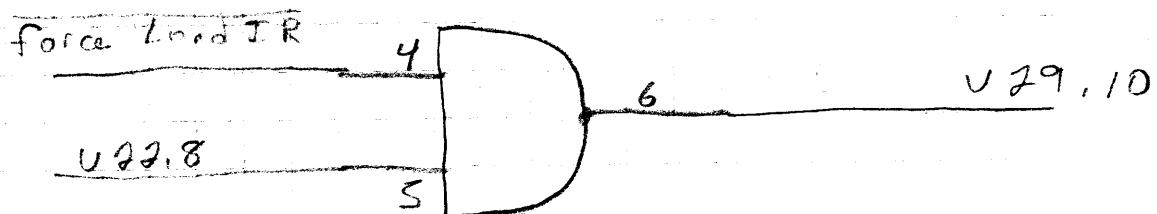
DG 1200 U12

9002
7400

OK



A 85

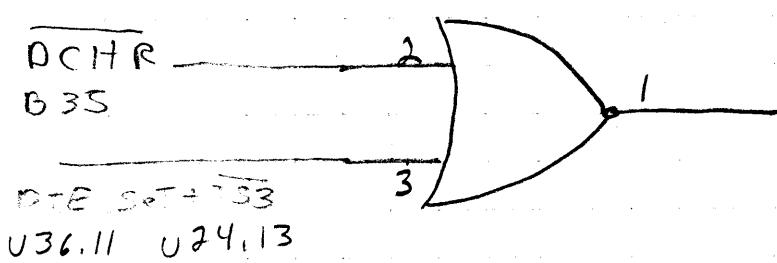


DG 1200 U13

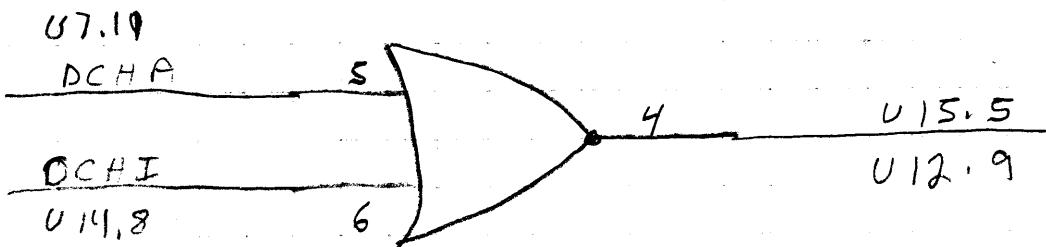
~~8885~~

7402

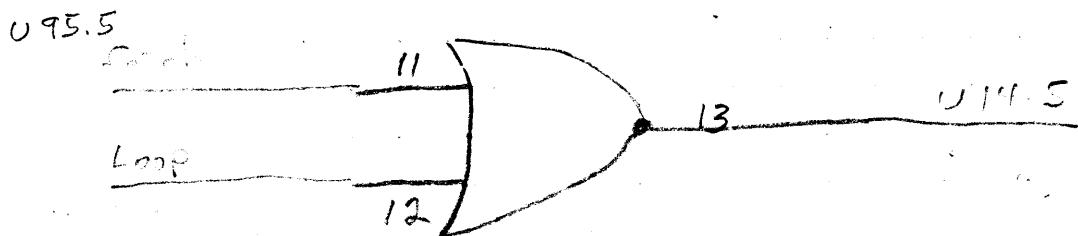
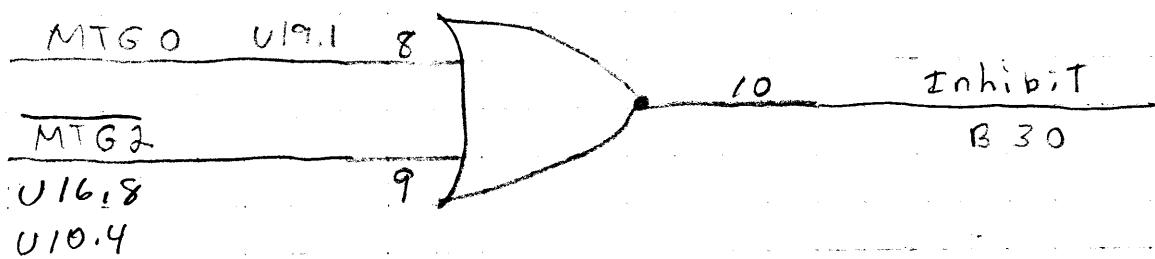
OK



DCHR Pend
U71.13



U15.5
U12.9

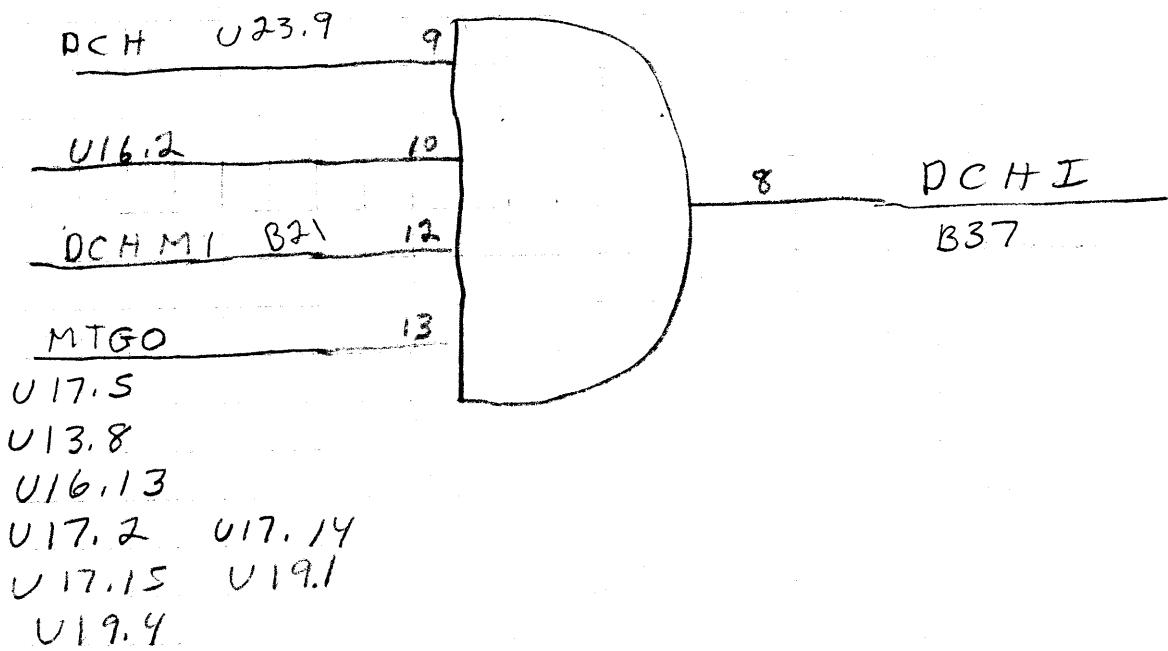
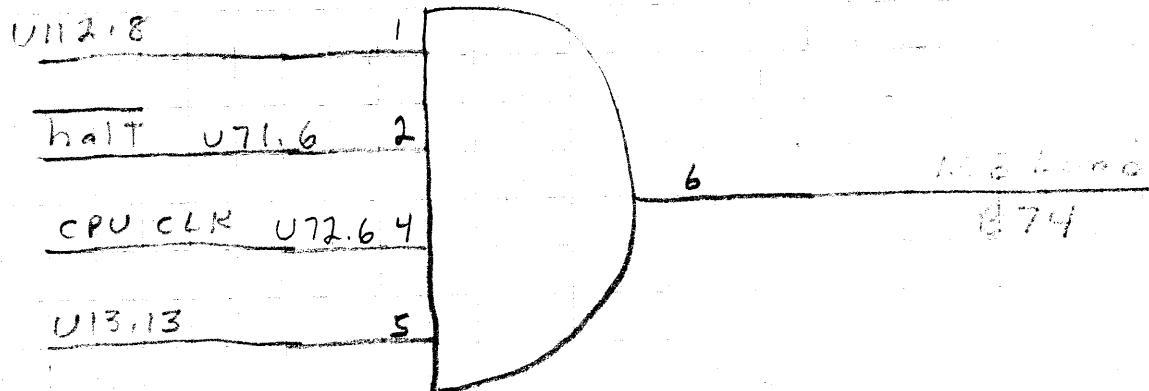


U22.5 U47.9
U64.5 U70.6
U103.7

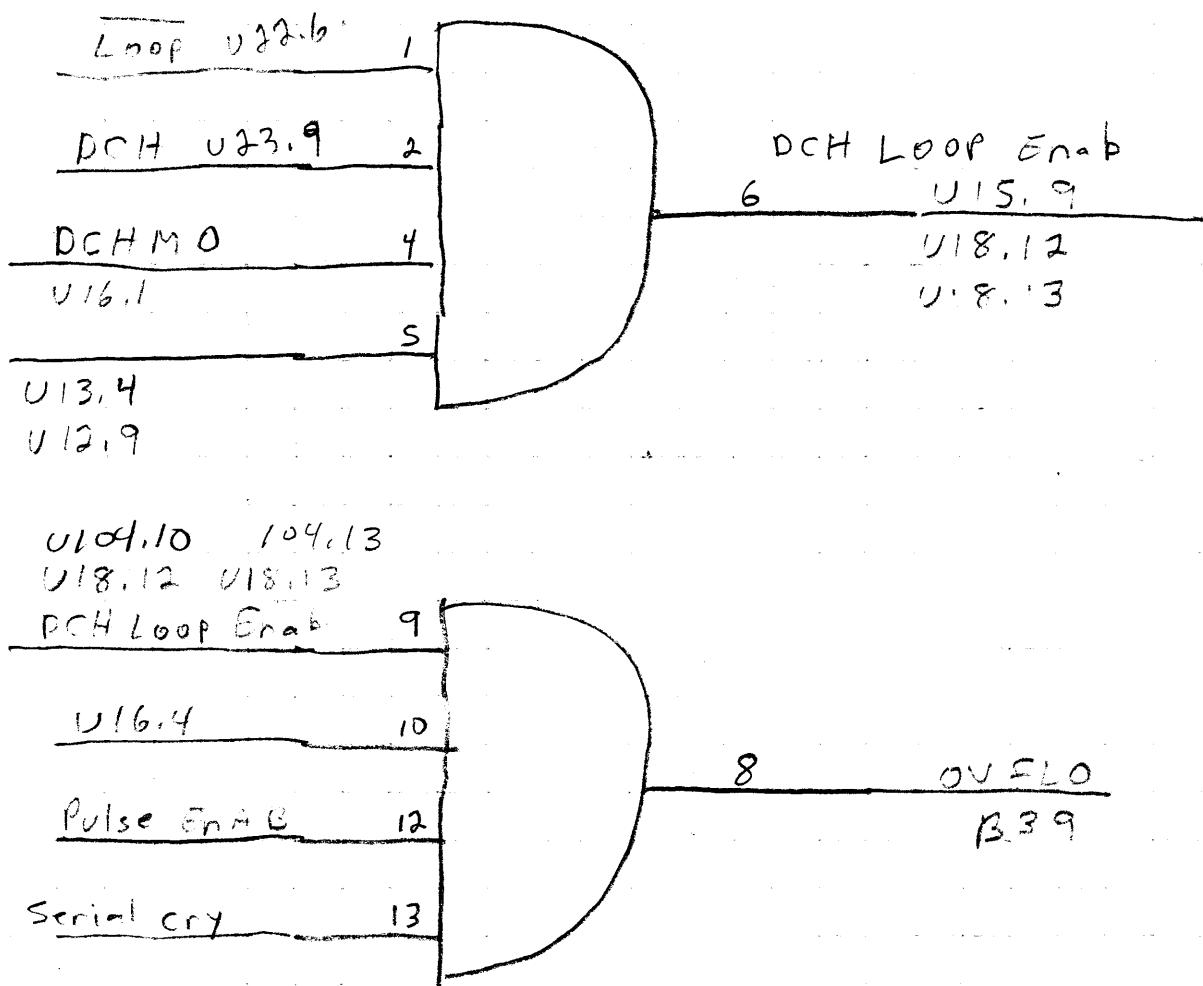
U1
R
D
U17
U13
U16
U17
U17
U1

DG 1200 U14 MC3026
74 H21

OK



DG 1200 U15 MC3026
74 H21



DG 1200 U16 81490 OK

OK

U15.4

DCHMO

B17

1

2

U14.10

DCHM1

B21

3

4

U15.10

MTG1

U16.11 U17.7

U19.10

5

6

RQENB

B41

MTG2

U18.5 U17.9

7

8

MTG2

U13.9

U17.7

MTG1 U16.5

U19.10

11

10

MTG1

U19.5

U18.10

U17.5

MTG0

U13.8

U14.13

U17.2

U17.14

U17.15

U19.1

U19.4

13

12

MTG0

U16.12 U17.10

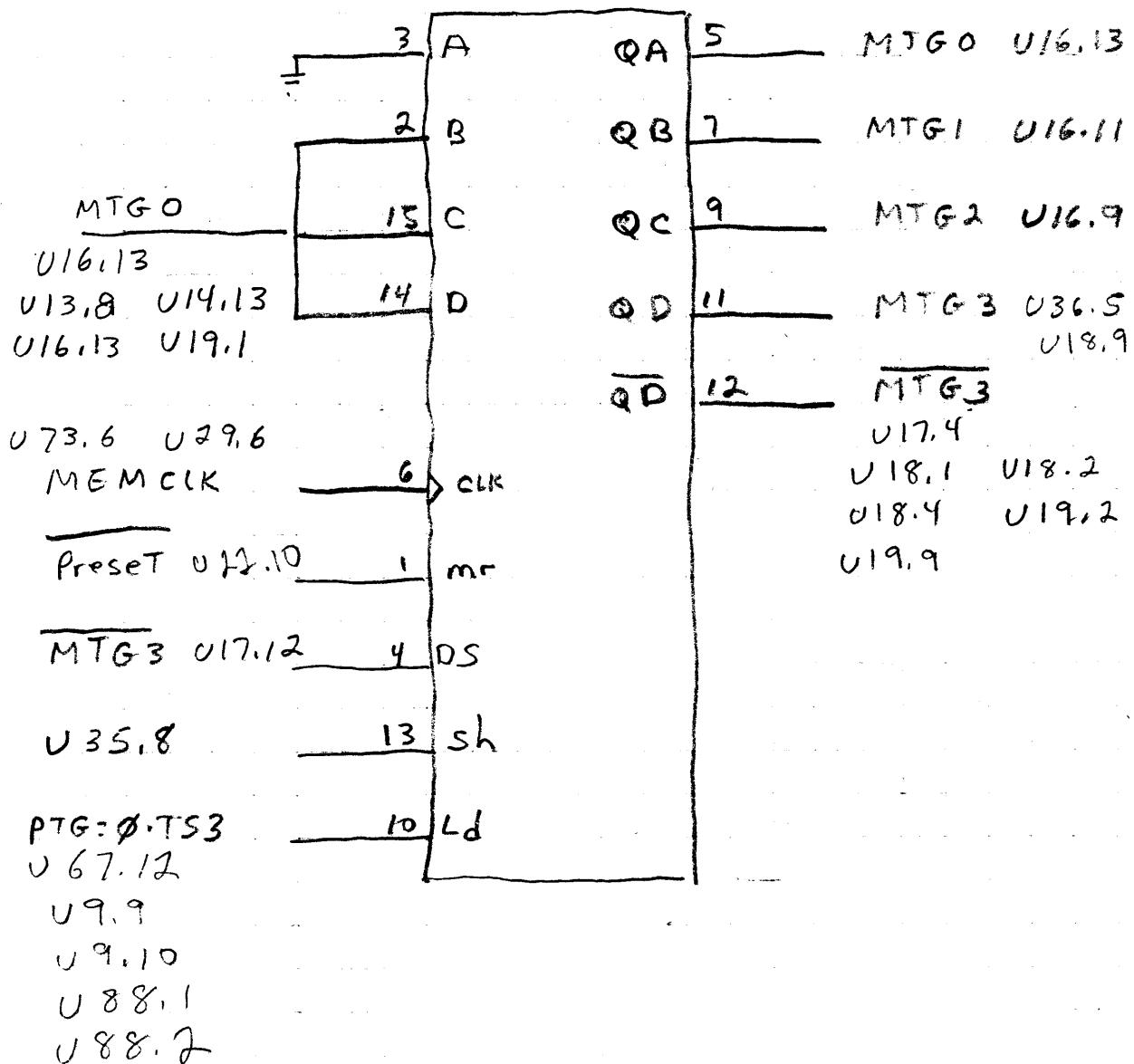
U13.6.9

U16.11

U17.11

D.G 1200 U17

8271 OK

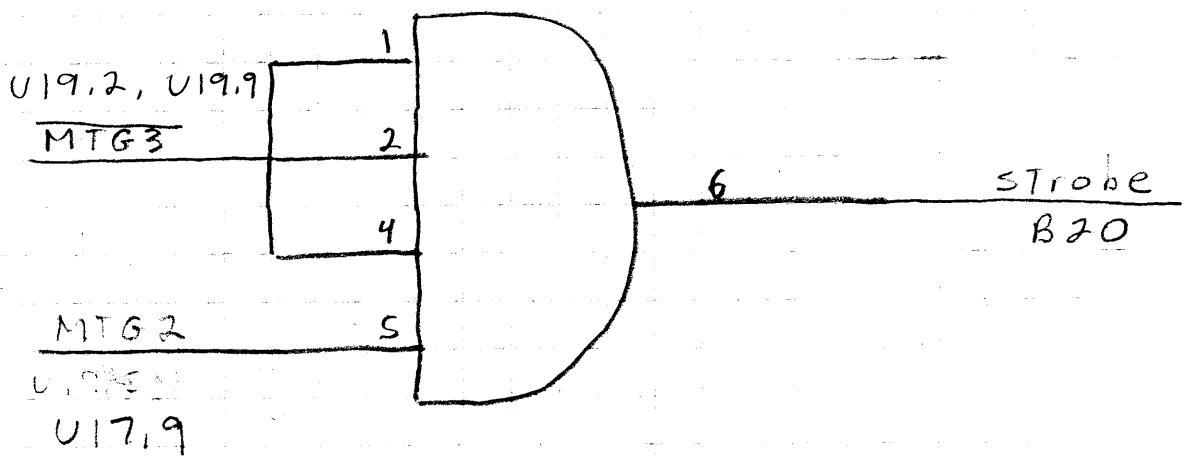


PG 1200 U18

MC 3026

74H21

OK



U17.11

MTG3

9

MTG1

10

U16.10

U19.5

12

U15.6

13

U15.9

U75.10

U104.10

8

DC HO

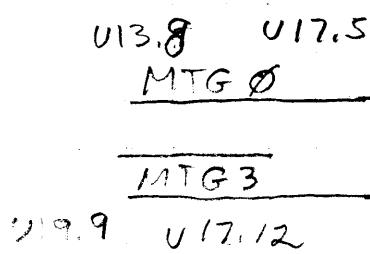
B33

PG 1200 U19

9002
74.00

OK

OK



U35.10

Read 1

B 87

MTG Ø U13.9

4

MTG1
U16.10

5

MB Clear

B 86

MTG3 U19.2

7

MTG1
U17.7

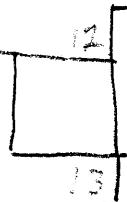
8

Read 2

B 90

Crystal
←
13.33 MHz 470

R69



U 20.3

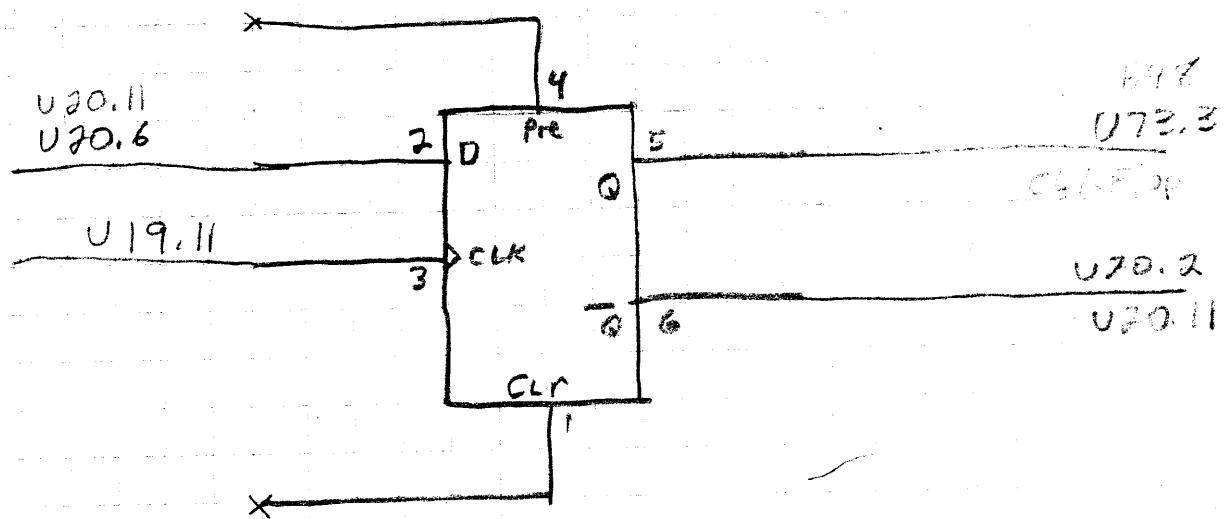
DG1200

U20

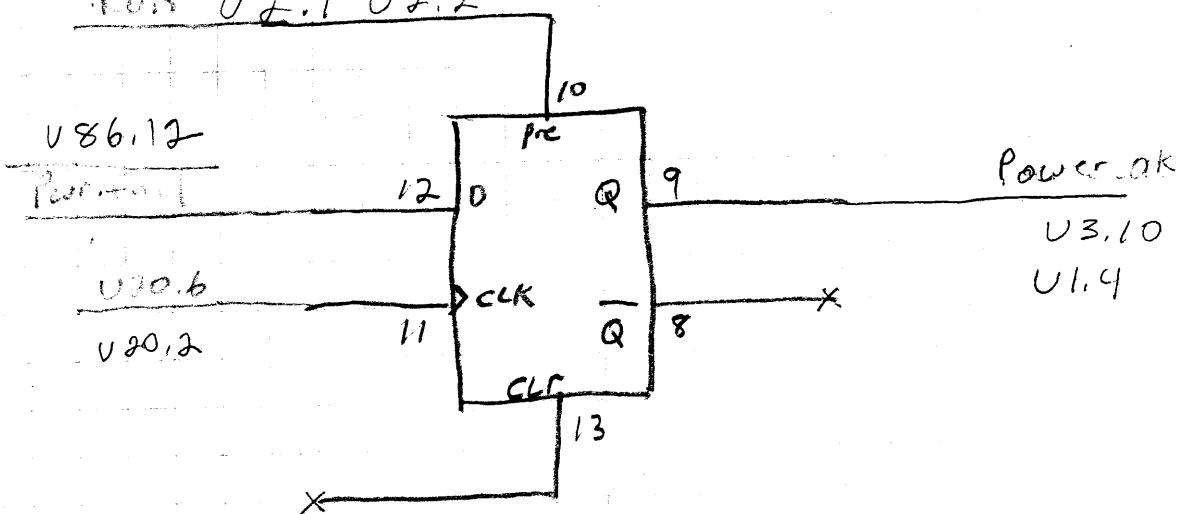
7474
8828

OK

OK



From U2.1 U2.2



DG 1200 U21

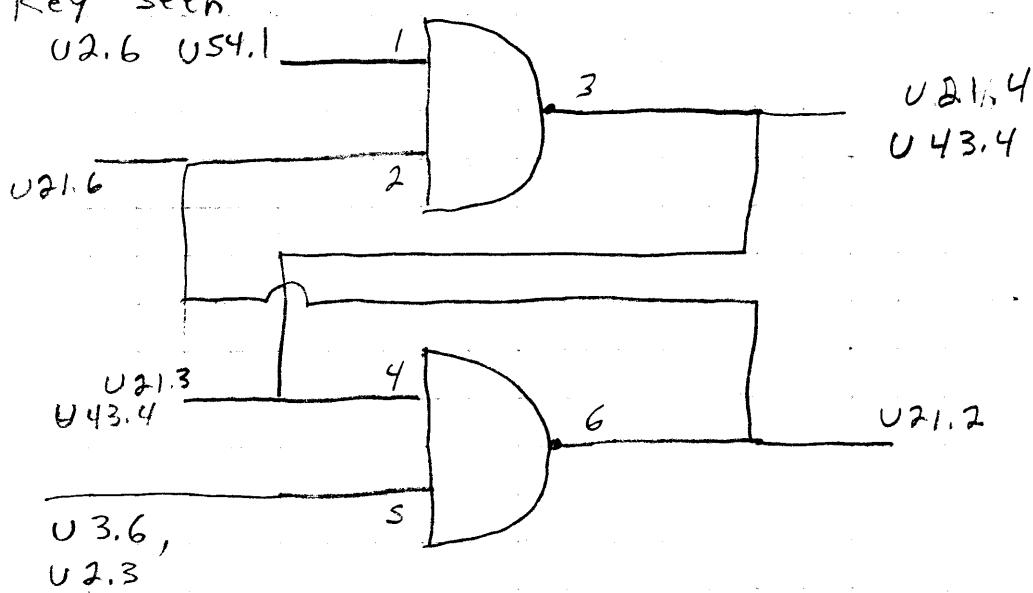
9002

7400

OK

Key Senc.

U21.6 U54.1

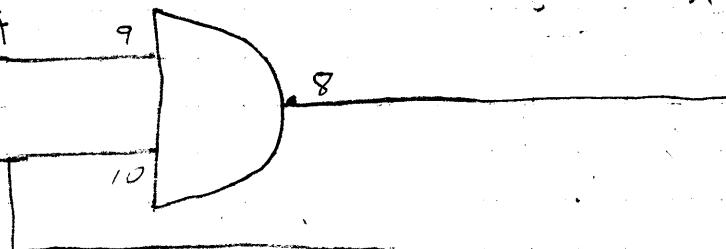


U62.8 Reset

U3.13

U83.9, U21.11

* U62.71

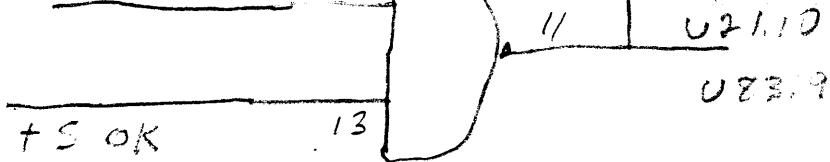


RST A30

+S OK

A 8

+50K · RST



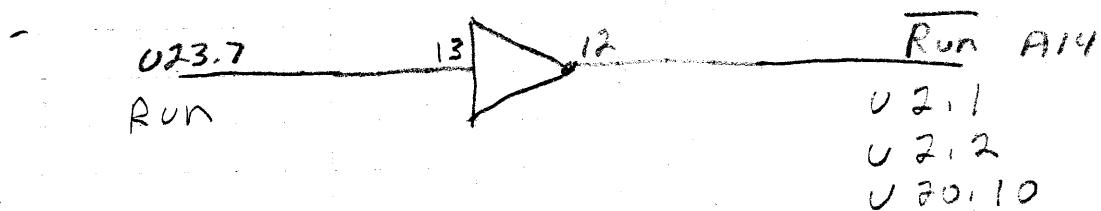
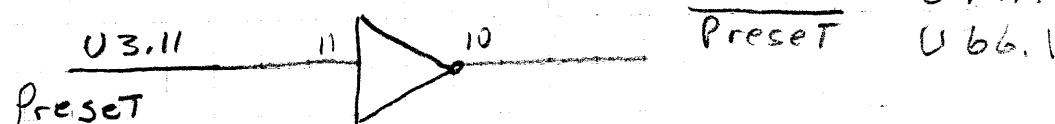
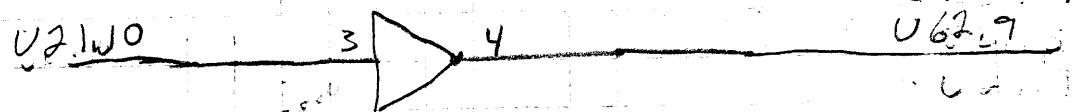
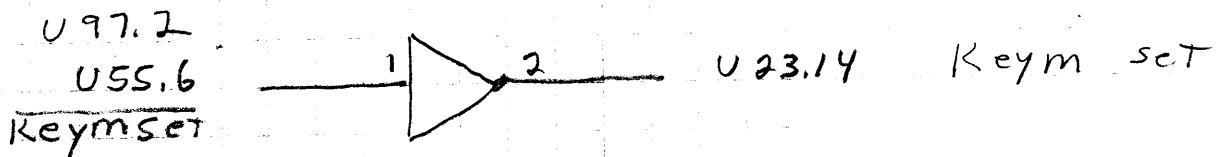
* changed To New Reset Circuit.

DG 1200

U22

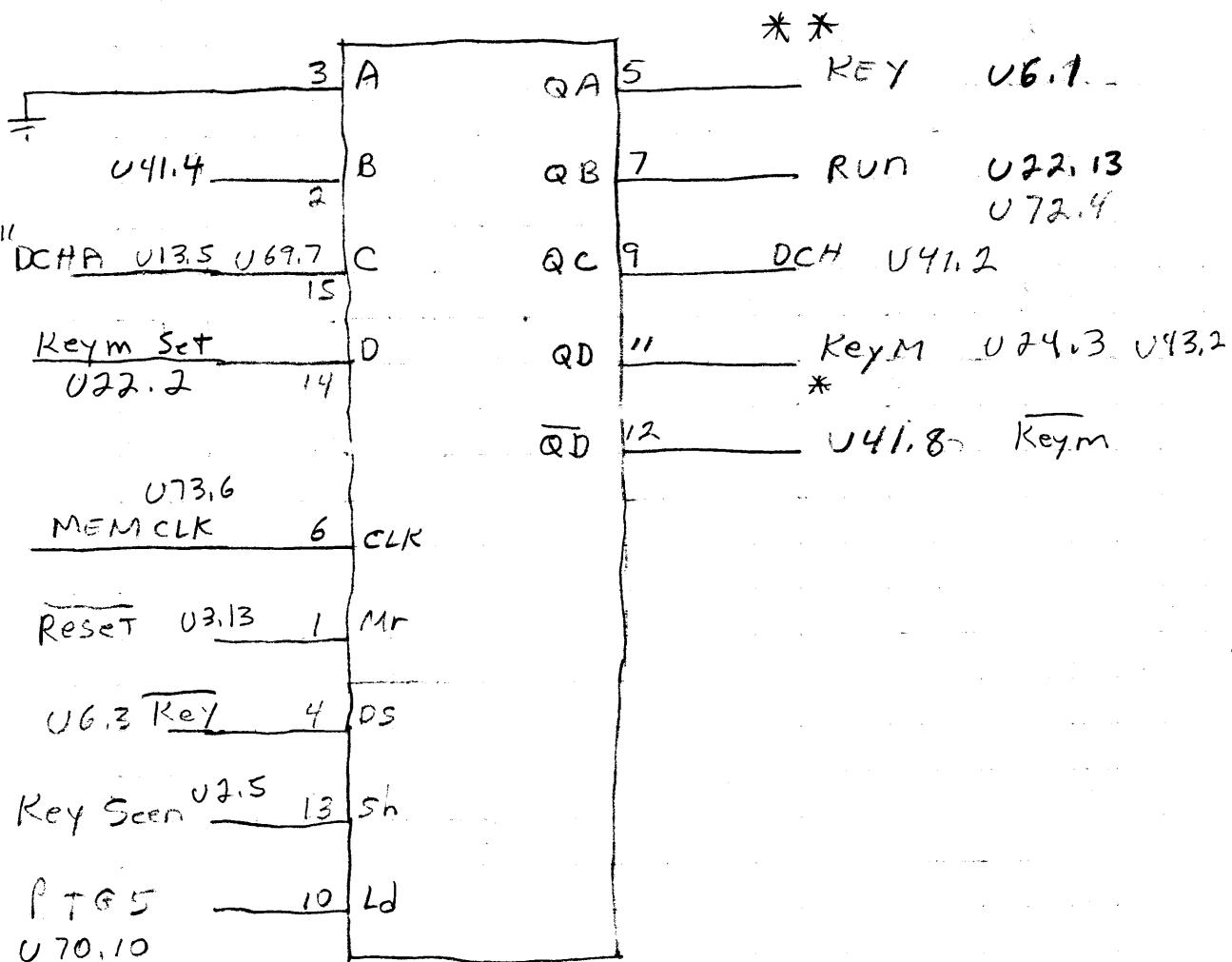
8490

OK



DG 1200 U23 8271

OK



* Temporarily U23.11 goes to U67.11

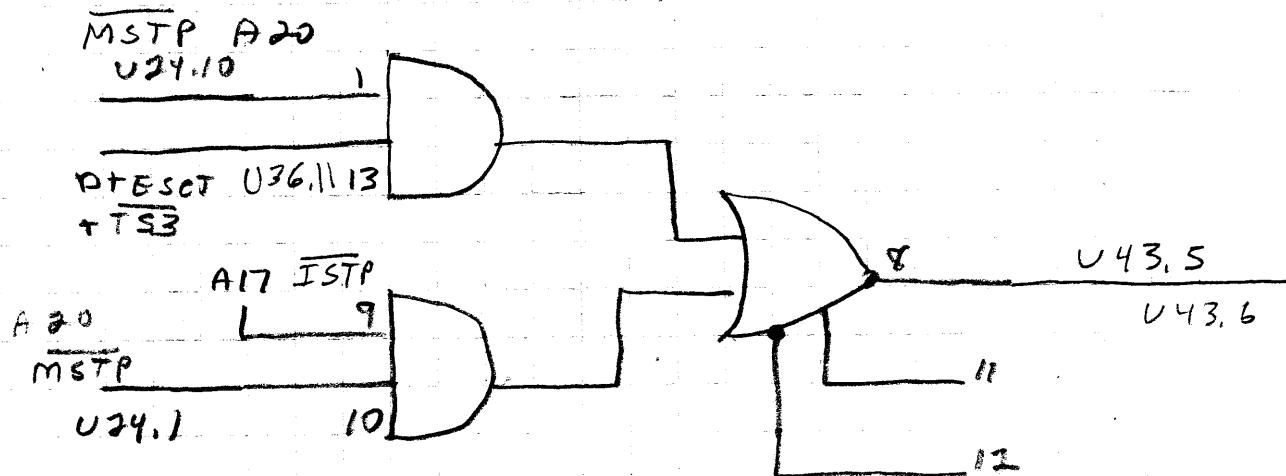
and U67.10 goes to U5.5

** Temporarily U23.5 goes to U67.5

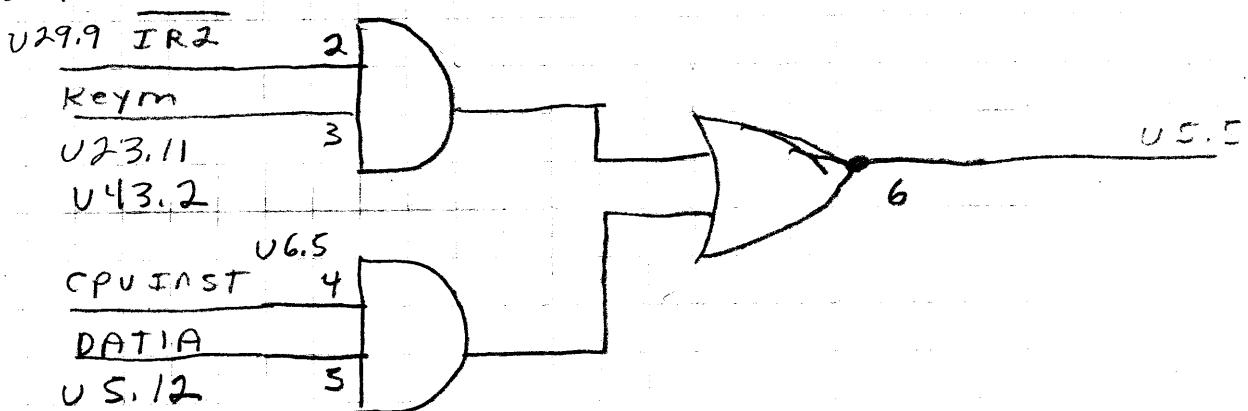
and U67.6 goes to U23.14

DG 1200 U24 9005
7450

OK



U49.1 U51.14 U52.14



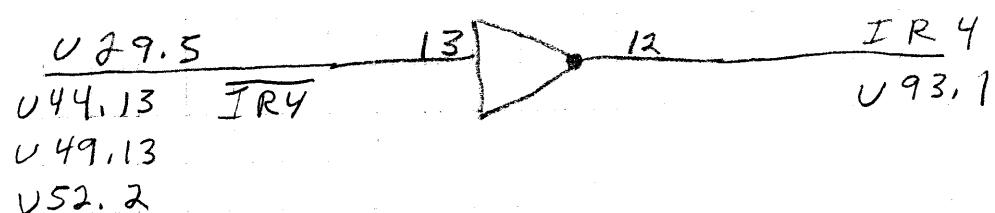
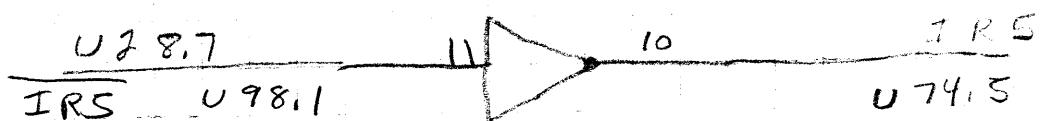
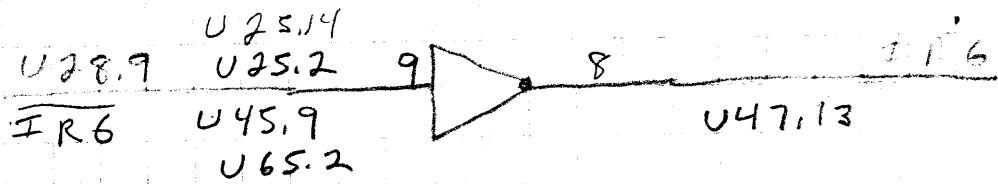
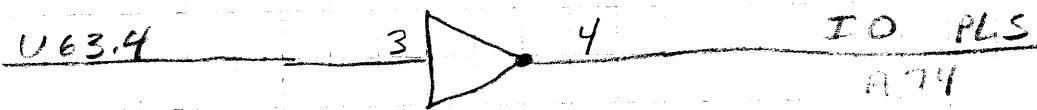
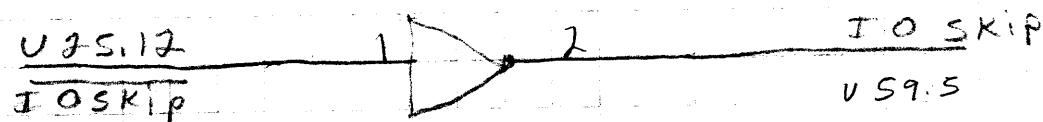
DG 1200 U25 9321
74139

OK

<u>U64.6</u>	1	E	03	7	
<u>IR6</u>	<u>U28.9</u>	2	AO	02	6 <u>U7.9</u>
<u>IR5</u>		3	AI	01	S <u>DATA6</u>
<u>U28.7</u>					<u>U7.13</u>
<u>U26.11</u>	<u>U46.9</u>			00	<u>U26.5</u>
<u>U66.8</u>	<u>U12.10</u>				
<u>INPUT</u>	15	E	03	9	<u>Data</u> <u>U5.13</u>
<u>IR6</u>	<u>U45.9</u>	14	AO	02	10 <u>U5.11</u>
<u>IR5</u>	<u>U65.2</u>				
<u>U25.3</u>		13	AI	01	11 <u>U7.5</u>
<u>U26.11</u>				00	<u>IO SKIP</u>
					<u>U26.1</u>

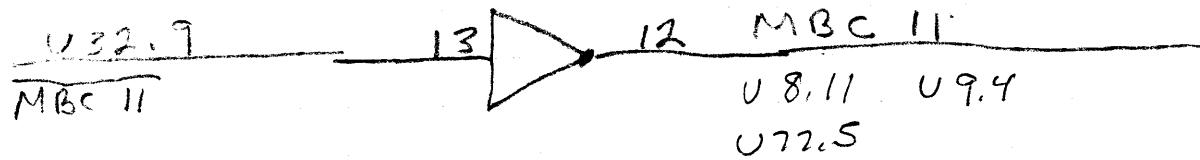
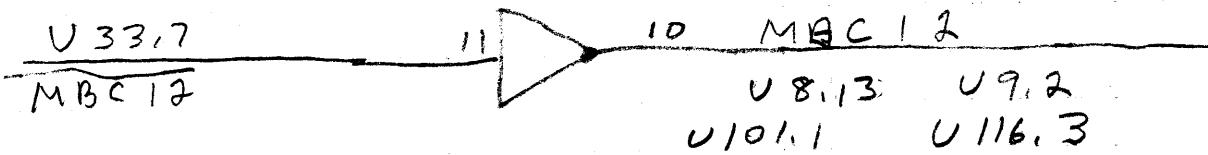
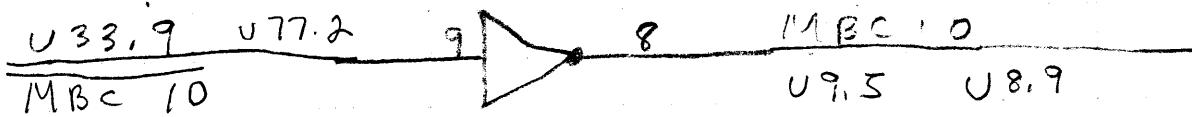
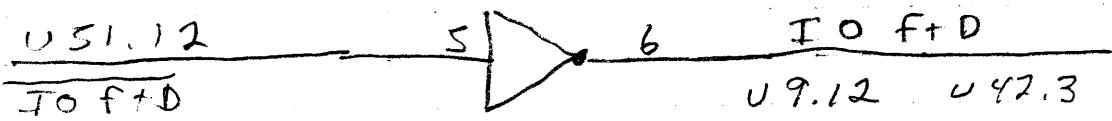
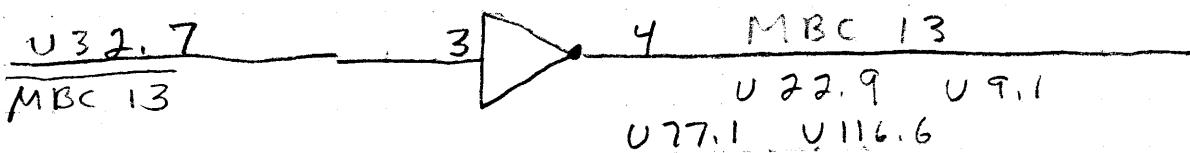
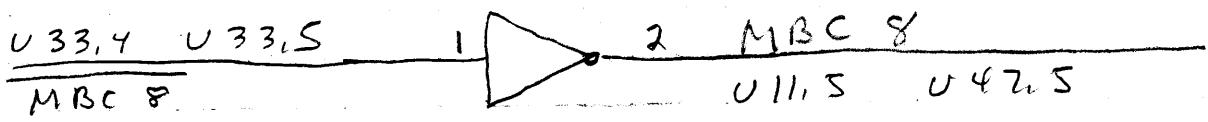
DG 1200 U26 8H90

OK



DG 1200 U27 8490

OK



DG 1200 U28 8271

OK

<u>U40.3</u>	<u>U28.3</u>						<u>U50.13</u>	<u>U51.1</u>
<u>ME110</u>		3	A	QA	5		<u>U43.10</u>	<u>U43.3</u>
ME115	<u>U39.2</u>	2	B	QB	7		<u>IR5</u>	<u>U26.11</u>
MEM6	<u>U37.2</u>	15	C	QC	9		<u>IR6</u>	<u>U26.9</u>
MEM7	<u>U38.214</u>	D		QD	11		<u>IR7</u>	<u>U44.4</u>
<u>U14.4</u>	<u>U72.6</u>				<u>QD</u>	12	<u>FR7</u>	<u>U9.13</u>
<u>CPU CLK</u>		6	CLK					
<u>RESTART</u>		1	mr					
		4	DS					
<u>U114.6</u>		13	sh					
<u>U34.1</u>		10	Ld					
Load IR								

DG 1200 U29 8271

OK

MEM4	U40.2	3	A	QA	5	$\overline{I}R4$	U26.13
MEM1	U39.3	2	B	QB	7	$\overline{I}R1$	U49.5
MEM2	U37.3	15	C	QC	9	$\overline{I}R2$	U24.2
MEM3	U38.3	14	D	QD	11	$\overline{I}R3$	U12.12
				\overline{QD}	12	$I\bar{R}3$	U48.9 U48.12
mem CLK	U73.6	6	CLK				
	U2.8	1	mr				
U12.11		4	DS				
U114.6		13	sh				
U12.6		10	Ld				

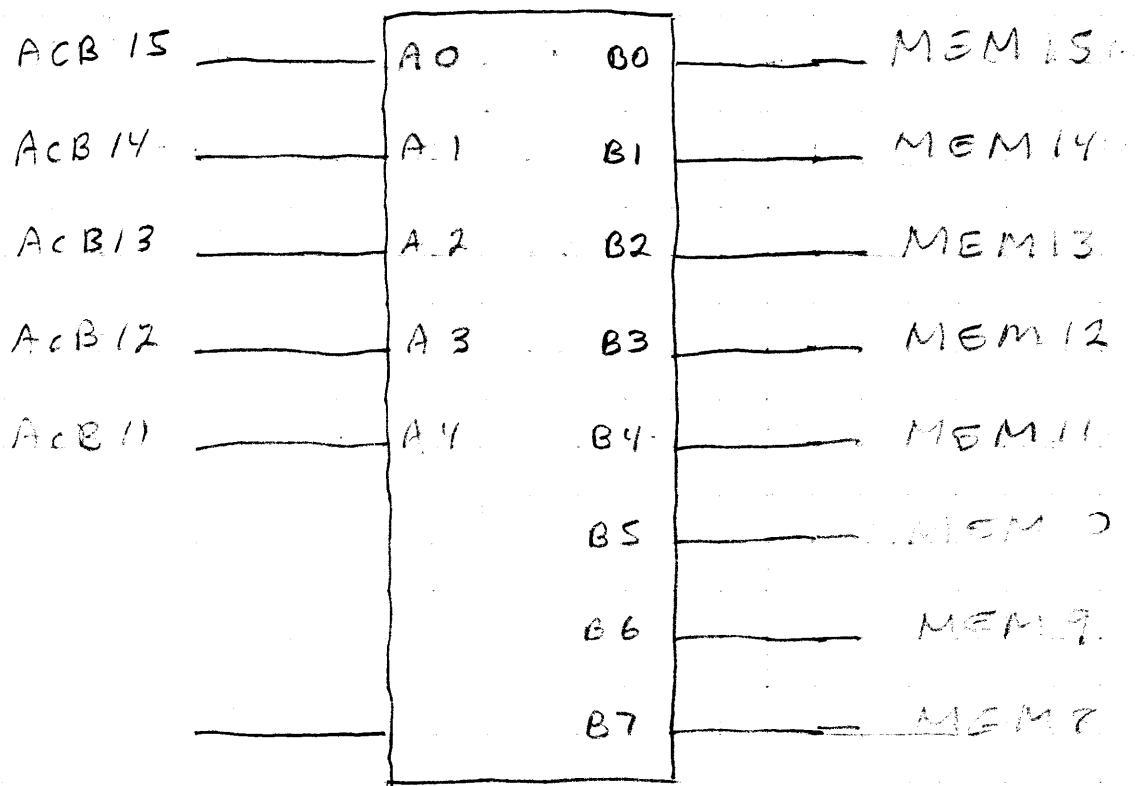
Re

DG 1200 U30 7488 Prom

6.13	ACB 15	10	A0	B0	MEM 7
9.5	ACB 14	11	A1	B1	MEM 6
24.2	ACB 13	12	A2	B2	MEM 5
12.12	ACB 12	13	A3	B3	MEM 4
18.9	ACB 11	14	A4	B4	MEM 3
8.12				B5	MEM 2
				B6	MEM 1
		15	CE	B7	MEM 0

Reym. PL TSØ

DG 1200 U31 7488 Prom



U39

M
V3

M

V

M

V

C
V7

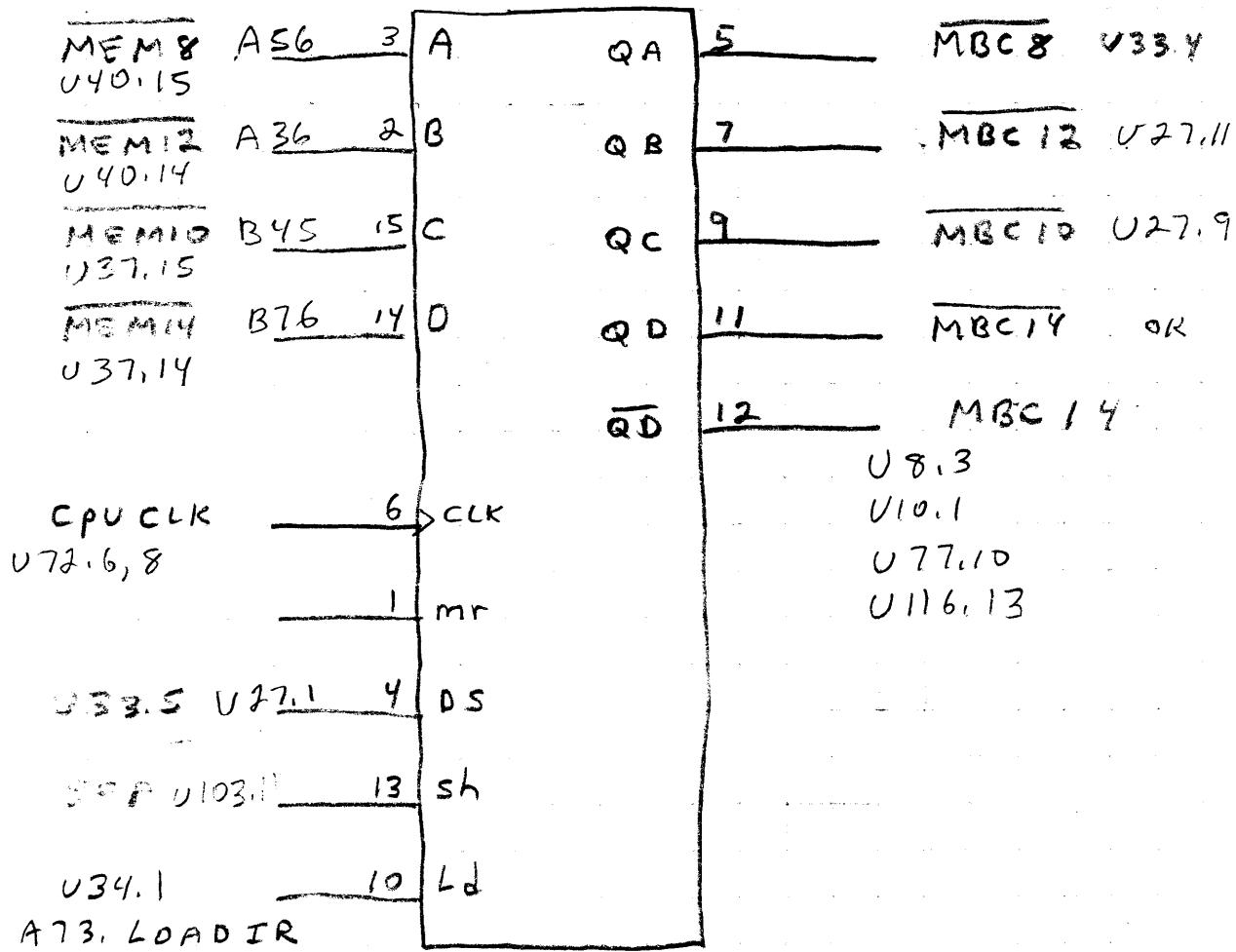
E

E
U10
U:
AT

DG 1200 U32 8271 OK

MEM9 A53	3	A	QF	5	mBC9	U79.8
U39.15		B	QB	7	mBC13	U27.3
MEM13 A35	2	C	QC	9	mBC11	U27.13
U39.14		D	QD	11	mBC15	80.4
MEM11 ASL	15			12	mBC15	
U38.13					U8.1	
MEM15 B18	14				U10.2	
U38.14					U116.10	
CPU CLK	6	CLR				
U72.6.8		1	MR			
EFA PTGI	U34.4	4	DS			
	U116.1					
EFA	13	sh				
U103.11						
U34.1	10	Ld				
A73 LoadIR						

DG 1200 U33 8271



DG 1200 U34

~~8885~~ 7402 OK

33.Y

U34.10

2

A73 Load IR

U27.11

PTG2 + Loop

3

U32.10

U27.9

U73.12

U79.2

1

U33.10

OK

EFA U103.12-5

PTG1

U69.11

6

4 EFA - PTG1

U32.4

U6.1

Key

8

10

U34.2

FeTch

9

U95.5

U66.5

TS3

11

13

U104.1

DCHM1

12

DG 1200 U35

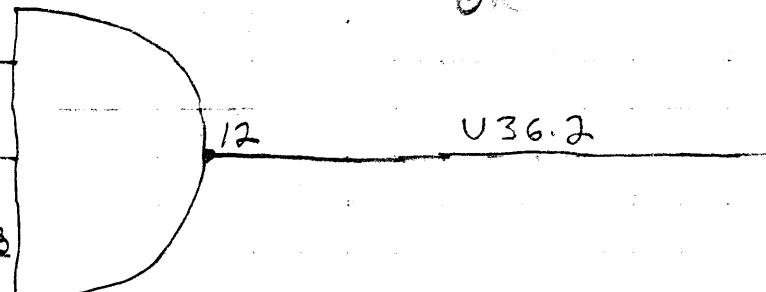
9003
7410

OK

U24.13
U13.3
U36.11

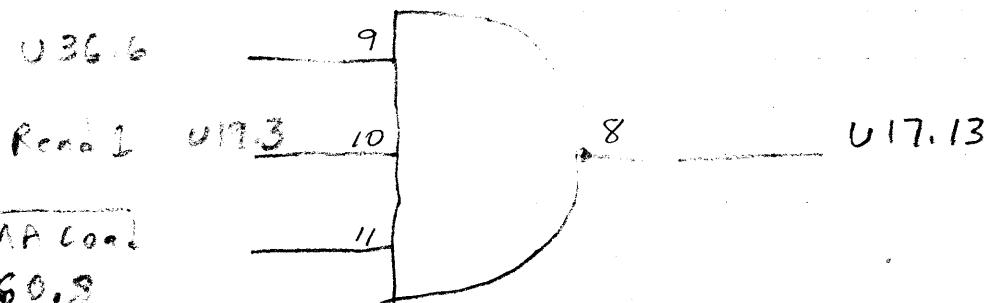
D+E Set + TSO

U35.6 Loop TSO
Skip Inc
U58.5
U58.6



U66.6
TSO
PI U95.11
Loop
U22.6
U36.10 U56.13

Loop TSO
U35.2



U36.6
Rena 1 U17.3
MP Load
60.8

U17.13

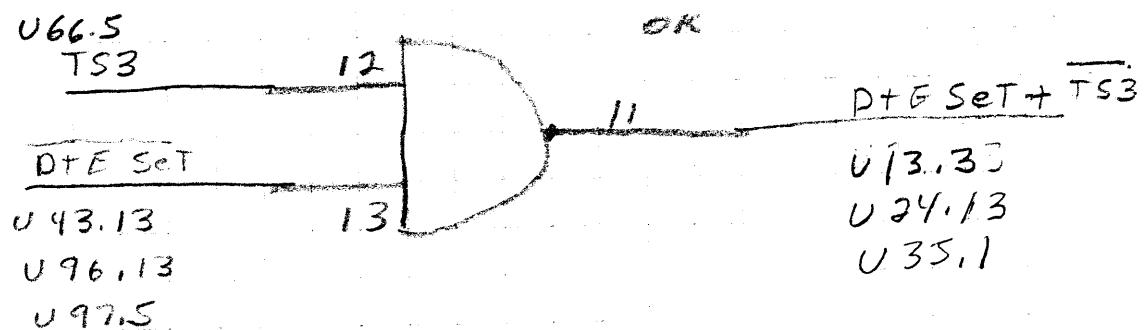
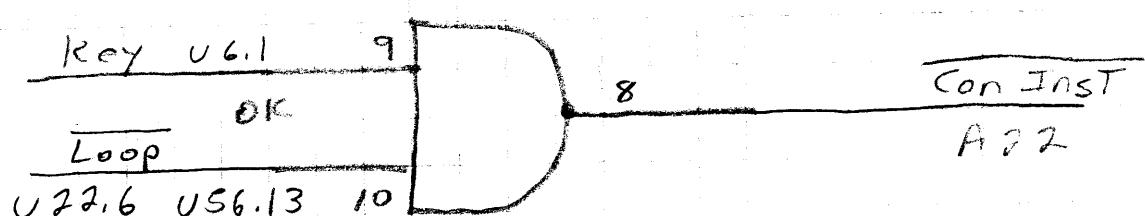
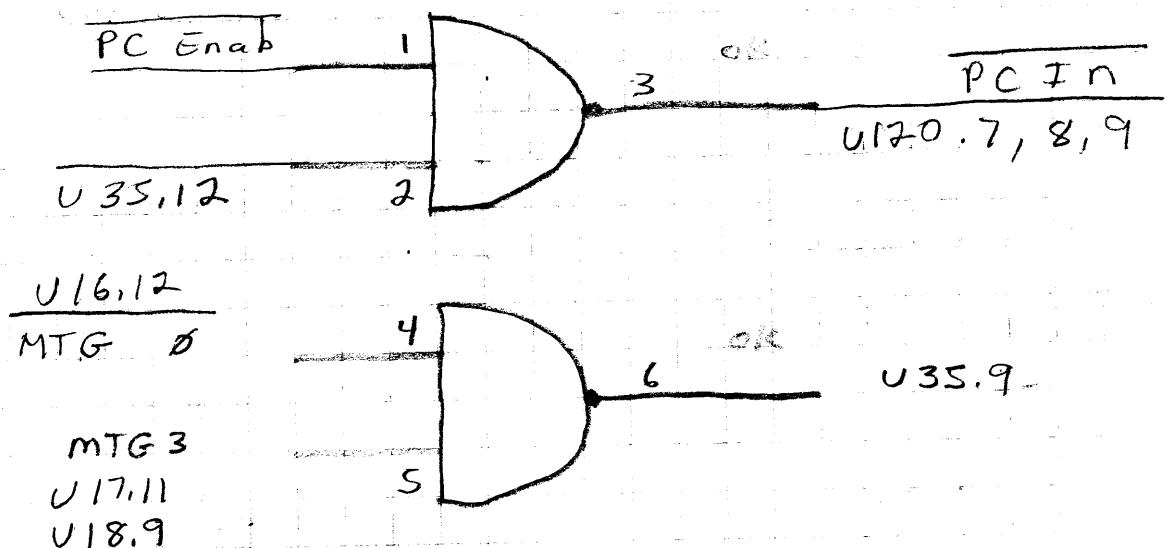
U3
U16
MTG

mJ
U17
U18
K
L
U23

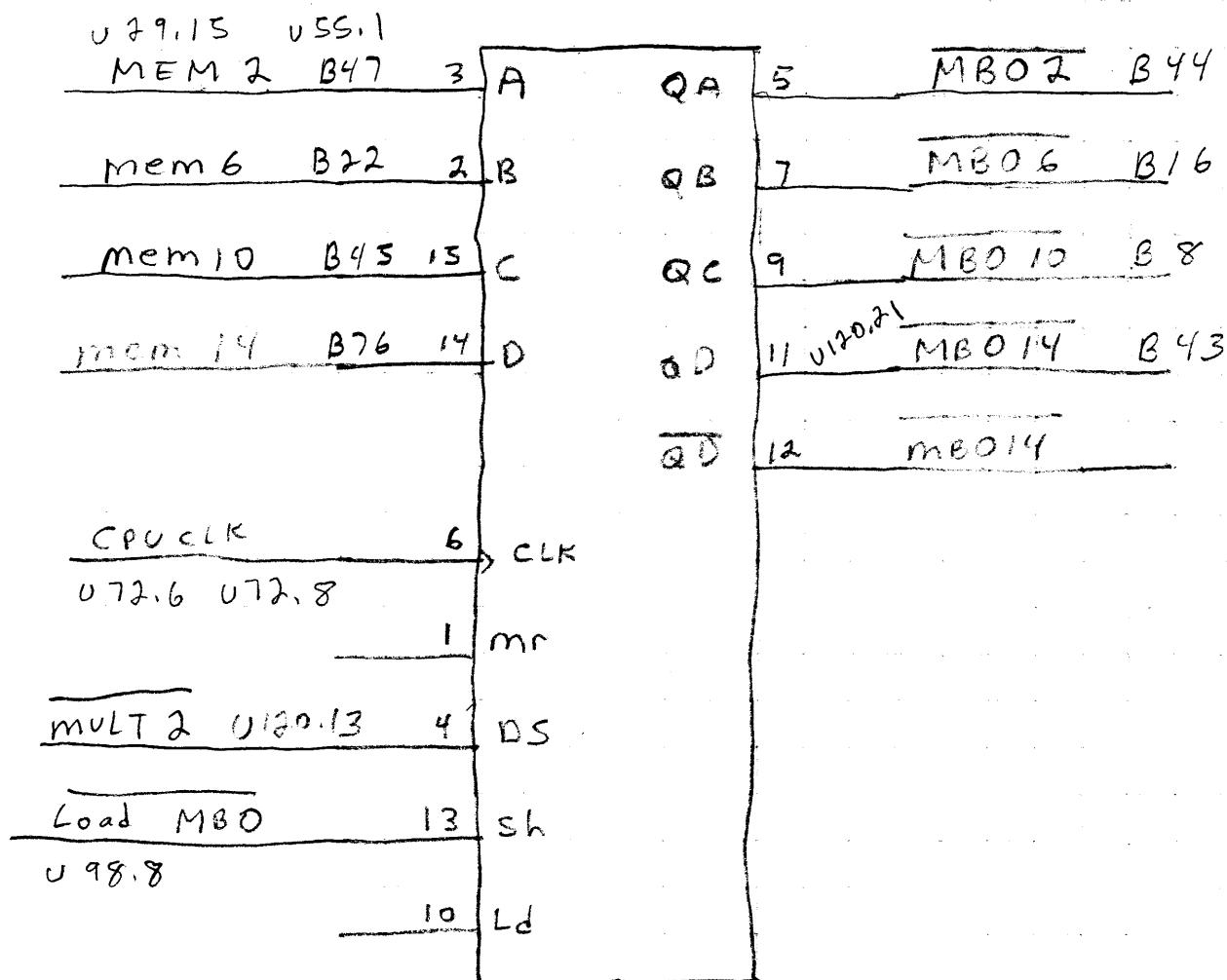
U66
T
DT
U4
U9
U9

DG 12.00 U36 9002 OR
 7400

U57.5 U61.8 U74.2



DG 1200 U37 8271 OK



OK

D G 1200 U38 8271

OK

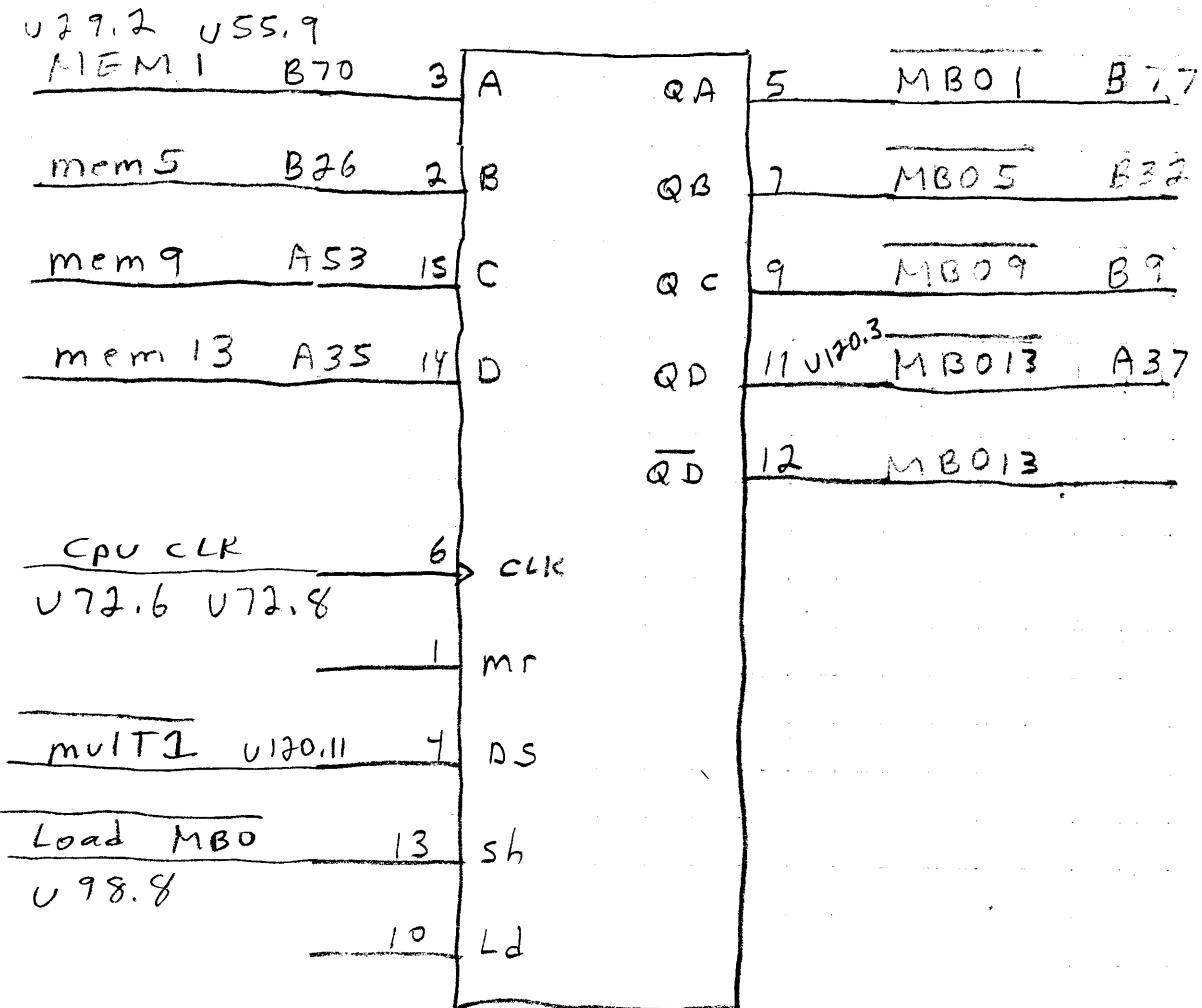
B44

<u>mem 3</u>	<u>B68</u>	3	A	<u>QA</u>	5	<u>M803</u>	<u>B43</u>
<u>mem 7</u>	<u>B74</u>	2	B	<u>QB</u>	7	<u>M807</u>	<u>B14</u>
<u>mem 11</u>	<u>A51</u>	15	C	<u>QC</u>	9	<u>M8011</u>	<u>B5</u>
<u>mem 15</u>	<u>B18</u>	14	D	<u>QD</u>	11. <u>U180.18</u>	<u>M8015</u>	<u>A41</u>
<u>CPU CLK</u>		6		<u>CLK</u>			
<u>U72.6</u>	<u>U72.8</u>			<u>mr</u>			
<u>MULT 3</u>	<u>U180.14</u>	4		<u>DS</u>			
<u>Load M80</u>		13		<u>sh</u>			
<u>U98.8</u>				<u>Ld</u>			

DG 1200 U39

8271

OK



DG 1200 U40 8271

OK

U55.13 U76.2

U28.3 U55.10

MEMD B71 3

J89.3 mem4 B28 2

J33.3 mem8 A56 15

J33.7 mem12 A36 14

U72.6 U72.8

U120.10 4

U98.8

A QA

B QB

C QC

D QD

mn

OS

sh

ld

5 U120 12 B79

7 U604 B42

9 U608 B12

11 U120.6 U120.12 A37

12 U120.15

6 CLK

OG 1200 U41

~~8885~~
7402

OK

U13.5 U14.9 U15.2

U23.9 U7.11

DCH

Keym
U23.11

2

1

U89.13

IOCF

MBC

crys

UG2.6

5

4

U23.2

U41.13

6

CP

Re

U2

Keym

U23.12

8

10

Keym-PL

U55.3

U57.2

U93.9

PT

U86.3 U82.9
Test Skip Set

11

13

U41.6

U7C

U2

U4

U6

U7

U

U

U

U43.8

U83.3

Run Led

A14

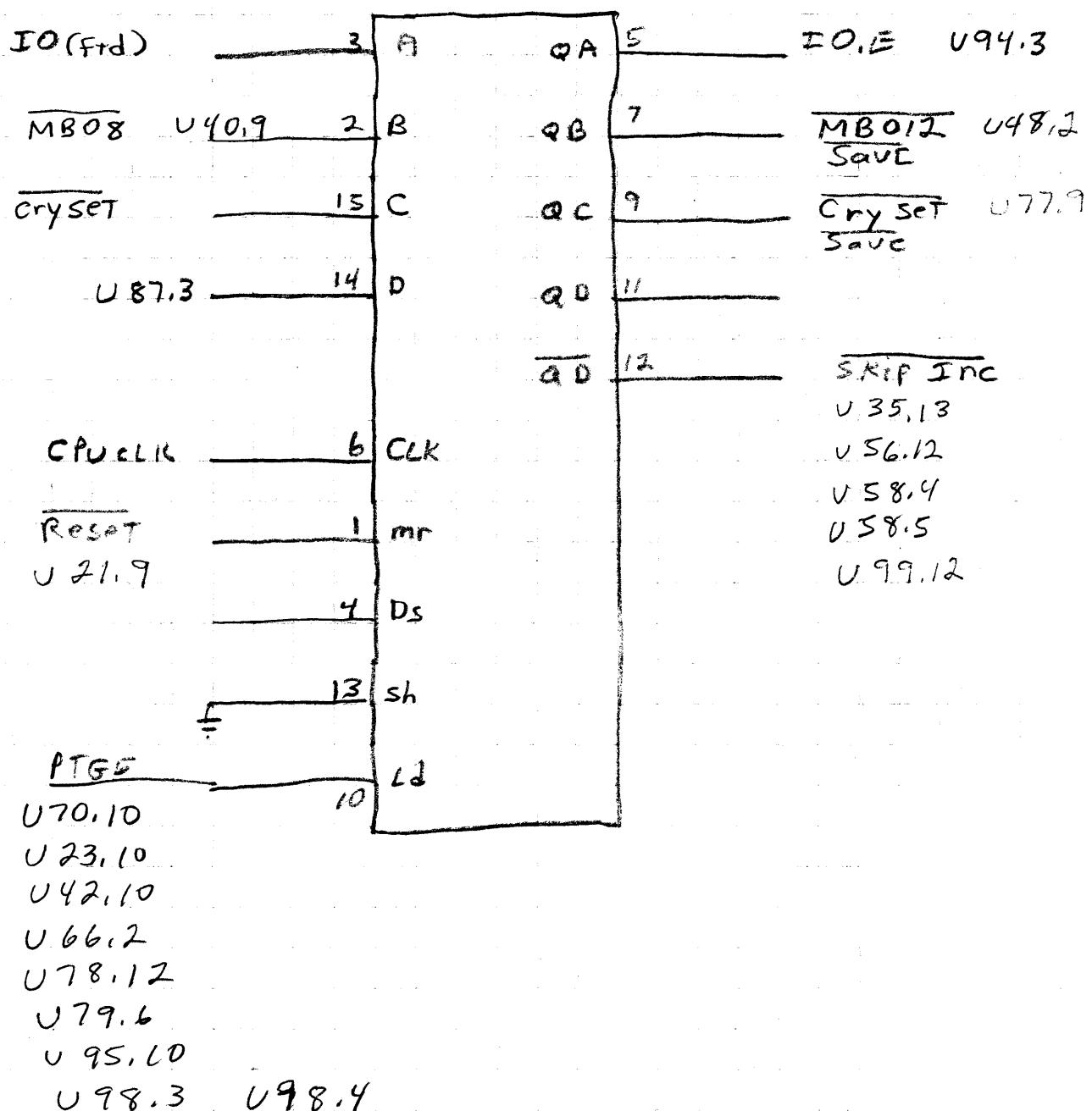
12

OK

DG 1200

U42

8271 OK



D.G 1200 043

9008
74HS4

OK

U96.13

D+E Set — 13

STOP sync

U102.5

U23.11 U24.3

Key M

PL

U41.9

U87.9

U6.1 U23.5

Key

IR Ø

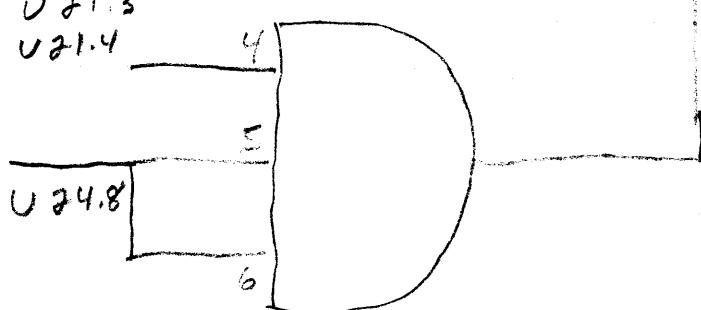
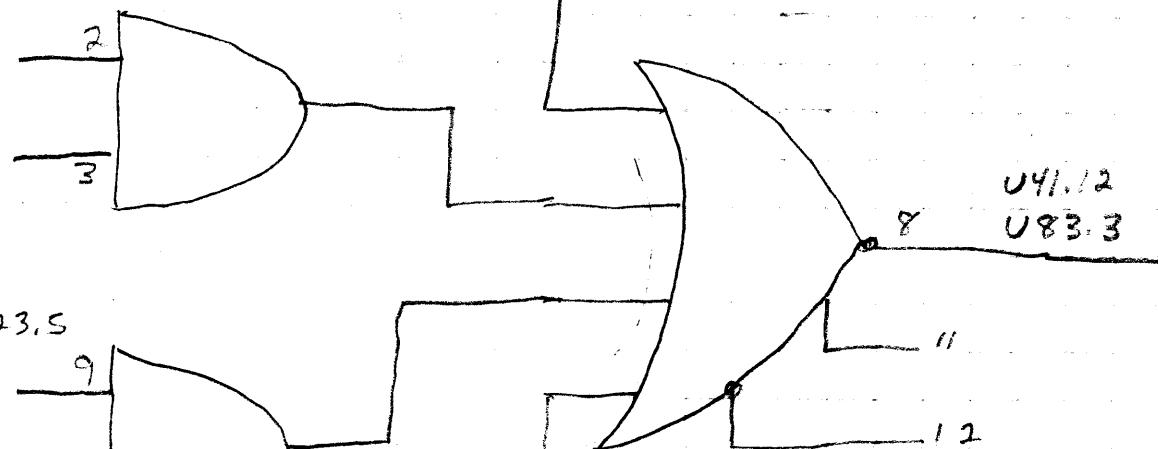
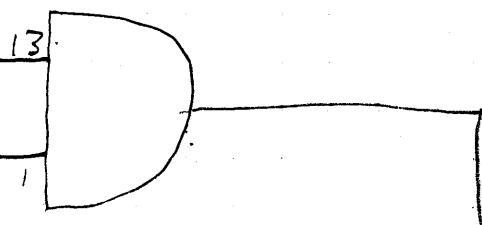
U28.5

U45.3

U21.3

U21.4

U24.8



EF

FR
U29
U40

EF

IR
U28
U46
U71.3

AL

IR
U28
U64.1

U8
IR

Ke
U6.1
U4.2
U23

OK

DG 1200 U44

9005

OK

7450

EFA U103,12 1

IR4 13
U29,5 U26,13
U49,13 US2,2

EFA U103,11 9

IR 10
U28,11
U46,5
U71,5

ALC 2
U50,8

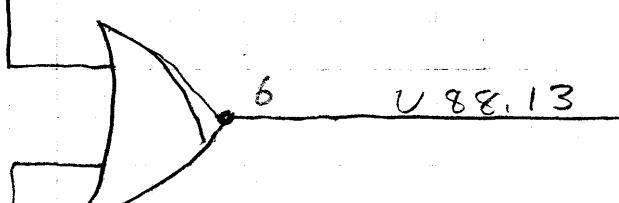
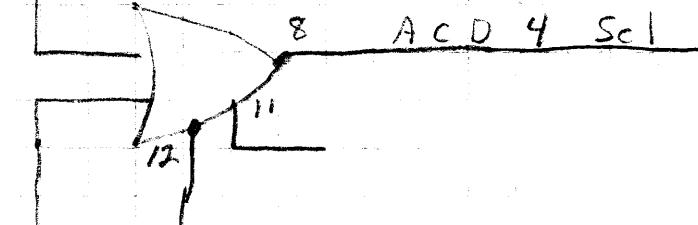
IR7 3
U28,12 U9,13
U64,13 U89,1

U86,10

IR7 4
U28,11

Key

U6,13
U4,2
U23,4

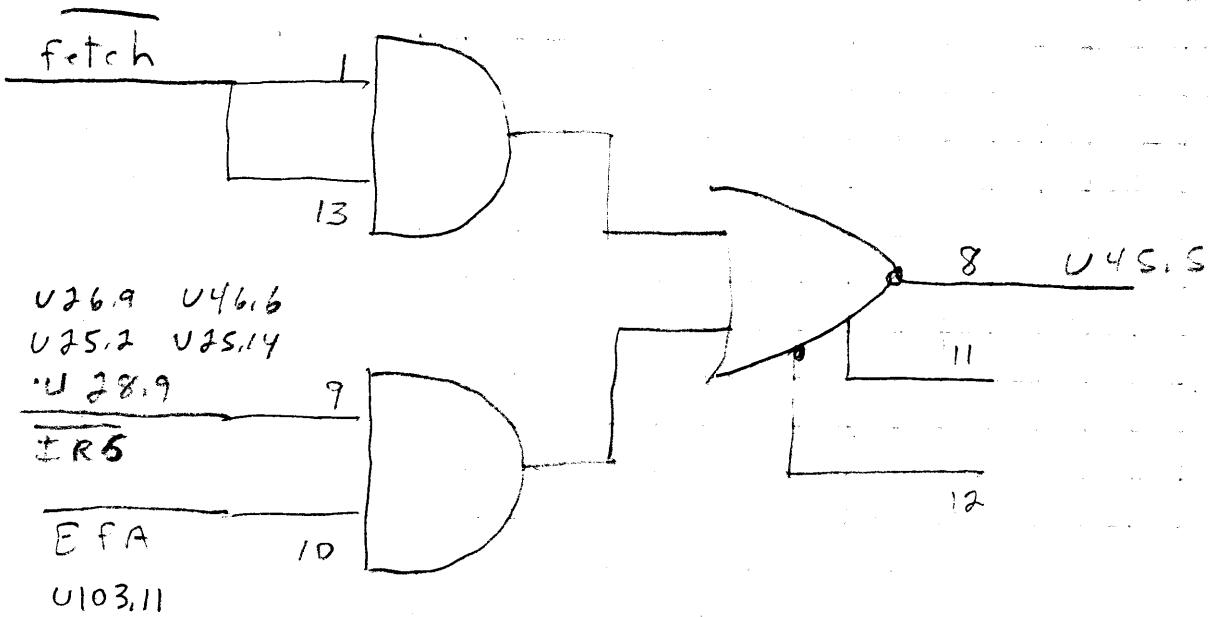


DG 1200 U45

9005
7450

012

U94.12 U75.1



U
K
U2
U4

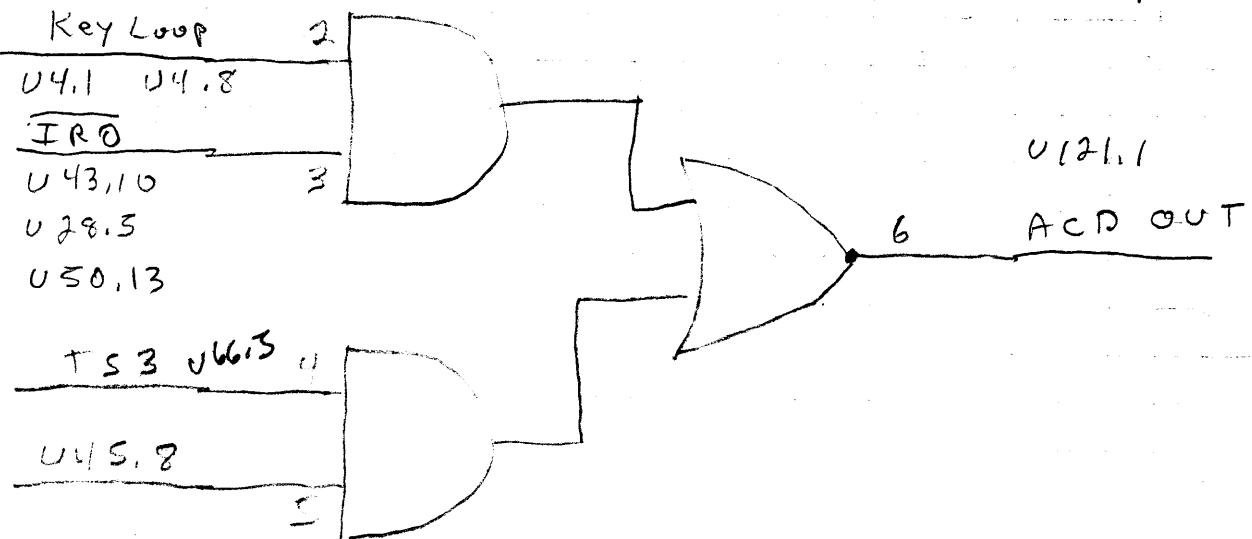
P
U95
U35.

U28.1

TRS
AL
U47.
U86.

U103

E
IP
J16
U2
J2
U4
U8



OK

DG 1200 U46

9008
741454

OK

U 87.8 13

Key
U 23.5
U 44.5

PI
U 95.11
U 35.4

U 28.7 U 25.3 U 65.3

IRS

AIC
U 47.11
U 86.5 U 94.6

U 103.11

EEP

IR7 U 28.11 5

JPG

U 28.9
U 25.2 U 25.14
U 45.9
U 55.4 U 65.2

U 47.6
U 53.2

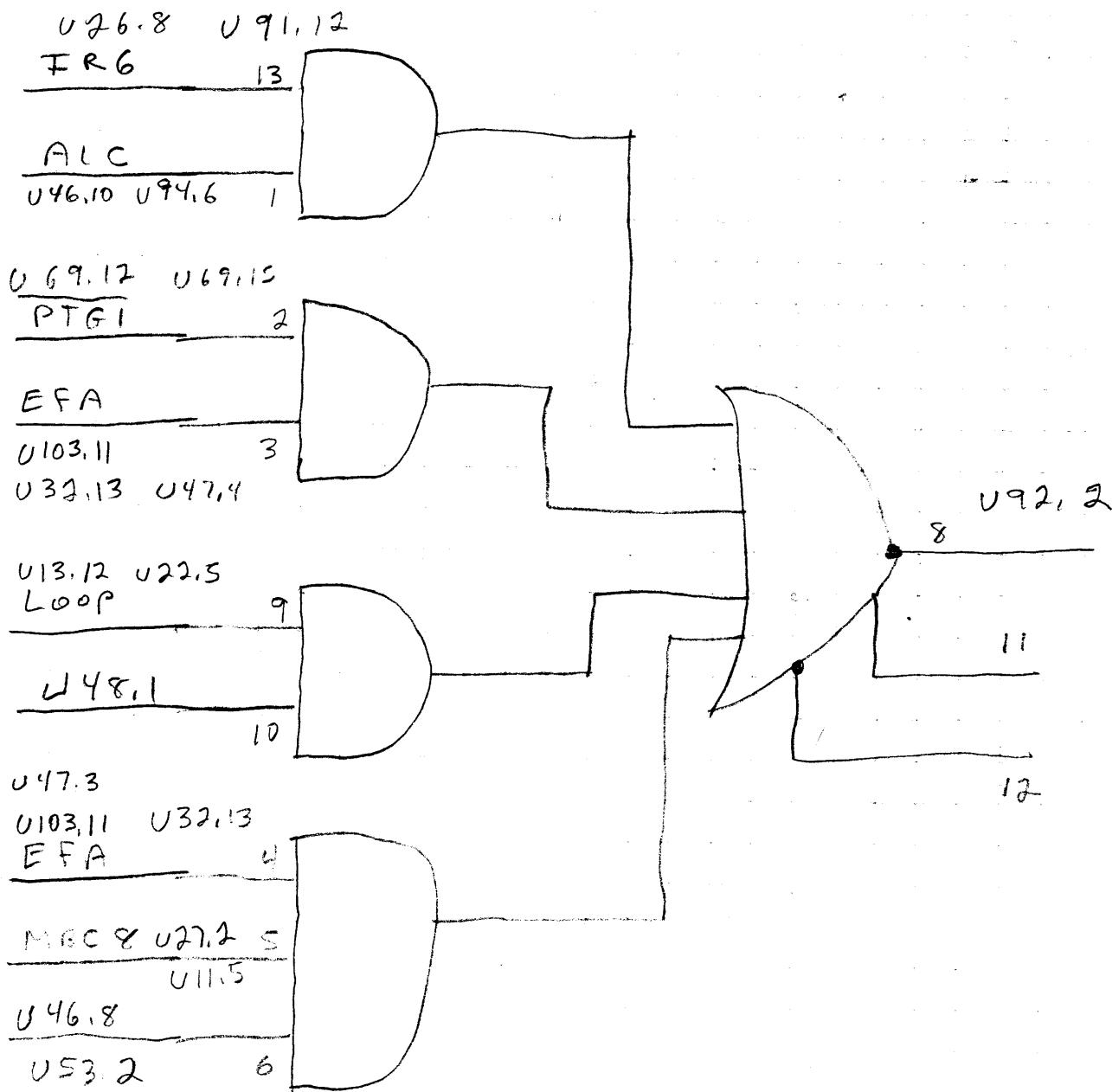
8

11

12

OG 1200 U47

9008 OK
74.4.5.4

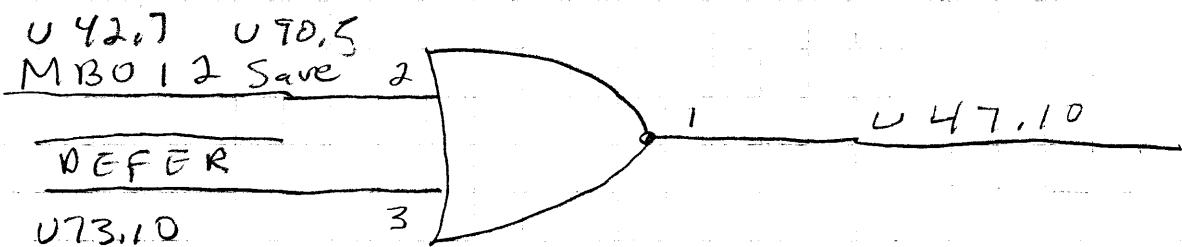


OK

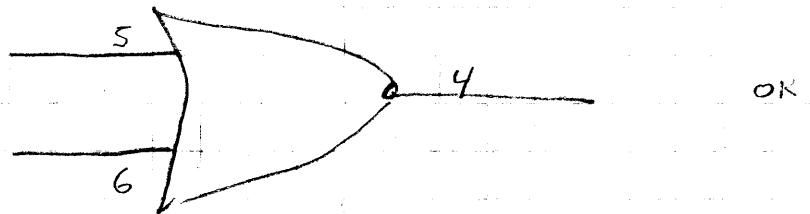
DG 1200 U98

~~8885~~
7402

OK



192.2



U109.12
U103.5

was JSR

8

JR3
U29.12

9

10

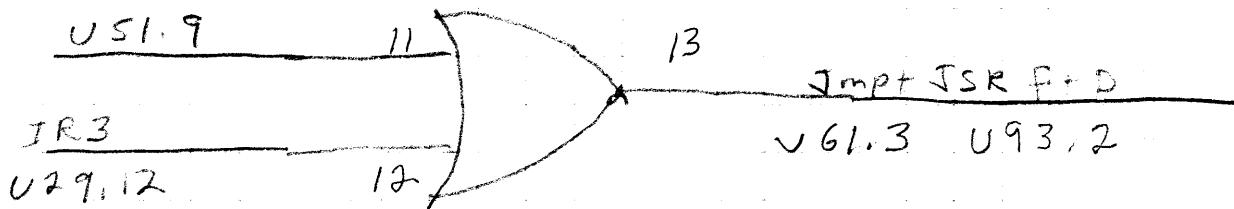
U49.9

A89 U50.5 U50.7

WAS JSR

11

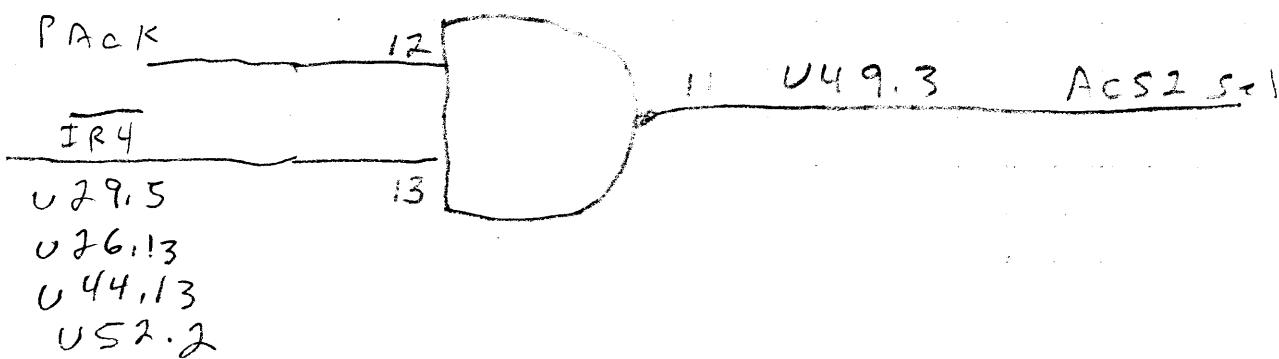
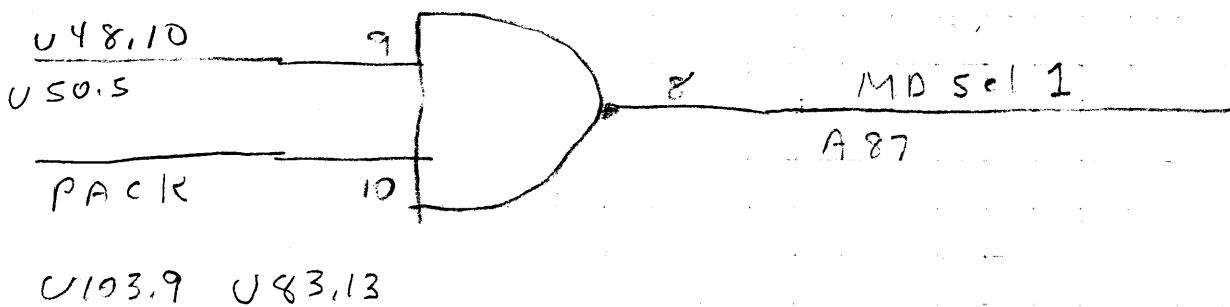
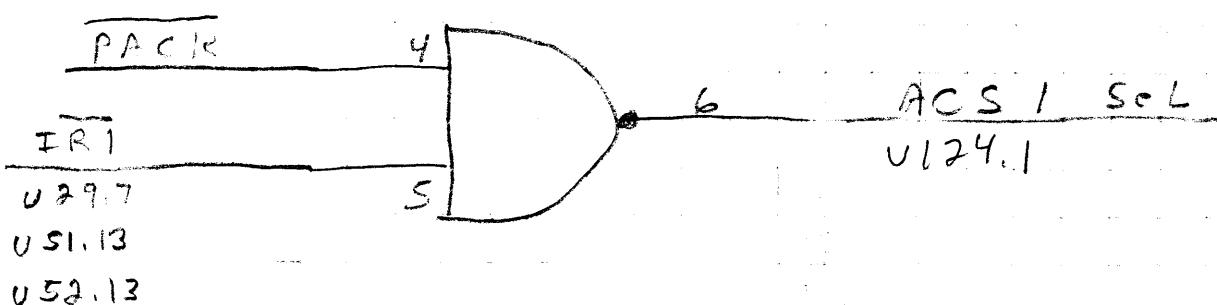
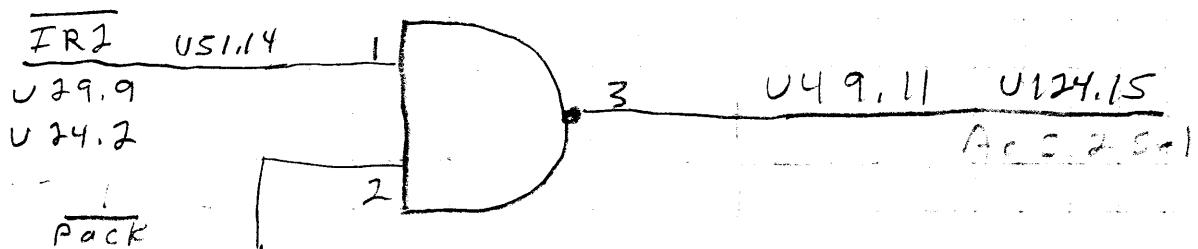
12



DG 1200 U49

7438

01C



OK

DG 1200 USO

9003

7410

OK

U74.13 U75.3
fetch + Dcfir

skip V78.6

IRO
U28.5 U43.10
U45.3

EFA U47.4
U103.11

V48.10

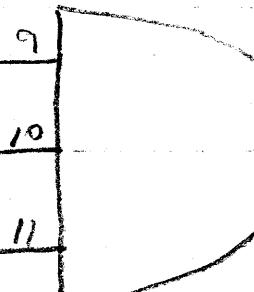
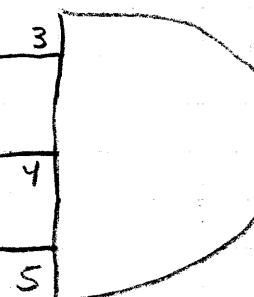
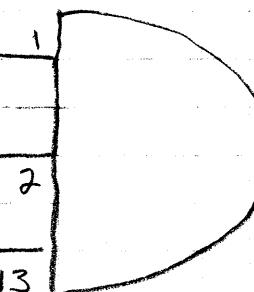
U95.5

FETCH

TS3 U66.5

IRO + SKIP

V50.12



DG 1200 US1

9321

7.4.1.39

OK

U45.3 U53.5 U53.6

U28.5 U43.10

<u>IR0</u>	1	E	03	7	→	
<u>MBC9</u>	2	AO	02	6	<u>U101.3 181.5</u>	<u>SHL</u>
<u>MBC8</u>	3	A1	01	5	<u>U101.5 181.6</u>	<u>SHR</u>
U27.1 U11.9 U33.4, U33.5 U63.13 U63.3			00	4	<u>U100.11</u>	<u>SWP</u>
<u>U50.12</u>	15	E	03	9		<u>U48.17</u>
<u>IR2</u> U29.9 U24.2	14	AO	02	10	→	
<u>IR1</u>	13	A1	01	11	→	
U29.7 U49.5 U52.13			00	12		<u>U27.5</u>

OK

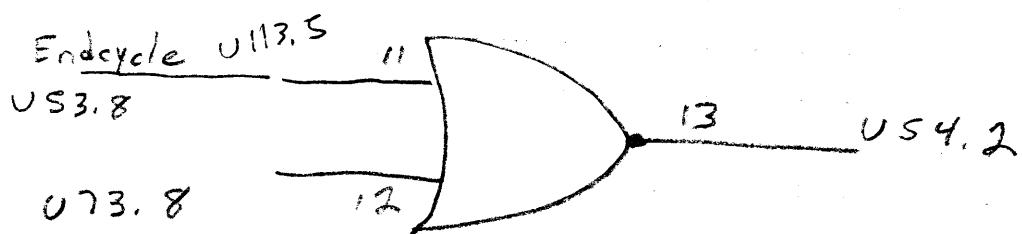
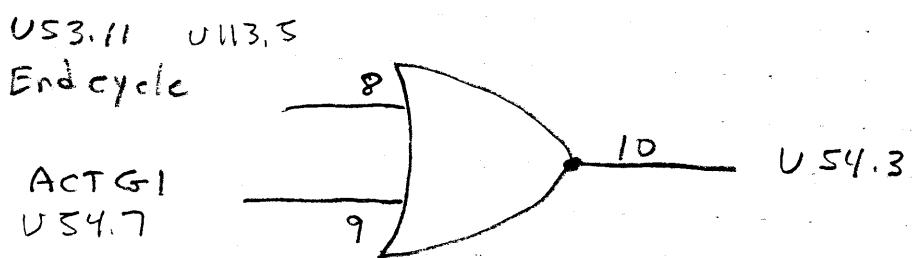
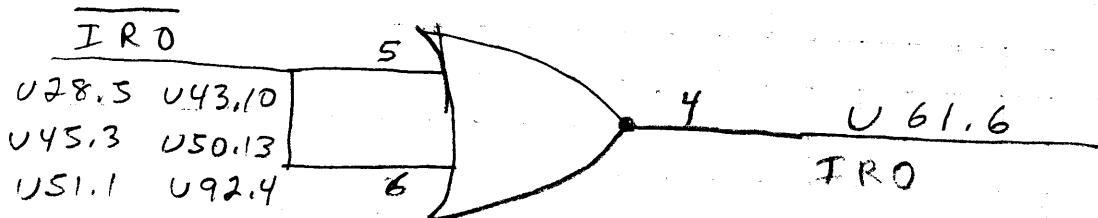
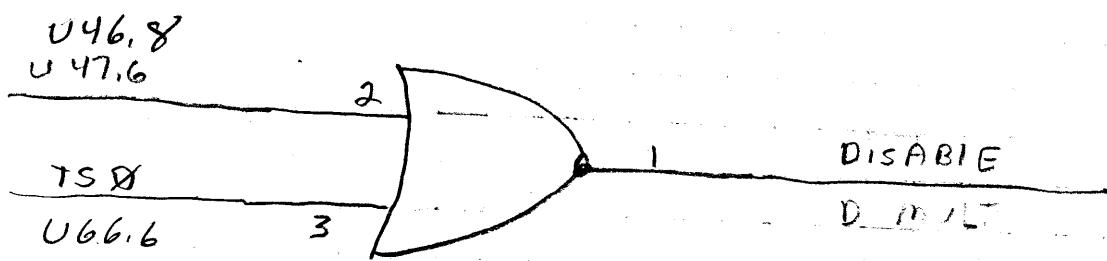
DG 1200 U52 9321 OK
74139

<u>U52.9</u>	1	E	03	7	→
<u>IR4 U49.13</u>	2	AO	02	6	→
<u>U92.8</u>	3	AI	01	5	<u>I52·E·TSØ</u>
			00	4	<u>I52·E·TSØ</u> U92.1
<u>U94.10</u>				7	<u>U52.1 TSZ+OSZ E</u>
<u>Exec AII</u>	15	E	03		
<u>IR2 U29.9 U24.214</u>		AO	02		<u>LDA·E U99.1</u>
<u>IR1</u>	13	AI	01		<u>STA·E U99.9</u>
U29.7			00		→
U49.5					
U51.13					

DG 1200 US3

~~8885~~
7402

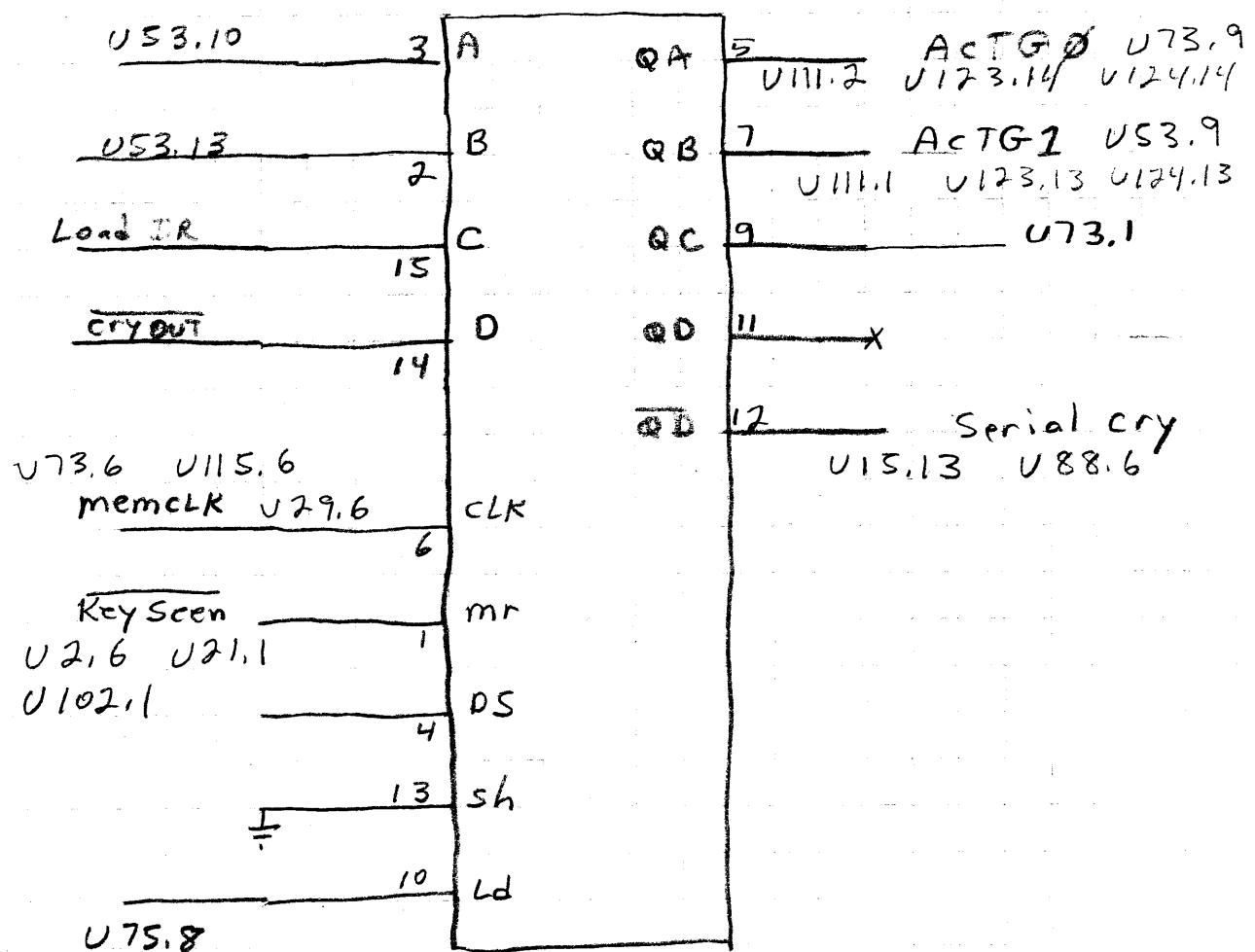
OK



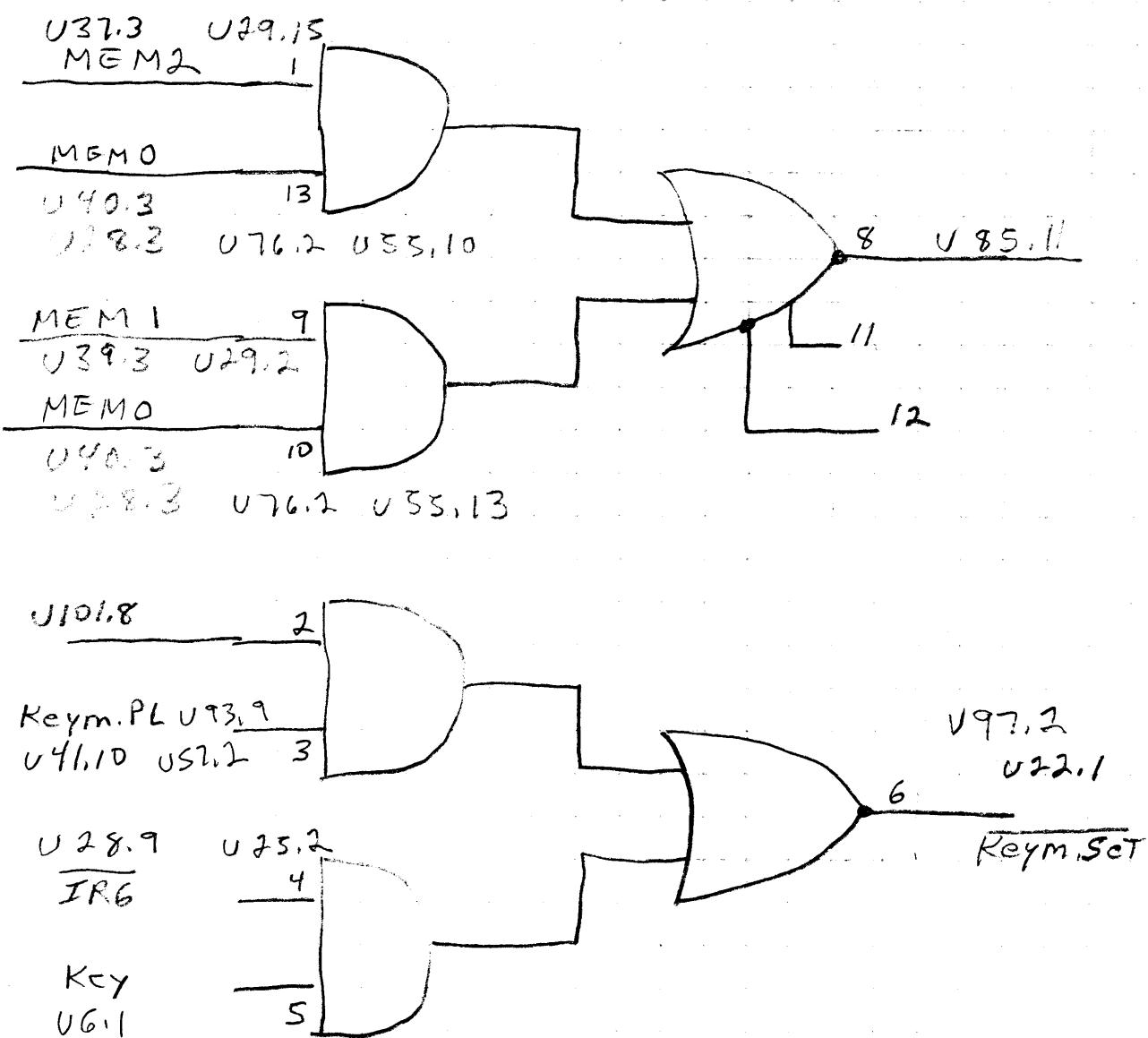
OK

D G 1200 US4

8271 OK



DG 1200 U55 9005
7450 OK



OK

DG 1 200 US6 MC 3026 OK
741121

U68.6

PTG5 ENAB

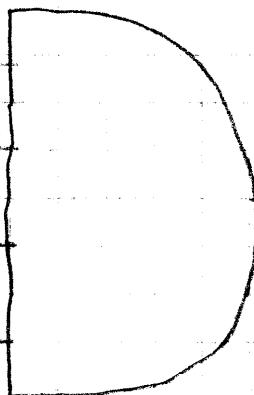
1

U24.6 US.5 2

Key US6.9 4

Keym.PL.TSO 5

US7.3 US7.4



Inh Trans

B45

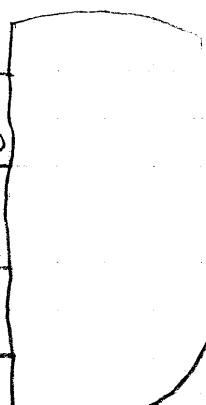
U23.4

U4.2

U6.3

Key

9



U60.9

CLK FLOP U93.5 10

Skip Inc US8.5 12

Loop

13

U22.6

U35.5

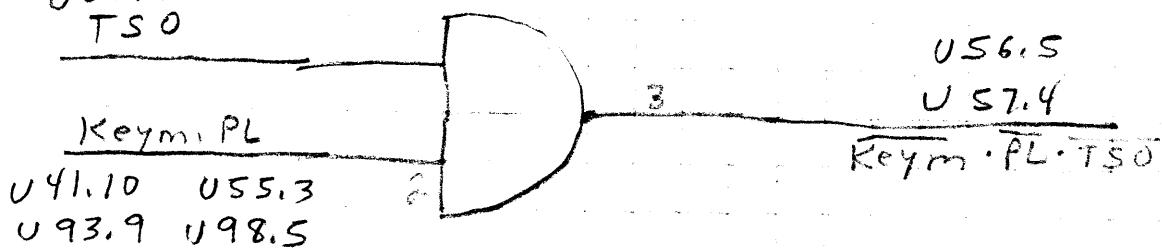
DG 1200 US7

9002
7400 OK

U35.3

U66.6

TSO



U56.5

U57.3

PC enab

U61.8

U57.9

U57.6

CPU CLK

Load PC

U119.12

U40.11

MB0 12

U60.1

PTG 1

U68.10

U57.13

U65.8

SI

U42

U5

U9

U11
PTG

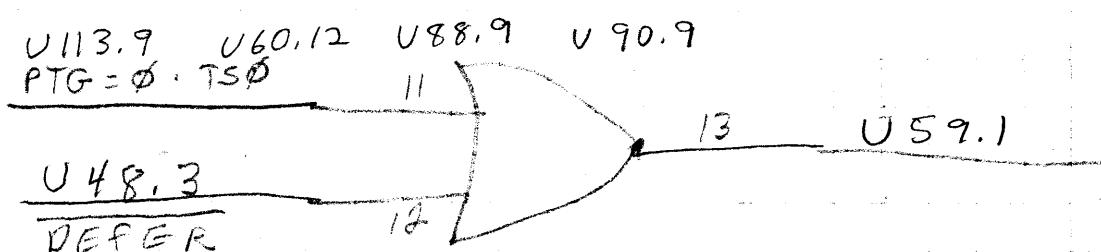
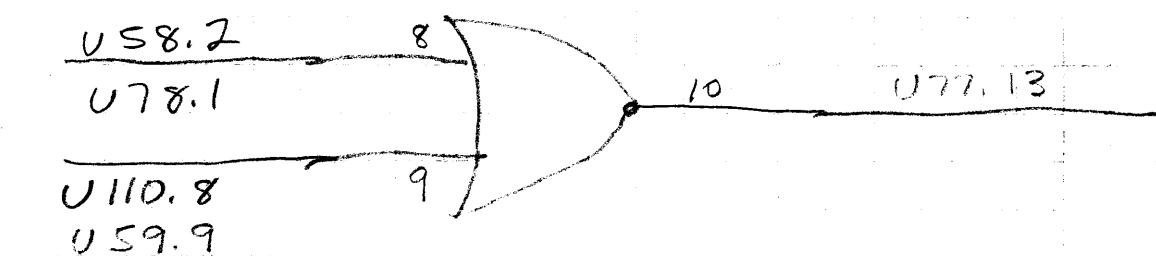
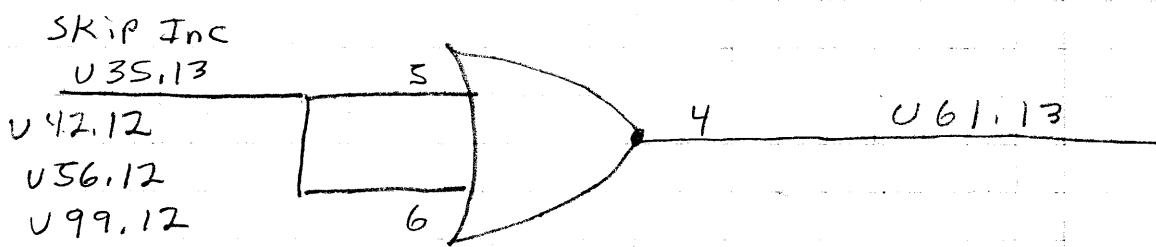
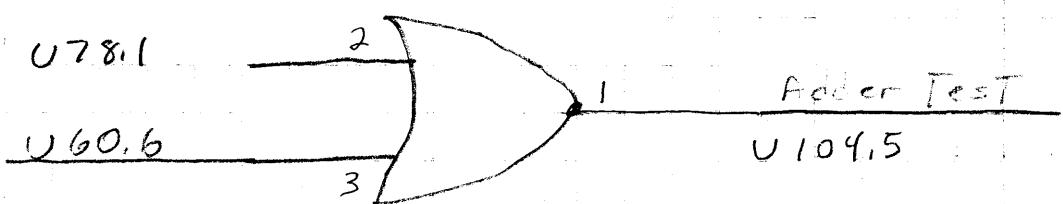
U
D6

OK

DG 1200 US8 ~~8885~~
7402

OK

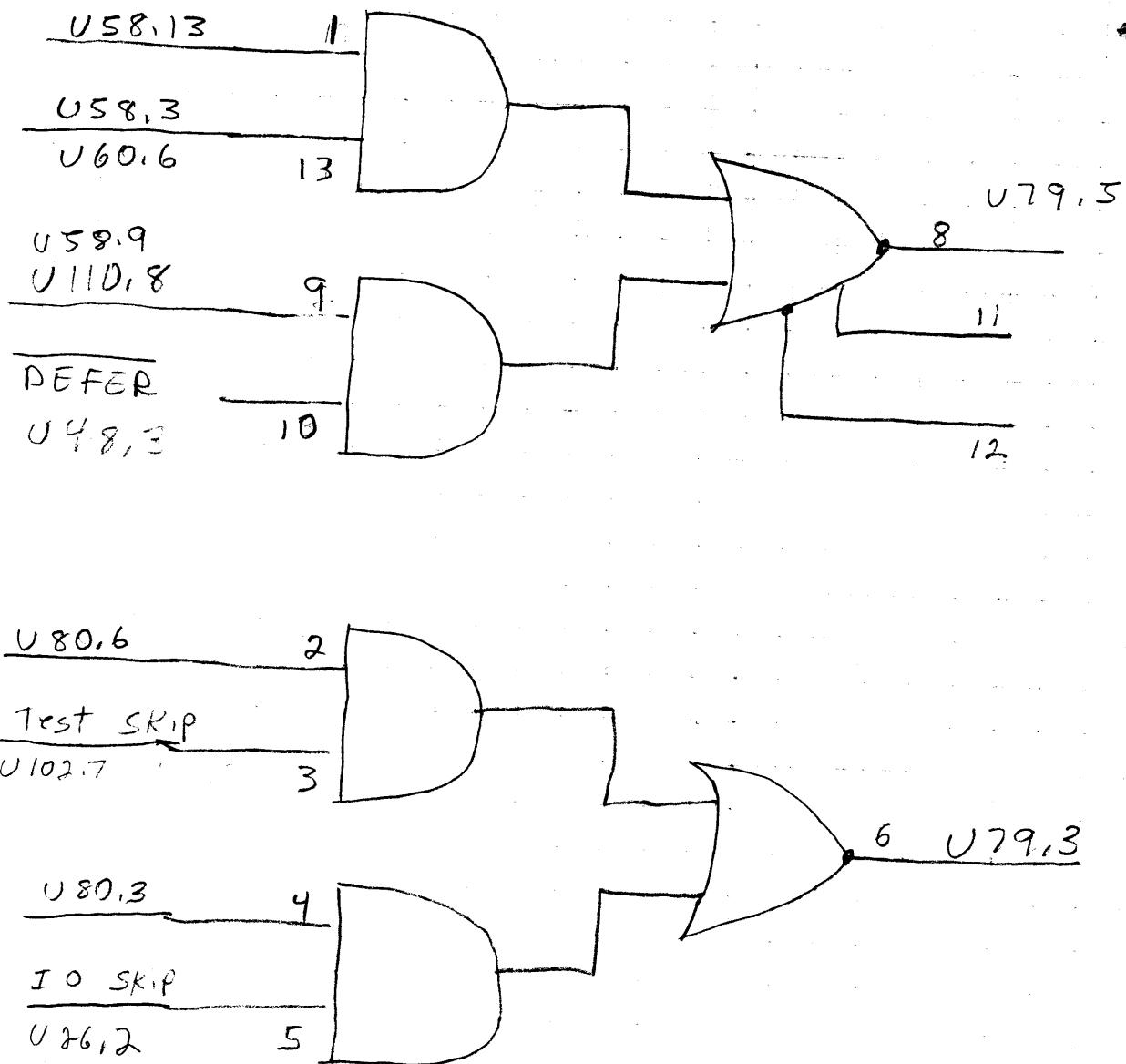
50



DG 1200 US9

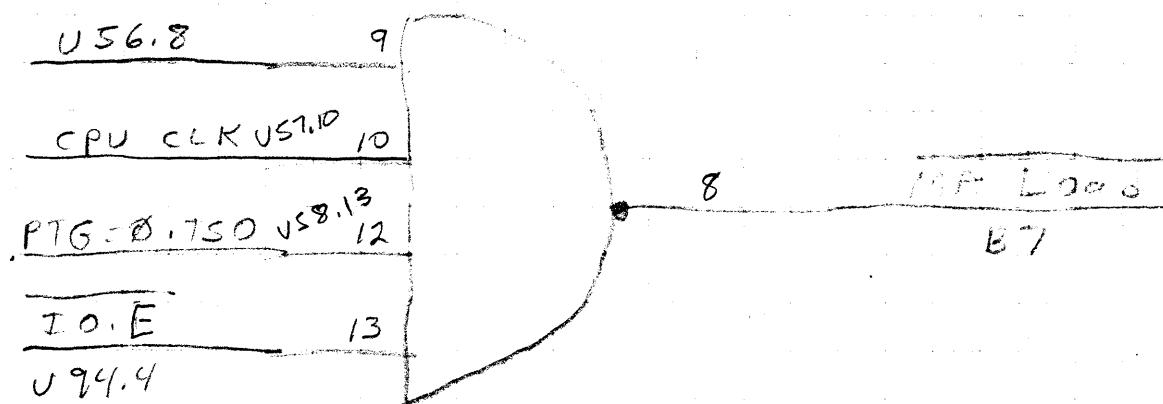
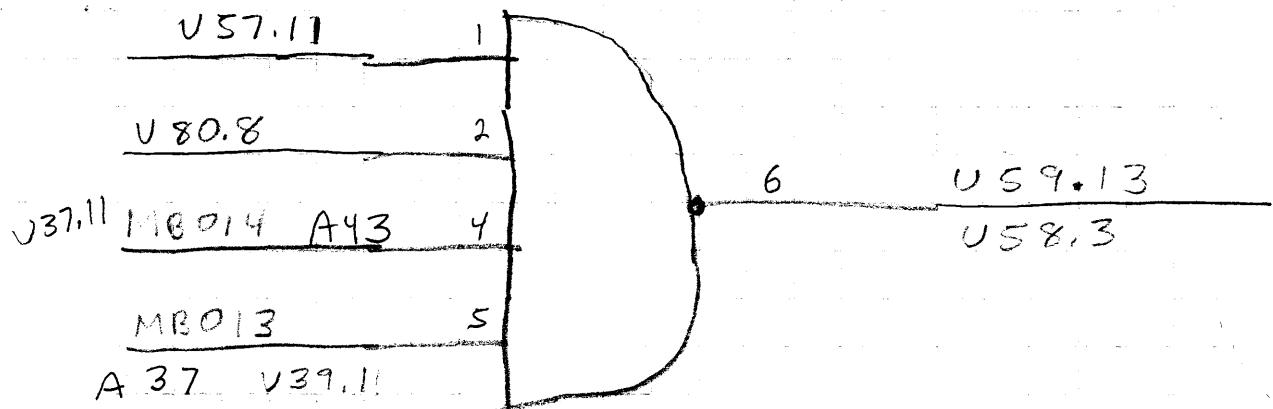
9005
7450

OK



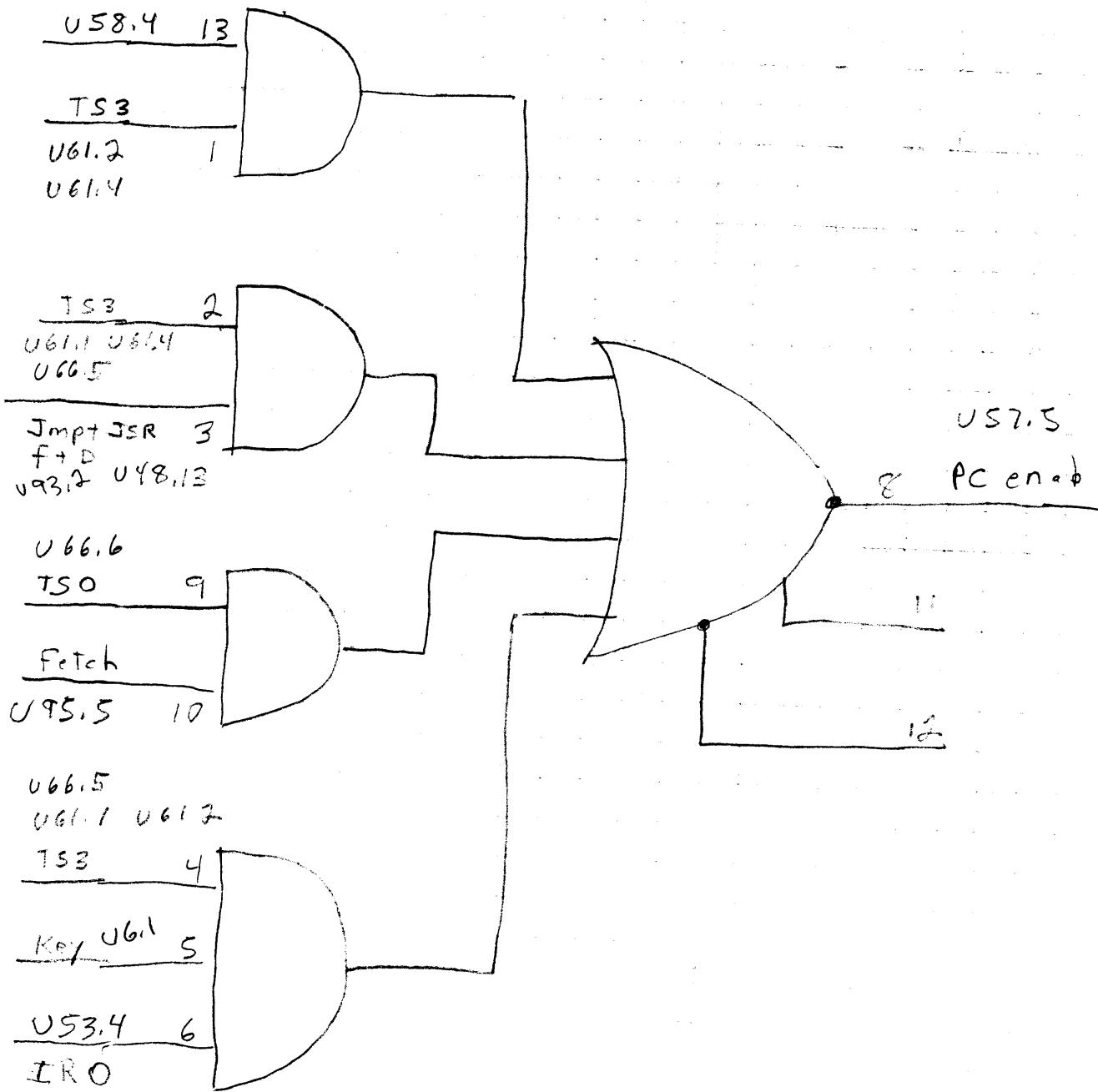
OK

DG 1200 U60 9009 OK
7420



DG 1200 U61 9008
74H54

OK



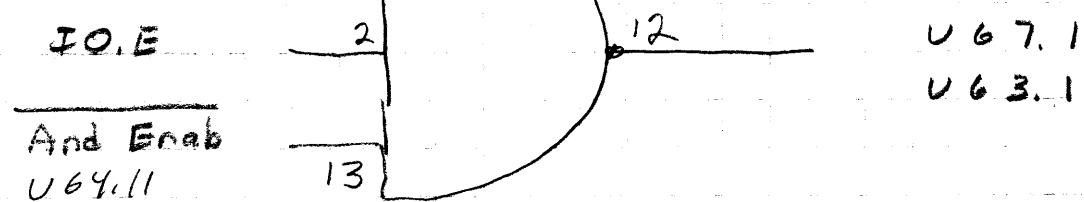
OK

DG 1200 U62

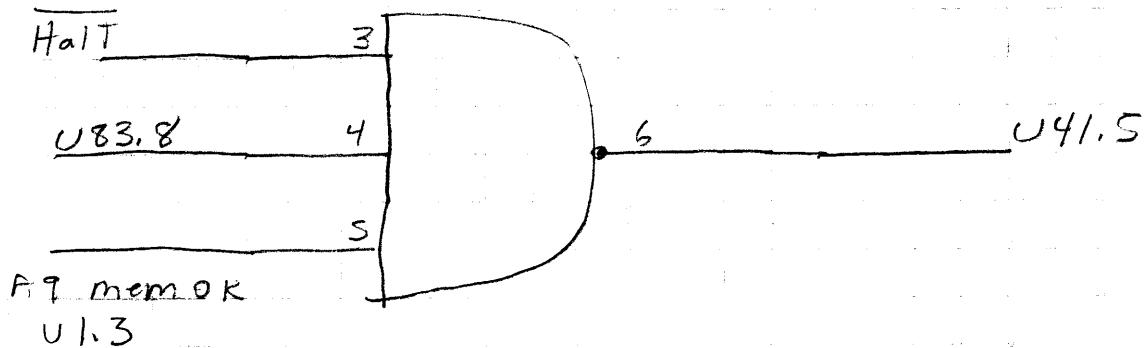
9003
7410

OK

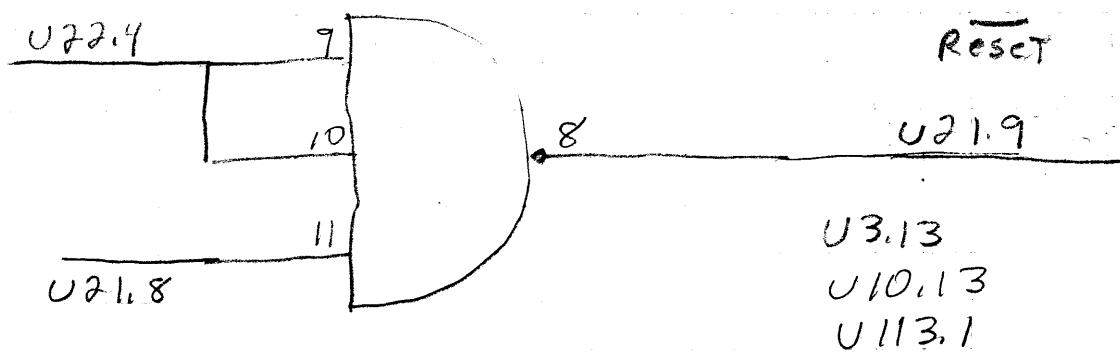
U15.12
U109.1 Pulse enab
U109.6



IO.E
And Enab
U64.11



S7.5
enab
A7 memOK
U1.3



U22.4
U21.8
Reset
U21.9
U3.13
U10.13
U113.1

DG 1200 U63

9321
74139 OKU62.12

E 03

7

U79.8 MBC9 U32.5 2

AO 02

6

U7.3MBC8

AI 01

5

U7.1U27.1 U11.9
U33.4 U33.5
U51.3

00

4

U26.5U64.3

E 03

9

MBC9

AO 02

10

U82.4

SECTIONMBC8
U27.1 U11.9
U33.4 U33.5
U51.3

AI 01

11

U84.4

CLR SECTION

00

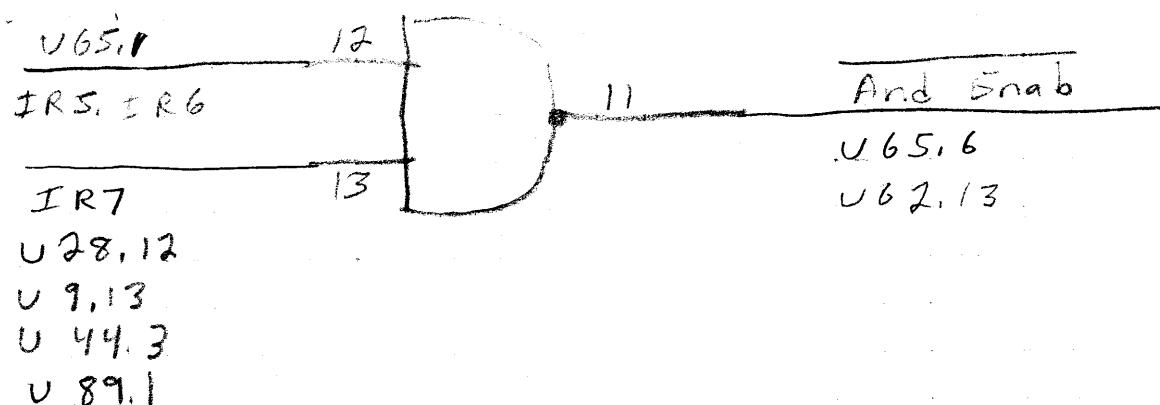
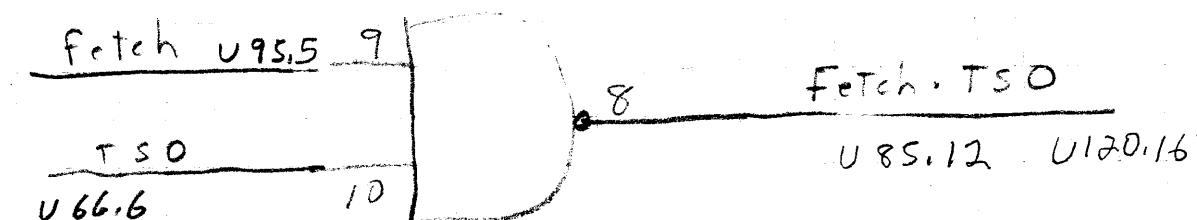
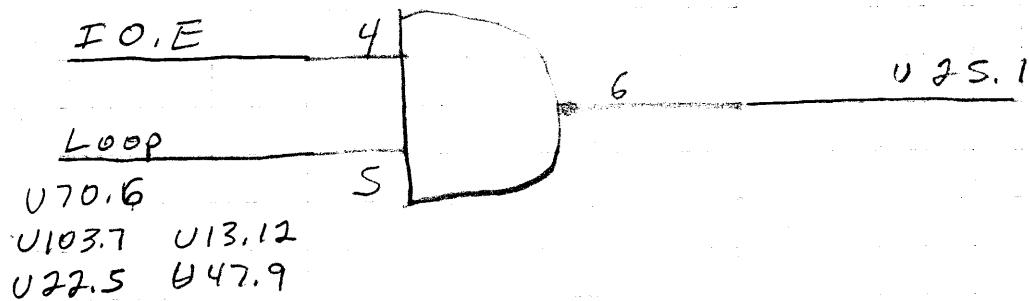
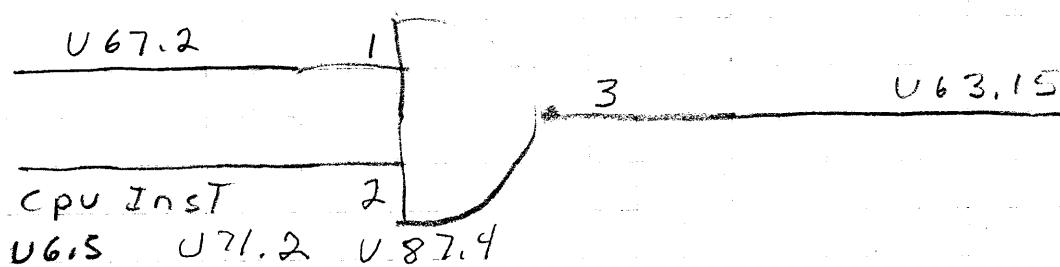
12

OK

DG 1200 U64

7002
7400

OK



DG 1200 U65

~~8885~~
7402

OK

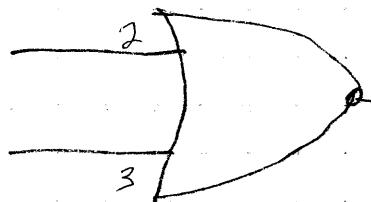
U55.4

U45.9 U46.6

U25.14 U26.9

U28.9 U25.2

JRC



IR5, IR6

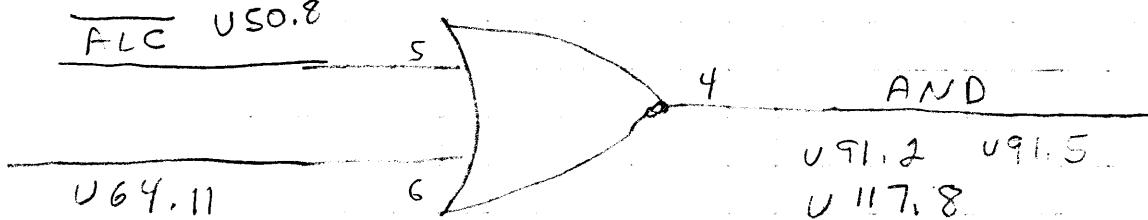
U71.4

U64.12

U28.7

U25.3 U98.1

FLC U50.8



AND

U91.2 U91.5

U117.8

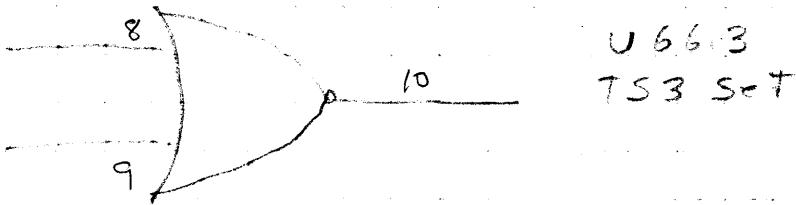
U68.10 U57.13

FIG2

Loop Set

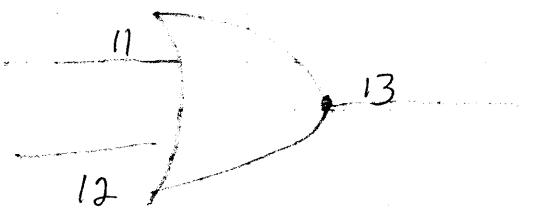
U83.2 U70.8

U103.2



U66.3

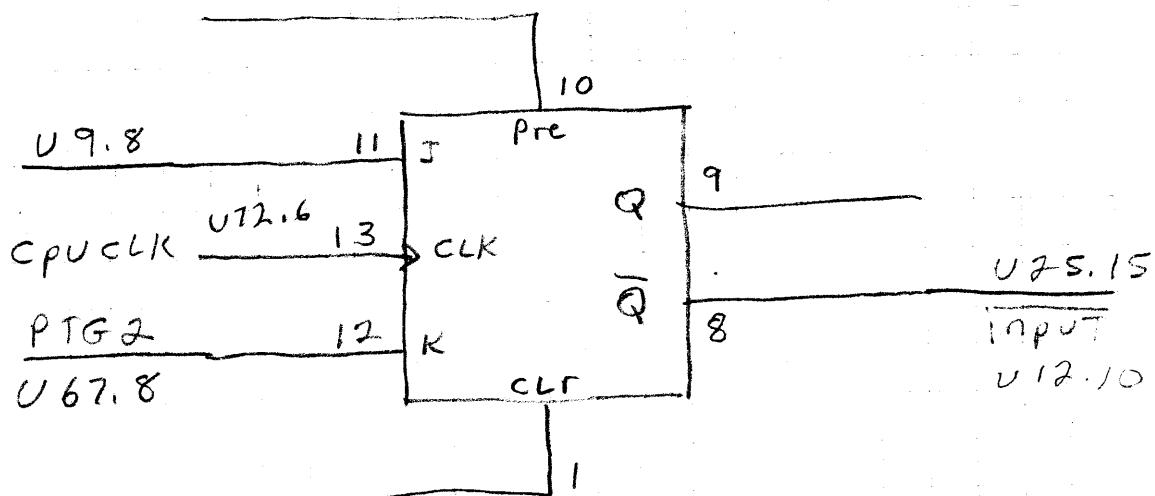
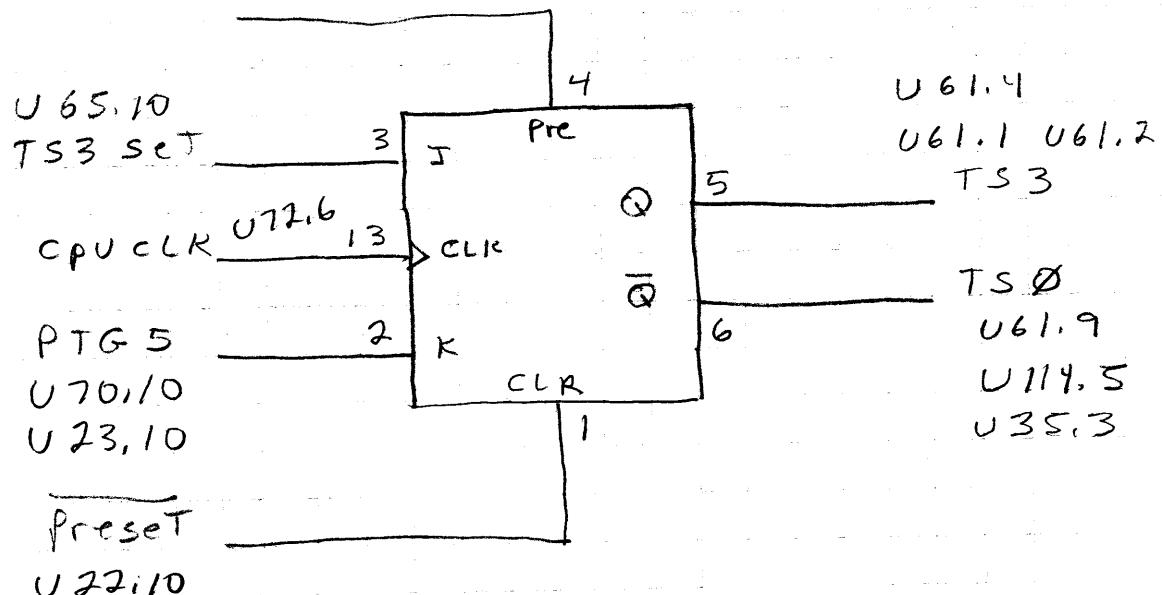
TS3 Set



OK

DG 1200 U66

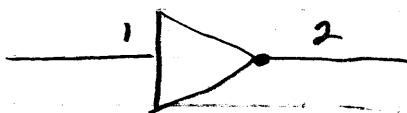
MC 3061 OK
74114



DG 1200 U67

81490 OK

U62.12
U63.1

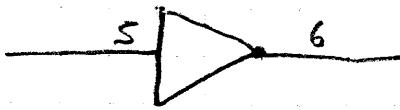


U64.1

DCHA SET
U71.8



U69.2



OK

PTG 2
U68.10
U57.13
U65.8
U67.9
U70.5



PTG 2
U66.12



OK

PTG = 0.1TS3
U68.4
U88.5



PTG = 0.1TS3

U9.9 U9.10
U17.10
U88.1 U88.2

U119

U69

P

U119.4

PT

U69

DG 1200 U68

U 68

9321

OK

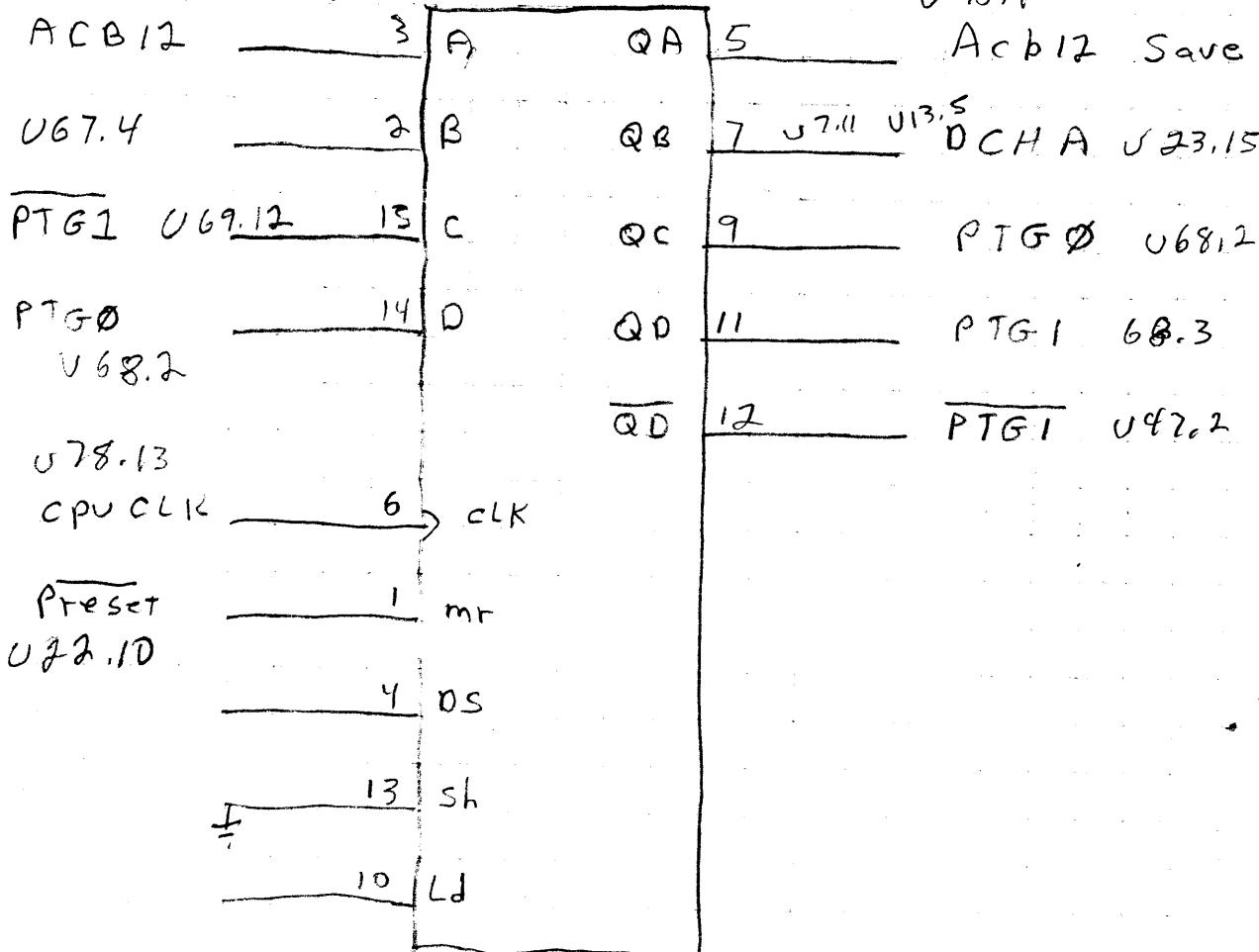
74139

<u>U66.6</u>	<u>TSØ</u>	<u>1</u>	E	03	<u>7</u>	<u>USG.1</u>
<u>PTG Ø</u>	<u>U69.7</u>	<u>2</u>	AO	02	<u>6</u>	<u>PTG 5 ENOB</u>
<u>U119.4</u>			A1	01	<u>5</u>	<u>PTG 1-753 U109.5</u>
<u>PTG 1</u>		<u>3</u>			<u>4</u>	<u>PTG 0-753</u>
<u>U69.11</u>						<u>U67.13 U88.5</u>
<u>U66.5</u>			E	03	<u>9</u>	
<u>TS3</u>		<u>15</u>	AO	02	<u>10</u>	<u>U57.13 PTG 2</u>
<u>PTG Ø</u>	<u>U68.2</u>	<u>14</u>	A1	01	<u>11</u>	<u>PTG 11 TSO</u>
<u>U119.4</u>					<u>12</u>	<u>U80.10 U93.11</u>
<u>PTG 1</u>		<u>13</u>				
<u>U69.11</u>						

D G 1200 U69

8271 OK

U105-H U109.9



U68.6 P

P70
U6
U7
U8
U9

OK

DG 1700 U70 ~~8885~~
7402 OK

Save

U23,15

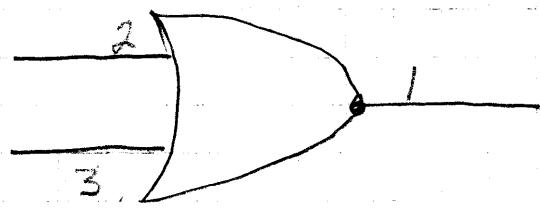
U68,2

68,3

U68,10

PTG2

Loop
U103,7



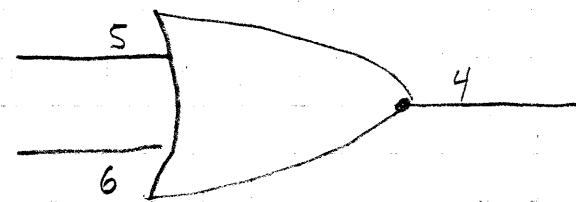
OK

U104,4

U104,3

U73,13

PTG2 - Loop



U83,2 U65,9

Loop Set

8

10

PTG5

U68,6 PTG5 Enab

9

U23,10

U78,12

U42,10

U79,6

U66,2

U95,10

U98,3

U98,4

Key

11

13

U92,5

PTG5 Enab

U68,6

12

U70,9

U79,12

U56,1

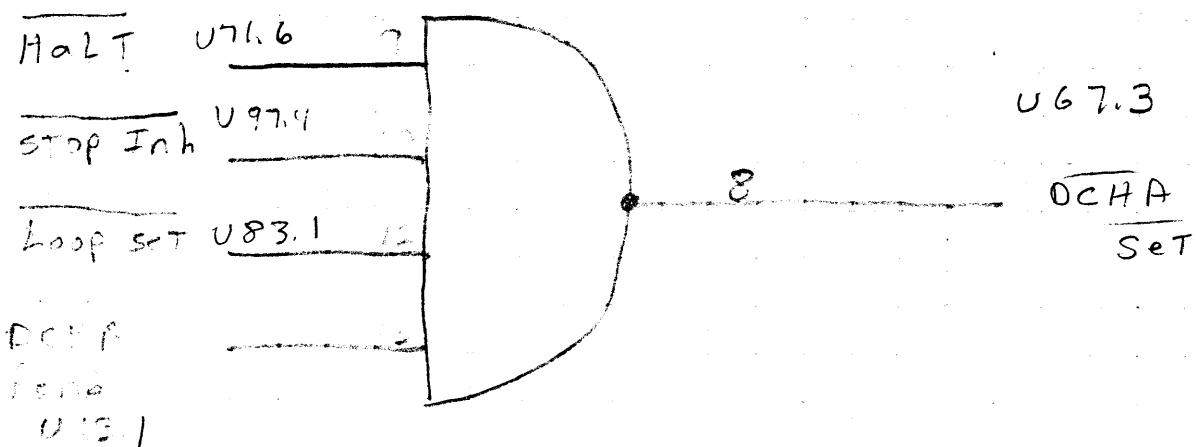
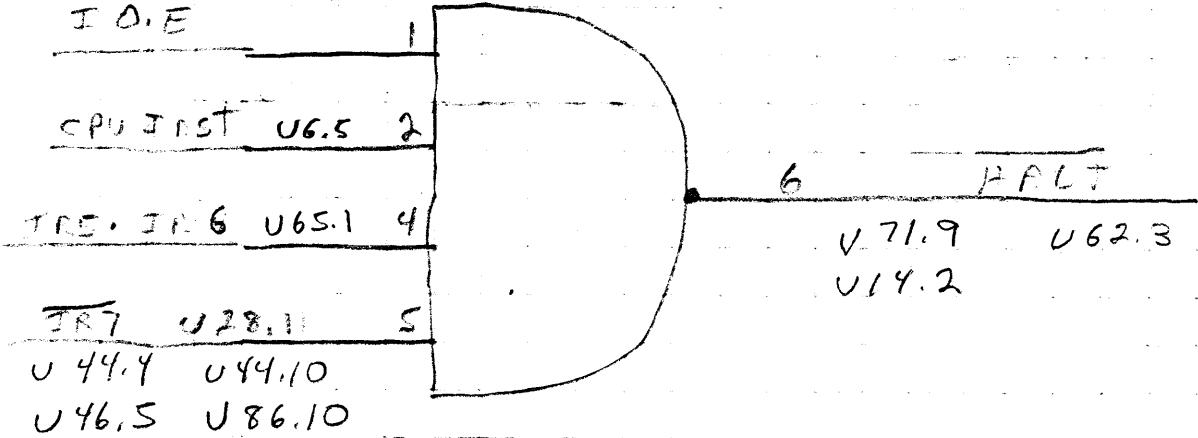
U100,12

U70,12

DG 1200 U71 9009
7420 - 7440 OR

U64.4 U62.2 U42.5
U94.3 U89.4 U86.9

I.O.E

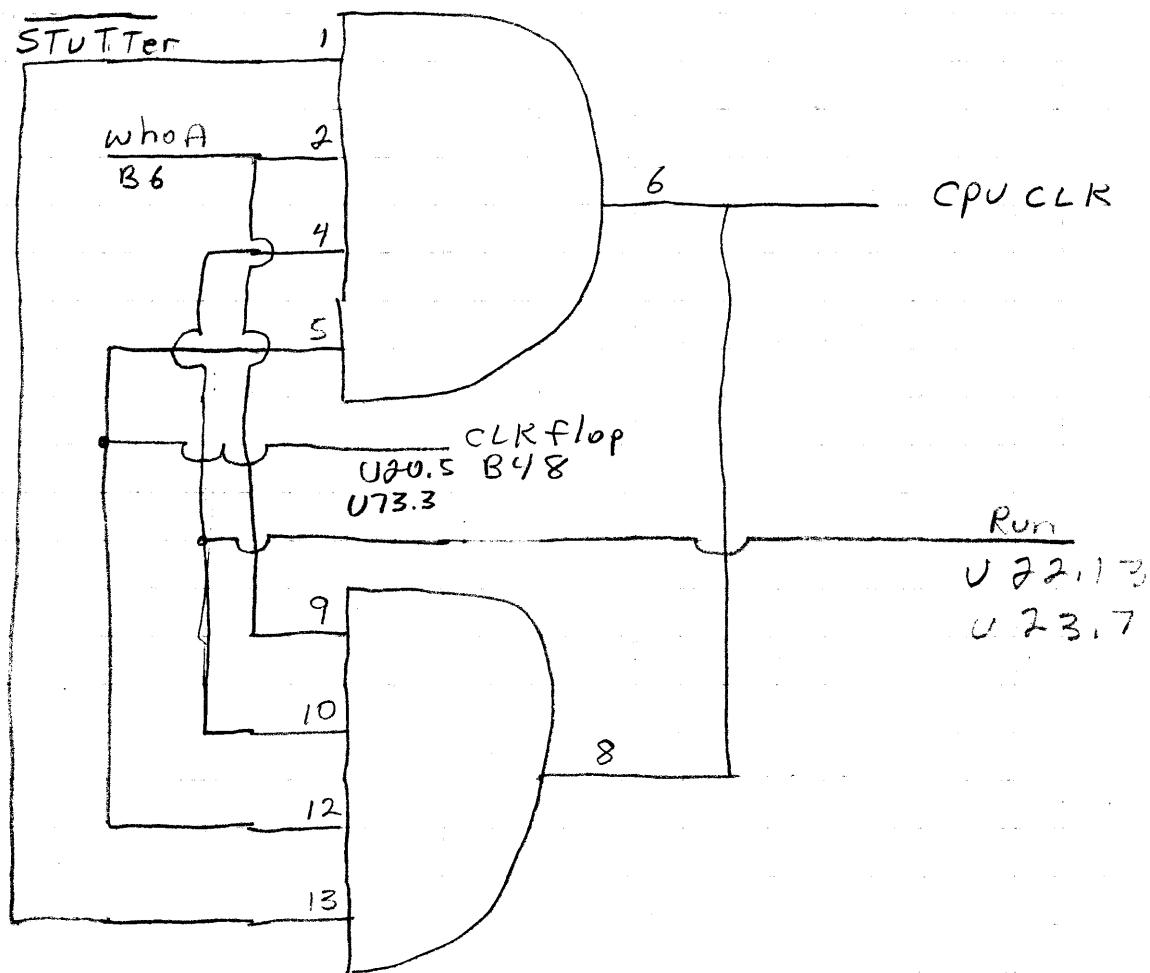


FCP

FCP

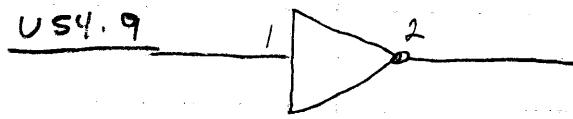
U13.1

OK
40
DG 1200 U72 MC3026 OK
74H21

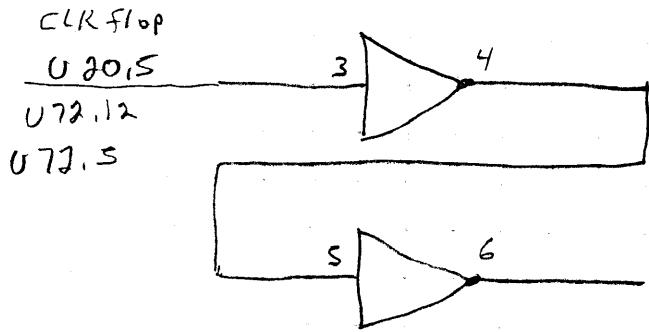


DG 1200 U73

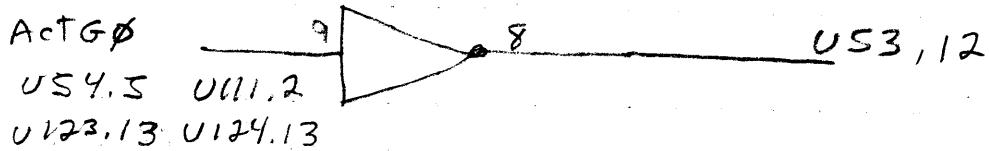
81+90 OK
74 404



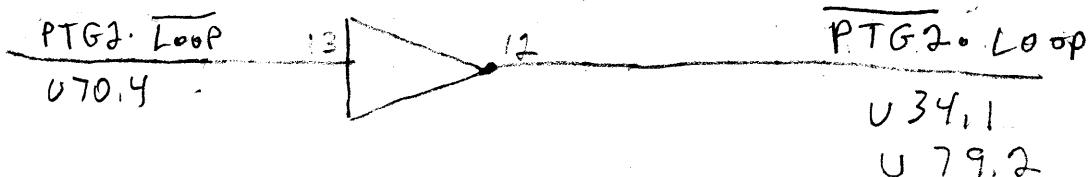
STUTTER U72.1
U72.13



memCLK



DEFER U48.3
A12



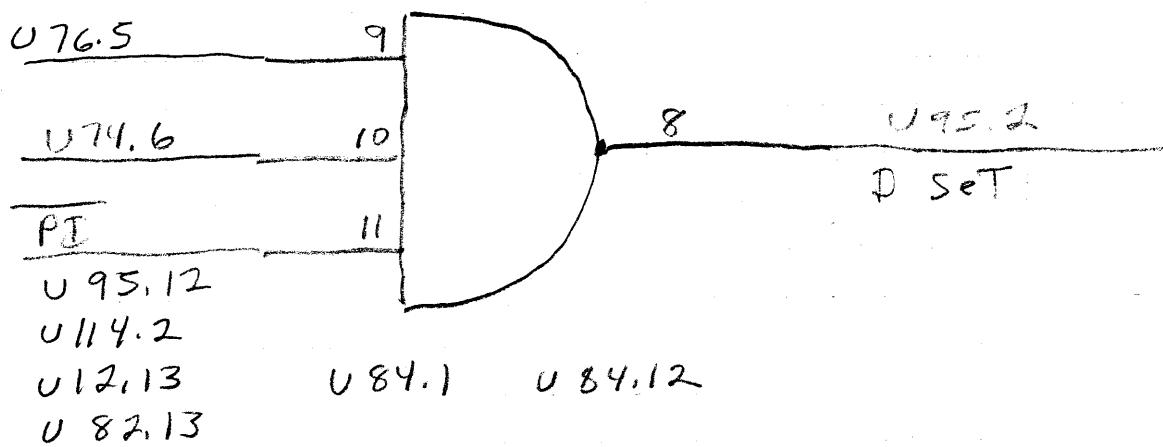
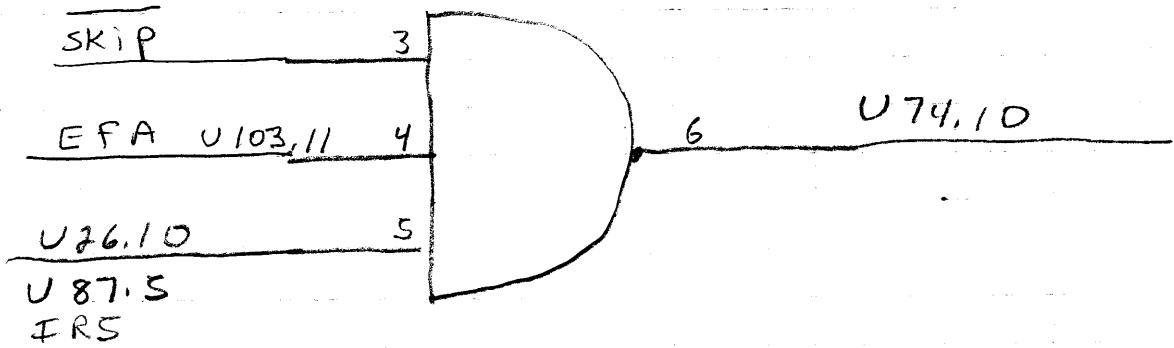
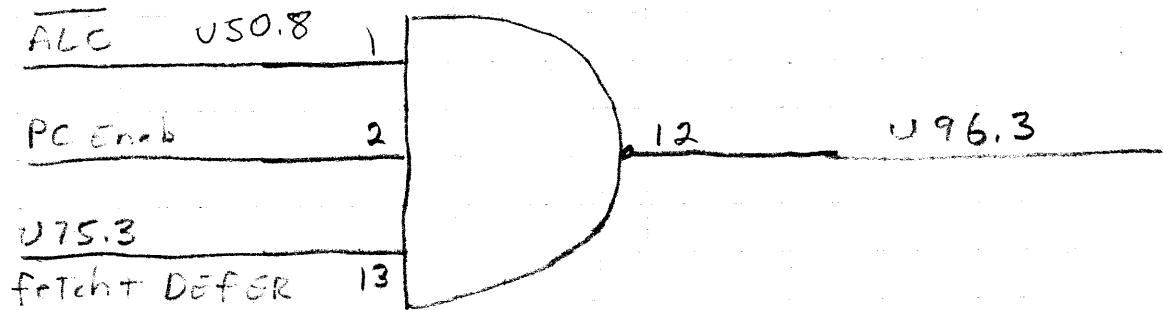
PTG2 Loop
U34.1
U79.2

OK

DG 1200 074

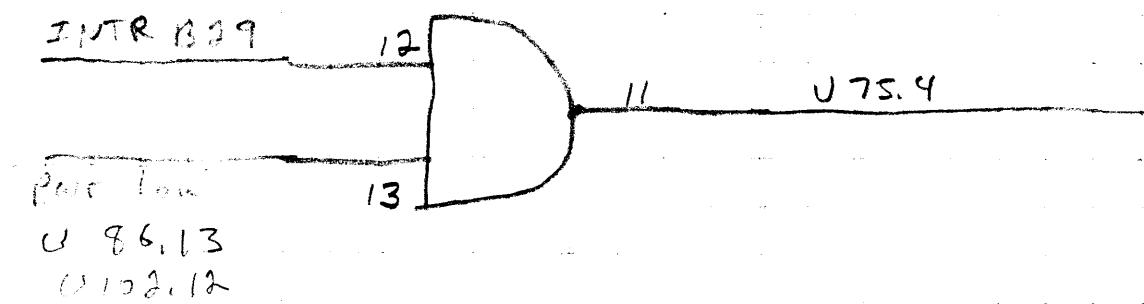
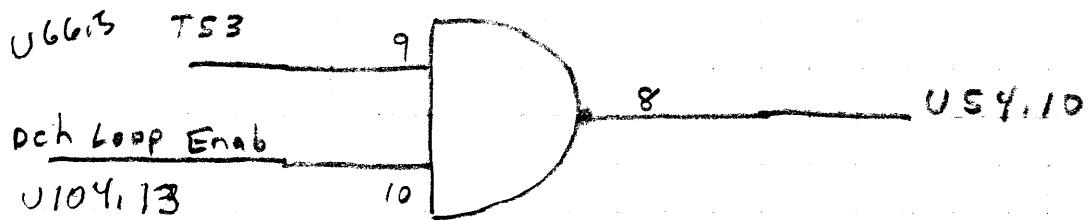
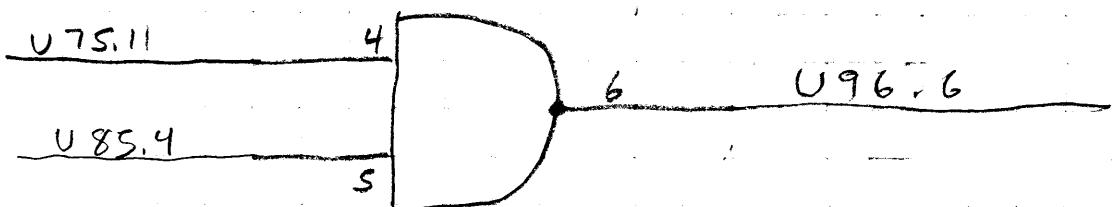
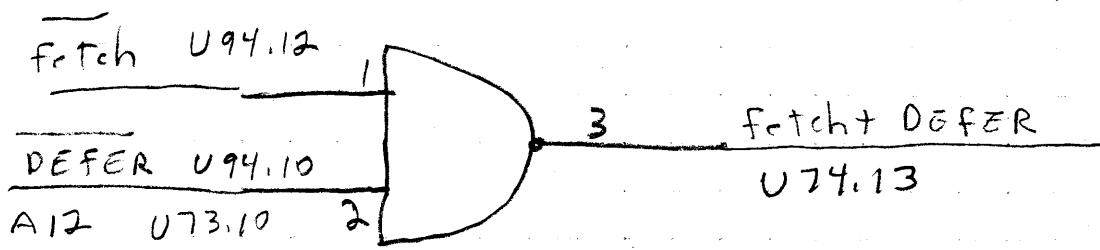
9003
7410

OK



18.3

DG 1200 U75 9002 .01C
7400

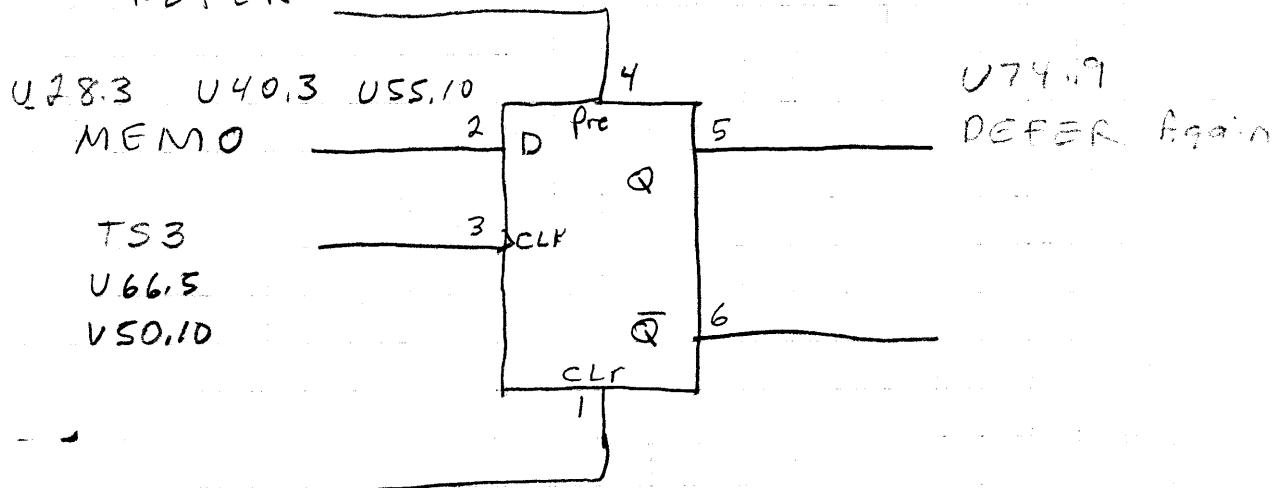


OK

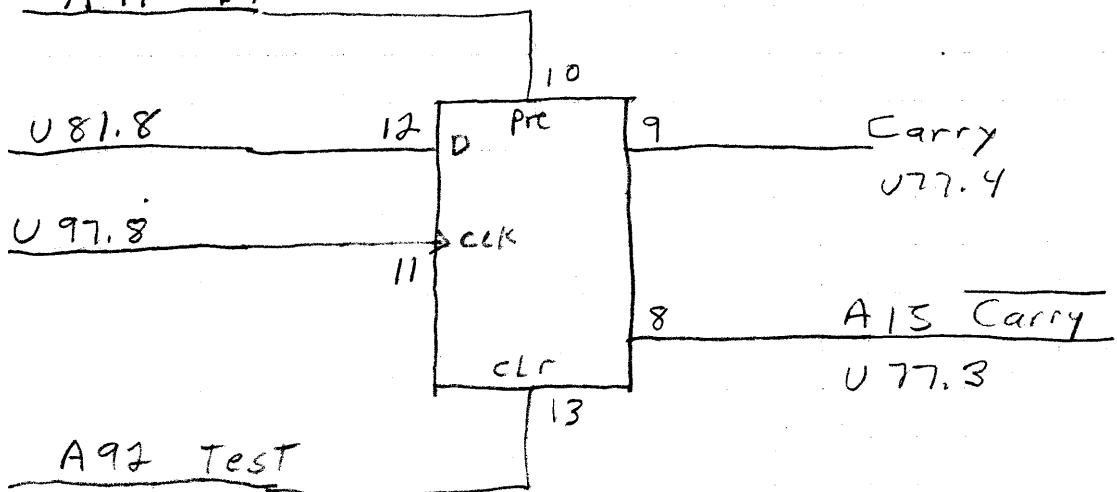
DG 1200 U76 7474 OK

U95.7

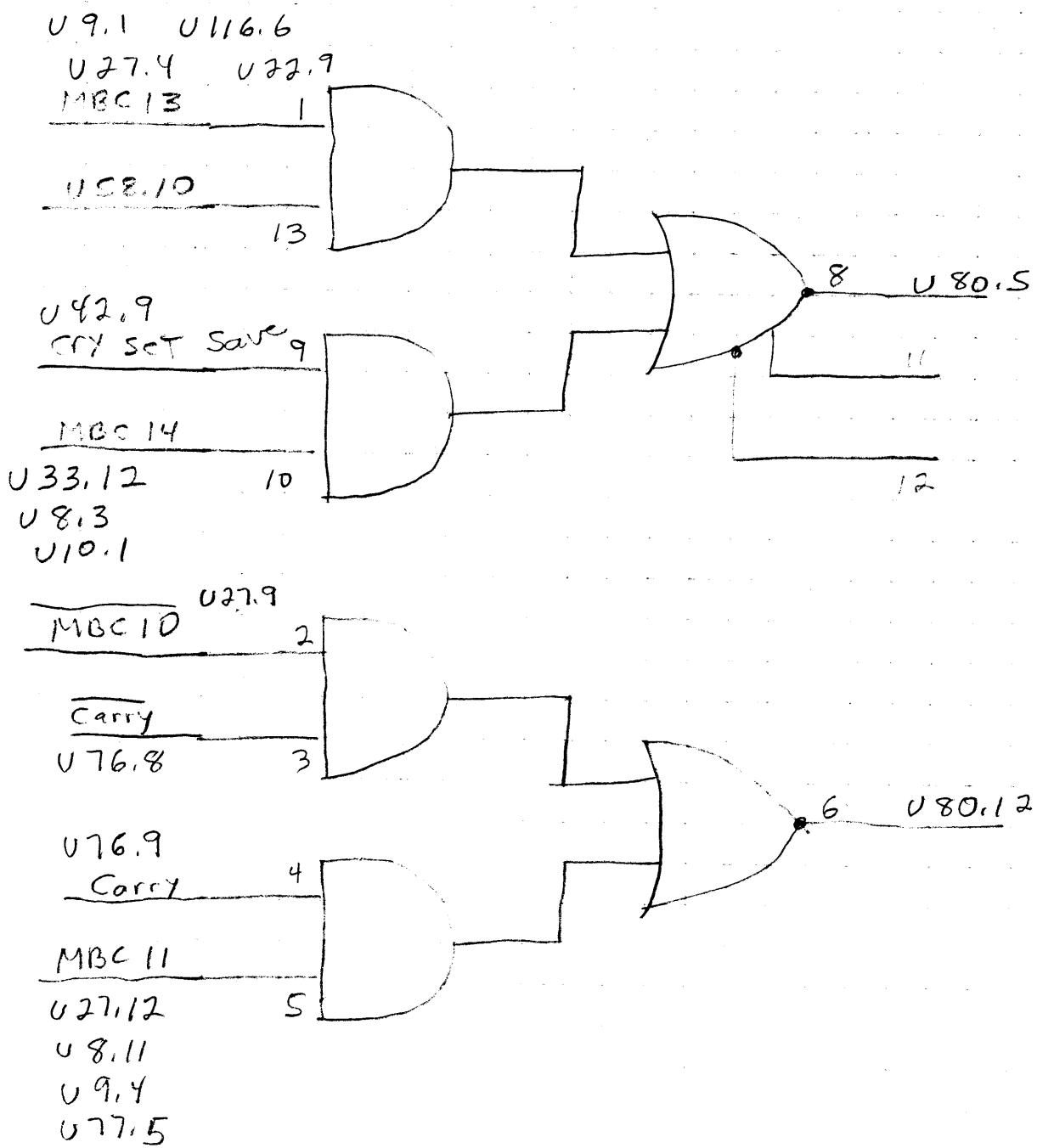
DEFER



A91 DN



DG 1200 U77 9005 OK
7450



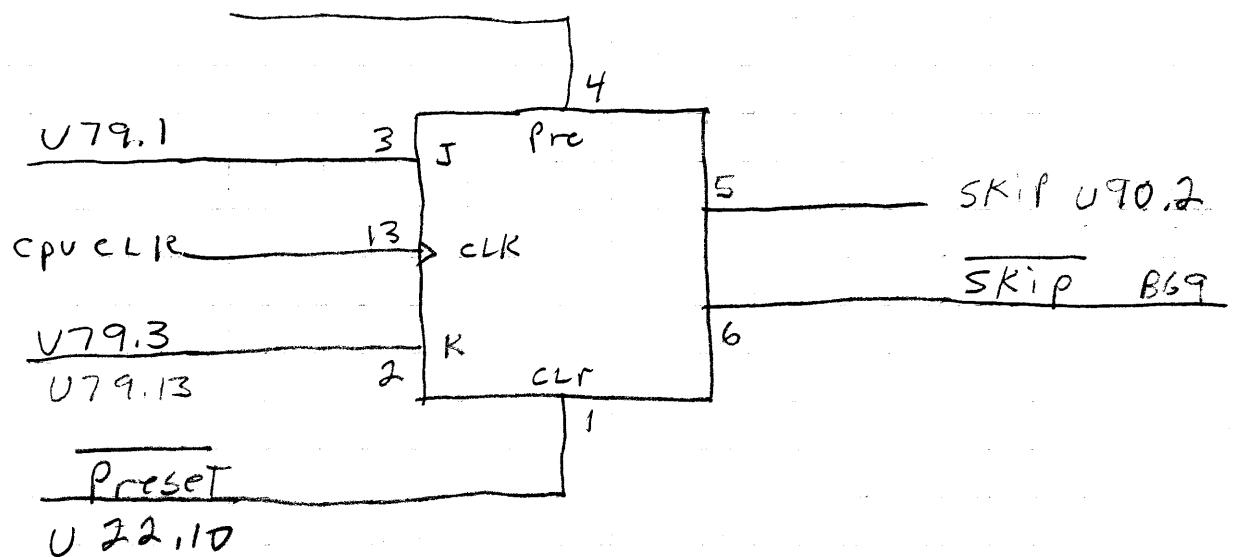
OK

DG 1200

U78

MC 3061 OK

74 114



DG 1200 U79

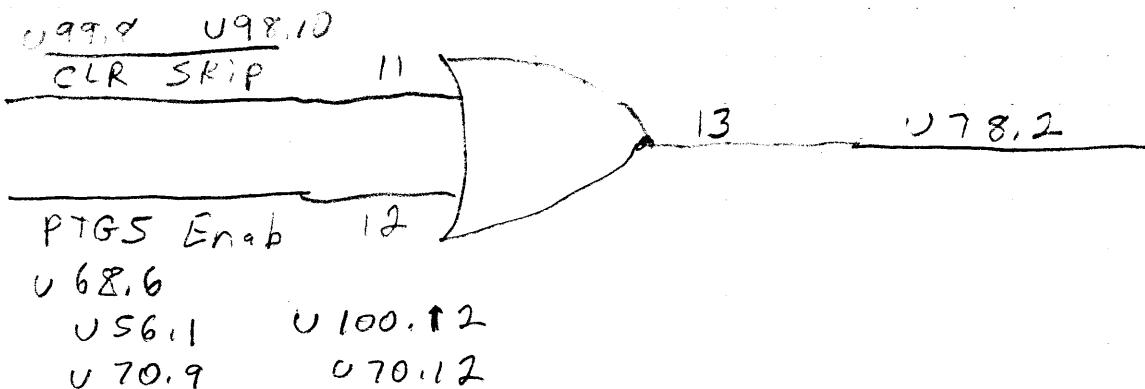
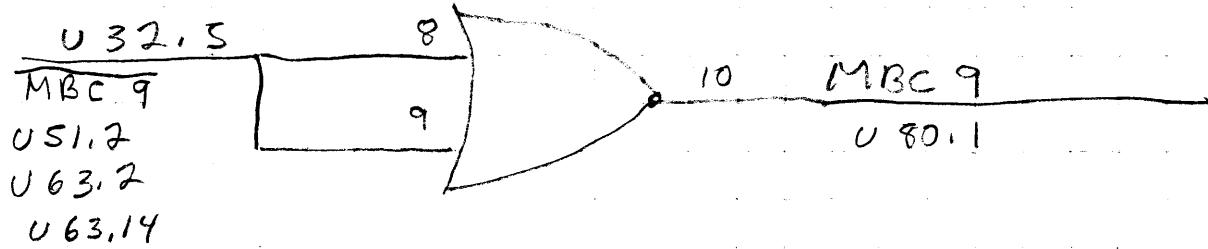
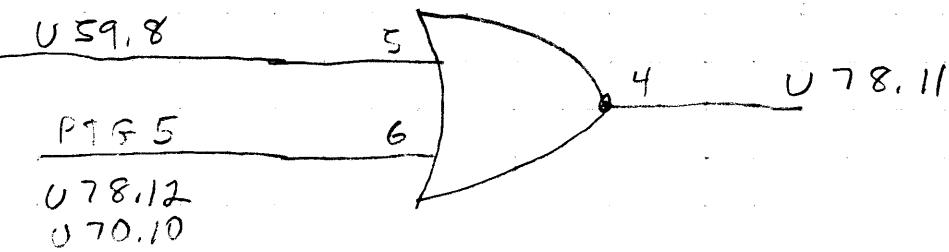
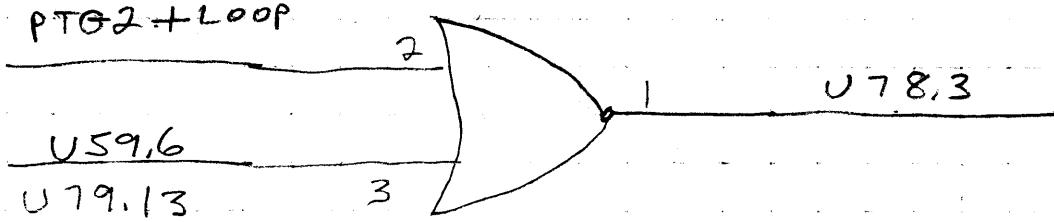
~~8885~~

7402

OK

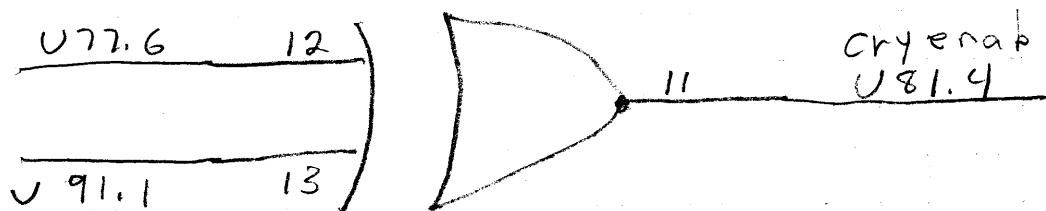
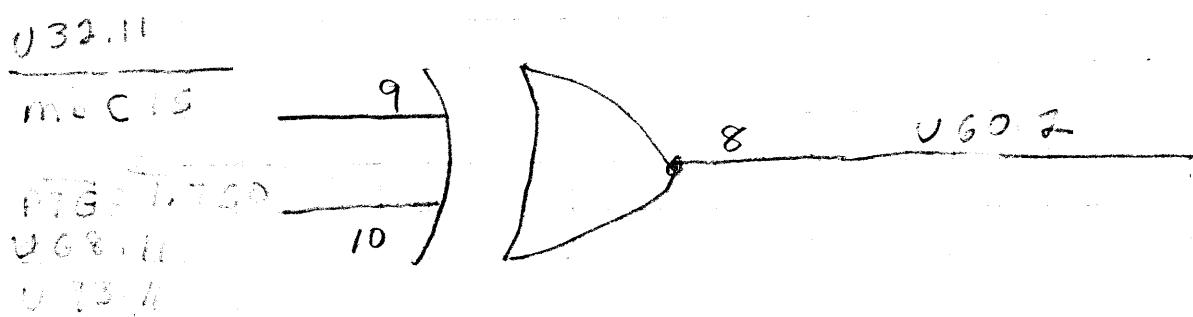
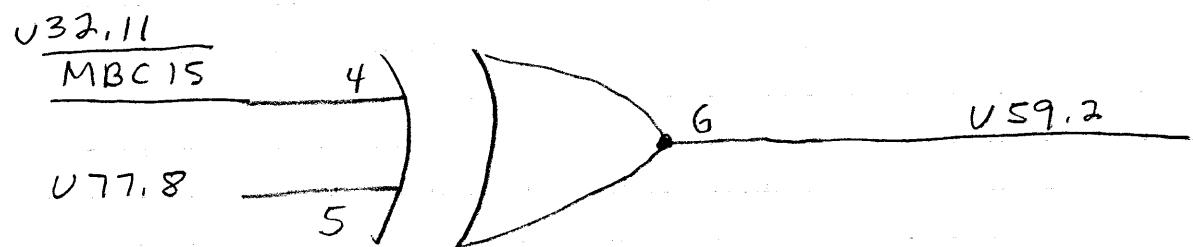
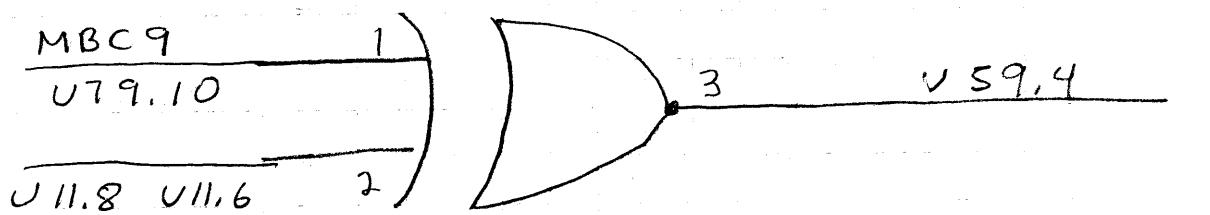
U29.1 U73.12

PTG2+LOOP



OK

DG 1200 U80 7486 DK

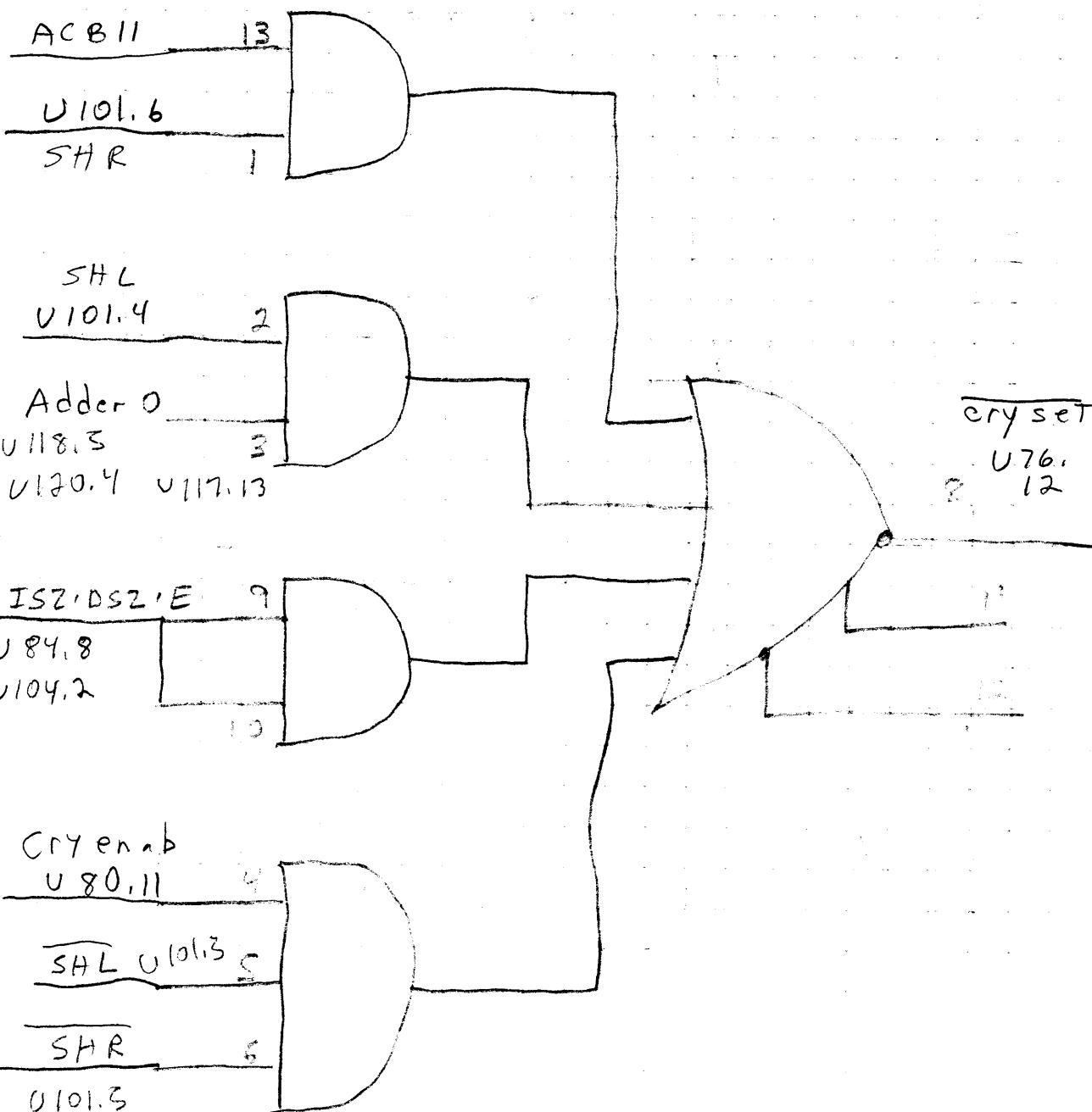


DG 1200 U81

9008 OK
74H54

U108.2 U114.2

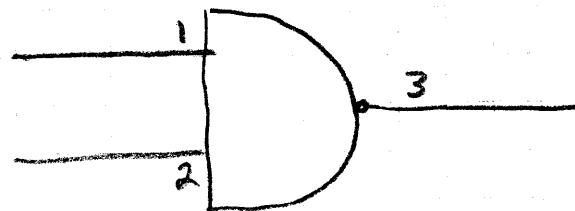
U108.9



OK

DG 1200 U82

9002
7400 OK



OK

U63.10

SET ION

FON A16

U84.6

U85.5

ry set

U76.
12

U86.3

Test skip set

U83.4

U86.4

skip

12

STOP INH

U97.4

U71.10

U87.2

P.I

U93.12

U114.2

U12.13

U74.11

U84.1 U84.12

13

11

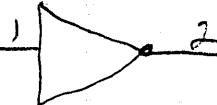
U88.3

DG 1200 U83

8H90 OK

Loop Set

U104.8
U71.12



Loop Set U103.2

U85.9
70.8

U43.8
U41.12



U82.10

AC CLR
U111.3



U111.13

U21.11
U21.10



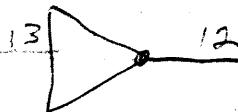
U62.4

U86.6
U86.2



U97.13
ALC. SKIP

U103.9



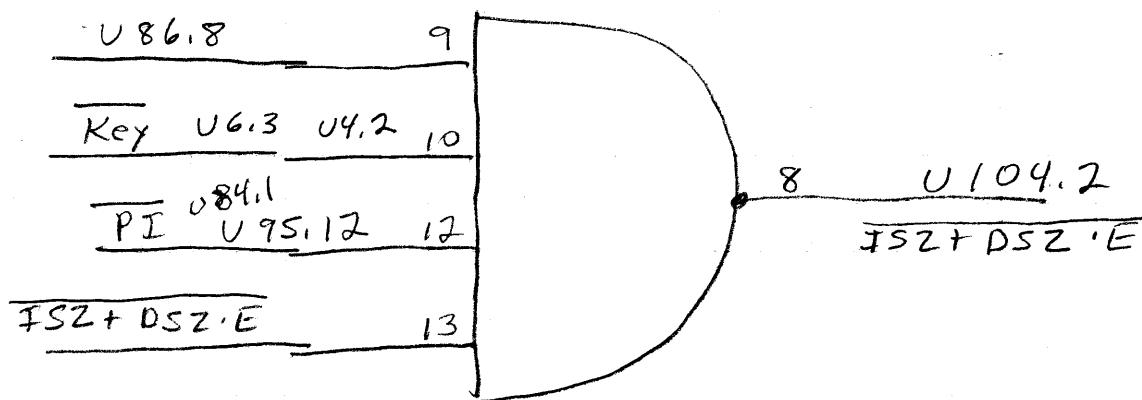
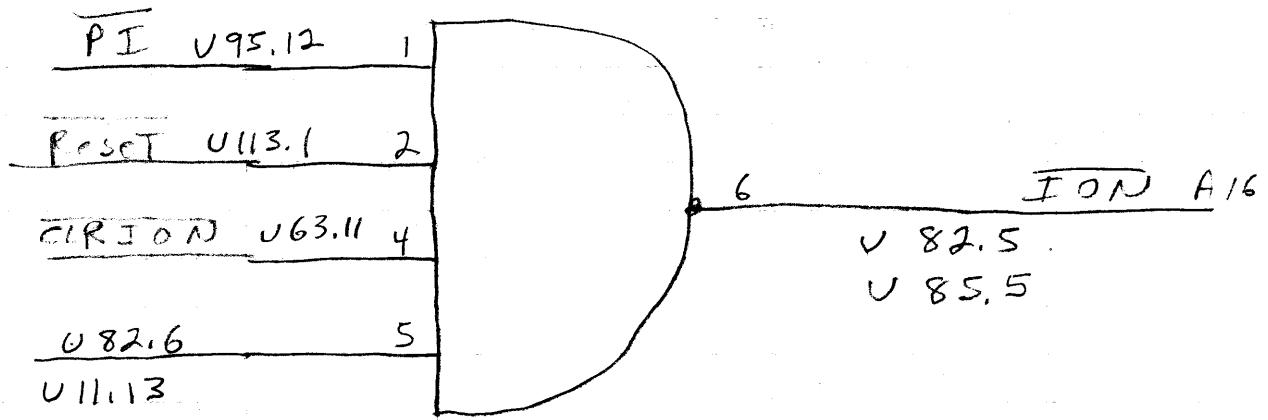
PACK

U103.9 U49.10 U49.12

OK

DG 1200 U84 9009 OK
7420

3.2
5.9
8

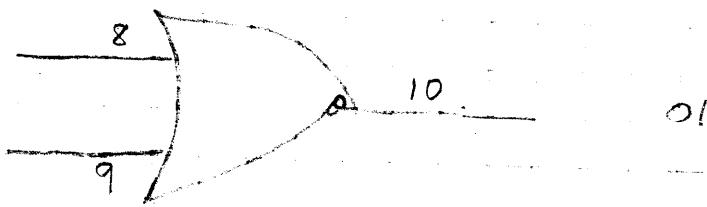
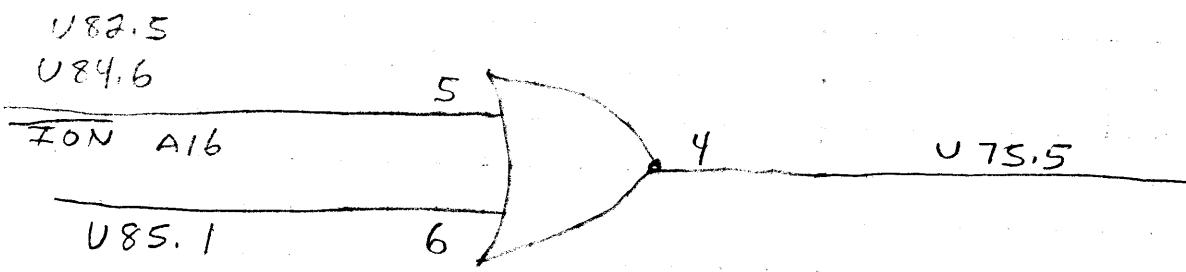
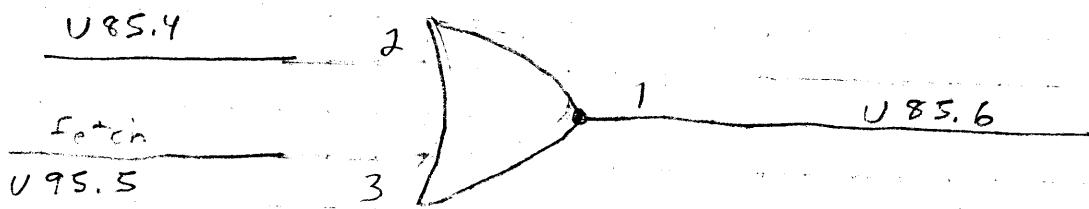


9,12

DG 1200 U85

~~8885~~
7402

OK



U9

I

V7

SKI

U4

U9

I

U28

U44

U44

U2

Pwr

A5

Pw

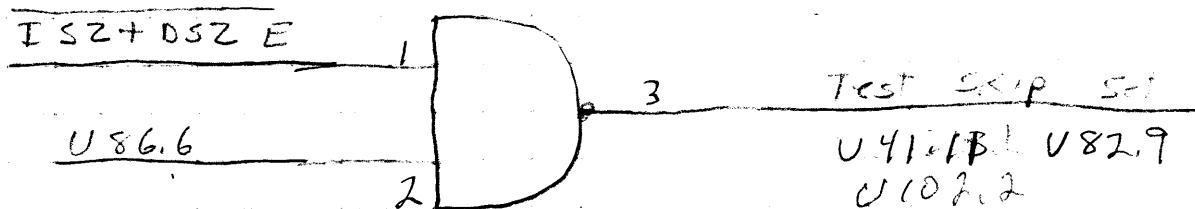
U10

OK

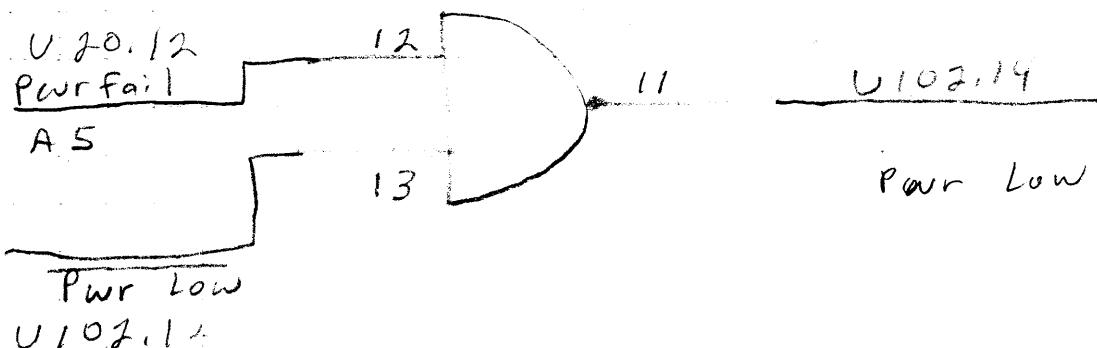
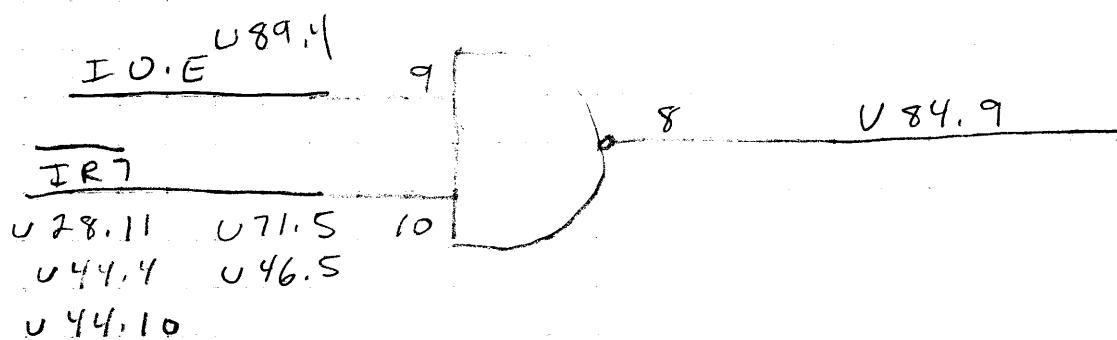
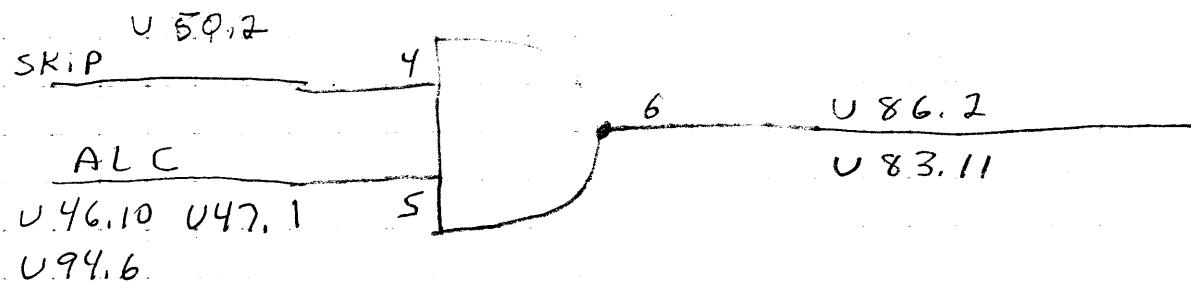
DG 1200 U86

9002 OK
7400

U84.13 U52.1 U52.9



V74.3 U78.6 U82.12



PG 1200

U87

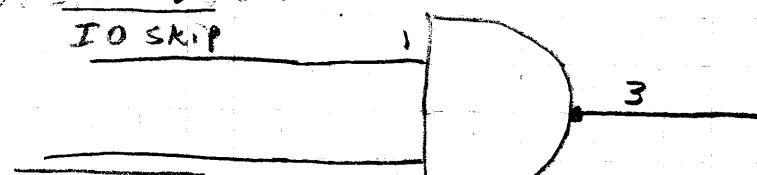
9002

7400

OK

U85.12 U86.1

IO SKIP



STOP in h

U97.4 U82.8 171.10

CPU INST U6.5

U26.10 U74.5

IR5

U41.9 U43.3

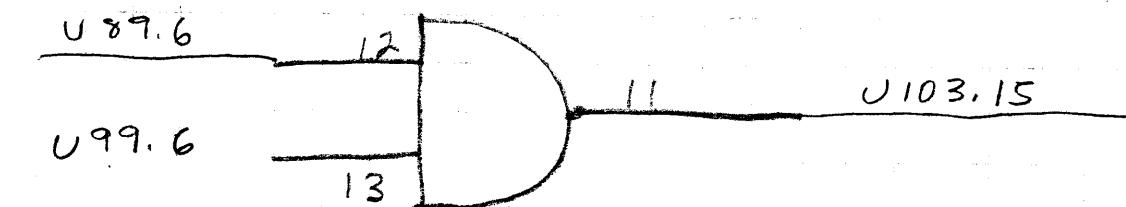
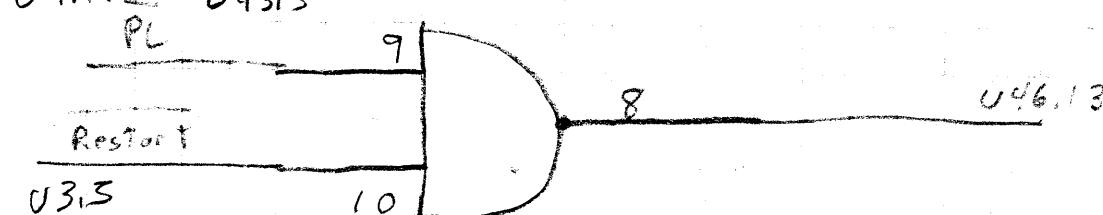
PL

Restart

U3.5

U89.6

U99.6



PTG=

U67.

U17.10

U8.

170

PTG=

U8

17

PTG=

PTG=CC

Seria

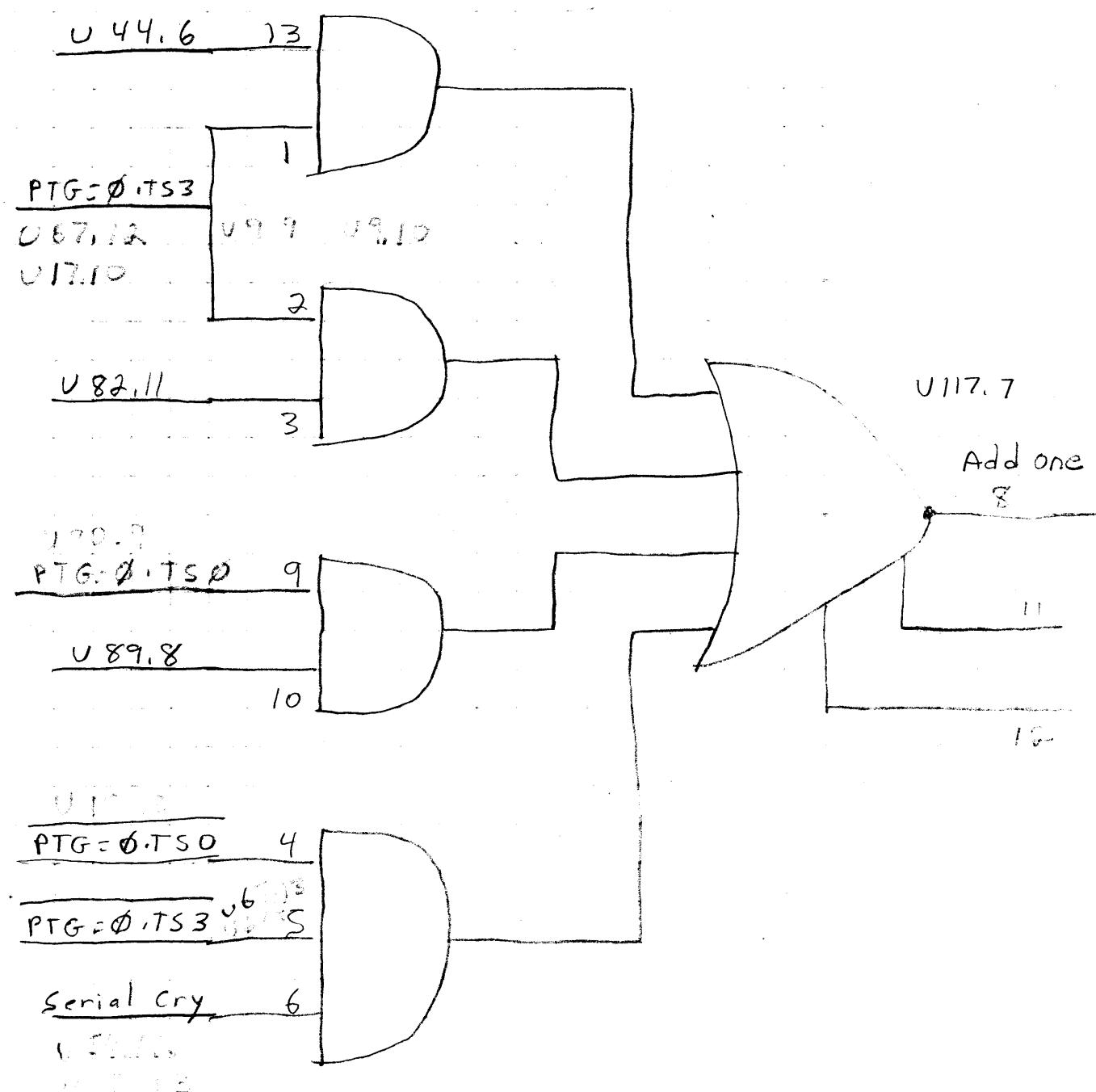
1 - 5

OK

D.G 1200 U88

9008
74H54

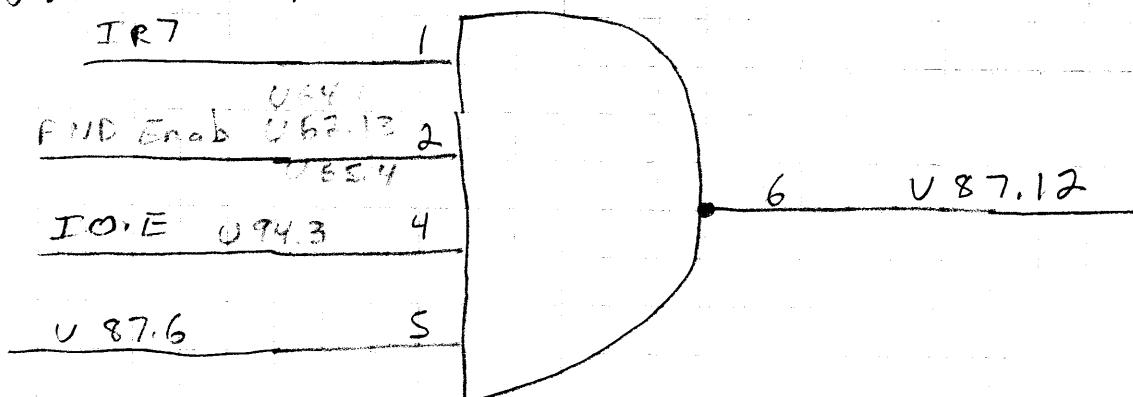
OK



DG 1200 U89

9009 OK
7420 1

U44.3 U64.13
U28.12 U9.13



U87.5

ISZ.E.TSO

9

U90.6

10

Fetch

U75.1 12

U41.1

13

8

U88.10

MB
U4

OK

DG 1200 U90

9005
7450

OK

U69.5

AcB12 Save 1

PTG=0.TSD

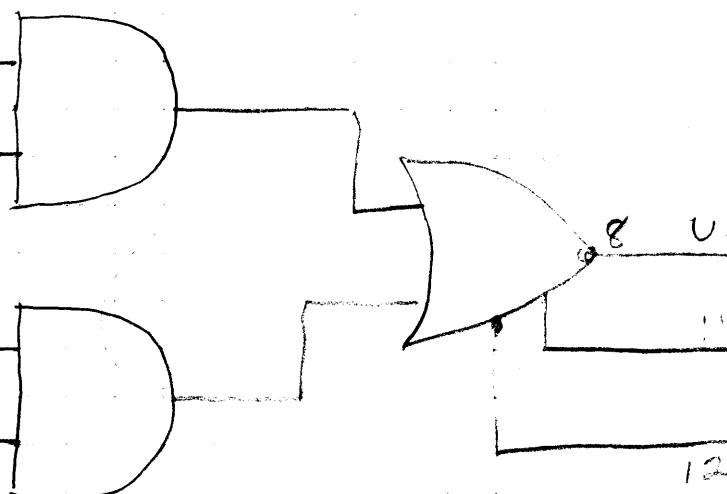
U613.8 U13.13

U13.9

PTG=0.TSD

Cry enab save

U102.9 U117.13 10



U78.5

SKIP

2

PI

U95.11 U35.4 3

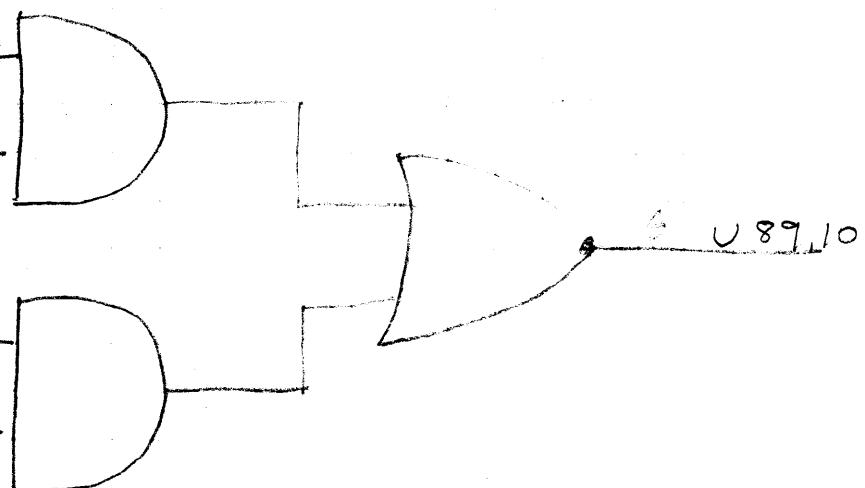
U95.7

DEFER

4

MIB012 Save

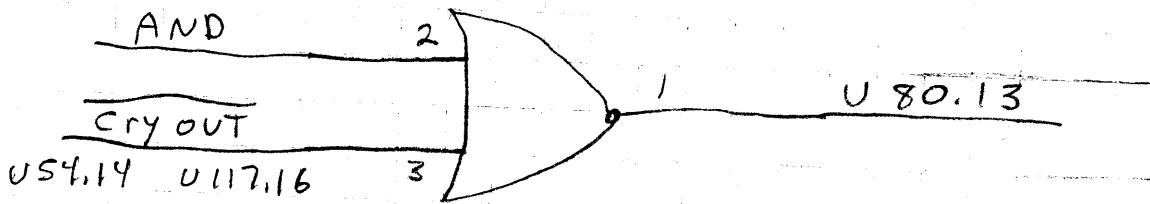
U48.2 U42.7 5



DG 1200 U91

~~8885~~
7402 OK

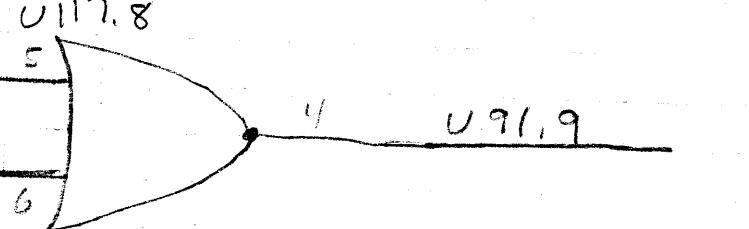
U65.4
U91.5 U117.8



U91.2 U65.6 U117.8

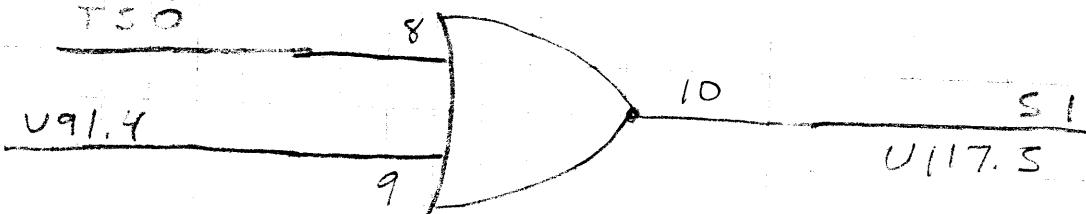
AND

U91.13

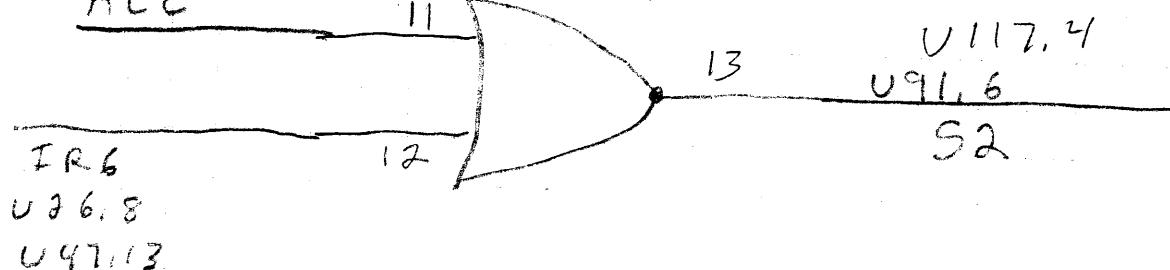


U66.6

T50



ALC U50.8



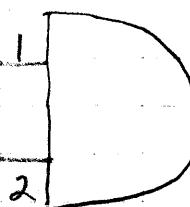
OK

D.G. 1200 U92

9002 ok
7400

US2.4
DSZ.E.TSP

U47.8



50

U117.3,6

U28.5 U43.10 US3.5 US0.13

US3.6 US1.1

TRD

U70.13

4

6

U99.4

5

ExeC

U94.11

9

8

US2.3

TSØ

U66.6

10



U93.8

12

11

JSR.EFA

U100.3

JSR.EFA

U99.2

U93.12

13



DG 1200 U93

9003
7410 OK

J R4 U26.12 1

Impt JSR F+D U48.11 2
U61.3

EFA

U103.11 U32.13

U33.13 U44.9 U45.10 U46.4
U47.3 U47.4 U24.4

13

12

JSR.EFA

U92.13

U99.2

U111.6

3

memclk

U73.6 U115.6 U122.6

4

6

Load AC

A77

U123.3

U124.3

U44.2

U74.1

U44.10

Keym. PL

9

PTG=0 TSO U113.8 10

PTG=1 TSO

U80.10 U68.11

11

8

U92.12

E

-V

F

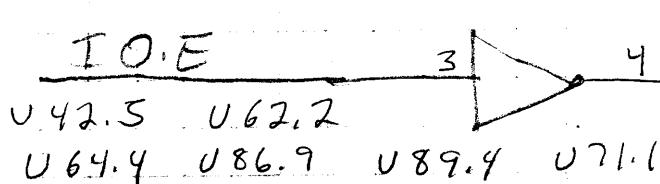
OK

DG 1200 U94

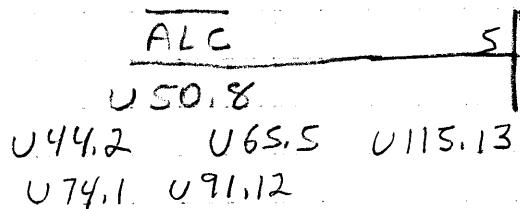
8490 : OK



OK



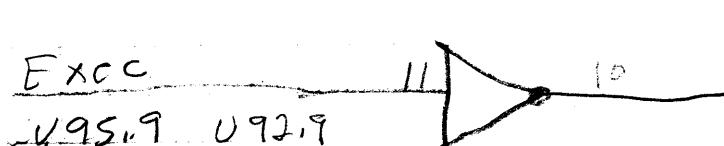
U 60.13



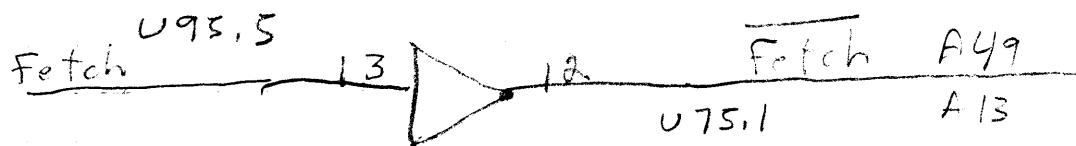
ALC
U 46.10 U 47.1
U 86.5



OK



U 52.15
A 11



A 49
A 13

DG 1200 U95 827.1 OR

U96.10 ————— 3 A QA 5 Fetch U94.13

DSet U96.2 ————— 2 B QE 7 Defer U76.4

ESet U96.1 ————— 15 C QC 9 Exec U94.11

U96.4 ————— 14 D QD 11 PI U35.4

PI Set

U72.6 U72.8

CPU CLK ————— 6 CLK

Preset ————— 1 Mr

U17.1 U22.10

————— 4 DS

————— 13 Sh

PTG5 ————— 12 Ld

U70.10

U23.10

U42.10

U66.2

U78.12

U79.6

U98.3 U98.4

U
U

U
U

U
U

U
U

U
U

U
U

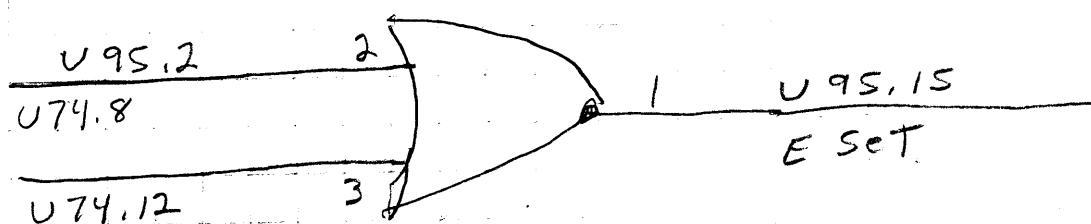
U
U

DG 1200 U96

~~8885~~
7402

OK

OK

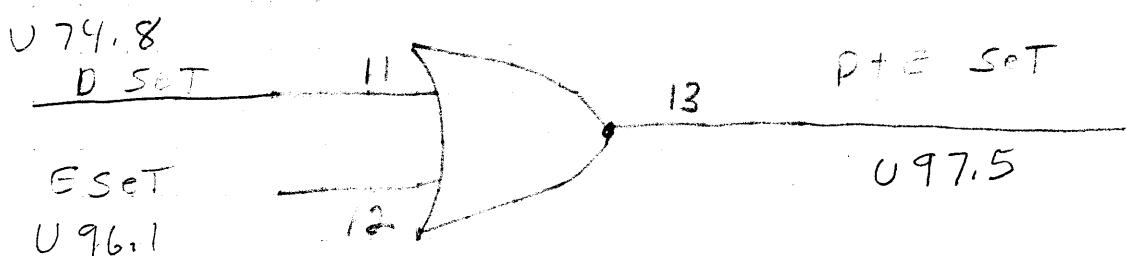
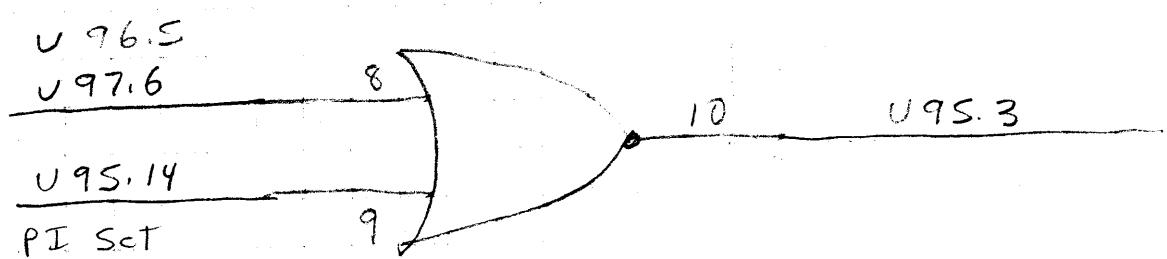
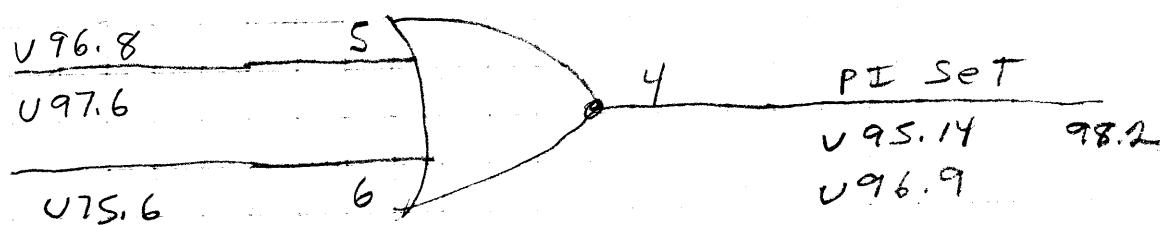


14.13

76.4

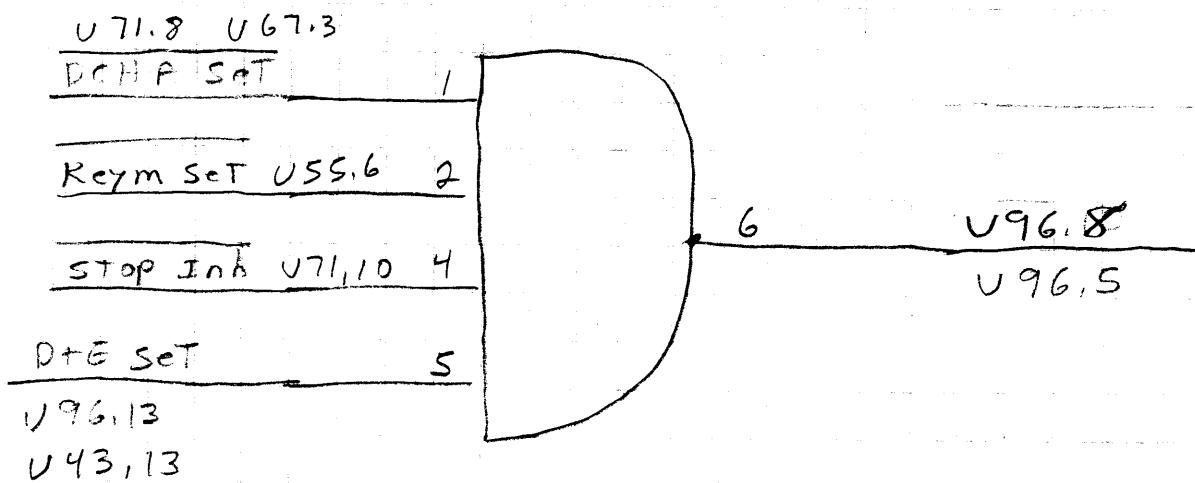
14.11

2

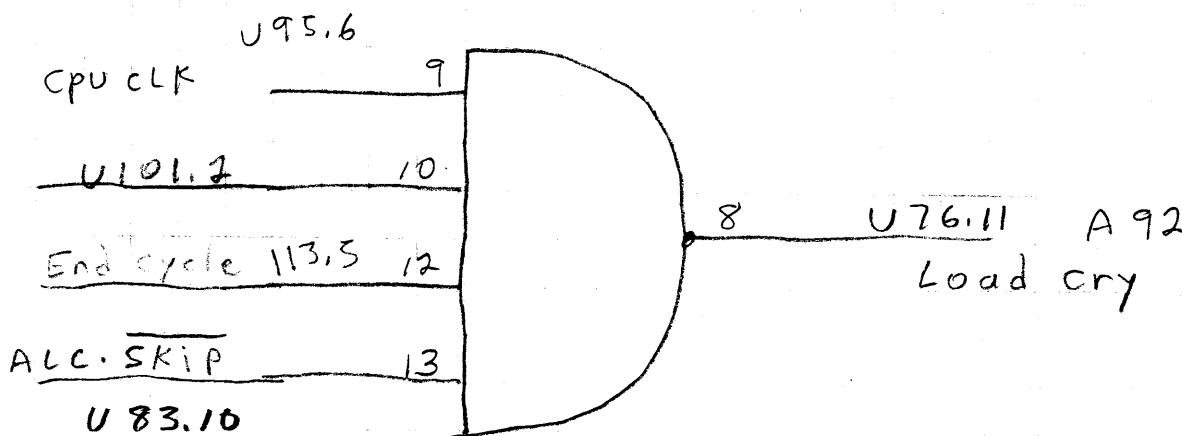


DG 1200 U97

9009 OK
7420



U4.
TR5
U78.
U75.3
U76.11
U65.3
PI
U70
U70
PTG2



U9
CLR
U79

U70
PTG
U41.
Key

ACB
U107

OK

DG 1200 U98

9008
741454 OK

U45.2

U4.1 U4.8

Key Loop 13

TRS

U28.7

U25.3 U25.13

U26.11 U46.9

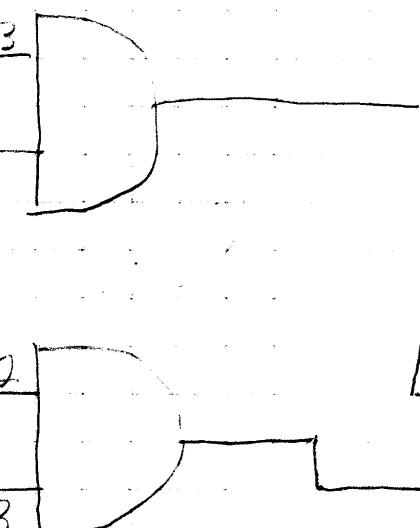
U65.3

PI Set

U96.4

PTGS

U70.10



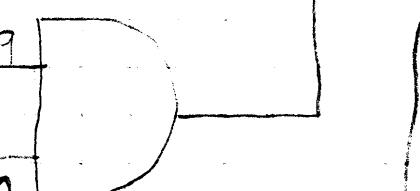
U70.4

PTG2. Loop 9

U99.8

CLR SKIP 10

U79.11

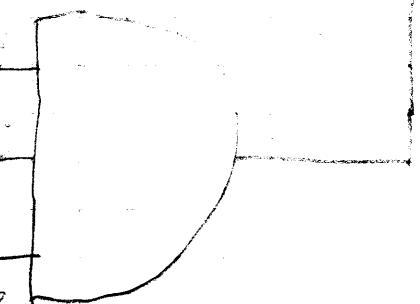


U70.10

PTGS

U41.10

Keym. PL



92

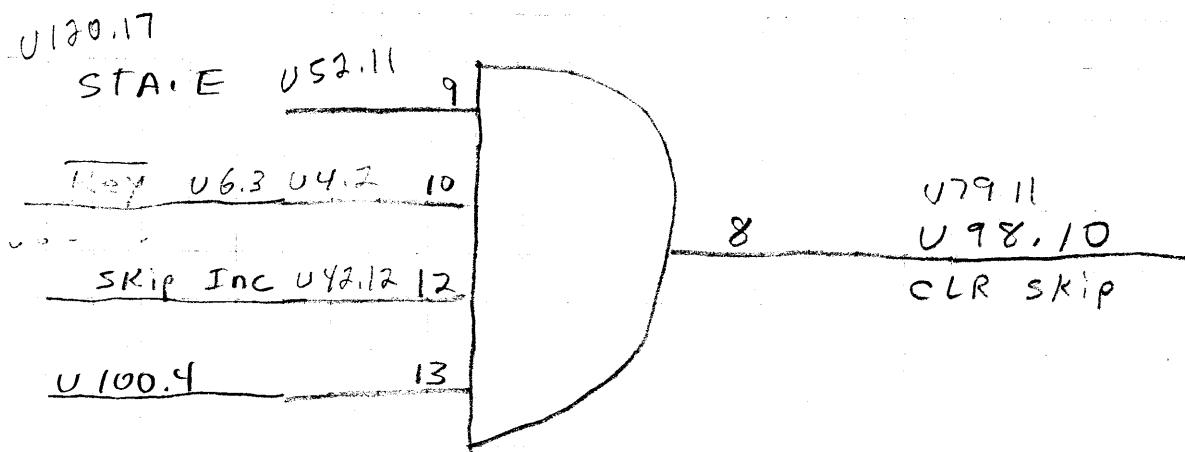
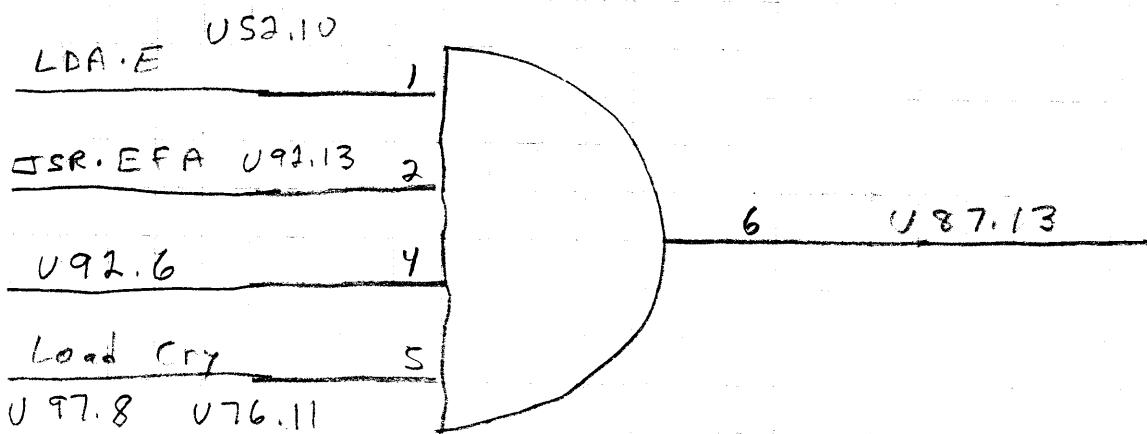
Load
MBO

8

DG 1200 U99

MC 3026

74H21 0K



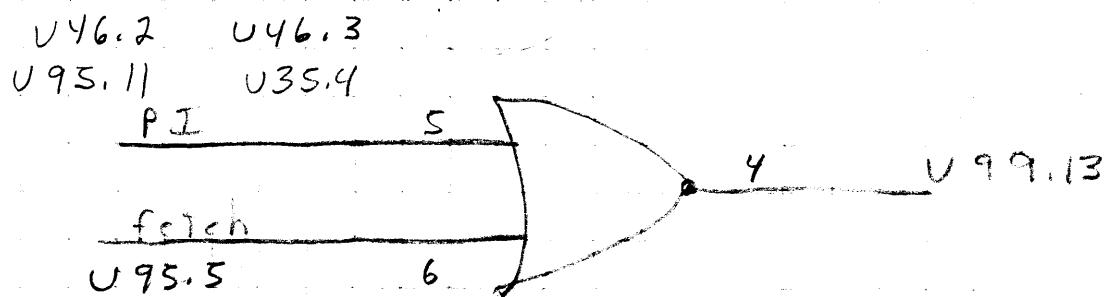
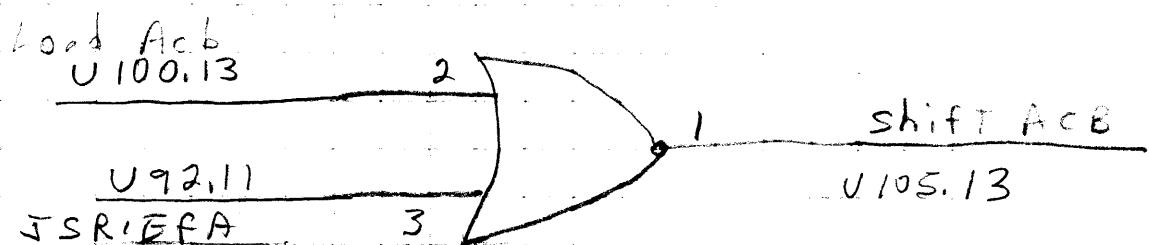
U6
U5
U7
U

DG 1200 U100

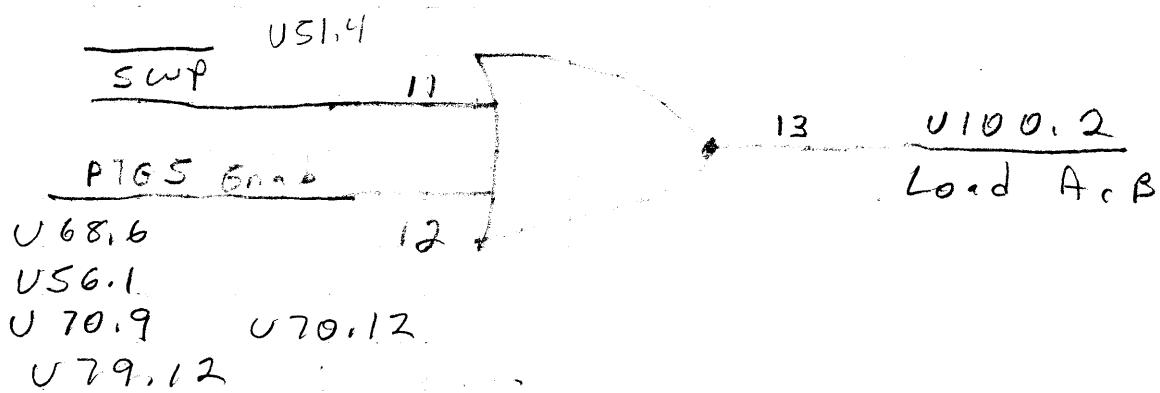
~~8885~~
7402

OK

OK

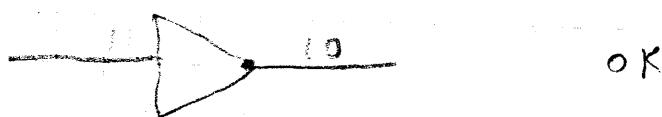
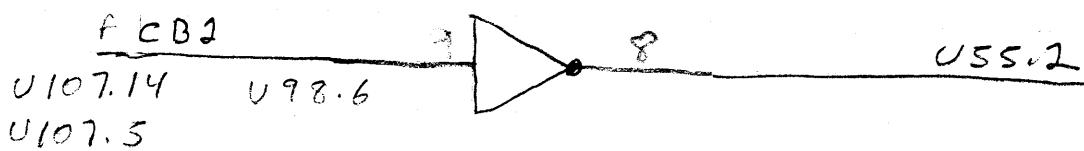
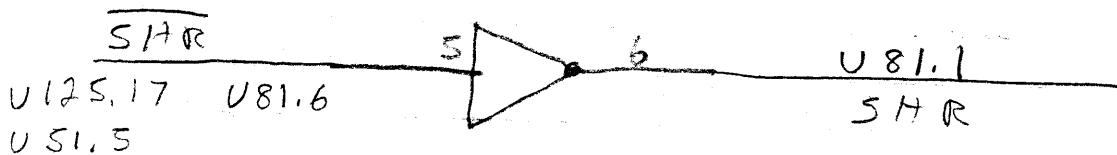
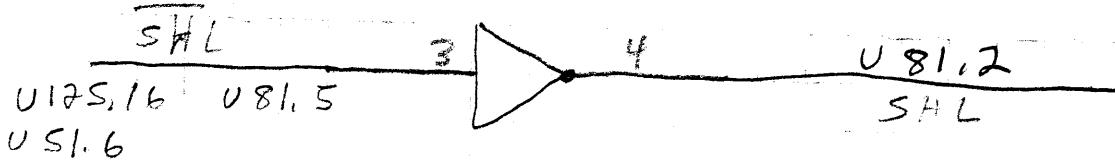
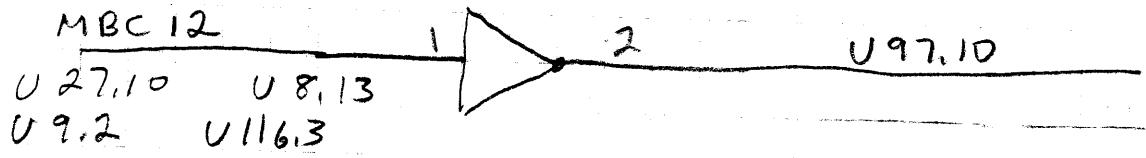


OK



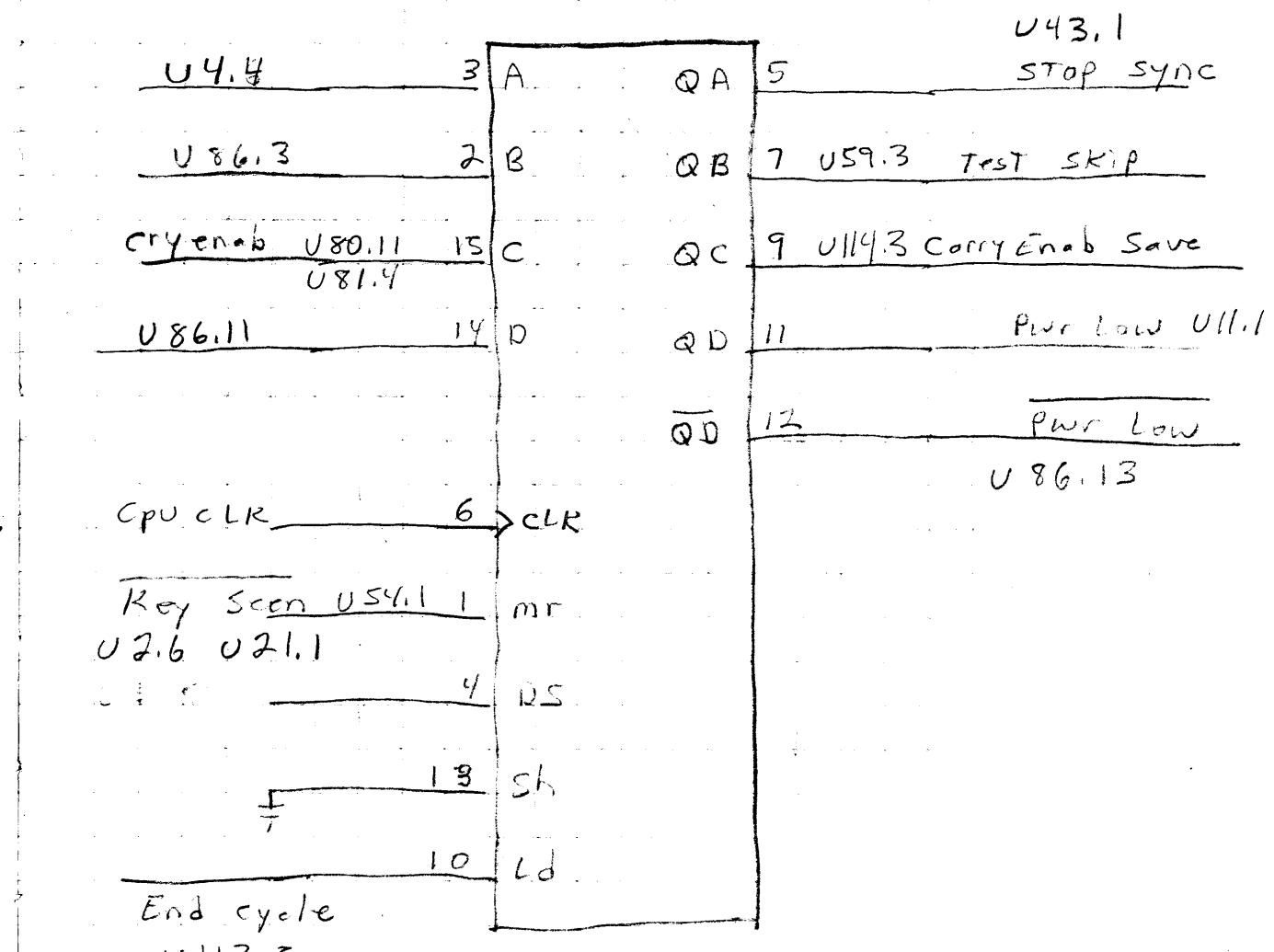
DG 1200 U101

8H90 OK



ok.

PG 1200 0102 8271 ok



DG 1200 U103

8271 OK

U100.1 U92.11

JSR-EFA

3

A

QA

5

U48.10 U109.12

was JSR

U83.2 Loop Set

2

B

QB

7

U22.5 Loop

U87.11

15

C

QC

9

U83.13 Pack

U85.13

14

D

QD

11

U93.13 EFA

CPU CLK

6 CLK

Reset

1 mr

4 DS

13 sh

End cycle

10 Ld.

QD

12

EFA

U34.5 U44.1

U50.3

EFA U32.13

U33.13 U44.9

U45.10 U46.4

U47.3 U47.4

U74.4 U93.13

U7

U10

PCH

U

U8C

ISZ

PTG

U70

DCHR

PCHL

U104.1

U7

PTG2

U58.3

ADD

DEFL

U104.

OK

D G 1200 U104

9008 OK
74H54

U75,10 U15,9
U104,10 U18,13

PCH Loop^{enab} 13

U34,13

U84,8
ISZ+DSZ.E 2

PTG2·Loop

U70,4 3

U83,1

Loop set

8

DCHR Pend 9

PCH Loop^{enab}

U104,13 10

U70,4

PTG2·Loop 4

V58,3
ADDER TEST 5

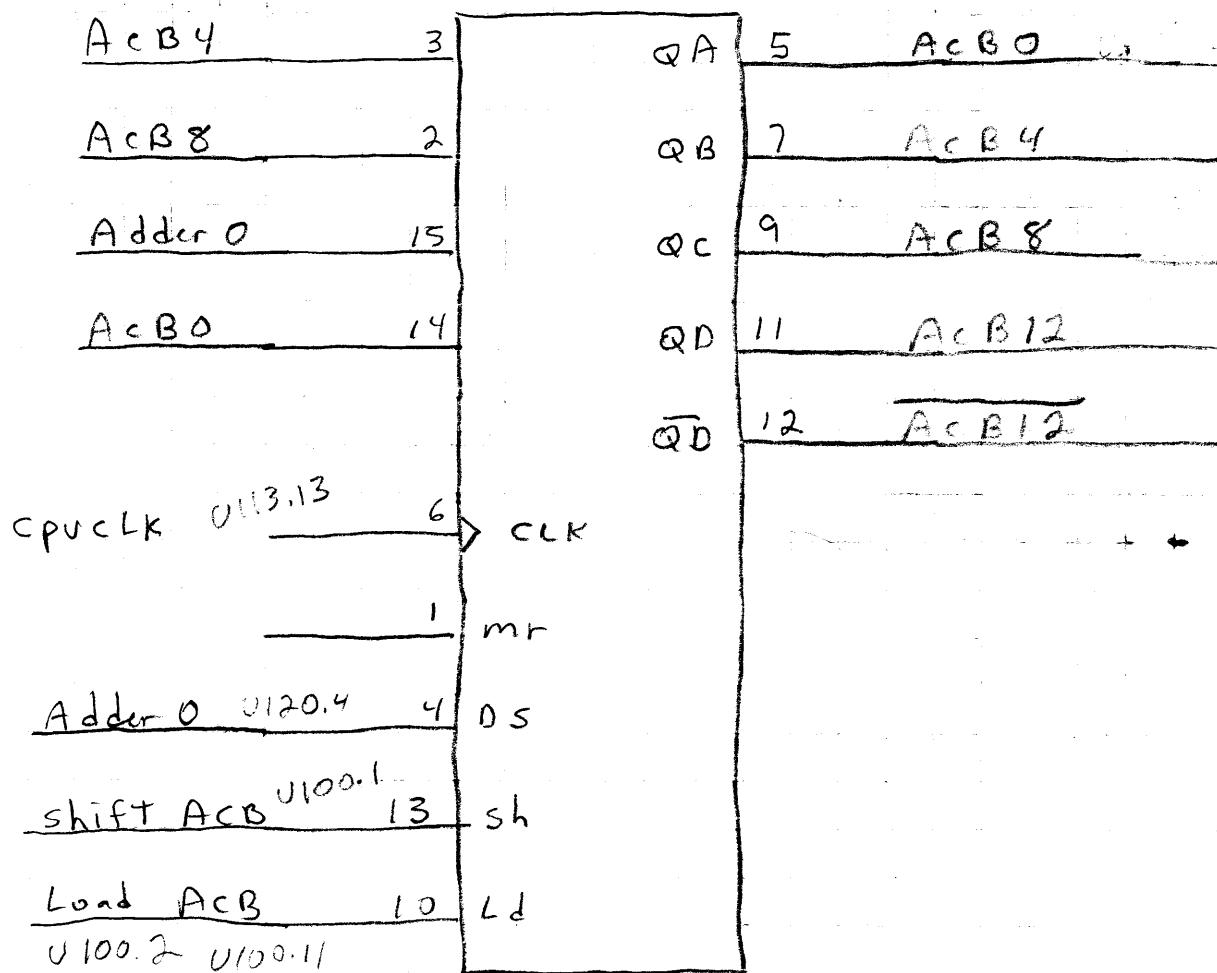
DEFER

U104,6

6

DG 1200 U105

8271 OK



OK

DG 1200 U106 8271 OK

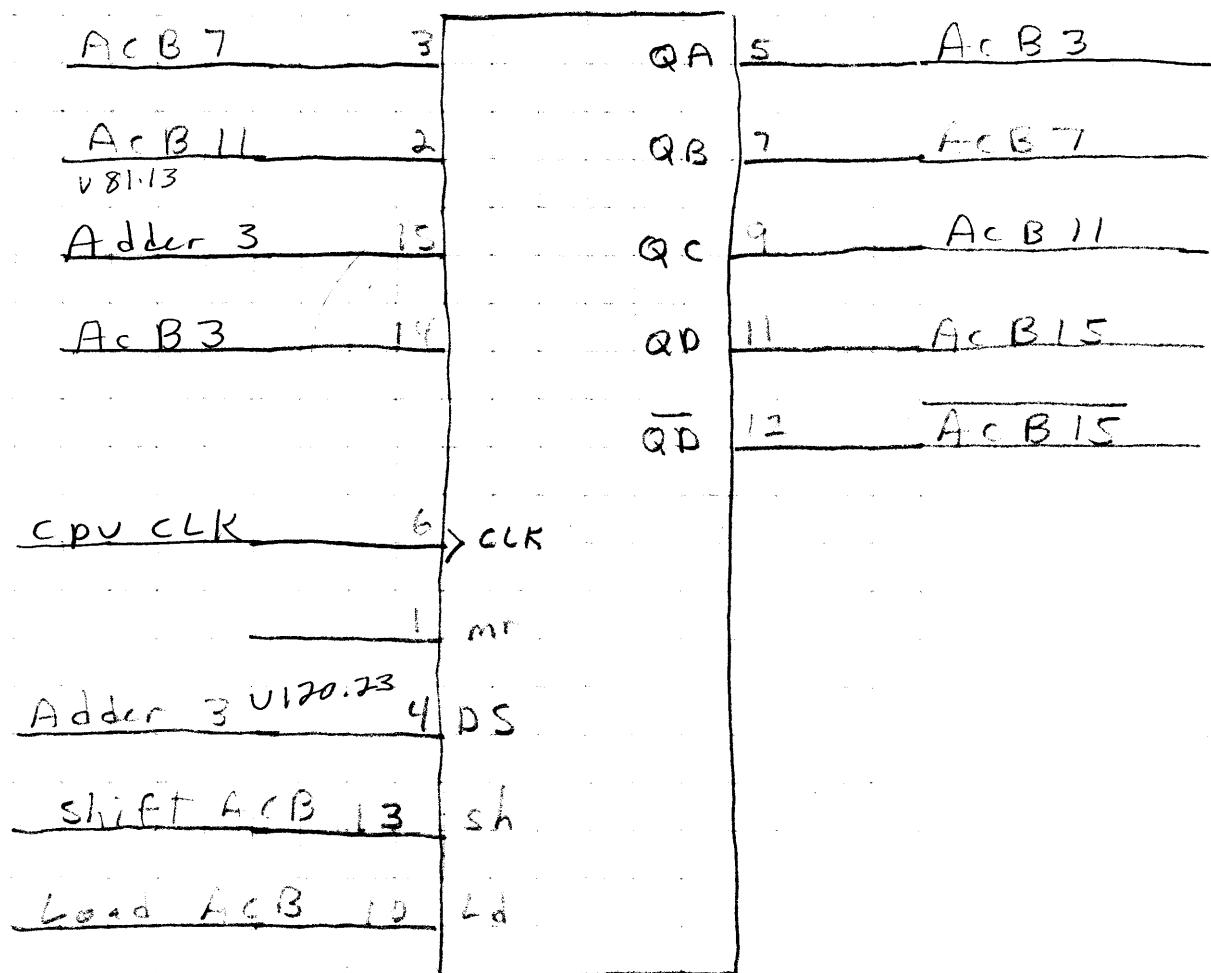
<u>ACB 5</u>	3	A	QA	5	F.c B !
<u>ACB 9</u>	2	B	QB	7	<u>ACB 5</u>
<u>Adder 1</u>	15	C	QC	9	<u>ACB 9</u>
<u>ACB 1</u>	14	D	QD	11	<u>ACB 13</u>
			QD	12	<u>ACB 13</u>
<u>Cpu CLK</u>	6	→	CLK		
	1	→	mr		
<u>Adder 1</u>	U120.1	4	DS		
<u>shift ACB 13</u>		sh			
<u>Load FrB 10</u>		Ld			

DG 1200 U107 8271 OK

<u>AcB6</u>	3	A	QA	5	<u>AcB2</u>
<u>AcB10</u>	2	B	QB	7	<u>AcB6</u>
<u>Adder 2</u>	15	C	QC	9	<u>AcB10</u>
<u>AcB2</u>	14	D	QD	11	<u>AcB14</u>
			\overline{QD}	12	<u>AcB14</u>
CPUCLK	6	CLK			
	1	mr			
<u>Adder 2 U120.23</u>	4	DS			
<u>Shift ACB</u>	13	sh			
<u>Load ACB</u>	10	Ld			

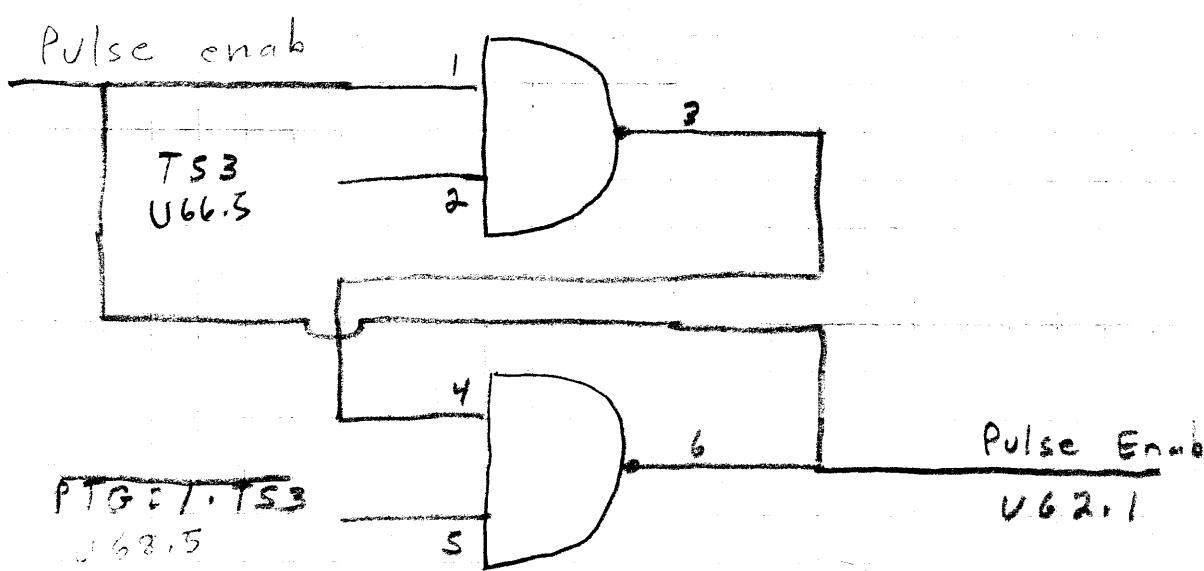
OK

DG 1200 U108 8271 OK



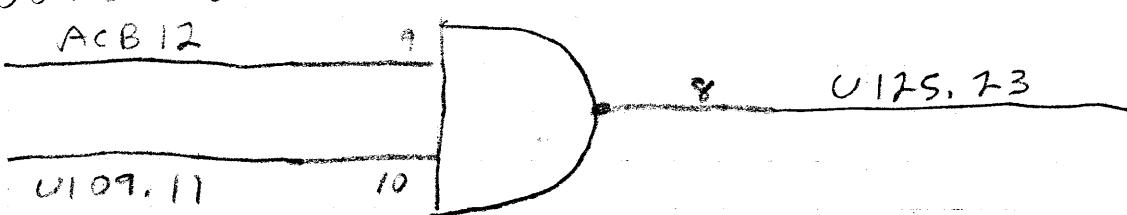
DG 1200 U109

9002 OK
7400



U69.3 U105.11

ACB 12

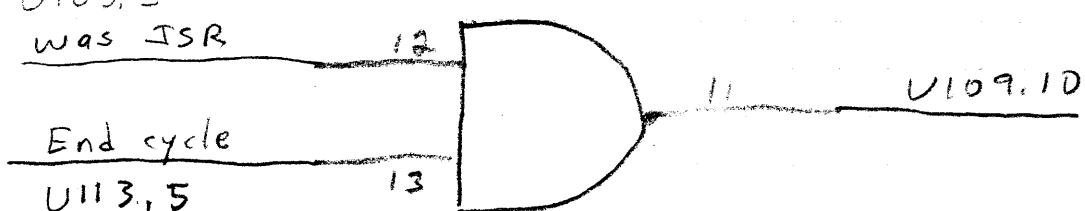


U103.5

was ISR

End cycle

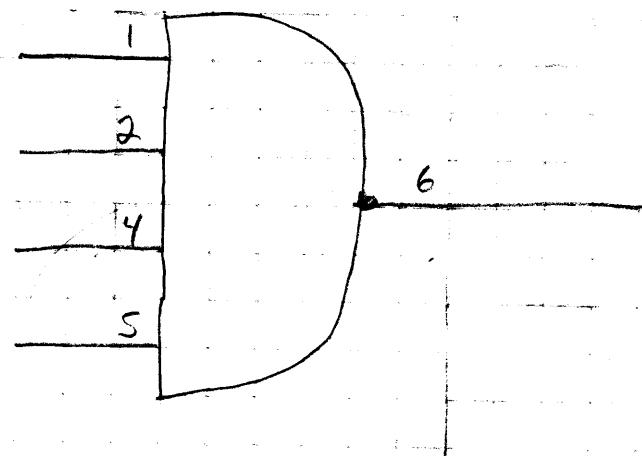
U113.5



OK

DG 1200 U110 9009 OK

7420
7440



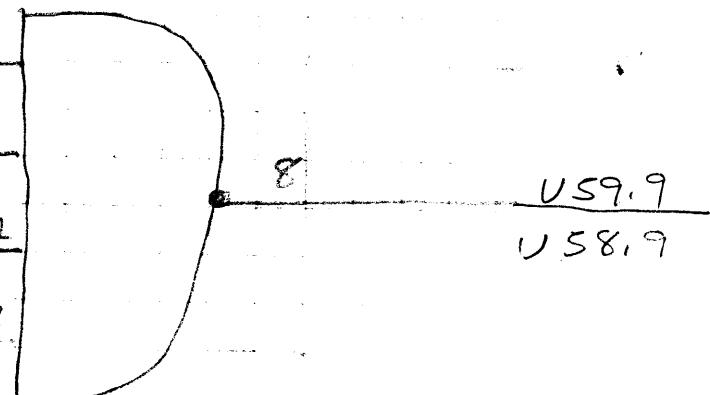
OK

shift 3 0125.10 q

shift 1 0125.14 10

shift 0 0125.13 12

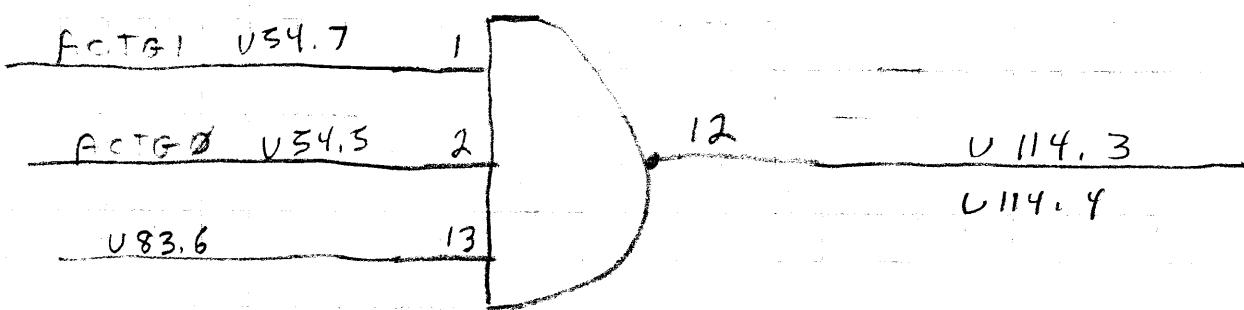
shift 2 0125.11 13



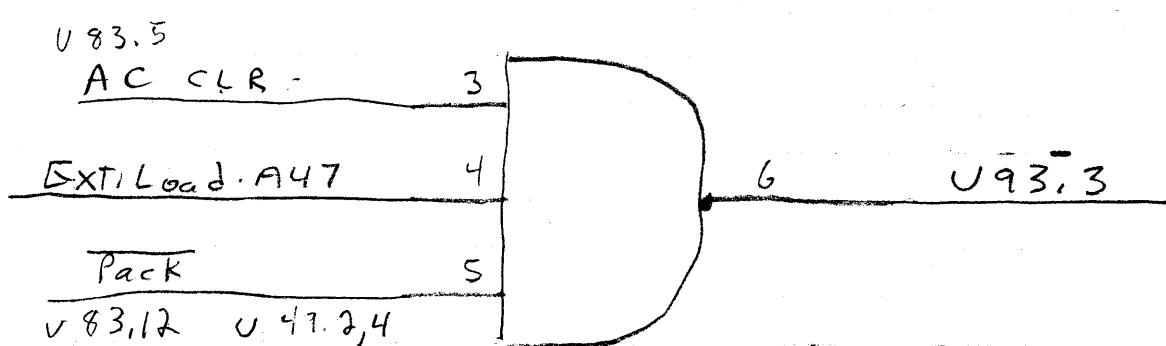
DG 1200 ULLI 1

9003 OK
7410

U 66.8

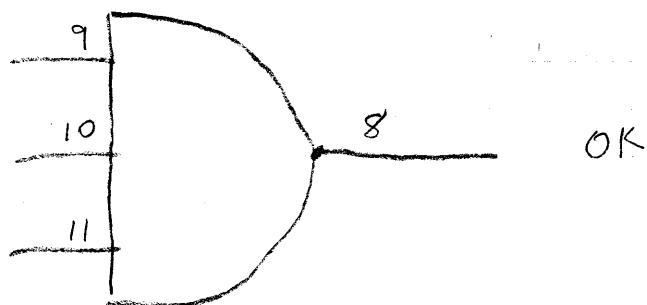


U 69
U 68.1



U 69
U 34
U 6

U 66
U 7



End
U 11
U 1

OK

DG 1200 U112

9005
7450 OK

U66.8 U12.10 U25.15

INPUT 112.9

PTG Ø

U69.9 U68.2 13

U68.14 U69.14

INPUT 112.1 9

PTG 1

U69.11 10

U34.6 U113.3

U68.3 U68.13

TS3 SET

U66.11

U9.8

2

3

6

U113.11

End cycle

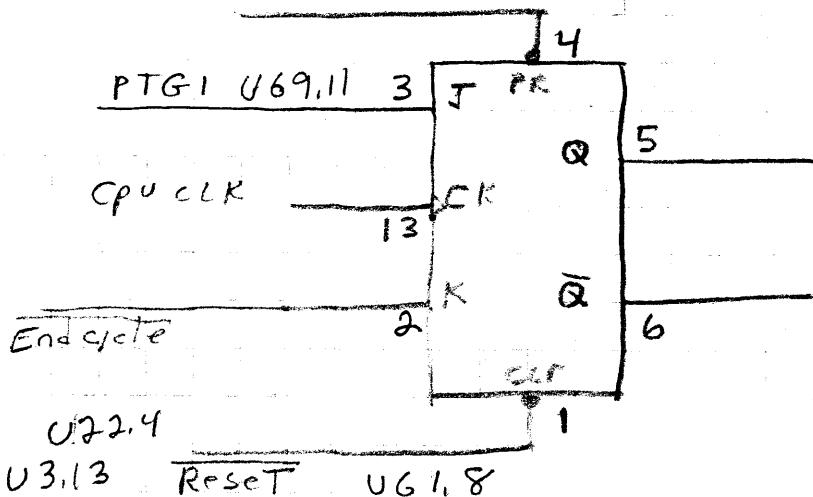
U113.6

U114.9

4

5

DG 1200 U113 MC3061 OK
74.11.4



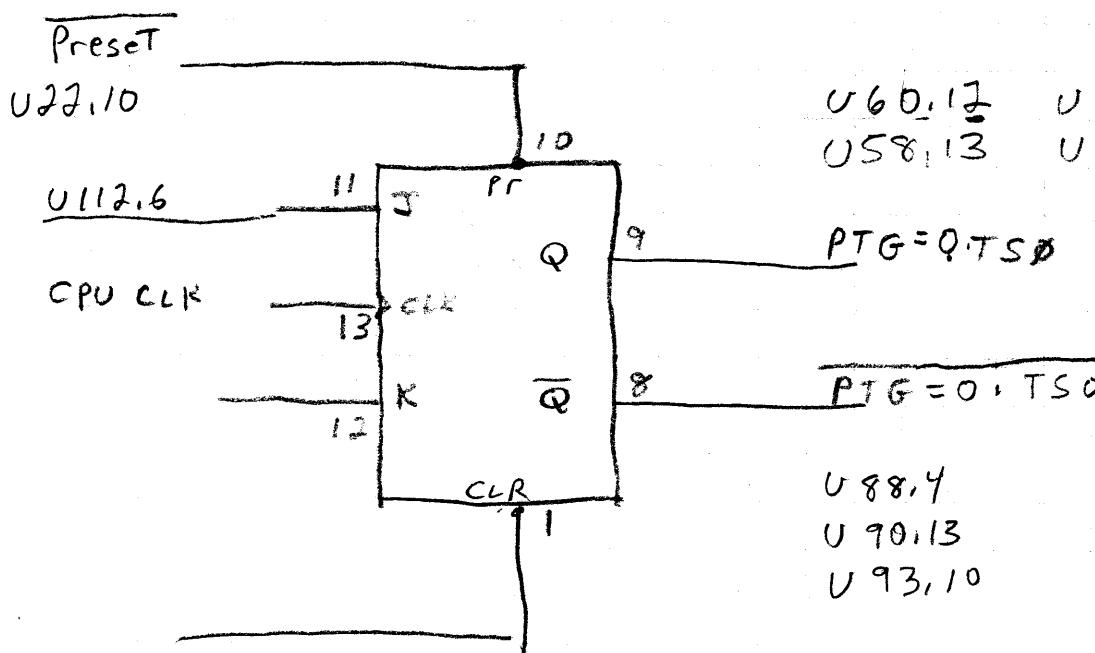
U114.1 U97.12
U102.10
End cycle

U1
End

Cry
U100

End

Ac
U10



U60.12 U90.9
U58.13 U88.9

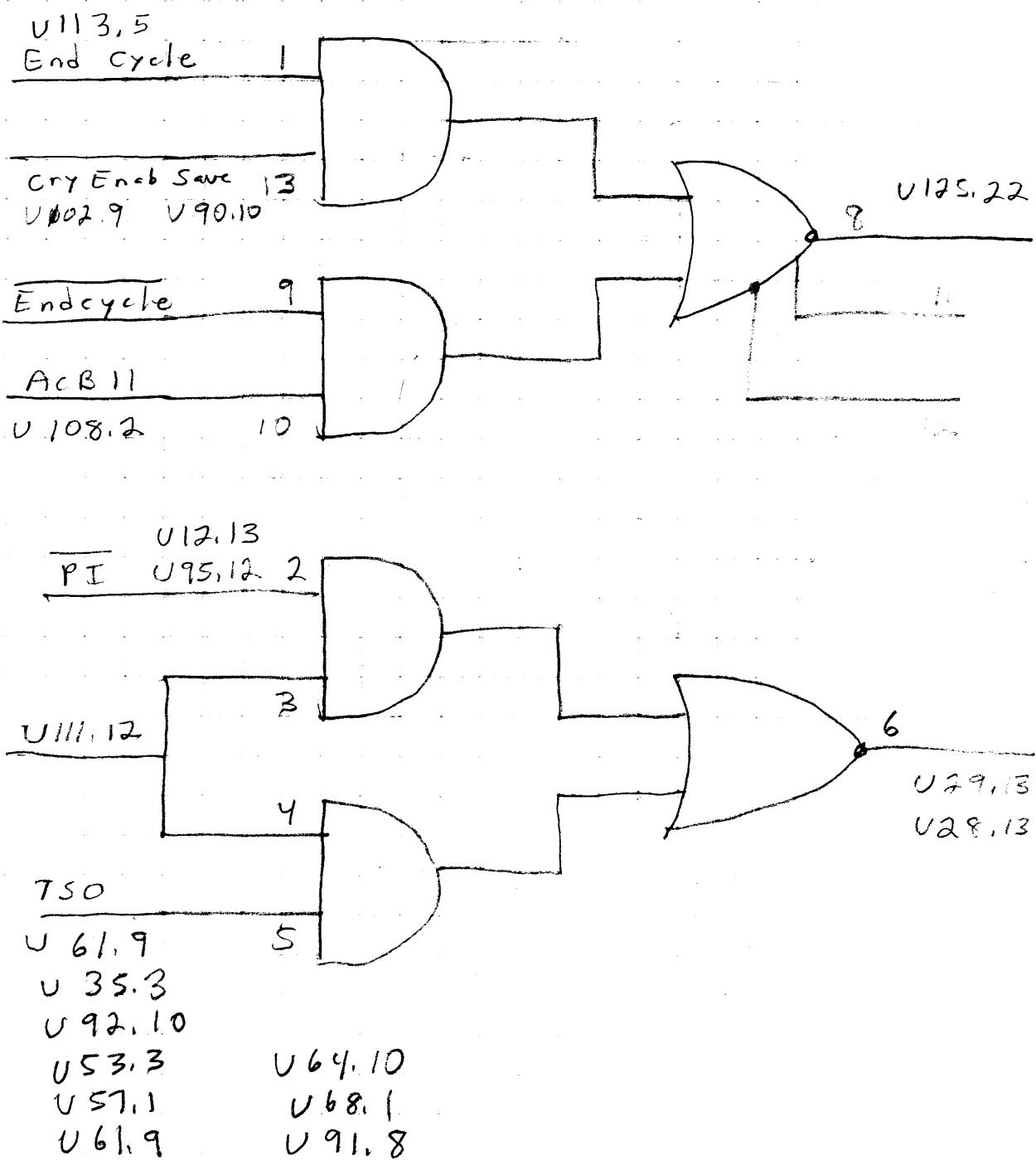
U111

TS
U6
U
U
U
U
U

OK

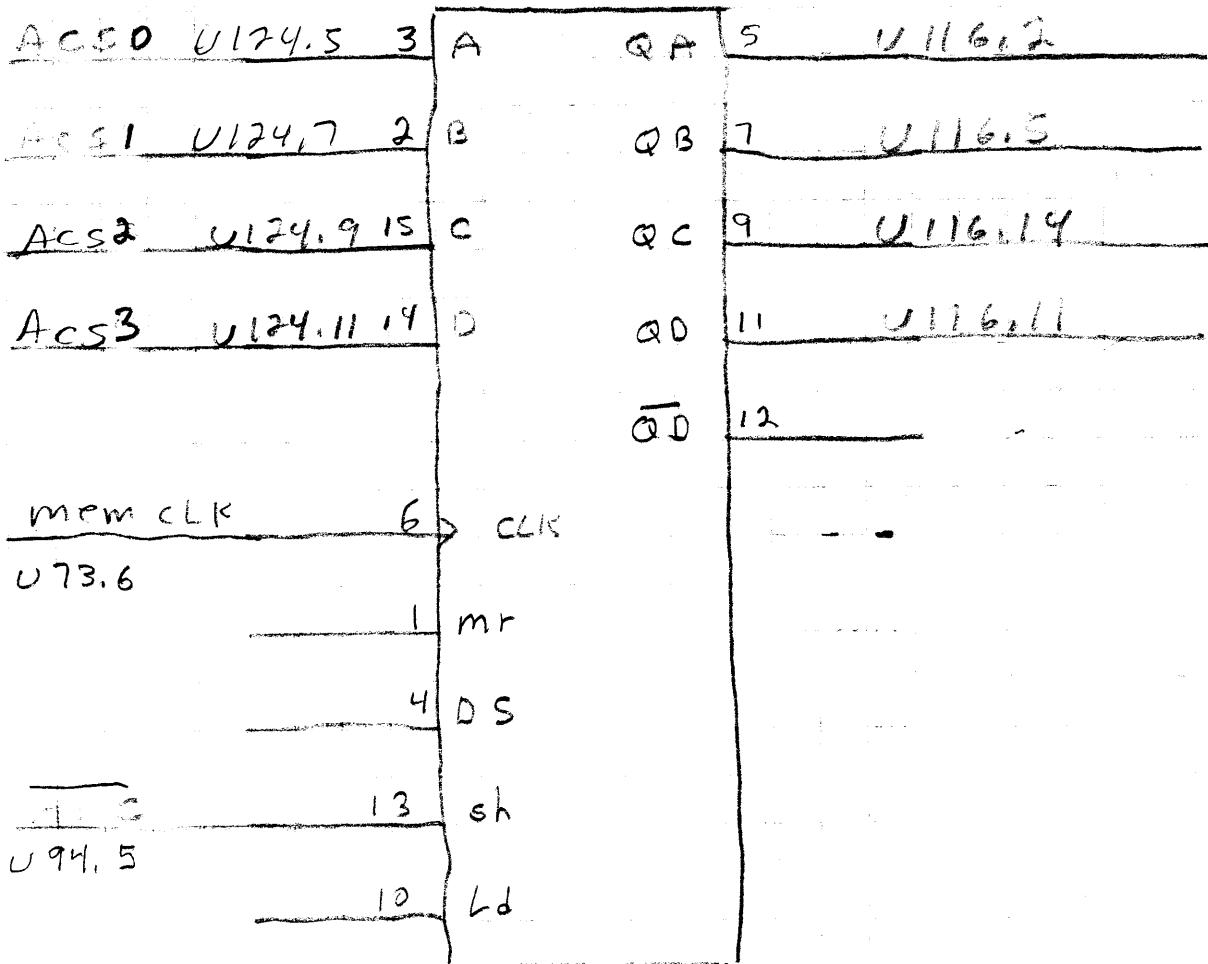
DG 1200 U114 9005 OK
7430

197.12



DG 1200 U115

8271 OK



1 OK

DG 1200 U116

9322
74157 OK

MBC 12 3
U27.10 U8.13
U9.1 U77.1
MBC 13 6
U27.4 U22.9
MBC 15 10
U8.1 U10.2
U32.12 14
MBC 14 13
U33.12 U8.3
EFA PTG 1 1
U32.4 U34.4
I 15

2a

4

U117.18

2b

7

U117.20

2c

9

U117.22

2d

12

U117.1

DG 1200 U117 74181 OK

<u>U121.9</u>	2	A0	F0	9	Adder 3 U120.20
<u>U121.12</u>	23	A1	F1	10	Adder 2 U120.23
<u>U121.7</u>	21	A2	F2	11	Adder 1 U120.1
<u>U121.4</u>	19	A3	F3	13	Adder 0 U120.4
<u>U116.9</u>	1	B0	cin	7	Add one U88.8
<u>U116.15</u>	22	B1			
<u>U116.7</u>	20	B2	Cn+4	16	U54.14 U91.3 cryout
<u>U116.4</u>	18	B3	A=B	14	
CO U92.3	6	SD		8.	AND U65.6 U91.2 U91.5
S1 U91.12	5	S1		17	
S2 U91.13	4	S2		15	
SO U92.3	3	S3			

OK

DG 1.2.00 U11.8

9002
7400 OK

3
U120.20

2
U120.23

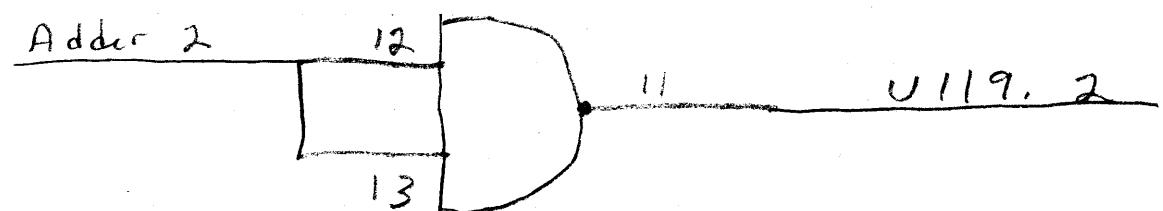
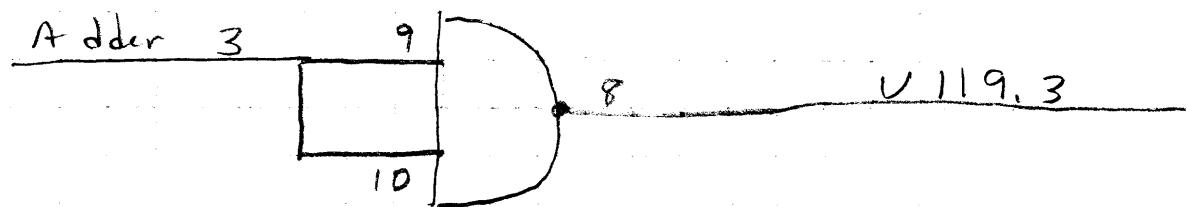
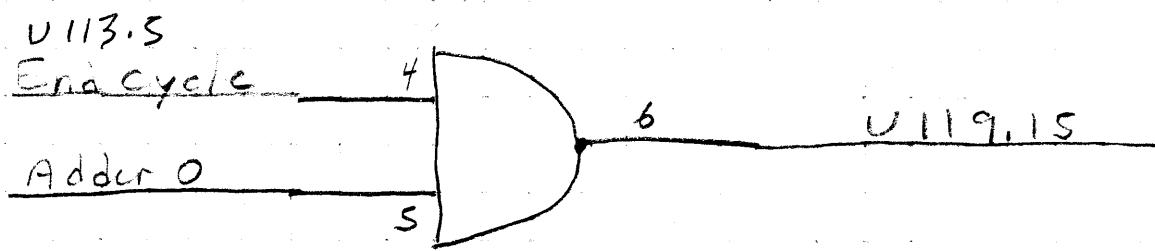
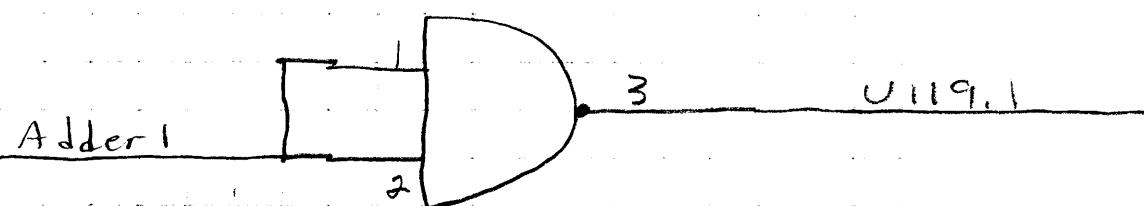
1
U120.1

0

4

8

U91.5



DG 1200 U119 74170 OK

<u>U118.6</u>	15	D1	Q1	10	<u>MULT 0</u>	<u>U120.10</u>
<u>U118.3</u>	1	D2	Q2	9	<u>MULT 1</u>	<u>U120.11</u>
<u>U118.11</u>	2	D3	Q3	7	<u>MULT 2</u>	<u>U120.13</u>
<u>U118.8</u>	3	D4	Q4	6	<u>MULT 3</u>	<u>U120.14</u>
<u>PTG1</u>	<u>U69.11</u>	14	wa	ra	5	<u>PTG1</u>
<u>PTG2</u>	<u>U69.9</u>	13	wb	Rb	4	<u>PTG2</u>
<u>PC Load</u>	<u>U57.8</u>	12	<u>EW</u>	<u>Er</u>	11	<u>PC IN</u>
						<u>U120.7,8,9</u>
						<u>U3613</u>

U117.

U117.1

U117.10

U117.9

U118.1

U122.3

U122.2

U122.15

U122.14

N

M

OK

DG 1200 U120

8264 OK

U117.13 U118.5

Adder 0

4

A0

f0

10

mult 0

U42.4

U120.10

U117.11 Adder 1 U118.12

A1

f1

11

mult 1

U39.4

U120.11

U117.10 Adder 2 U118.13

A2

f2

13

mult 2

U37.4

U120.13

U117.9 Adder 3 U118.9,10

A3

f3

14

mult 3

U38.4

U120.14

U122.3 ACD 0

B0

U122.2 ACD 1

B1

Comp

15

X

U69.9

U122.15 ACD 2

B2

U122.14 ACD 3

B3

s0

17

STA.E

8,9

MBO 12 U40.11

C0

OE0

7

MBO 13 U39.11

C1

OE1

8

PC IN

8,9

MBO 14 U37.11

C2

OE2

9

U119.11

MBO 15 U38.11

C3

U36.3

DG 1200 U121 OK 9322
74157

<u>U122.5</u>	2	
<u>MBO 12</u>	<u>U120.6</u>	3
<u>U122.7</u>	5	
<u>MBO 13</u>	<u>U120.3</u>	6
<u>U122.11</u>	11	
<u>MBO 15</u>	<u>U120.18</u>	10
<u>U122.9</u>	14	
<u>MBO 14</u>	<u>U120.2</u>	13
<u>FCP OUT</u>	<u>U45.6</u>	1
<u>Disable</u>	15	
<u>DMULT</u>	<u>US3.7</u>	

U120.5
A

U120.2

U120.22

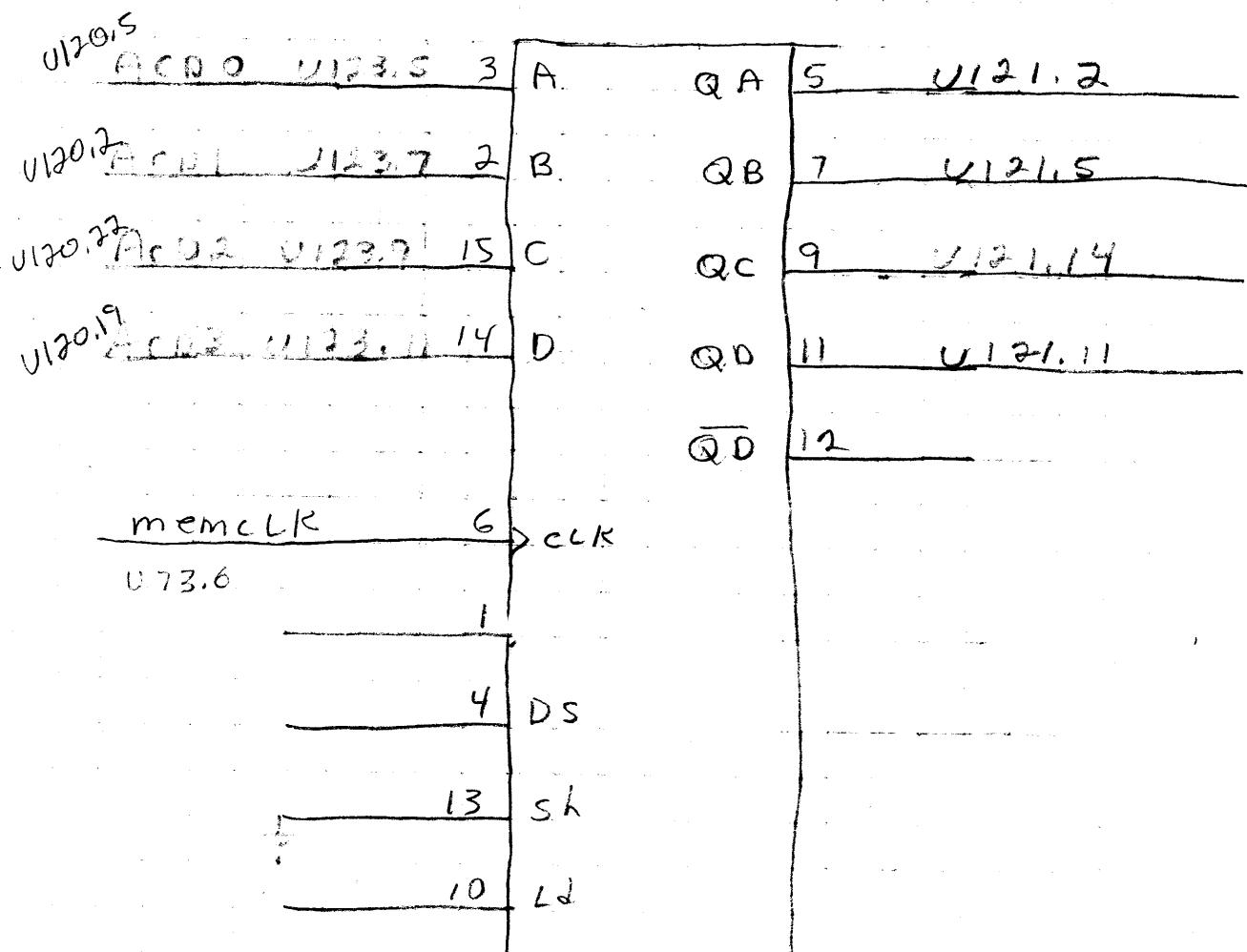
U120.19

m

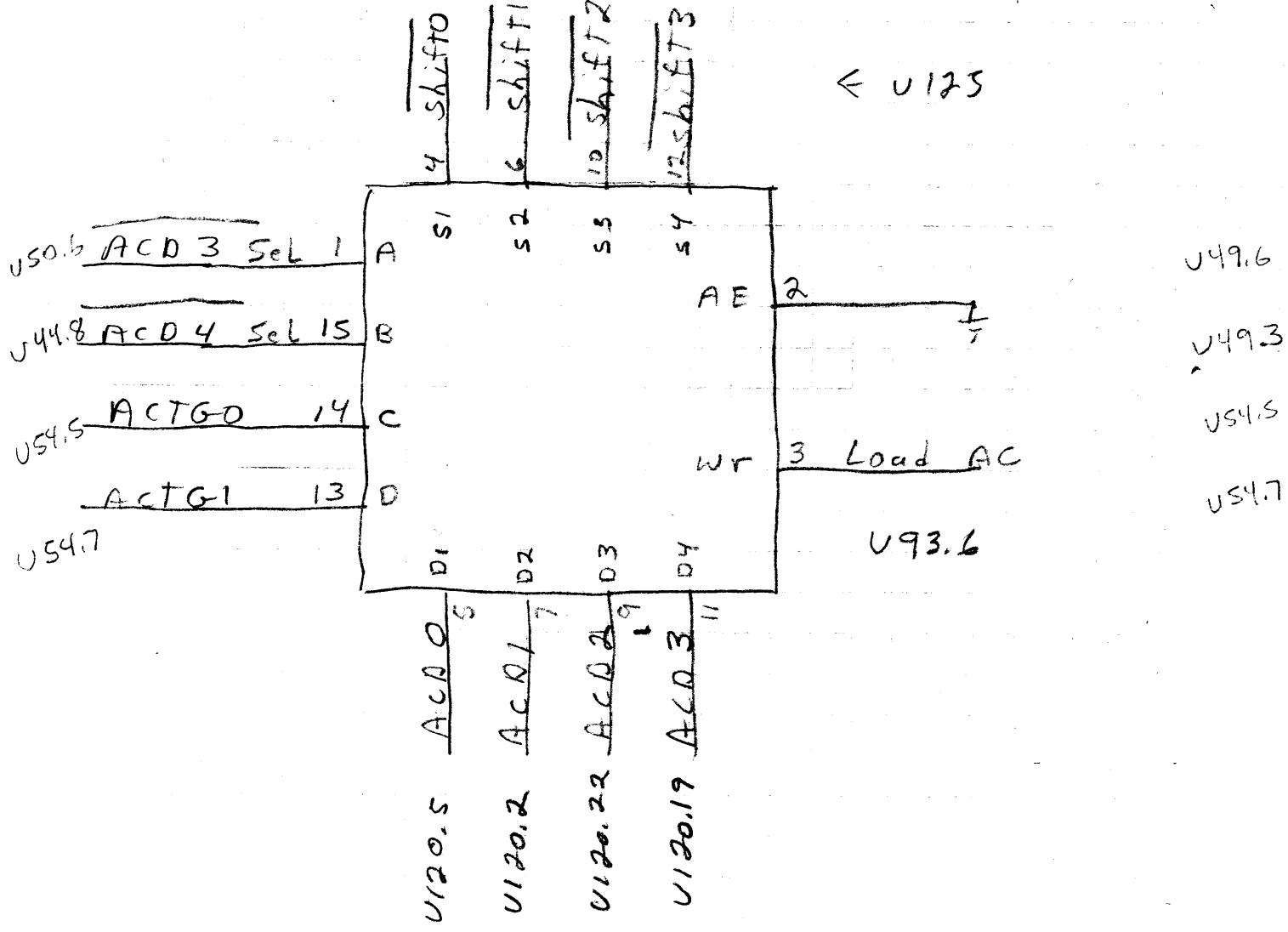
U

DG 1200 U122

8271 OK



DG 1,200 U123 3101 ok



Shift 0 U124.4 U125.13

1 U124.6 U125.14

2 U124.10 U125.11

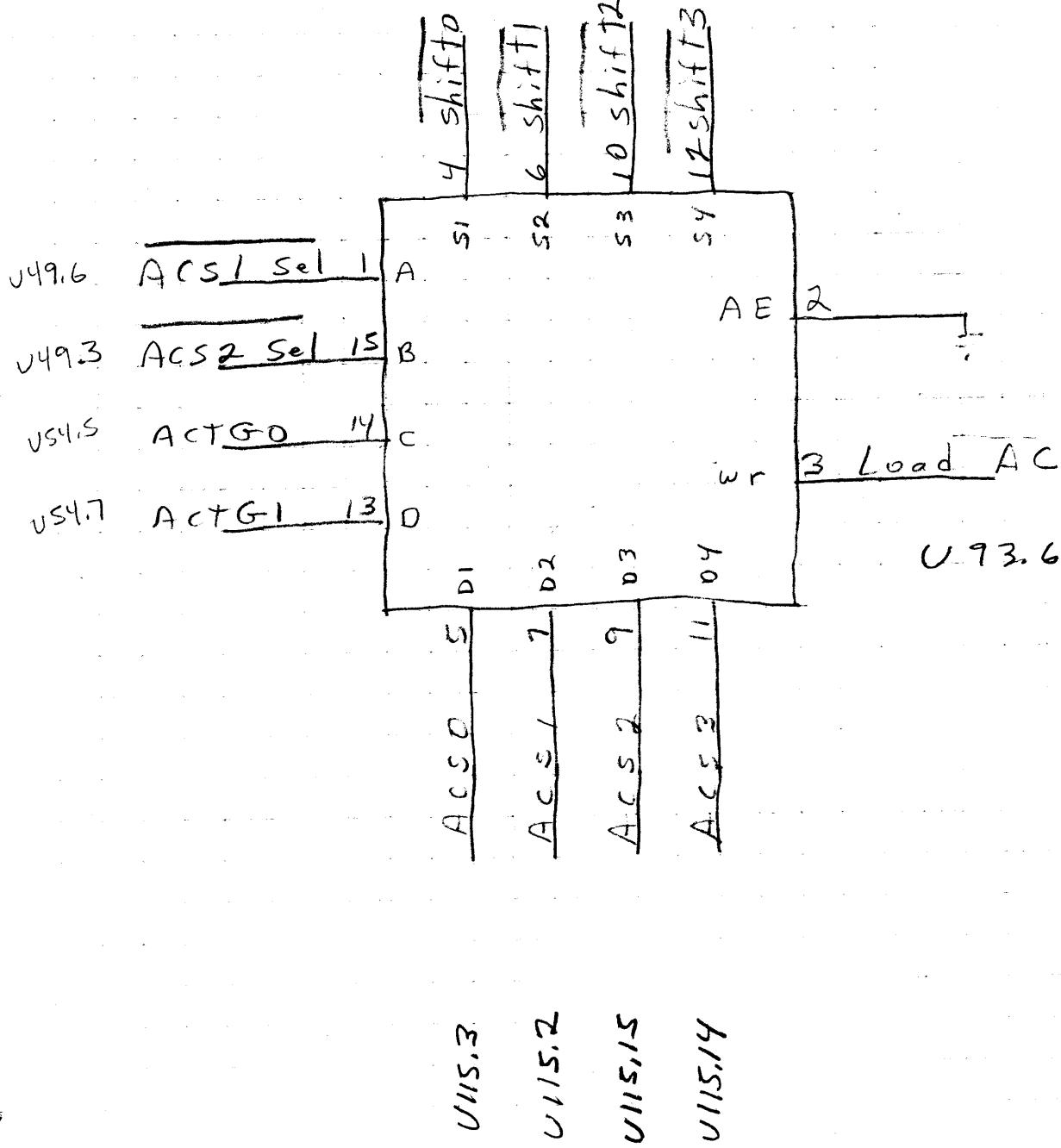
3 U124.12 U125.10

OK

D G 1200

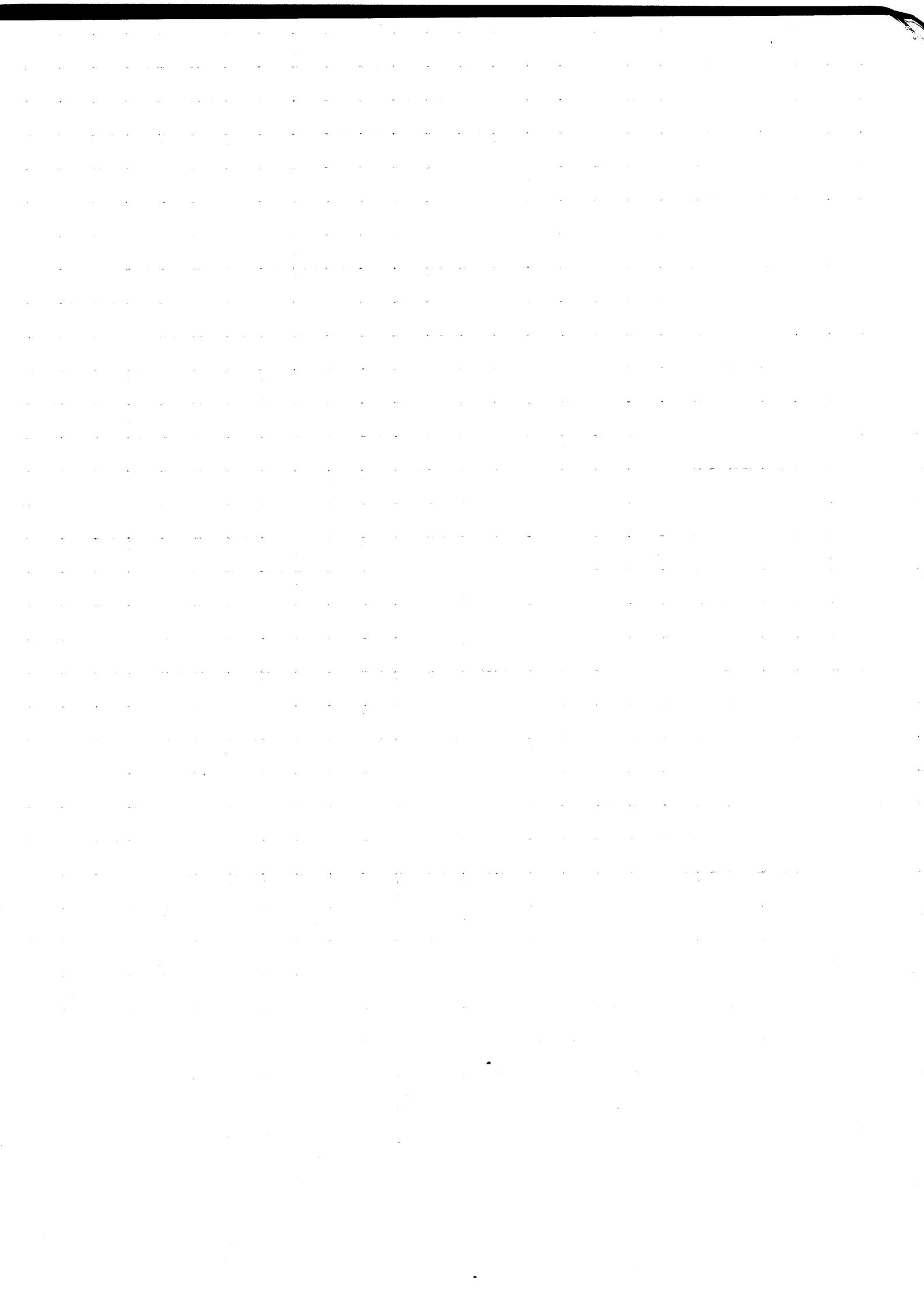
C 124

3101 OK



DG 1200 U125 OK 8264

<u>V108.12</u>						
<u>ACB15</u>	4	A0	F0	10	<u>shift 3</u>	B91
<u>ACB14</u>	1	A1	F1	11	<u>shift 2</u>	B93
<u>V109.8</u>	23	A2	F2	13	<u>shift 0</u>	B94
<u>ACB13</u>	20	A3	F3	14	<u>shift 1</u>	B96
<u>ACB14</u>	5	B0	-			
<u>ACB13</u>	2	B1	Comp	15	±	
<u>V114.8</u>	22	B2				
<u>ACB12</u>	19	B3		17	<u>SHR</u>	V101.6
V105.12				18	<u>SHL</u>	V101.4
<u>V90.8</u>	6	C0				
<u>ACB15</u>	3	C1	OEO	7	<u>Power OK</u>	V3.10
<u>ACB13</u>	21	C2	OEI	8	<u>EXT Load</u>	B49
<u>ACB14</u>	18	C3	OEZ	9	<u>EXT Load</u>	B49
<u>V107.12</u>						



✓ MTG Ø U17.5, U13.8 U14.13
U16.13 U17.2, 14, 15
U19.1 U19.4

✓ MTG Ø U16.12 U36.4

✓ MTG 1 U17.7 U16.5 U16.11
U19.10

✓ MTG 1 U16.10 U19.5 U18.10

✓ MTG 2 U17.9 U16.9
U18.5

✓ MTG 2 U16.8 U13.9 U10.4

✓ MTG 3 U17.11 U18.9 U36.5

✓ MTG 3 U17.12 U17.4
U18.1, 2, 9 U19.2, 9

✓ MBC 9 U79.8 U80.1

✓ MBC 9 U32.5 U51.2 U63.2
U63.14 U79.9 U79.10

✓ MBC 8 U27.2 U11.5 U47.5

✓ MBC 8 U33.5 U11.9 U27.1 U33.4
U51.3 U63.3 U63.13

- ✓ MBC 1.5 U32.12 U8.1
U10.2 U116.10
- ✓ MBC 15 U32.11 U80.4
- ✓ MBC 14 U33.12 U8.3
U10.1 U77.10 U116.13
- ✓ MBC 14 U33.11
- ✓ MBC 13 U27.4 U22.9
U9.1 U77.1 U116.6
- ✓ MBC 13 U32.7 U27.3
- ✓ MBC 12 U27.10 U8.13
U9.2 U101.1 U116.3
- ✓ MBC 12 U33.7 U27.11
- ✓ MBC 11 U27.12 U8.11
U9.4 U77.5
- ✓ MBC 11 U32.9 U27.13
- ✓ MBC 10 U27.8 U9.5
U8.9
- ✓ MBC 10 U33.9 U27.9 U77.2

B71✓	MEMO	U40.3	U28.3	✓	B79
B70✓	MEM1	U39.3	U29.2	✓	B77
B71✓	MEM2	U37.3	U29.15	✓	B44
B68✓	MEM3	U38.3	U29.14	✓	B43
B28✓	MEM4	U40.2	U29.3	✓	B42
B66✓	MEM5	U39.2	U28.2	✓	B32
B22✓	MEM6	U37.2	U28.15	✓	B16
B24✓	MEM7	U38.2	U28.14	✓	B14
A55✓	MEM8	U40.15	U33.3	✓	B12
A53✓	MEM9	U39.15	U32.3	✓	B9
A45✓	MEM10	U37.15	33.15	✓	B8
A51✓	MEM11	U38.15	U32.15	✓	B5
A56✓	MEM12	U40.14	33.2	✓	A39
A55✓	MEM13	U39.14	U32.2	✓	A37
B76✓	MEM14	U37.14	U33.14	✓	B73
B18✓	MEM15	U38.14	U32.15	✓	A71

B79	MB0	0	V40.5	B79.9
B77✓	MB0	1	V39.5	B77.
B44✓	NB0	2	V37.5	B44
B43✓	MB0	3	V38.5	B43
B42✓	MB0	4	V40.7	B42
B32✓	MB0	5	V39.7	B32
B16✓	MB0	6	V37.7	B16
B14✓	MB0	7	V38.7	B14
B12✓	MB0	8	V40.9	V42.2 B12
B9✓	MB0	9	V39.9	B9
B8✓	MB0	10	V37.9	B8
B5✓	MB0	11	V38.9	B5
A39✓	MB0	12	V40.11 A39	V121.3 V57.12 V120.6
A37✓	MB0	13	V39.11 A37	V60.5 V121.6
B43✓	MB0	14	V37.11 A43	V60.4 V121.13
A41✓	MB0	15	V38.11 A41	V84.9 V120.10 V121.18
	MB0	12 Save	V42.7	V48.2 V90.5

✓ <u>I R O</u>	U 28.5	✓
✓ I R T	U 29.7	✓
✓ <u>I R 2</u>	U 29.9	✓
✓ <u>I R 3</u>	U 29.11	✓
✓ <u>I R 4</u>	U 29.5	✓
✓ <u>I R 5</u>	U 28.7	✓
✓ <u>I R 6</u>	U 28.9	✓
✓ <u>I R 7</u>	U 28.11	✓
✓ I R 7	U 28.12	✓
✓ I R 3	U 29.12	✓

continued on Next Pages

B7 <u>MEMO</u>	U 28.3	U 40.3	U 55.10	U 55.13	
	U 76.2				
B70 <u>MEMO</u>	U 29.2	U 39.3	U 55.9		B86
B47 <u>MEMO</u>	U 29.15	U 37.3	U 55.1		
B68 <u>mem 3</u>	U 29.14	U 38.3			

- ✓ MBC 8 U33.5
✓ MBC 9 U32.5
✓ MBC 10 U33.9
✓ MBC 11 U32.9
✓ MBC 12 U33.7
✓ MBC 13 U32.7
✓ MBC 14 U33.11
✓ MBC 15 U32.11
✓ MBC 14 U33.12
✓ MBC 15 U32.12

S.13 Continued on another page

B86 mb clear U19.6

✓ Key U4.2 U6.3 U23.4 U44.5 US6.4
U70.11 U84.12 U99.10 US6.9

✓ Key M U23.11 U24.3 U43.2 U41.3

✓ Keym U41.8 U41.3

Key U6.1 U34.8 U23.5 U55.5
U46.1 U67.5 U36.9 U43.9

✓ Key enab U3.3 U3.12 U6.2

✓ KeyLoop U4.1 U4.8 U45.2 U98.13

✓ D+E Set + U43.13 U96.13 U97.5

✓ D+E Set +TS3 U36.1F U13.3
-U24.13 U35.1

✓ STOP Inh U97.4 U71.10
U82.8 U87.2

✓ STOP Sync U102.5 U43.1

✓ PL U41.9 U43.3 U87.9 A19

FO, RST U10.8

56.4
5.9
1.3

✓ SKiP Inc U35.13 US8.5 US8.6

✓ PC enab U61.8 US7.5

✓ PCin U36.3 U119.11

✓ FRO U28.5 U43.10 U45.3
U50.13 U51.1 U53.5
U53.6 U92.4

✓ FR1 U29.7 U49.5 US1.13 US2.13

✓ FR2 U29.9 U24.2 U49.1 US1.14
US2.14

✓ FR3 U29.12 U48.9 U48.12

✓ FR3 U29.11 U12.12

Was ISR U103.5 U48.10 U109.12

Was ISR U48.8 A89

✓ IR4 U29.5 U26.13
U44.13 U49.13 U52.2 ✓

✓ IR4 U26.12 U93.1 ✓

✓ IR5 U28.7 U25.3 U25.13
U26.11 U46.9 U65.3
U98.1 ✓

✓ IRS U26.10 U74.5 U87.5 ✓

✓ IR6 U28.9 U25.2 U25.14
U26.9 U45.9 U46.6
U55.4 U65.2 ✓

✓ IR6 U26.8 U47.13 U91.12 ✓

✓ IR7 U28.11 U44.4 U44.10 ✓
U46.5 U71.5 U86.10

✓ IR7 U28.12 U9.13 U44.3 ✓
U64.13 U89.1

✓ Run U22.13 U23.7
U72.4 U72.10

✓ Run U22.12 U2.1 U2.2
A14 U72.10

✓ Restart U3.5 U82.10

✓ Reset U3.13 U10.13.1 U21.9
U22.4 UGL8 U113.1

✓ STOP U4.5 U4.6

✓ Con-data A28 U4.10

✓ Con Inst A22 U36.8

✓ Con RQ A27 U3.9

✓ Rst A30 U71.12

✓ Stop A31 U4.5 U4.6

✓ Restart Enable A32 U2.12

✓ MBC 8

U27.1 U11.9
U33.5 U33.4
U51.3 U63.3 U63.13

✓

✓ MBC 8

U27.2 U11.5 U47.5

✓

✓ MBC 9

U32.5 U51.2 U63.2
U63.14 U79.8 U79.9

✓

✓ MBC 9

U79.10 U80.1

✓

✓ MBC 10

U33.9 U27.9 U77.2

✓

✓ MBC 10

U27.8 U7.5 U8.9

✓

✓ MBC 11

U32.9 U27.13

✓

✓ MBC 11

U27.12 U8.11 U9.4
U77.5

✓

✓ MBC 12

U33.7 U27.11

✓

✓ MBC 12

U27.10 U8.13 U9.2
U101.1 U116.3

✓

P

- ✓ MBC 13 U32.7 U27.3
- ✓ MBC 13 U27.4 U27.9 U9.1
U77.1 U116.6
- ✓ MBC 14 U33.11
- ✓ MBC 14 U33.12 U8.3 U10.1
U77.10 U116.13
- ✓ MBC 15 U32.11 U 80.4
- ✓ MBC 15 U32.12 U8.1 U10.2
U116.10
- ✓ PC In U36.3 U119.11 U120.7,8,9
- ✓ PI U95.11 U35.4 U90.3 U100.5
U46.2 U46.3
- ✓ PI U95.12 U114.2 U12.13
U74.11 U82.13 U84.1 U84.12
- ✓ PI set U96.4 U95.14 U96.9 U98.2

- ✓ Key M, PL U 41.10 U 55.3 U 57.2
 U 93.9 U 98.5
- ✓ Key M, PL, TSO U 57.3 U 56.5 U 57.4
- ✓ Key M set U 55.6 U 22.1 U 97.2
- ✓ Key M Set U 22.2 U 23.14
- ✓ Key Seen U 2.6 U 21.1 U 54.1
 U 102.1
- ✓ Key Seen U 2.5 U 3.1 U 23.13
- ✓ Fan Led A 14 U 41.12 U 43.8
- ✓ ION Led A 16 U 82.5, U 84.6, U 85.5
- ✓ Fetch Led A 13 U 94.12
- ✓ Deref Led A 12 U 73.10
- ✓ execute Led A 11 U 94.10
- ✓ Carry Led A 13 U 76.8
- ✓ TESTP A 17 U 24.9
- ✓ MSTP A 90 U 24.1
- ✓ Cont + Test + Mstp A 26 U 3.2

✓ PTG Ø U68.2 U68.14
U69.9 U69.14 U119.4 U119.13
U112.13

✓ PTG 1 U34.6
U68.3 U68.13 U69.11
U113.3 U117.5 U119.14 U112.10

✓ PTG 1 U69.12 U47.2 U69.15

✓ PTG 2 U67.8 U66.12

✓ PTG 2 U57.13 U65.8
U67.9 U68.10 U70.5

✓ PTG 5 U23.10 U42.10
U66.2 U70.10 U78.12 U79.6
U75.10 U98.3 U98.4

✓ PTG 5 Enab U56.6 U68.6 U70.9
U70.12 U79.12 U100.12

20.72

✓	<u>Key enab</u>	U3.3	U3.12	U6.2	
	CPU Inst	U6.5	U6.10	U6.11	U11.2
	U11.12	U24.9	U64.2	U71.2	U87.4
					A73
✓	<u>CPU Inst</u>	U10.6	U4.17	U6.12	U6.13
A44	✓ Datia	U5.12	U24.5		✓
✓	<u>Datia</u>	U25.9	U5.13		✓
	Datib	U5.10			
✓	Defer	U95.7	U76.4	U70.4	
		U73.11	U104.6		✓
A12	✓ Defer	U73.10	U48.3	U58.12	✓A16
		U59.10	U75.2		
✓	Exec	U95.9	U94.11	U92.9	
A11	✓ Exec	U52.15	97.10		
	fetch	U95.5	U13.11	U34.9	U100.6
	U64.7	U64.9	U50.7	U85.3	✓U94.13
A13	✓ fetch	U94.12	U45.1	U45.13	U75.1
		U87.12			
	fetch + defer	U75.3	U50.1		
		U74.13			

2
4
13

CLK flop U20.5 U56.10 U72.2 U72.12
U73.3 U93.5
CLK flop U20.6 U20.2

A73 Load. I R U34.3 U28.10 U72.9
U32.10 U33.10 U54.15

✓ I0 f+D U51.12 U27.5

✓ I0 f+D U27.6 U9.12 U42.3

✓ ION U82.6 U11.13 U84.5

✓ A16 ION U84.6 U82.5 U85.5

Input U66.8 U12.10 U25.15
U112.1 U112.9

halt U71.6 U14.2 U62.3 U71.9

100.6
194.13
95.1

CPU CLK U72.6 U72.8 U14.4 U28.6
U32.6 U33.6 U37.6 U38.6 U39.6
U40.6 U42.6 U57.10 U60.10 U66.13
U69.6 U78.13 U95.6 U97.9 U102.6
U103.6 U105.6 U106.6 U107.6 U113.3

B48

DCH U 23.9 U 14.9 U 15.2 U 41.2
U 7.11 U 13.5

DCHM1 U 16.4 U 15.10

B21 DCHM1 U 14.12 U 16.3 U 34.12

DCHO U 18.8 B 33

✓ Reset U 22.10 U 17.1 U 66.1
U 69.1 U 78.1 U 95.1

✓ Restart U 3.5 U 87.10 U 2.8

B87

✓ PLC U 94.6 U 46.10 U 47.1
U 86.5

B90

✓ AEC U 50.8 U 44.2 U 65.5
U 74.1 U 91.12 U 94.5 U 115.13

✓ ALC, Skip U 83.10 U 77.13

B7

Disable Dymo 10 U 53.3 U 121.15

B48 MEMCLK U73.6 U17.6 U23.6 U54.6
U93.4 U115.6 U122.6 U29.6

Serial cry U54.12 U15.13 U88.6

✓ Adder Test U58.3 U104.5

TS0 U66.6 U35.3
U53.3 U57.1 U61.9 U64.10 U68.1
U91.8 U92.10 U114.5

TS3 U66.5 U34.11 U36.12 U45.4
U50.10 U61.1 U61.2 U61.4
U68.15 U75.9 U76.3 U109.2

B87 Read 1 U19.3 U35.10

B90 Read 2 U19.8

Read IO U12.3

Read JO U18.6

PC enab U6.3 U7.1 U10.1
U36.1 U57.5 U61.8 U74.2

B7 MA Load U60.8 U35.11

Cry Set U 81.8 U 42.15 U 76.12

Cry Set Save U 42.9 U 77.9

ACT GO U 54.5 U 73.9 U 111.2
U 123.14 U 124.14

ACT GI U 54.7 U 53.9 U 111.7
U 123.13 U 124.13

✓ EFA U 103.12 U 34.5 U 44.1
U 50.3

✓ *EFA U 103.11 U 32.13 U 33.13 U 74.4
U 44.9 U 45.10 U 46.4 U 47.3 U 47.4 U 93.13

ACD OCT U 45.6 U 121.1

✓ ACD O U 123.5 U 120.5 U 122.3

✓ ACD I U 123.7 U 120.2 U 122.2

✓ ACD 2 U 123.9 U 120.22 U 122.12

✓ ACD 3 U 123.11 U 120.19 U 122.19

ACD 3 Sel U50.6 U123.1

ACD 4 Sel U444.8 U123.15

ACSI 1 Sel U124.1 U49.6

ACSI 2 Sel U124.15 U49.3 U49.11

SHR U51.5 U81.6 U101.5 U125.17

SWP U51.4 U100.11

SIC U51.6 U800.5 U101.3 U125.16

EFA. PTG 1 U34.4 U32.4 U116.1

Pack - U83.12 U49.4 U49.2 : U111.5

Pack U103.9 U49.10 U49.12 U83.13

LDA. E U52.10 U99.1

✓ STA. E U52.11 U99.9 U120.17

✓ PTG = 0. TS Ø U113.9 U58.11 U60.12
U88.9 U90.9

✓ PTG = 0. TS Ø U113.8 U88.4 U90.13
U93.10

✓ PTG = 0. TS 3 U67.12 U9.9 U9.10
U17.10 U88.1 U88.2

✓ PTG = 0. TS 3 U68.4 U67.13 U88.3

PTG = 1. TS 0 U68.11 U80.10 U93.11

PTG = 1. TS 3 U68.5 U109.51

A5

Adder 0 U118.5 U120.4 U117.13
U81.3

Adder 1 U118.1 U118.2 U120.1
U117.11

Adder 2 U118.12 U118.13 U120.23
U117.10

Adder 3 U118.9 U118.10 U120.20
U117.9

Pulse crab U109.6 U15.12 U62.1

0.12

Load ^{Temp} PC U57.8 U119.12

0.13

Loop Set U83.2 U65.9 U70.8 U103.2

9.10

Loop Set U104.8 U71.12 U83.1

18.5

Loop U13.12 U22.5 U47.9
U64.5 U70.6 U103.7

13.11

Loop U22.6 U35.5 U36.10
U56.13

A5 Power fail U86.12

3

Power low U11.1 U102.11

.23

Power Low U75.13 U86.13 U102.12

20

D.SZ-E-TSO U52.4 U92.1

PS D.SZ-E-TSO U52.5 U89.9

STUTTER U73.2 U72.1 U72.13

DCH Loop crab V15.6 V15.9 V18.12
V18.13 V75.10 V104.10 V104.13

Carry V76.9 V77.4

Carry V76.8 V77.3

Skip Inc V42.12 V35.13 V56.12
V58.5 V58.6 V99.12

Skip V78.5 V90.2

Skip V78.6 V50.2 V74.3 V82.12
V86.4

CLR Skip V99.8 V79.1 V98.10

IO Skip V26.2 V59.5

IO Skip V25.12 V26.1 V87.1

TEST SKIP V102.7 V59.3

Test skip Set V86.3 V41.13 V82.9

V102.2

ISZ·DSZ·E V84.8 V81.9 V81.10
V104.2

✓

ISZ·DSZ·E V52.9 V52.1 V84.13
V86.1

SET ION U 63.10 U 82.4

CLR ION U 63.11 U 84.4

Cry enab Save U 102.9 U 90.10 U 114.13

Cry OUT U 117.16 U 54.14 U 91.1

And U 65.4 U 91.2 U 91.5 U 117.8

And Enab. U 64.11 U 62.13 U 65.4
U 89.2

ADD one U 88.8 U 117.7

D \$ E SET U 96.11 U 36.13

D SET U 74.8 U 95.2 U 96.1 U 96.11

E. SET U 96.8 U 95.15 U 96.12

P + E SET + TS3 U 24.13 U 36.11 U 13.3 U 35.1

JSR. EFA U 92.11 U 100.1 U 103.3

JSR. EFA U 93.12 U 92.13 U 99.2

✓ Temp JSR F + D U 48.11 U 61.3 U 93.2

I R O + Skip U 50.12 U 50.11 U 51.15
E SET

Load Cry U 97.8 U 76.11 U 99.5

Total MED 198.8 U37.13 U38.13
U39.13 U40.13

Loop Set U83.2 U65.9 U70.8
U103.2

Loop Set U104.8 U71.12 U83.1

Shift Acb U100.3 U105.13 U106.13
U107.13 U108.13

✓ Fetch, TSO. U64.8 U85.12 U120.16

PTG2 + Loop U73.12 U34.1 U79.2

PTG2, Loop U70.4 U109.3 U104.4
U73.13 U98.9

B37

✓ PCH Loop enab U15.6 U15.9 U75.10
U18.12 U18.13 U104.10 U104.13

B35

Load ACB U100.11 U100.2 U105.10
U106.10 U107.10 U108.10

T53 Set U9.8 U66.11 U112.2
U112.3

A9

N

End cycle U 113.5 U 102.10 U 114.1
U 118.4 U 109.13 U 103.10

End cycle U 113.6 U 113.2
U 112.4 U 112.5 U 114.9

DCHA U 69.7 U 7.11 U 13.5 U 23.15

DCHA U 7.10 (AGO)

DCHA Set U 71.8 U 67.3 U 97.1

DCHA Set U 67.4 U 69.2

B37 DCHI U 14.8 U 13.4

⁰
4.13 B35 DCHR Pend U 13.3 U 71.13 U 104.7

I.O. E U 94.3 U 42.5 U 64.4 U 62.2 U 86.9 U 89.4
U 71.1

I.O. E U 94.4 U 60.13

A9 memok U 62.5 U 83.5 U 125.7

Acb 0	U105.5	U105.14
Acb 1	U106.5	U106.14
Acb 2	U107.5	U107.14 U98.6 U101.9
Acb 3	U108.5	U108.14
Acb 4	U105.7	U105.3
Acb 5	U106.7	U106.3
Acb 6	U107.7	U107.3
Acb 7	U108.7	U108.3
Acb 8	U105.9	U105.2
Acb 9	U106.9	U106.2
Acb 10	U107.9	U107.2
Acb 11	U108.9 U108.2	U81.13 U114.10
Acb 12	U105.11	U69.3 U107.9
<hr/>		
Acb 12	U105.12	U125.19
Acb 13	U106.11	
<hr/>		
Acb 13	U106.12 U125.21	U125.2 U125.20

Acb 14 U107.11

Acb 14 U107.12 U125.1 U125.5
U125.18

Acb 15 U108.11

Acb 15 U108.12 U125.3

Acb 12 Save U69.5 U90.1

Preset U22.10 U17.1 U66.1
U69.1 U78.1 U95.1

reset U22.4 U3.13 U10.13 U84.2
U21.9 U23.1 U42.1 U103.1

Preset 3.11 U22.11

A 1,2	Gnd	
A 3,4	+5 (Power)	
A 5	Power fail	U 86,12
A 6	-5 Volts	NC
A 7	NC	
A 8	+5 OK	
A 9	MEMOR	U 1,3 , U 62,5
A 10	+V Inh	NC
A 11	<u>Exec</u>	U 52,15
A 12	<u>DEFER</u>	U 48,3
A 13	<u>Fetch</u>	U 45,13
A 14	<u>Run</u>	U 22,12
A 15	<u>Carry</u>	U 76,8
A 16	<u>ION</u>	U 85,5
A 17	<u>I STP</u>	U 24,9
A 18	<u>NC</u>	
A 19	<u>PL</u>	U 87,9
A 20	<u>M STP</u>	U 24,1
A 21	<u>NC</u>	
A 22	Con INST	U 36,8
A 23	NC	
A 24	NC	
A 25	Con + I STP + M STP	U 3,2
A 26	NC	
T A 27	Con RQ	U 3,4
B A 28	Con data	U 4,10
A 29	NC	
B A 30	<u>RST</u>	U 21,12
T A 31	<u>STOP</u>	U 4,6
B A 32	RESTART Enable	U 2,12
A 33	Gnd	

T
B

	A 3 4	Gnd
T	A 3 5	MEM 13
B	A 3 6	MEM 12
	A 3 7	<u>MBO 13</u>
	A 3 8	MSK 0
	A 3 9	<u>MBO 12</u>
	A 4 0	INTA
	A 4 1	<u>MBO 15</u>
	A 4 2	DATIB
	A 4 3	<u>MBO 14</u>
	A 4 4	DATIA
	A 4 5	<u>MEM 10</u>
	A 4 6	DS 3
	A 4 7	EXT. Load
	A 4 8	DATOC
	A 4 9	Fetch
	A 5 0	<u>CLR</u>
	A 5 1	MEM 11
	A 5 2	STRT
	A 5 3	<u>MEM 9</u>
	A 5 4	DATIC
	A 5 5	<u>MEM 8</u>
	A 5 6	DATO B
	A 5 7	NC
	A 5 8	DATOA
	A 5 9	<u>NC</u>
	A 6 0	DCHA
	A 6 1	<u>NC</u>
	A 6 2	DS 4
	A 6 3	<u>NC</u>
	A 6 4	DS 5
	A 6 5	<u>NC</u>
	A 6 6	DS 2

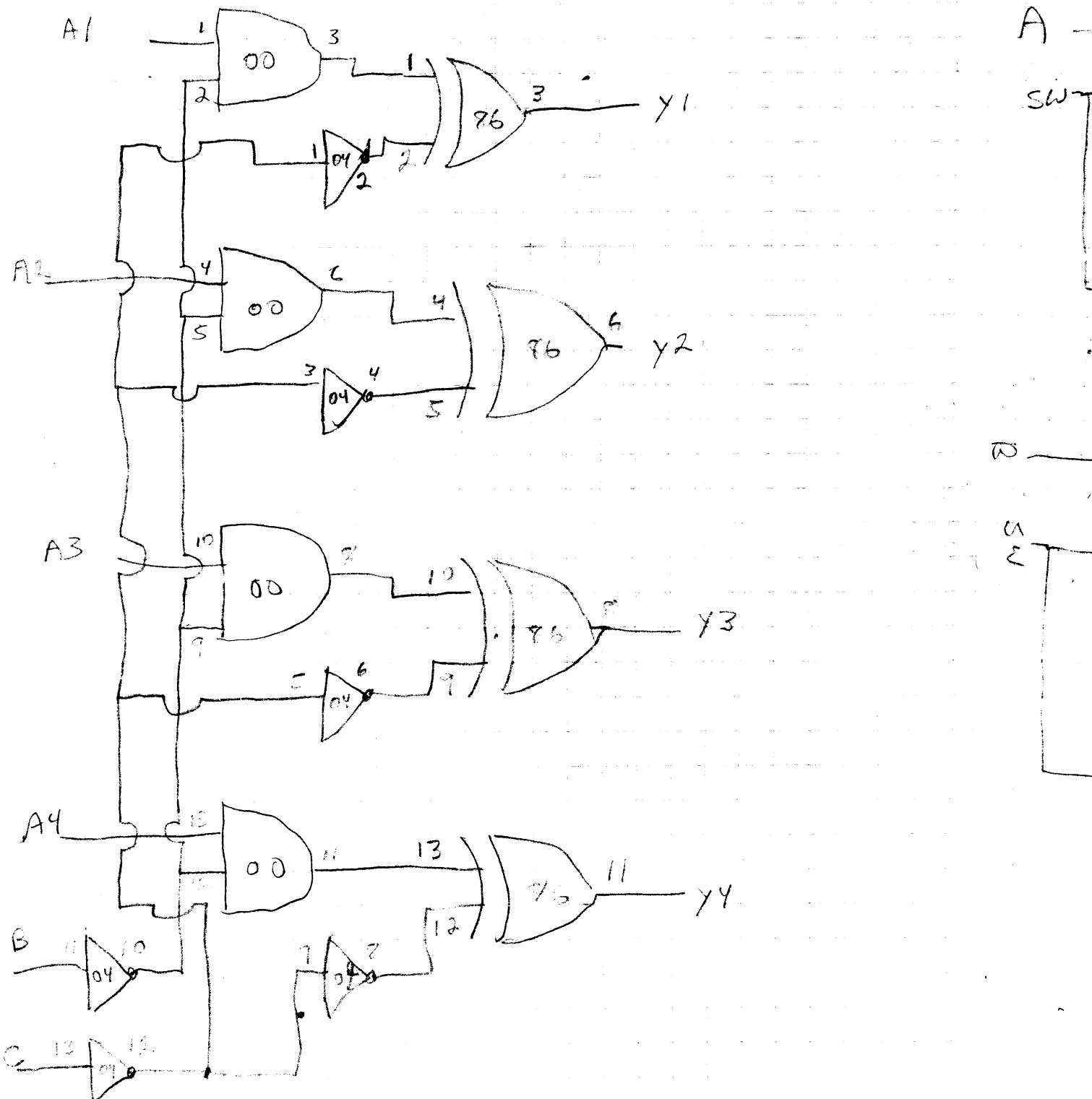
A67
A68 DS1
A69 NC
A70 F0 RST
A71 NC
A72
A73 Load IR
A74 TO PLS
A75 NC
A76 NC
A77 Load AC
A78 NC
A79 NC
A80 SELD
A81 NC
A82 SELB
A83 NC
A84 NC
A85 force load IR
A86 NC
A87 NO SEL1
A88 NC
A89 WRS JSR
A90 NC
A91 PTU
A92 TEST
A93 NC
A94 NC
A95 NC
A96 NC
A97, 98 +5 (Power)
A99, 100 Gnd

B 1,2	Gnd
B 3,4	+5 (Power)
B 5	MBO 11
B 6	<u>whoA</u>
B 7	<u>MR LOAD</u>
B 8	MBO 10
B 9	MBO 9
B 10	NC
B 11	NC
B 12	<u>MBO 8</u>
B 13	<u>NC</u>
B 14	<u>MBO 7</u>
B 15	<u>NC</u>
B 16	<u>MBO 6</u>
B 17	<u>DCH M0</u>
B 18	MEM 15
B 19	NC
B 20	Strobe
B 21	<u>DCH M1</u>
B 22	MEM 6
B 23	<u>NC</u>
B 24	MEM 7
B 25	NC
B 26	MEM 5
B 27	NC
B 28	MEM 4
B 29	INTR
B 30	INHIBIT
B 31	NC
B 32	MBO 5
B 33	DCHO

B 3 4	<u>NC</u>
B 3 5	<u>DCHR</u>
B 3 6	NC
B 3 7	<u>DCHI</u>
B 3 8	NC
B 3 9	<u>OVF10</u>
B 4 0	NC
B 4 1	<u>RQENB</u>
B 4 2	<u>MB04</u>
B 4 3	<u>MB03</u>
B 4 4	<u>MB02</u>
B 4 5	Inhibit Transmission
B 4 6	<u>NC</u>
B 4 7	<u>MEM2</u>
B 4 8	<u>CIR Flop</u>
B 4 9	<u>EXT Load</u>
B 5 0	Gnd
B 5 1	NC
B 5 2	NC
B 5 3	NC
B 5 4	<u>NC</u>
B 5 5	<u>Data 7</u>
B 5 6	<u>Data 14</u>
B 5 7	<u>Data 5</u>
B 5 8	<u>Data 11</u>
B 5 9	<u>Data 12</u>
B 6 0	<u>Data 8</u>
B 6 1	<u>Data 4</u>
B 6 2	<u>Data 0</u>
B 6 3	<u>Data 9</u>
B 6 4	<u>Data 13</u>
B 6 5	<u>Data 1</u>
B 6 6	<u>Data 15</u>

B 6 7	NC
B 6 8	<u>MEM3</u>
B 6 9	<u>SKIP</u>
B 7 0	<u>MEM1</u>
B 7 1	<u>MEM0</u>
B 7 2	<u>MB Load disable</u>
B 7 3	<u>Data3</u>
B 7 4	<u>MB Load</u>
B 7 5	<u>Data10</u>
B 7 6	<u>MEM14</u>
B 7 7	<u>MB01</u>
B 7 8	NC
B 7 9	<u>MB06</u>
B 8 0	NC
B 8 1	NC
B 8 2	<u>Data2</u>
B 8 3	<u>Read I O</u>
B 8 4	NC
B 8 5	<u>NC</u>
B 8 6	<u>MB Clear</u>
B 8 7	<u>Read 1</u>
B 8 8	<u>Drive I O</u>
B 8 9	Gnd
B 9 0	<u>Read 2</u>
B 9 1	<u>shift3</u>
B 9 2	Gnd
B 9 3	<u>Shift2</u>
B 9 4	<u>Shift0</u>
B 9 5	<u>Data6</u>
B 9 6	<u>Shift1</u>
B 9 7,	B 9 8
B 9 9,	B 100

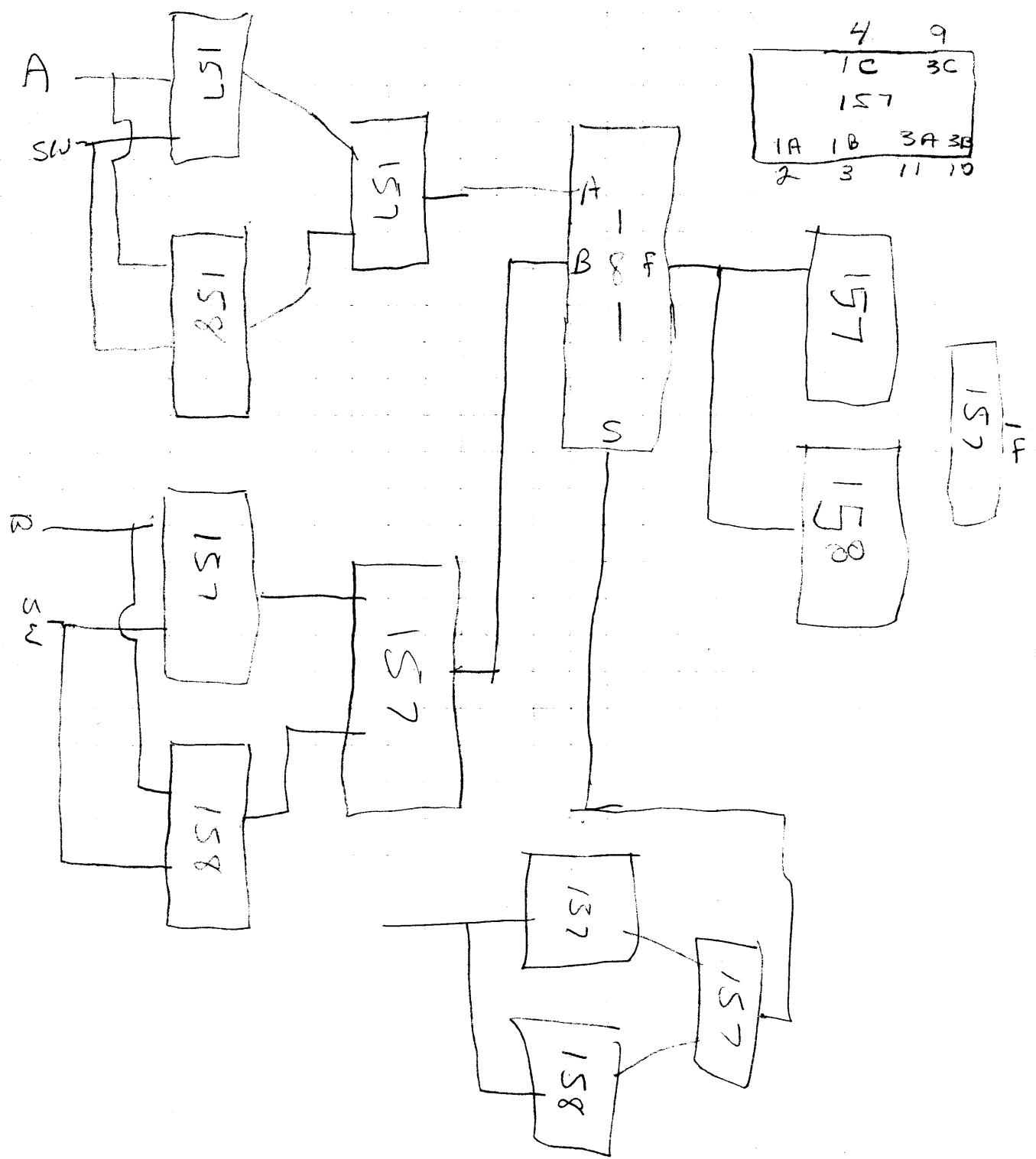
74 + 87 Eguiv



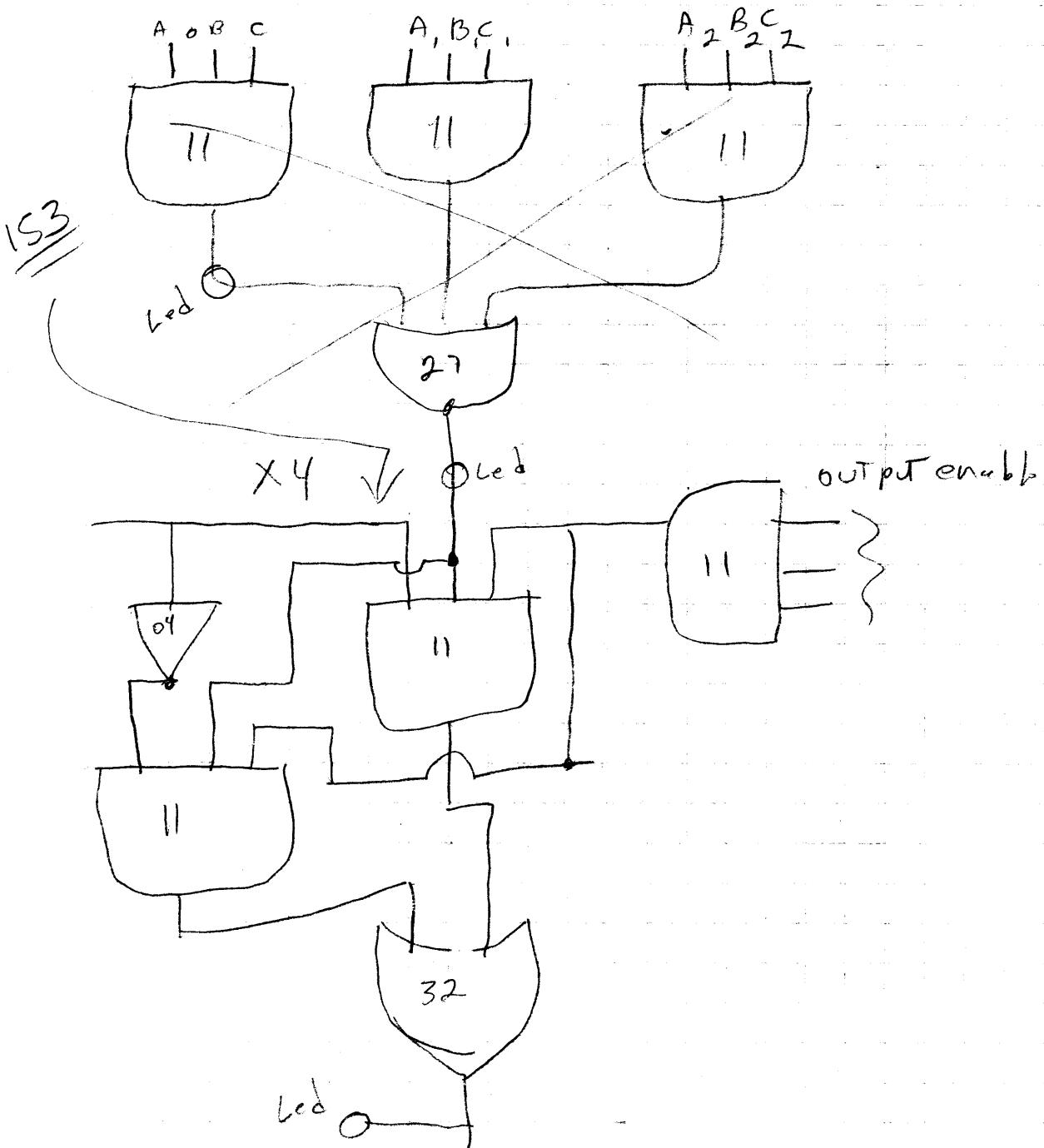
74181

(use ~~XOR's~~)

USE = 87

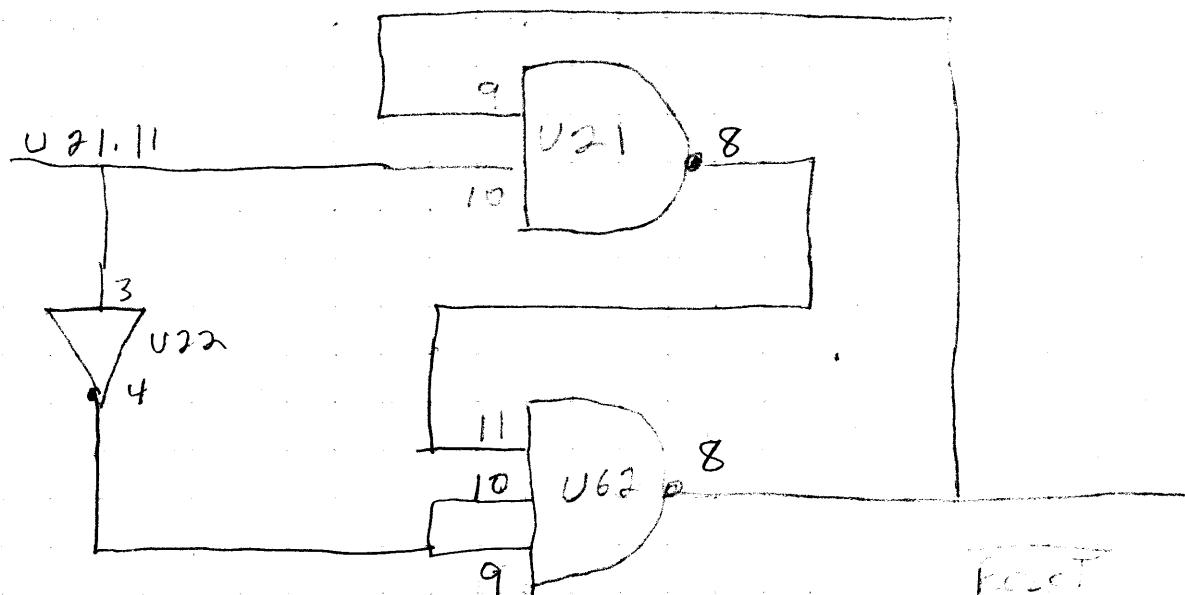


8264



New Reset Circuit

DG Nova 1200 CPU



U12,3

74179
8271

U17 U23 U28 U29

U32 U33 U37 U38

U39 U40, U42 U54

U69 U95 U102 U103

U105 U106 U107

U108 U115 U122

74114 U66 U78 U113

74170 U179

74181 U117

3101 U123 U124

8264 U120 U125

9601 U1

✓ 7410 U35 U50 U62 U74 U93
9003
U111

✓ 7420 U10 U60 U71 U84 U89
7440
9009 U97 U110

✓ 74H21 U9 U14 U15 U18 U56
U72 U99

✓ 7438 U11 U49

✓ 7474 U2 U20 U76
8828

✓ 7486 U80

- 7488 U30 U31 Prom

✓ 74139 U25 U51 U52 U63 U68

✓ 74157 U116 U121

1
2
3
4
5
6
7
8
9
10
11
12

✓ 9008 U43 U46 U47 U61
 ✓ 74454 U81 U88 U98 U104

✓ 7450 U24 U44 U45 U55
 U59 U77 U90 U112
 U114

✓ 9002 U3 U6 U12 U19 U21
 ✓ 7400 U36 U57 U64 U75 U82
 U86 U87 U92 U109
 U118

✓ 7402 U4 U13 U34 U41 U48
 U53 U58 U65 U70 U79
 U85 U91 U96 U100

✓ 8490 U5 U7 U8 U16 U22
 ✓ 74404 U26 U27 U67 U73
 U83 U94 U101

Ta
60
6

Ta
8
4

Tab
312

Tab

Misc

1 bu.
1 b.
cu. feet
1 gall

Circle dia.

Circle dia.

Atoms

sq

13.5 cu

Em is