DESCRIPTION

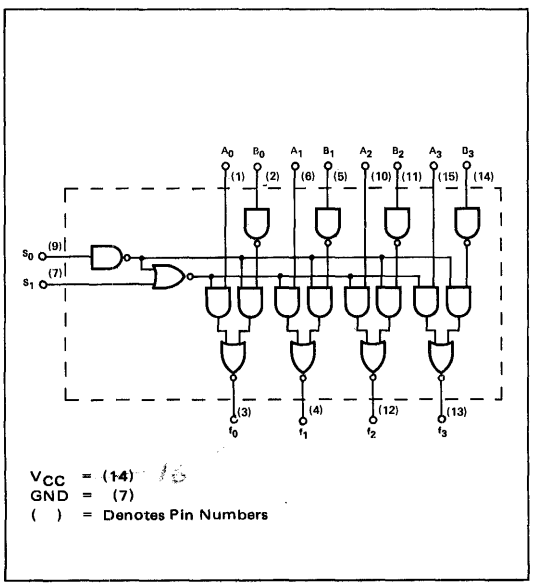
The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state S_0 = S_1 = 1 can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM

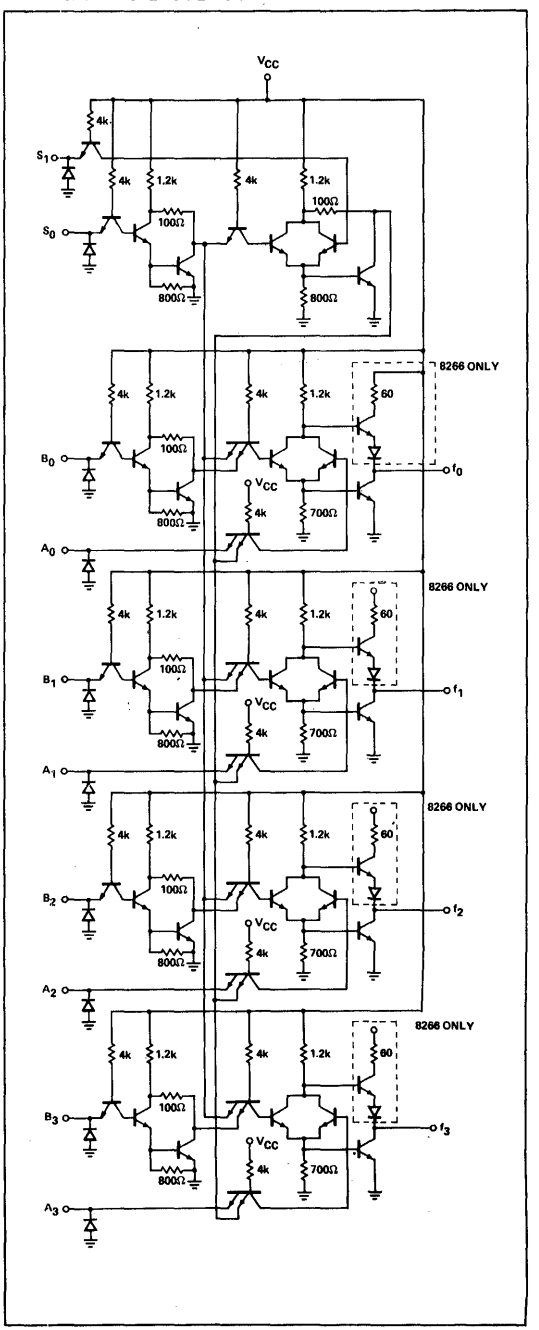


V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

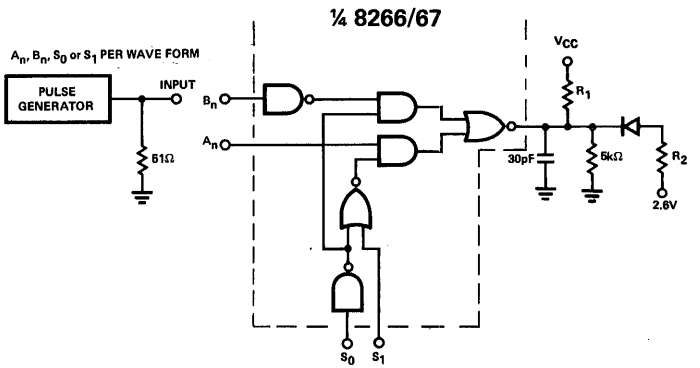
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
"1" Output Voltage (8266)	2.6	3.5		V	0.8V	2.0V	0.8V	0.8V	-800μA	7
"0" Output Voltage			0.40	V	2.0V	2.0V	2.0V	0.8V	16mA	8
"1" Output Leakage Current (8267)			25	μA	0.6V	2.0V	2.0V	0.8V		10
"0" Input Current										
A_n, B_n	-0.1		-1.6	mA	0.4V	0.4V	0V	0V		
S_0, S_1	-0.1		-1.6	mA			0.4V	0.4V		
"1" Input Current										
A_n, B_n			40	μA	4.5V	4.5V		2.0V		
S_0, S_1			40	μA			4.5V	4.5V		
Input Voltage Rating										
S_0, A_n, B_n	5.5			V	10mA	10mA	10mA	2.0V		
S_1	5.5			V			2.0V	10mA		
Output Short Circuit Current (8266)	-20		-70	mA					0V	11, 12

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1	OUTPUTS	
Propagation Delay (8266)										
S_0 to f_n (short path)		18	28	ns						9
S_0 to f_n (long path)		20	30	ns						9
A_n to f_n		13	20	ns						9
B_n, S_1 to f_n		14	25	ns						9
Propagation Delay (8267)										
S_0 to f_n		27	36	ns						9
A_n to f_n		15	20	ns						9
B_n, S_1 to f_n		21	28	ns						9
S_0 to f_n (short path)		18	28	ns						9
Power/Current Consumption		200/ 38.1	275/ 52.4	mW/ mA	4.5V	0V	4.5V	0V		12

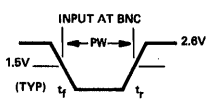
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
11. Not more than one output should be shorted at a time.
12. V_{CC} = 5.25 volts.

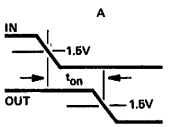
AC TEST FIGURE AND WAVEFORMS

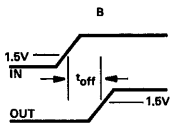


	8266	8267
R_1	∞	330Ω
R_2	84.5Ω	470Ω

NON-INVERTING PATHS

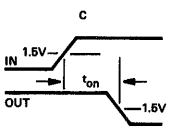


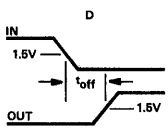




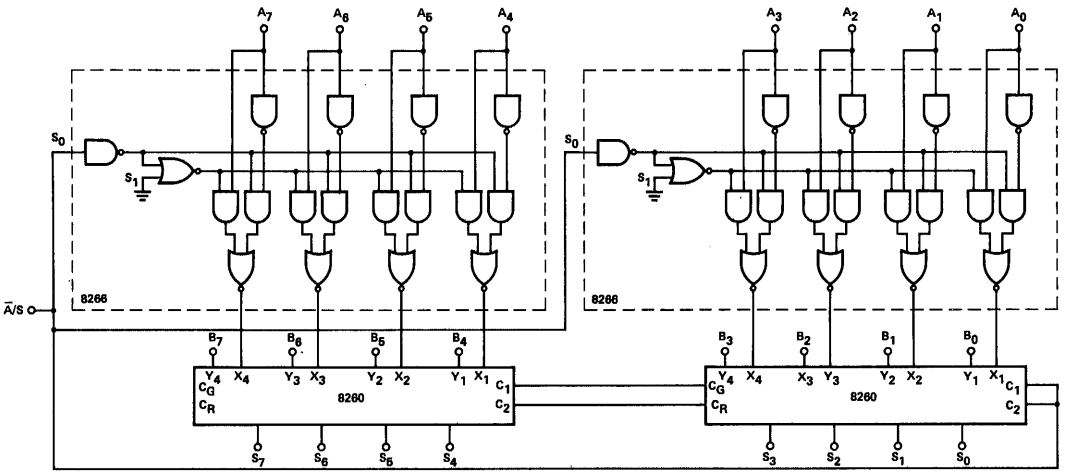
$t_r = t_f \leq 5ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

INVERTING PATHS





TYPICAL APPLICATIONS



The 8266 can be used in conjunction with the 8260 (Look-Ahead Carry Adder) to form an adder-subtractor.