DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit suybsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A HIGH or LOW at data input will be transferred to the associated output when the strobe input is LOW. For additional felxibility, both units are provided with a reset input which is common to all four bits. A LOW on the Reset line forces all four outputs LOW.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

PIN CONFIGURATION

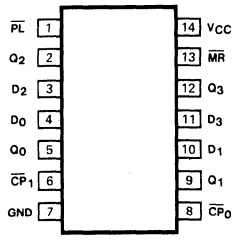


Figure A

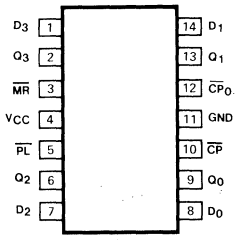


Figure B

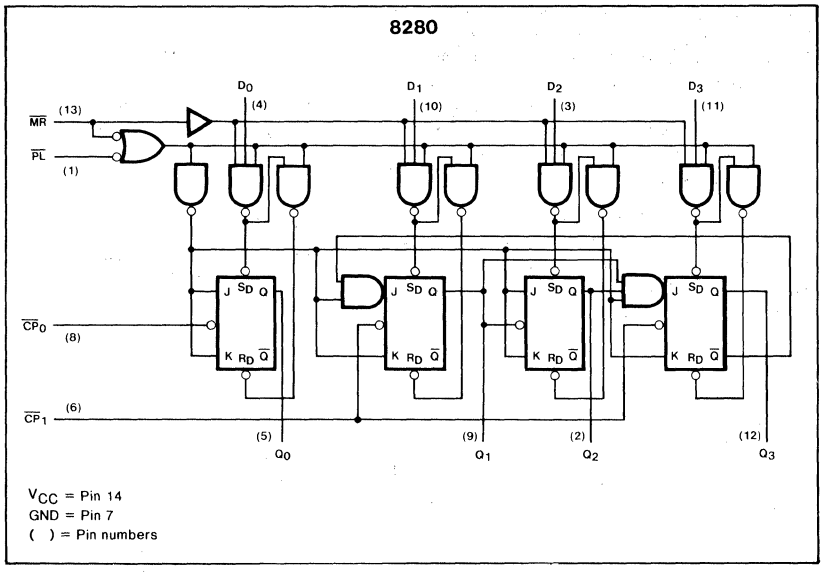
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +75°C	MILITARY RANGES V_{CC}=5V±5%; T_A=−55°C to +125°C
Plastic DIP	Fig. A	N8280N • N8281N	
Ceramic DIP	Fig. A	N8280F • N8281F	S8280F • S8281F
Flatpak	Fig. B		S8280W • S8281W

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	8280		8281		UNIT
			Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = 4.75V, I_{OH} = −800μA	2.6		2.6		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75, I_{OL} = 16mA		0.4		0.4	V
I_{IH}	Input HIGH current	V_C = 5.25V, V_{IN} = 4.5V					
	Strobe, Data inputs			40		40	μA
	Reset, Clock 1			80		80	μA
	Clock 2			80		40	μA
I_{IL}	Input LOW current	V_{CC} = 5.25V, V_{IN} = 0.4V					
	Strobe input		−0.1	−1.6	−0.1	−1.6	mA
	Data input		−0.1	−1.2	−0.1	−1.2	mA
	Reset, Clock 1		−0.1	−3.2	−0.1	−3.2	mA
	Clock 2		−0.1	−3.2	−0.1	−1.6	mA
V_{BD}	Input breakdown voltage	V_{CC} = 4.75V, I_{IN} = 10mA	5.5		5.5		V
I_{OS}	Output short circuit current	V_{CC} = 5.25V, V_{OUT} = OV	−10	−60	−10	−60	mA
I_{CC}	Supply current	V_{CC} = 5.25V		45		45	mA

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

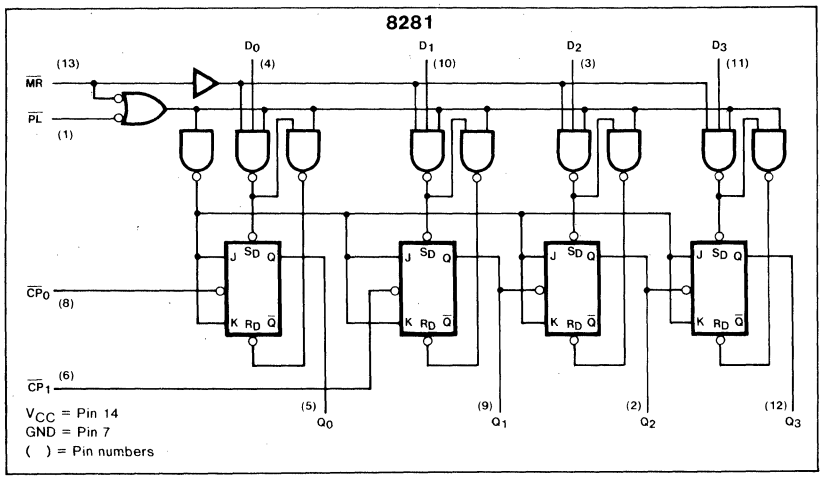
COUNT SEQUENCES for 8280

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES

b. Input applied to CP_0; Q_0 connected to CP_1.
c. Input applied to CP_1; Q_3 connected to CP_0.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

COUNT SEQUENCES for 8281

COUNT	4-BIT BINARY(b)			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE

b. Q_0 connected to $\overline{CP}_1$; input applied to $\overline{CP}_0$

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H H	L L	X X	L H	L H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW Clock Transition

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

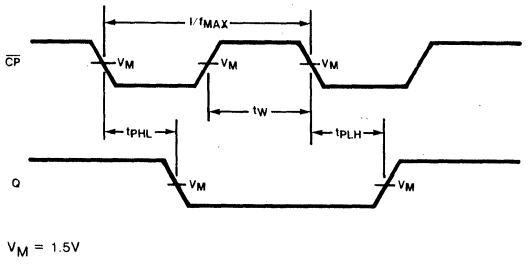
PARAMETER		TEST CONDITIONS		8280 C_L = 24pF R_1 = ∞Ω R_2 = 84.5Ω		8281 C_L = 24pF R_1 = ∞Ω R_2 = 84.5Ω		UNIT
				Min	Max	Min	Max	
f_{MAX}	Maximum count frequency	Figure 1	$\overline{CP}_0$	20		20		MHz
			$\overline{CP}_1$	10		10		MHz
t_{PLH} t_{PHL}	Propagaton delay $\overline{CP}_0$ to Q_0	Figure 1			25 25		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1	Figure 1			25 25		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Figure 1			50 50		50 50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_3	Figure 1			25 25		75 75	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Figure 2			40 35		40 35	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Figure 3			40 35		40 35	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Figure 4			45		45	ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		8280		8281		UNIT
				Min	Max	Min	Max	
t_W	Clock pulse width	Figure 1	$\overline{CP}_0$	25		25		ns
			$\overline{CP}_1$	25		25		ns
t_W	$\overline{MR}$ pulse width	Figure 4		35		35		ns
t_W	$\overline{PL}$ pulse width	Figure 3		35		35		ns
t_{rec}	Recovery time $\overline{MR}$ to $\overline{CP}$	Figure 4		75		75		ns
t_{rec}	Recovery time $\overline{PL}$ to $\overline{CP}$	Figure 3		40		40		ns

AC WAVEFORMS

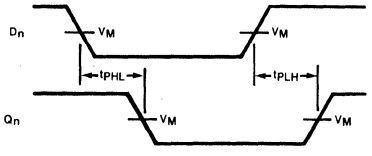
CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



V_M = 1.5V

Figure 1

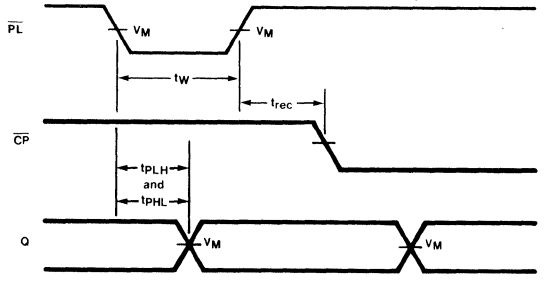
PARALLEL DATA TO OUTPUT DELAYS



V_M = 1.5V

Figure 2

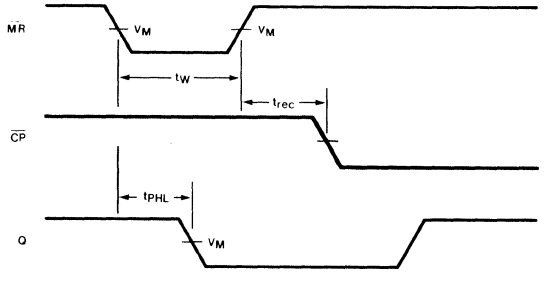
PARALLEL LOAD PULSE WIDTH,
PARALLEL LOAD TO OUTPUT DELAY AND
PARALLEL LOAD TO CLOCK RECOVERY TIME



V_M = 1.5V

Figure 3

MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME

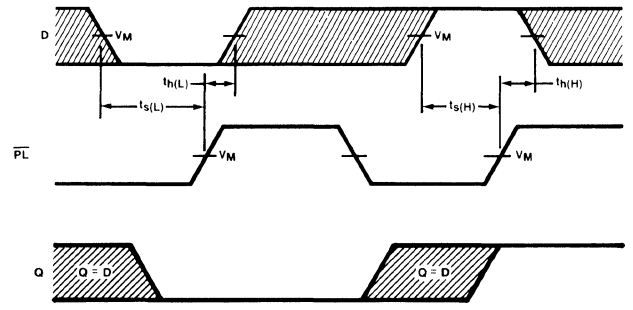


V_M = 1.5V

Figure 4

AC WAVEFORMS (Cont'd)

DATA SETUP AND HOLD TIMES



V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5