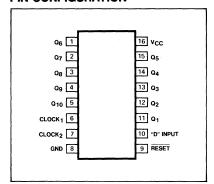
#### **DESCRIPTION**

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

### PIN CONFIGURATION



## ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES  COMMERCIAL RANGES  VCC=5V±5%; TA=0°C to +75°C		MILITARY RANGES V <sub>CC</sub> =5V±5%; T <sub>A</sub> =-55°C to +125°C
Plastic DIP	N8273N	
Ceramic DIP	N8273F	S8273F
Flatpak		S8273W

### MODE SELECT—FUNCTION TABLE

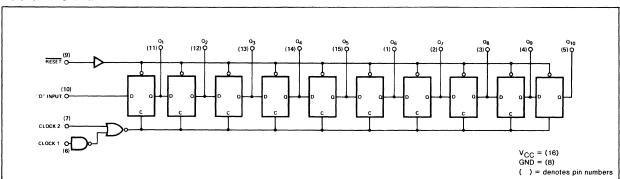
INPUT	RESET	CLOCK 1	CLOCK 2	OUTPUTS Q <sub>n</sub>
н	н	<b>↓</b>	L	н
L	Н	1	L	L
н	Н	Н	<b>†</b>	н
L	Н	Н	<b>†</b>	L
Н	Н	↓ ↓	H	$Q_{n-1}$
L	Н	<b>i</b>	Ĥ	Q <sub>n-1</sub>
Н	H	L	<b>1</b> • • • • • • • • • • • • • • • • • • •	Q <sub>n-1</sub>
L	Н	L	<b>†</b>	Q <sub>n-1</sub>
X	L	X	×	L

NOTE

The unused clock input performs the INHIBIT function.

RESET = 0 Q = 0

#### **LOGIC DIAGRAM**



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

	* :		8273		
	PARAMETER	TEST CONDITIONS	Min	Max	UNIT
VOH	Output HIGH voltage	$V_{CC} = 4.75V, I_{OH} = -500\mu A$	2.6		· V
VOL	Output LOW voltage	V <sub>CC</sub> = 4.75V, I <sub>OL</sub> = 9.6mA		0.4	٧
lН	Input HIGH current	V <sub>CC</sub> = 5.25V, V <sub>IN</sub> = 4.5V		40	μΑ
I <sub>IL</sub>	Input LOW current	$V_{CC} = 5.25V, V_{IN} = 0.4V$		-1.6	mA
V <sub>BD</sub>	Input breakdown voltage	V <sub>CC</sub> = 5.25V, IN = 10mA	5.5		٧
los	Output short circuit current	V <sub>CC</sub> = 5.25V, V <sub>OUT</sub> = OV	-20	-70	mA
ICC	Supply current	V <sub>CC</sub> = 5.25V		103	mA

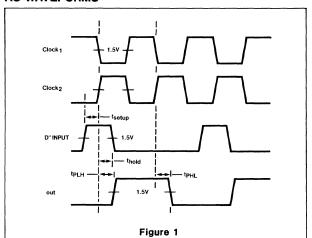
## AC CHARACTERISTICS: T<sub>A</sub> = 25°C (See Section 4 for Waveforms and Conditions)

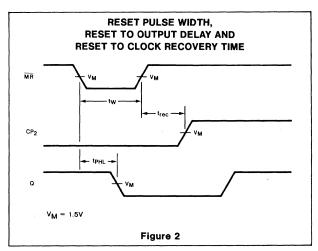
				$8273$ $C_{L} = 18pF$ $R_{1} = \infty\Omega$ $R_{2} = 150\Omega$	
PARAMETER		TEST CONDITIONS	R <sub>1</sub> =		
			Min	Max	1
fMAX	Maximum Clock Frequency	Figure 1	25		MHz
tPLH tPHL	Propagation delay CP <sub>1</sub> to output	CP <sub>2</sub> = OV, Figure 1		40 40	ns ns
tPLH tPHL	Propagation delay CP <sub>2</sub> to output	CP <sub>1</sub> = 4.5V, Figure 1		40 40	ns ns
tPHL	Propagation delay Reset to output	Figure 2		50	ns

# AC SET-UP REQUIREMENTS: T<sub>A</sub> = 25° C (See Section 4 for Waveforms and Conditions)

			82	8273	
	PARAMETER	TEST CONDITIONS	Min	Max	UNIT
tw	CP <sub>1</sub> pulse width	Figure 1	25		ns
ts	Setup time Data to CP <sub>1</sub>	Figure 1	15		ns
th.	Hold time Data to CP <sub>1</sub>	Figure 1	15		ns
tw	CP <sub>2</sub> pulse width	Figure 1	20		ns
ts	Setup time Data to CP <sub>2</sub>	Figure 1	10	-	ns
th	Hold time Data to CP <sub>2</sub>	Figure 1	10		ns

## **AC WAVEFORMS**



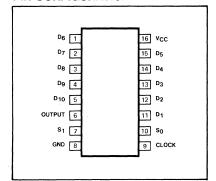


#### **DESCRIPTION**

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D $_1$  input can also be used for serial entry. Two control inputs, S $_0$  and S $_1$ , determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse.

Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmission, Pseudo-Random Code generation and Modulo-N Frequency Division

#### PIN CONFIGURATION



# ORDERING CODE (See Section 9 for further Package and Ordering Information)

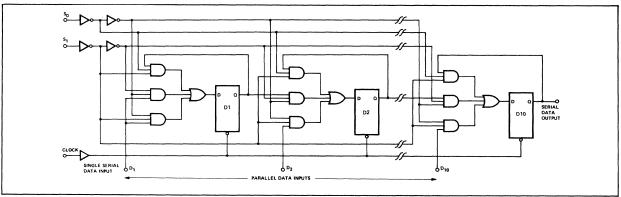
PACKAGES	COMMERCIAL RANGES  VCC=5V±5%; TA=0°C to +75°C  CCC=5V±5%; TA=-	
Plastic DIP	N8274N	166-24 7 2 2 4 4 1 2 2 5 4 4 1 1 2 5 5 6 1 4 1 1 2 5 5 6 1 4 1 1 2 5 5 6 1 4 1 1 2 5 5 6 1 4 1 1 2 5 6 1 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Ceramic DIP	N89274F	S8274F
Flatpak		\$8274W

### MODE SELECT— FUNCTION TABLE

s <sub>0</sub>	S <sub>1</sub>	OPERATING MODE
L	L	Hold
L	н	Clear
н	L	Load
н	н	Shift

H = HIGH voltage level L = LOW voltage level

#### LOGIC DIAGRAM



NOTE

 a. The slashed numbers indicate different parametric values for Military Commercial temperature ranges respectively.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

			82	8274	
	PARAMETER	TEST CONDITIONS	Min	Max	UNIT
VOH	Output HIGH voltage	$V_{CC} = 4.75V, I_{OH} = -800\mu A$	2.6		٧
VOL	Output LOW voltage	V <sub>CC</sub> = 4.75V, I <sub>OL</sub> = 16mA		0.4	٧
ΉΗ	Input HIGH current	V <sub>CC</sub> = 5.25V, V <sub>IN</sub> = 4.5V		40	μΑ
ΊL	Input LOW current D <sub>n</sub> , S <sub>0</sub> , S <sub>1</sub> Clock	$V_{CC} = 5.25V, V_{IN} = 0.4V$	-0.2 -0.2	-1.2 -1.6	mA mA mA
V <sub>BD</sub>	Input breakdown voltage	V <sub>CC</sub> = 5.0V, I <sub>IN</sub> = 10mA	5.5		V
los	Output short circuit current	V <sub>CC</sub> = 5.0V, V <sub>OUT</sub> = OV	-20	-70	mA
Icc	Supply current	V <sub>CC</sub> = 5.0V		108	mA

# AC CHARACTERISTICS: T<sub>A</sub> = 25° C (See Section 4 for Waveforms and Conditions)

				8274	
PARAMETER		TEST CONDITIONS	$C_L = 18pF$ $R_1 = \infty \Omega$ $R_2 = 84.5 \Omega$		UNITS
				Max	
fMax	Maximum clock frequency	Figure 1	25		MHz
tPLH tPHL	Propagation delay Clock to output	Figure 1		40 40	ns ns

# AC SET-UP REQUIREMENTS TA = 25°C (See Section 4 for Waveforms and Conditions)

			8274		
PARAMETER	PARAMETER	TEST CONDITIONS	Min	Max	UNIT
tw	Clock pulse width	Figure 1	20		ns
ts	Set-up time	Figure 1			
	Dn		10		ns
	S <sub>0</sub> ,S <sub>1</sub>		25	,	ns

## **AC WAVEFORMS**

